United States Defensive Publication [19] (H) [11] T106,201

Balyoz et al. [43] Mar. 4, 1986

[54] MASTER IMAGE CHIP ORGANIZATION TECHNIQUE OR METHOD

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[21] Appl. No.: **457,786**

[22] Filed: **Jan. 13, 1983**

Related U.S. Application Data

[60] Continuation of Ser. No. 224,240, Jan. 12, 1981, abandoned, which is a division of Ser. No. 974,576, Dec. 29, 1978, Pat. No. 4,295,149.

[51] **Int. Cl.**[4] **H01L 21/88**

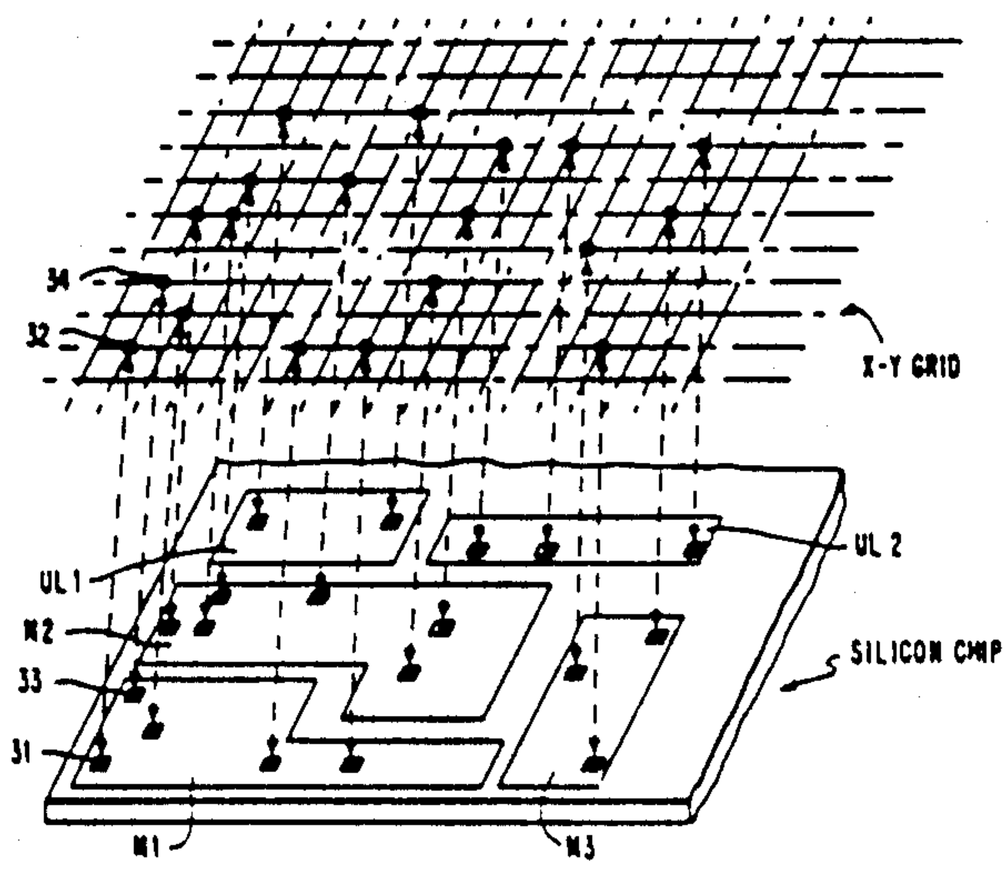
[52] **U.S. Cl.** ..... **29/577 C**

[57] **ABSTRACT**

A method for forming an improved integrated circuit chip structure having a surface from which regions of different conductivity type are arranged in a plurality of electrically isolated macro circuits, each macro circuit including interconnected components, a first X pattern of equally spaced parallel conductors overlying and electrically insulated from said chip structure surface, said first X pattern of conductors being selectively connected to at least certain ones of said plurality of macro circuits, a second Y pattern of equally spaced parallel conductors overlying and electrically insulated from said first pattern of parallel conductors, said second Y pattern of conductors being selectively connected to at least selected certain ones of said first pattern of electrical conductors, said spacing one from another of said first X pattern of conductors being equal to said spacing one from another of said second Y pattern of conductors, said first pattern of conductors being orthogonal of said second pattern of conductors, and each of said connections occurring exclusively at points in space corresponding to X-Y intersections of an X-Y coordinate system, where said X-Y coordinate system geometrically corresponds identically to said X-Y pattern of conductors.

1 Claim, 15 Sheets Drawing,

82 Pages Specification



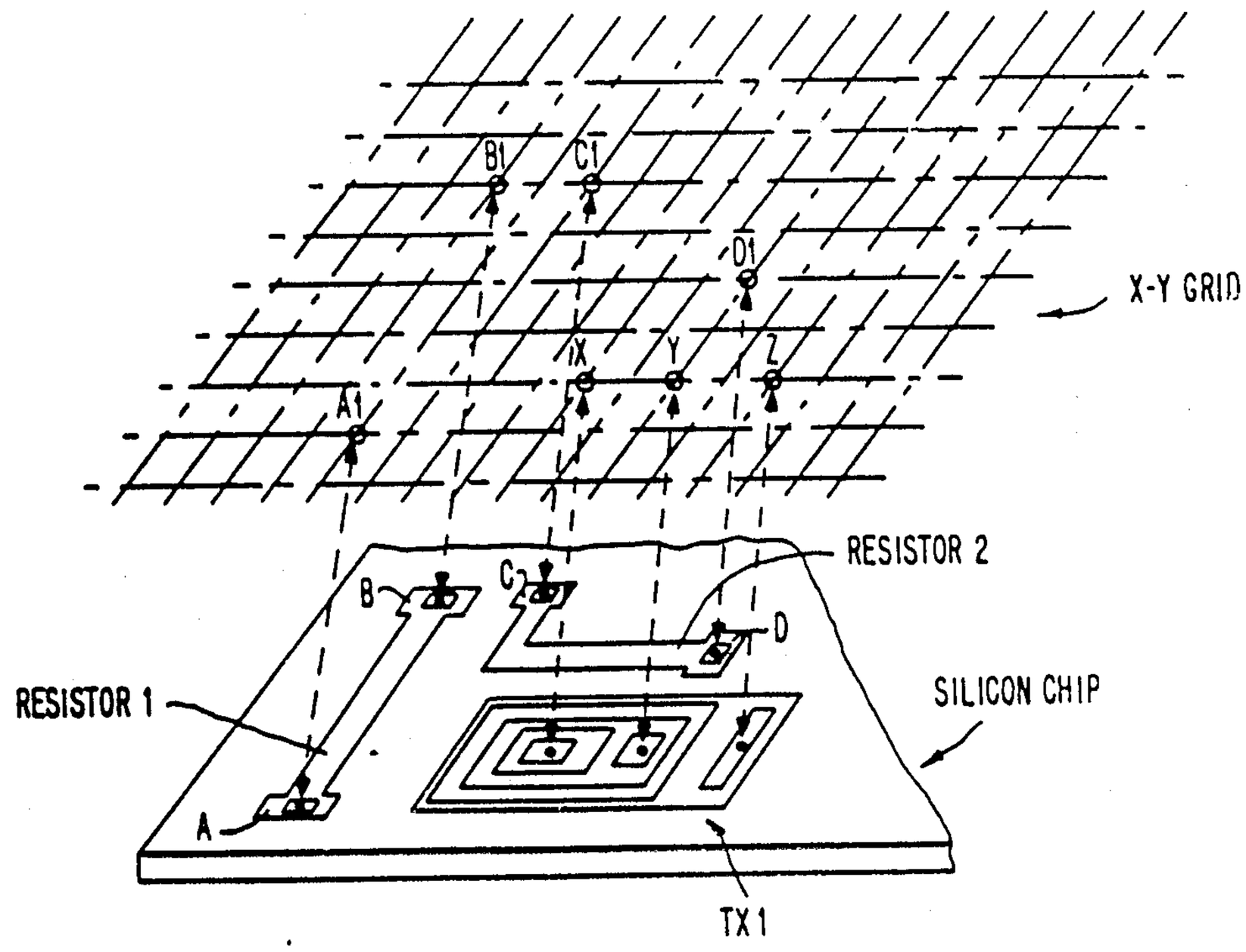

B1
C1
D1
X-Y GRID
IX
Y
Z
A1
RESISTOR 2
B
C
D
RESISTOR 1
SILICON CHIP
A
TX1

FIG. 1

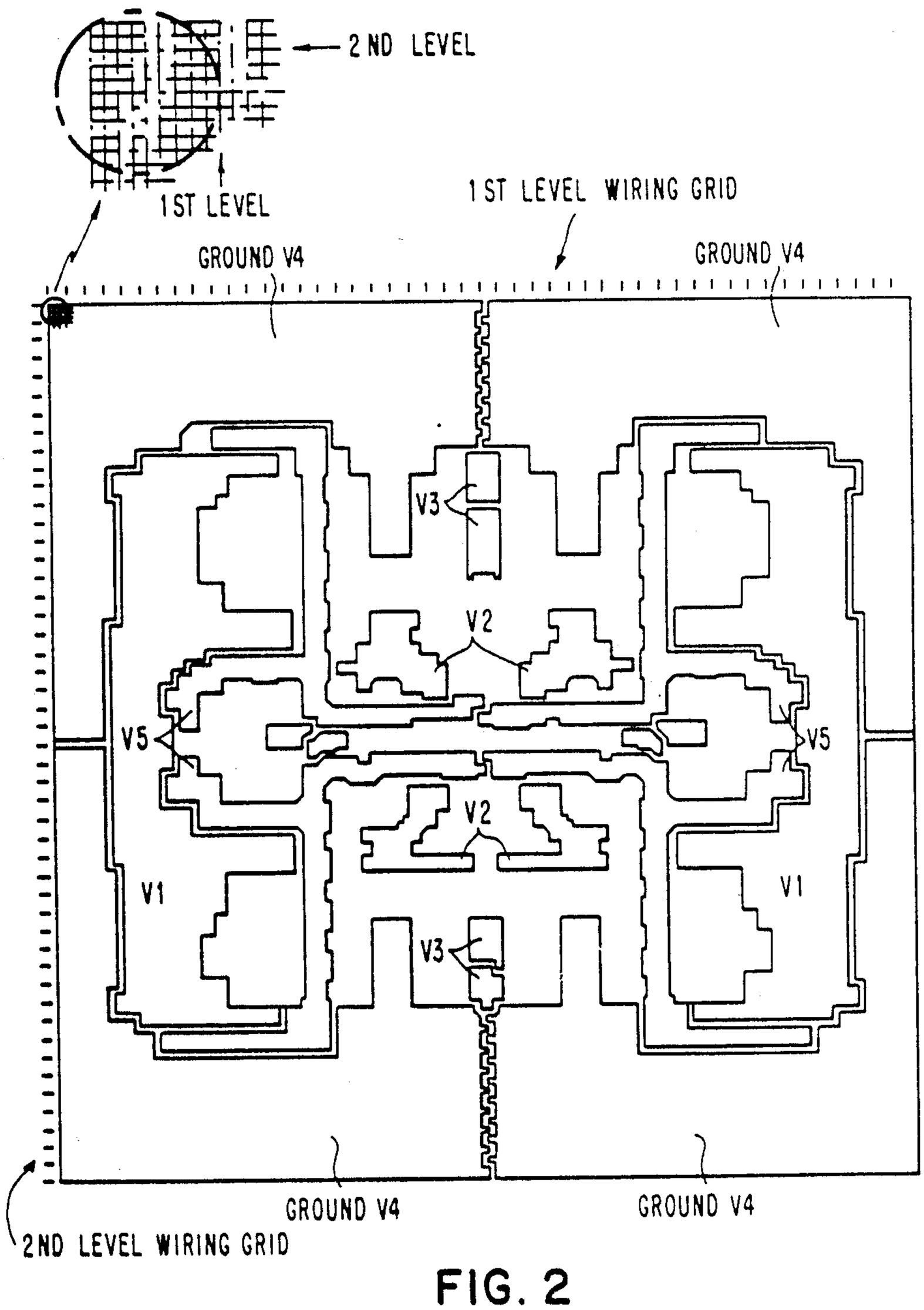

2 ND LEVEL
1ST LEVEL
1 ST LEVEL WIRING GRID
GROUND V4
GROUND V4
V3
V2
V5
V5
V2
V1
V1
V3
GROUND V4
GROUND V4
2ND LEVEL WIRING GRID

FIG. 2

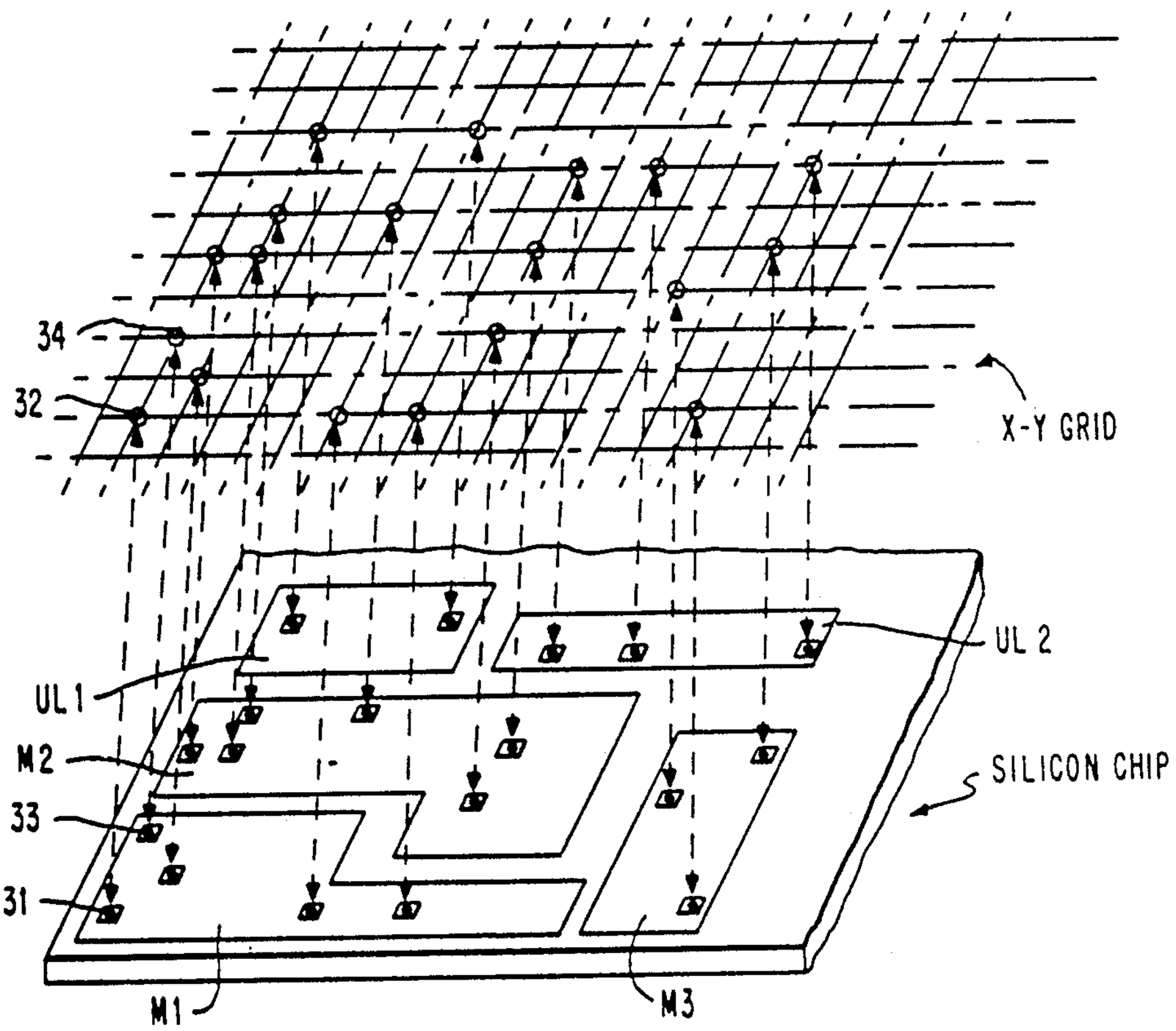


FIG. 3

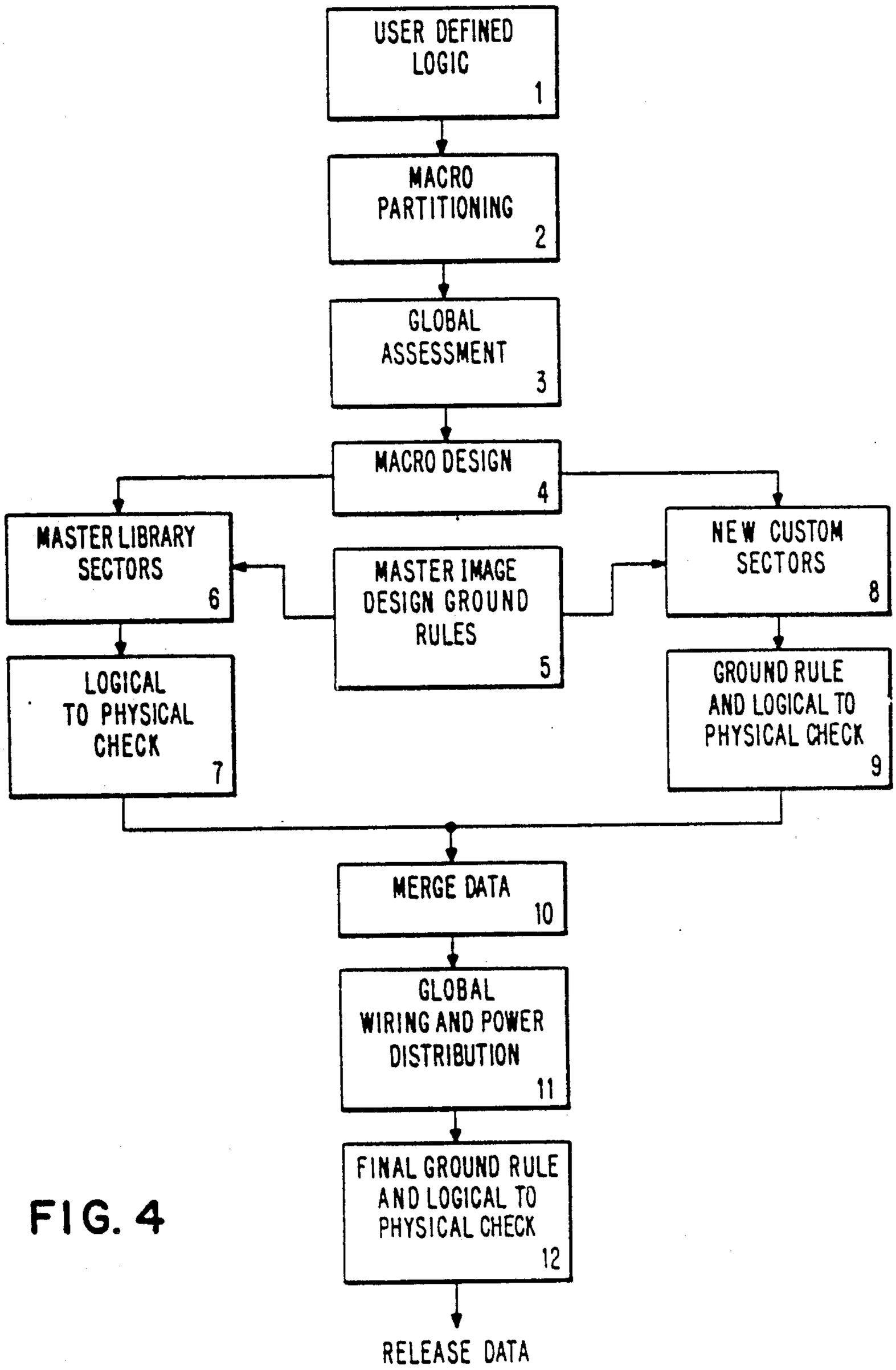
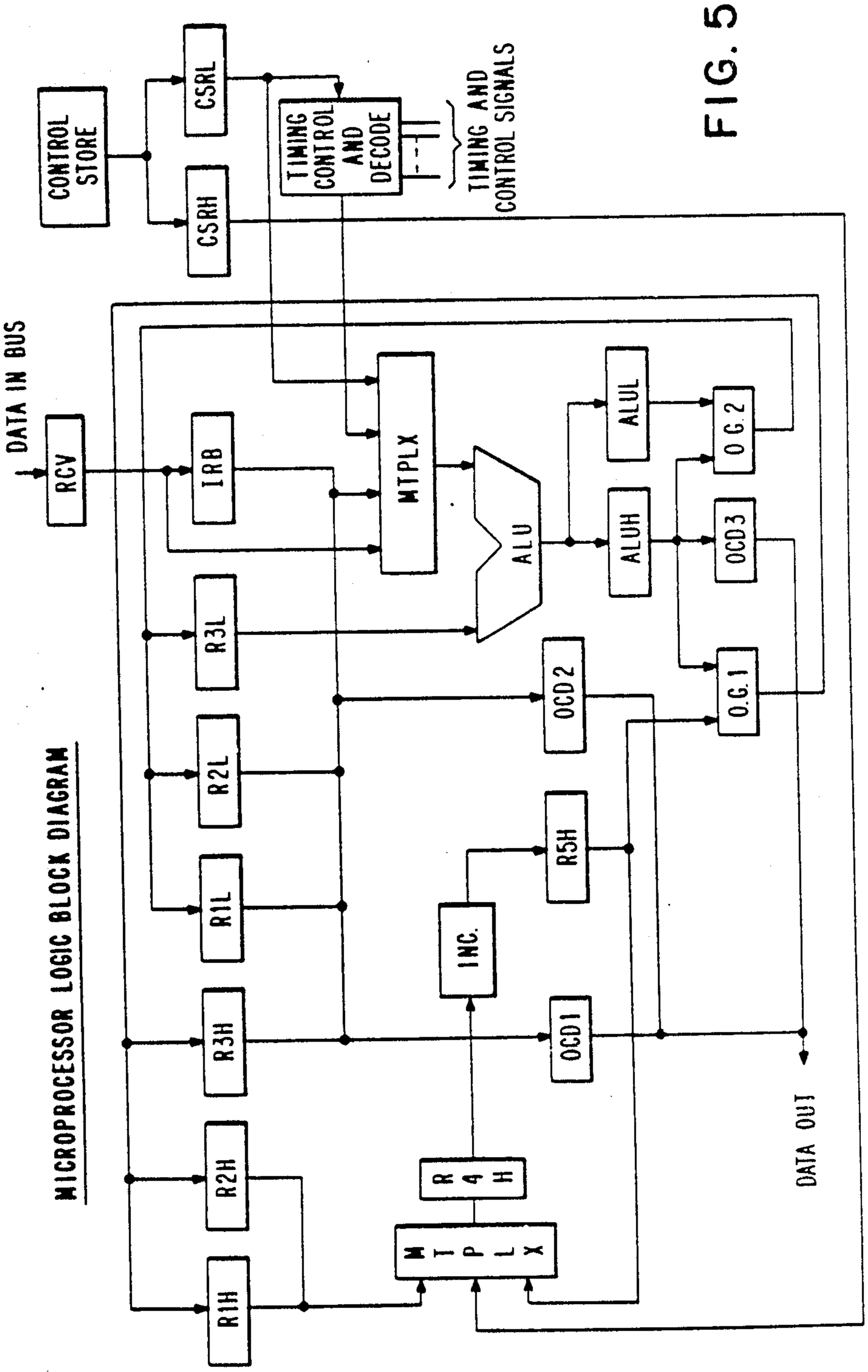
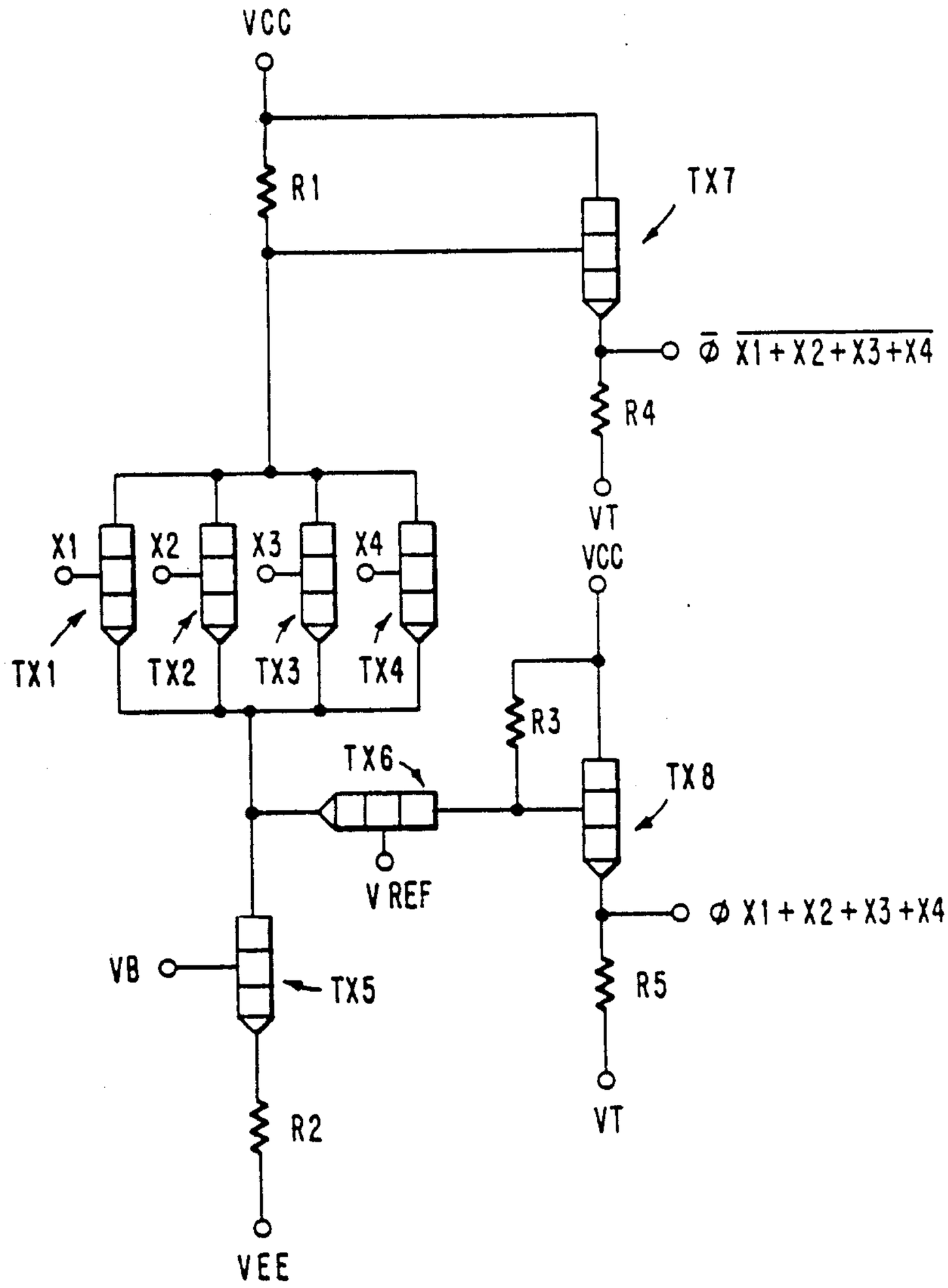

USER DEFINED LOGIC 1
MACRO PARTITIONING 2
GLOBAL ASSESSMENT 3
MACRO DESIGN 4
MASTER LIBRARY SECTORS 6
MASTER IMAGE DESIGN GROUND RULES 5
NEW CUSTOM SECTORS 8
LOGICAL TO PHYSICAL CHECK 7
GROUND RULE AND LOGICAL TO PHYSICAL CHECK 9
MERGE DATA 10
GLOBAL WIRING AND POWER DISTRIBUTION 11
FINAL GROUND RULE AND LOGICAL TO PHYSICAL CHECK 12
RELEASE DATA

FIG. 4

FIG. 5


MICROPROCESSOR LOGIC BLOCK DIAGRAM
CONTROL STORE
CSRL
CSRH
TIMING CONTROL AND DECODE
TIMING AND CONTROL SIGNALS
DATA IN BUS
RCV
IRB
MTPLX
ALU
ALUL
ALUH
O.G.2
OCD3
O.G.1
OCD2
R3L
R2L
R1L
R5H
INC.
OCD1
R3H
R2H
R1H
R4H
MTPLX
DATA OUT



BASIC CURRENT SWITCH EMITTER FOLLOWING CIRCUIT WITH IN-PHASE AND OUT OF-PHASE OUTPUTS

(4 INPUTS, 2 OUTPUTS)

FIG. 6

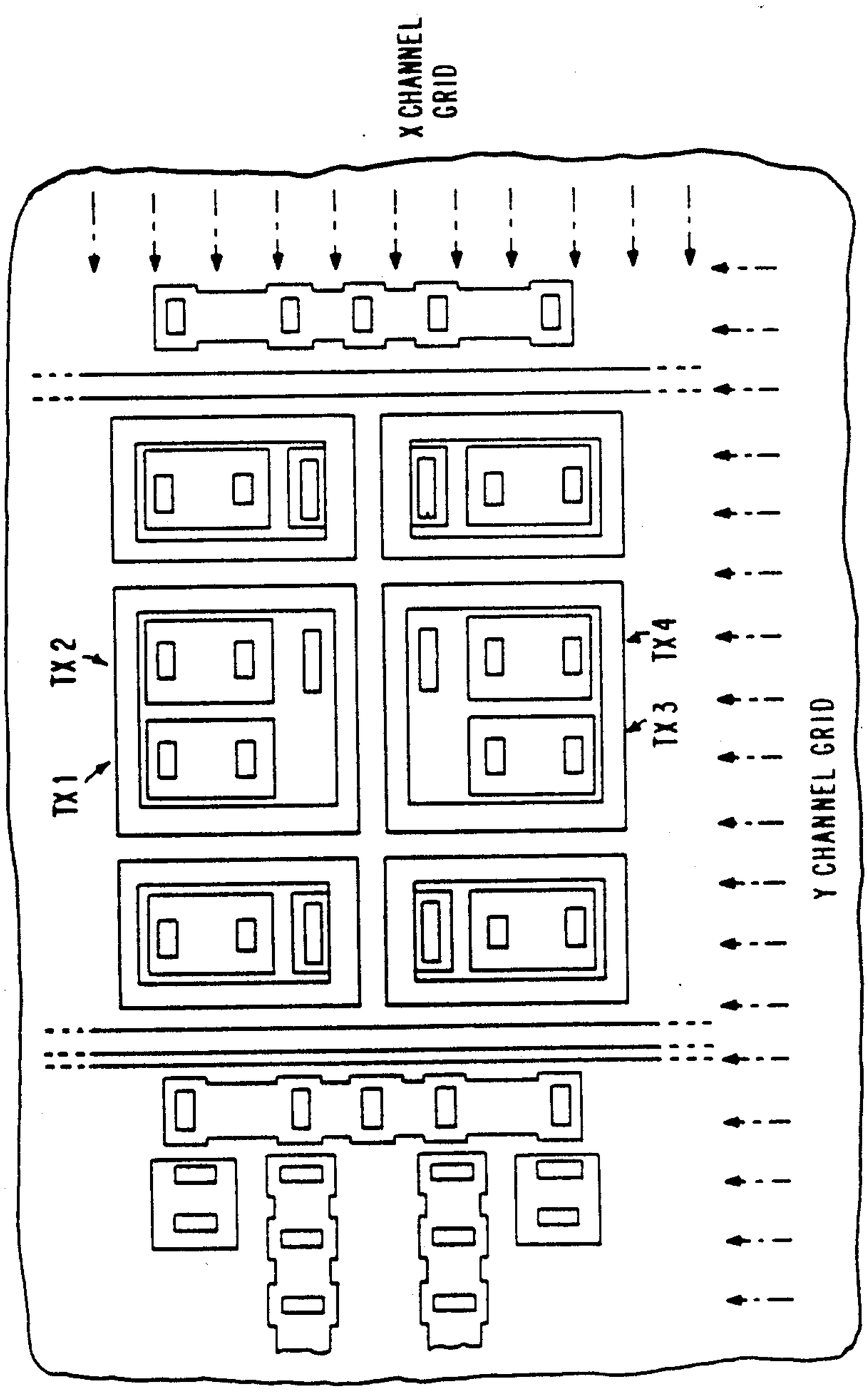


FIG. 7

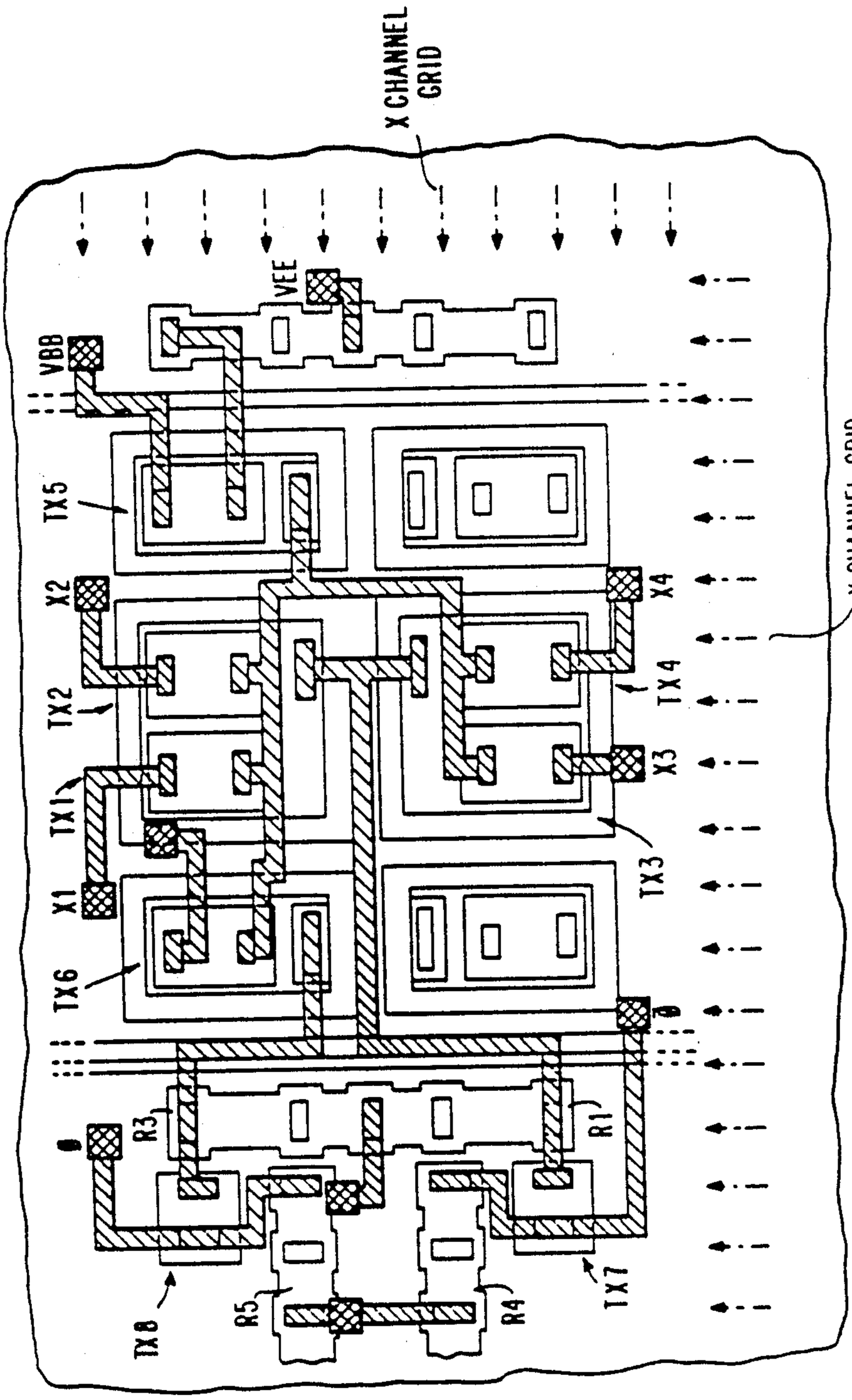

X CHANNEL GRID
VEE
VBB
TX5
X2
TX2
TX1
X1
TX6
TX8
R5
R4
TX7
R3
R1
TX3
X3
TX4
X4
Y CHANNEL GRID

FIG. 8

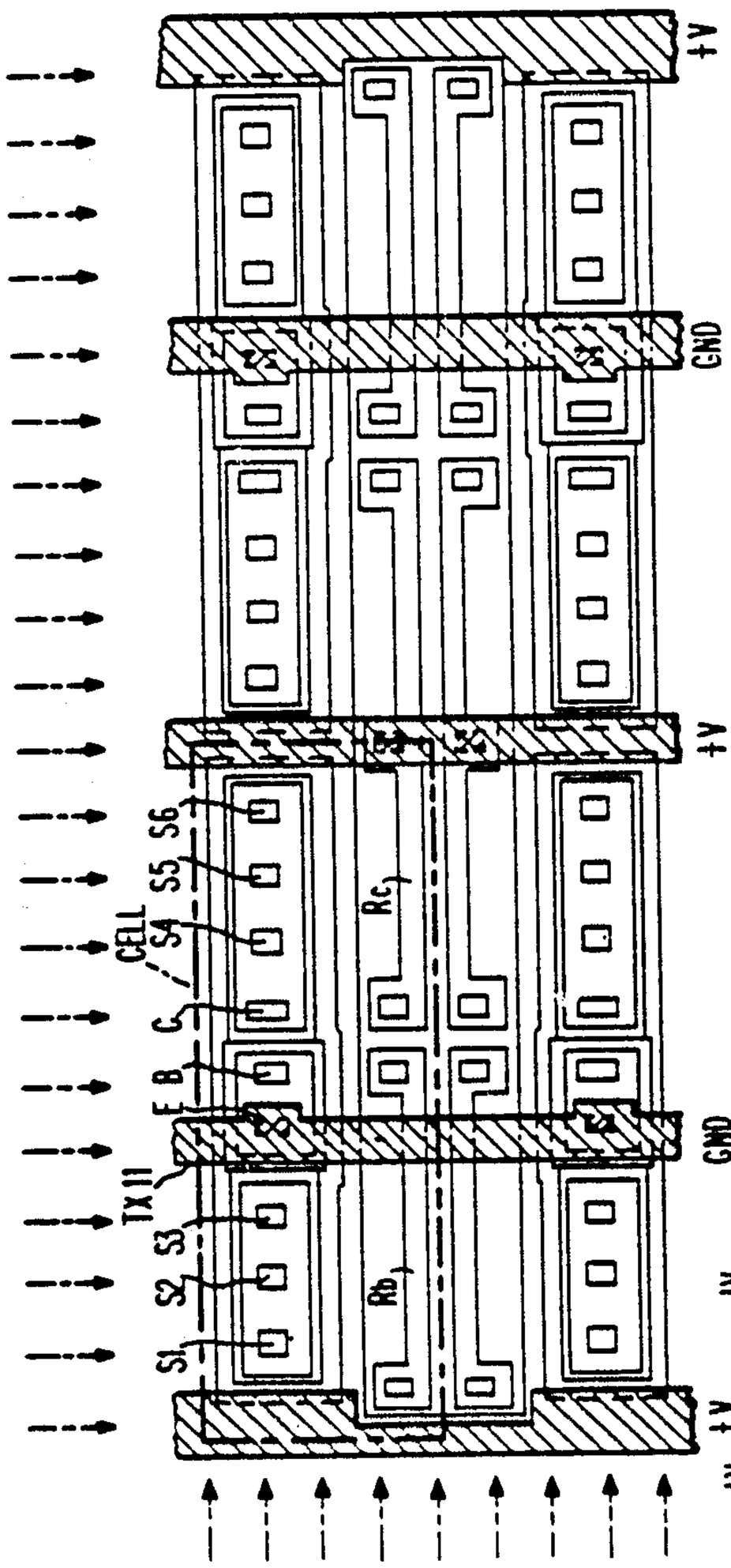
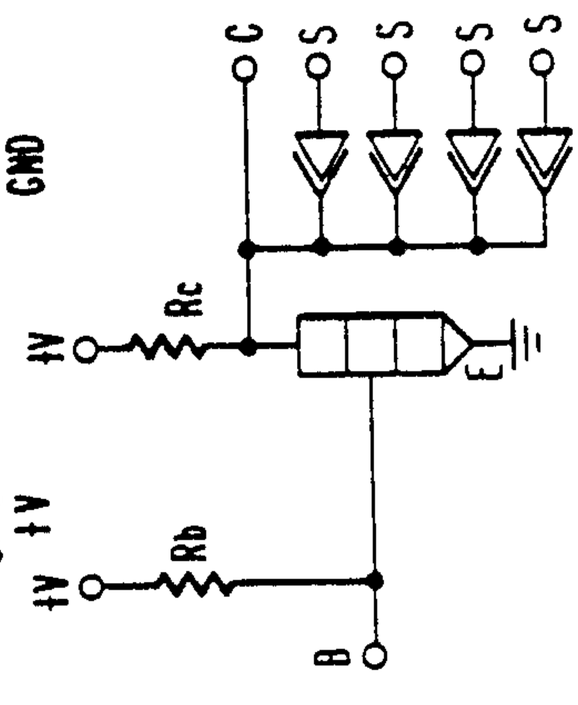


FIG. 9

STL LOGIC BLOCK

FIG. 9B



STL CIRCUIT DIAGRAM

FIG. 9A

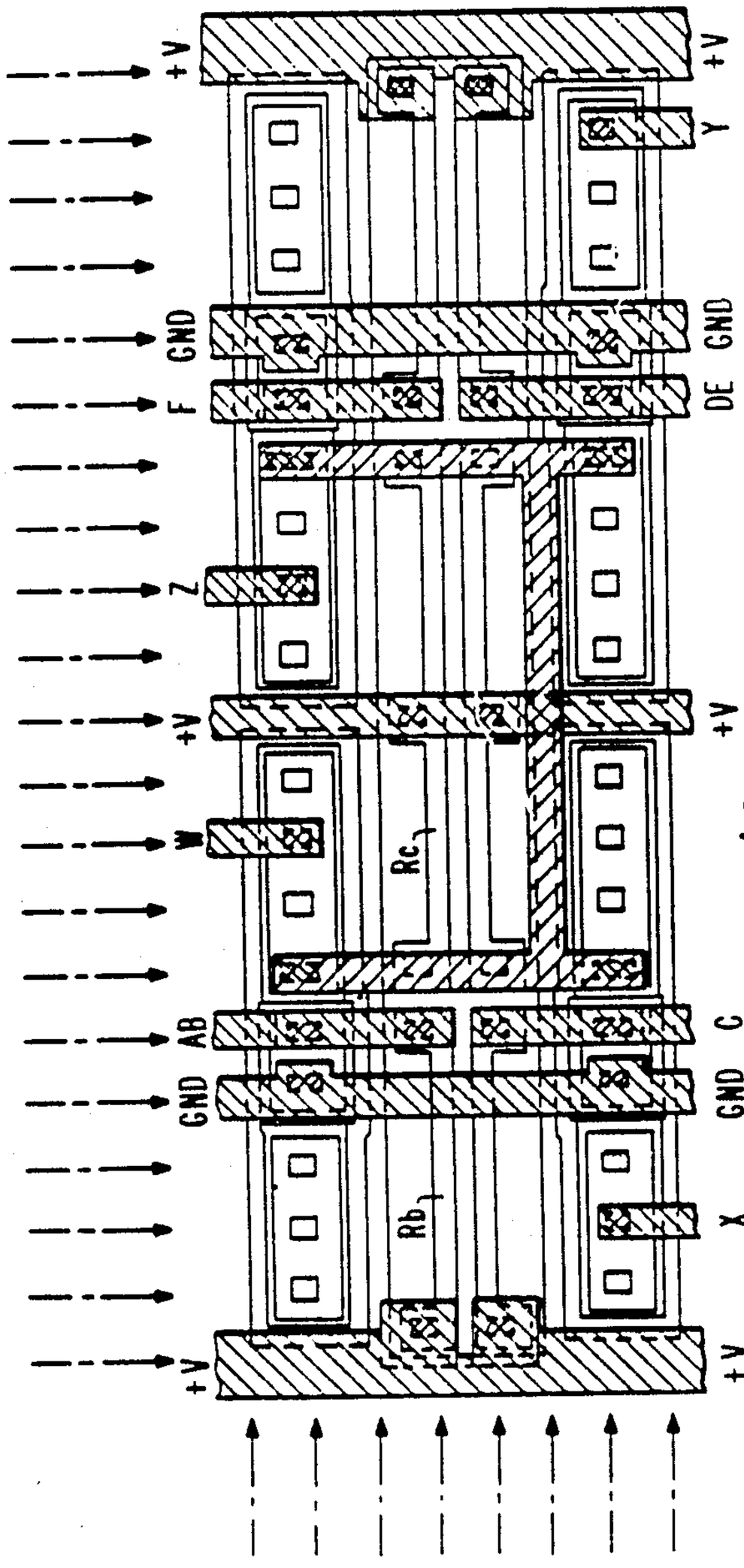


FIG. 10

SIL - 4 WAY AOI
CELL LAYOUT

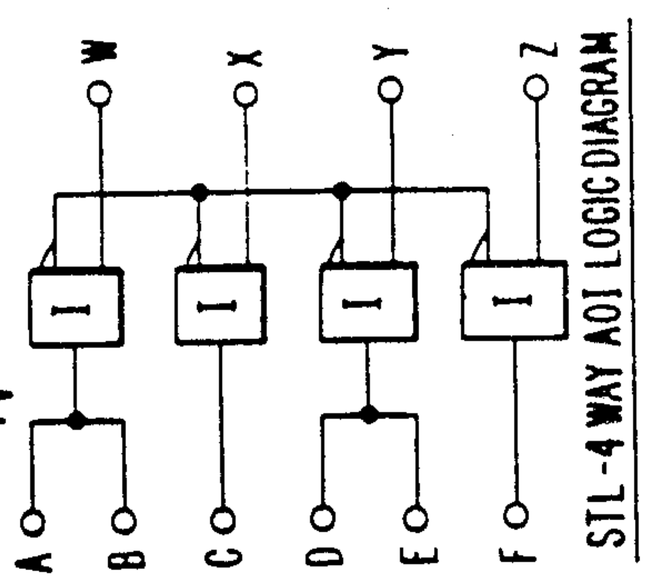


FIG. 10A

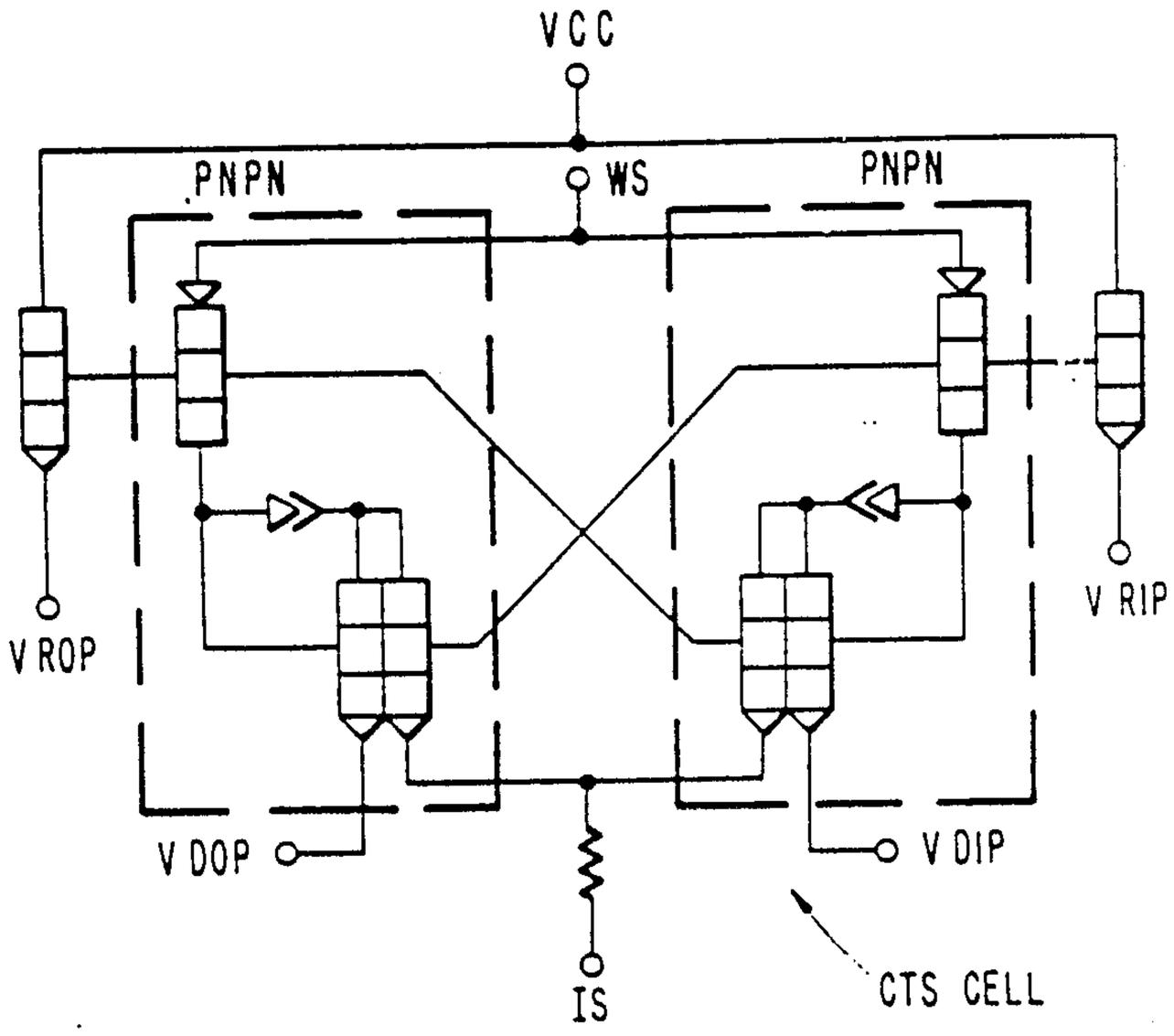

VCC
PNPN
WS
PNPN
V ROP
V RIP
V DOP
V DIP
IS
CTS CELL

FIG. 11

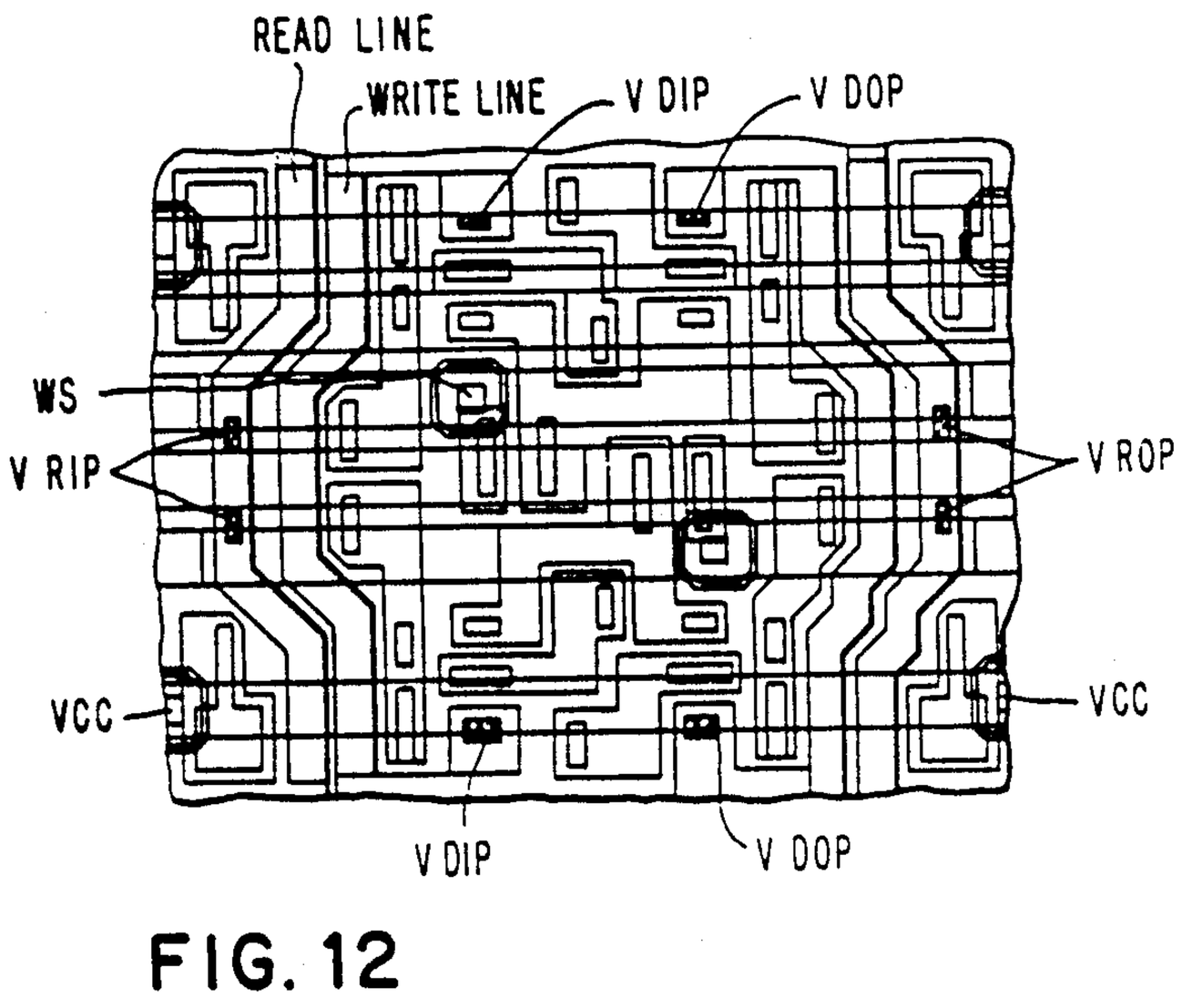

READ LINE
WRITE LINE
V DIP
V DOP
WS
V RIP
V ROP
VCC
VCC
V DIP
V DOP

FIG. 12

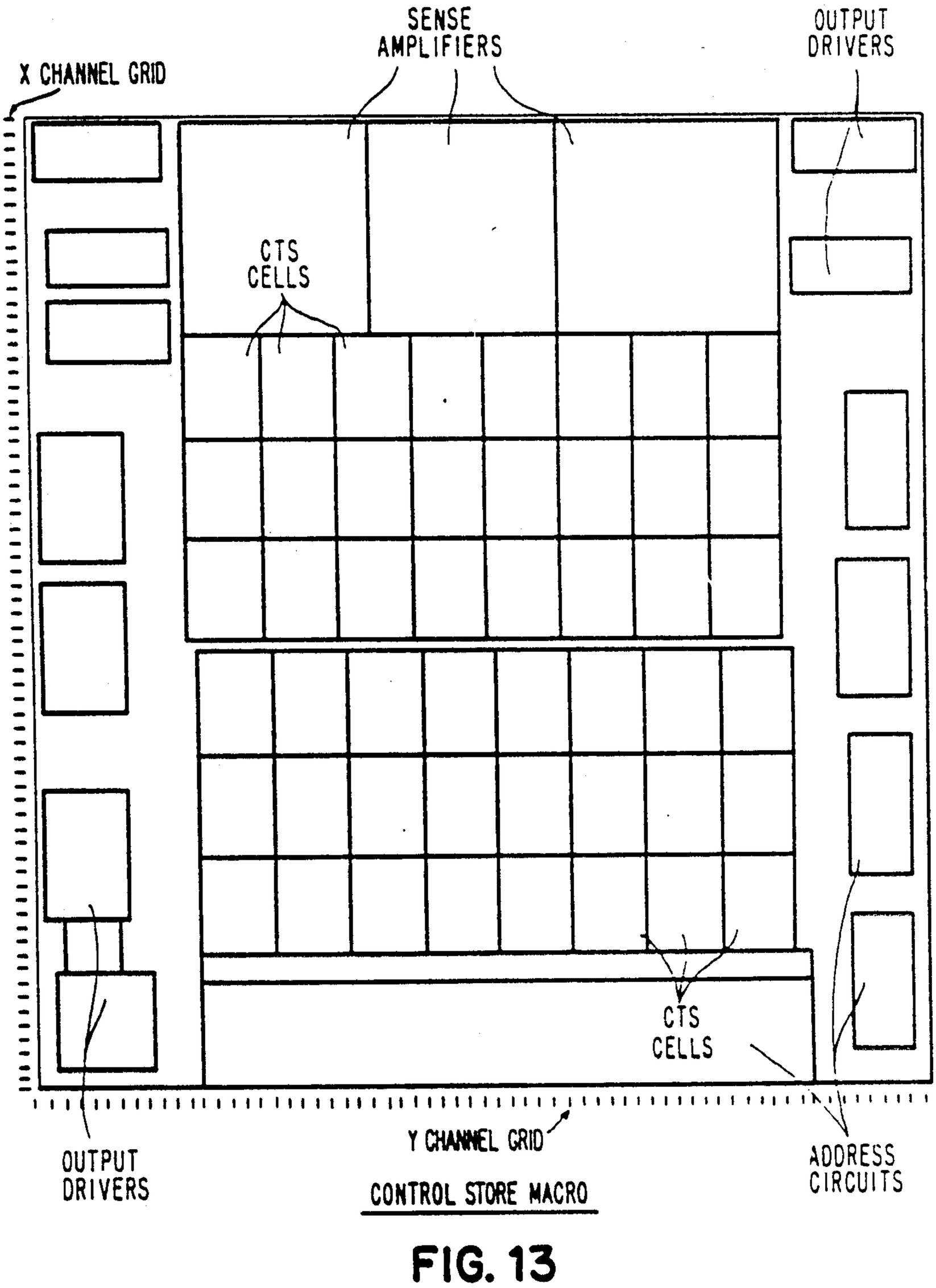

SENSE AMPLIFIERS
OUTPUT DRIVERS
X CHANNEL GRID
CTS CELLS
CTS CELLS
OUTPUT DRIVERS
Y CHANNEL GRID
ADDRESS CIRCUITS
CONTROL STORE MACRO

FIG. 13

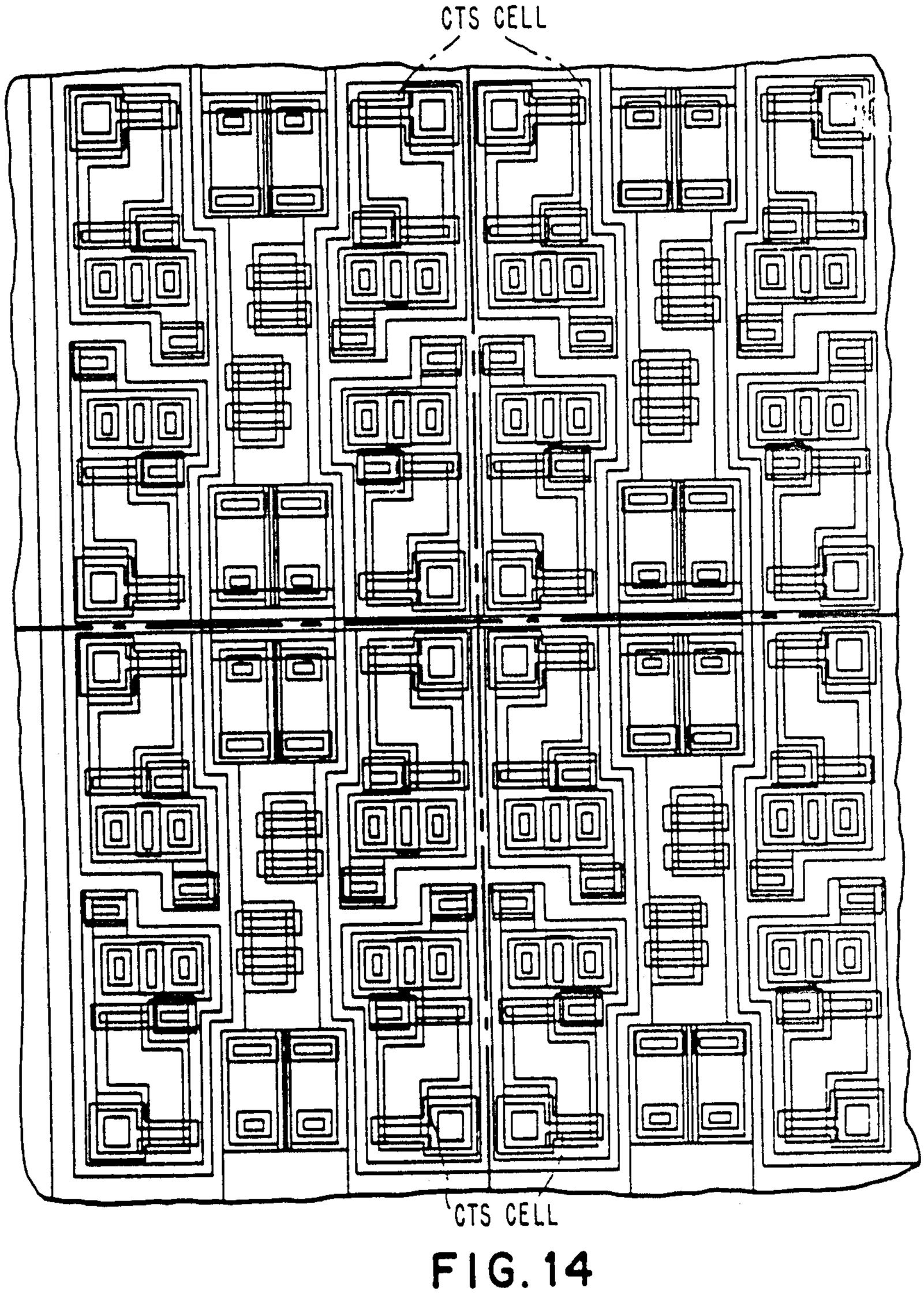


FIG. 14

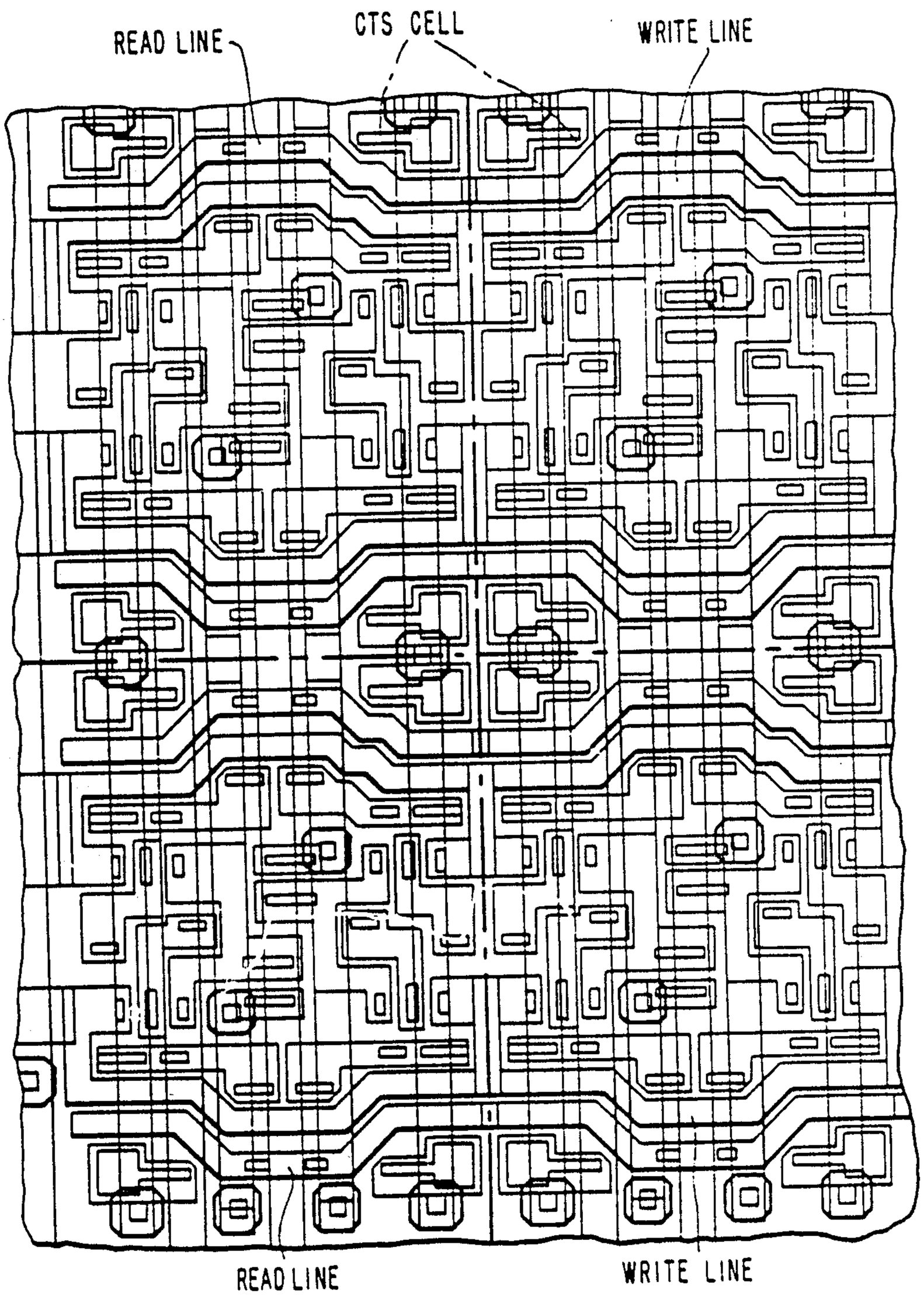
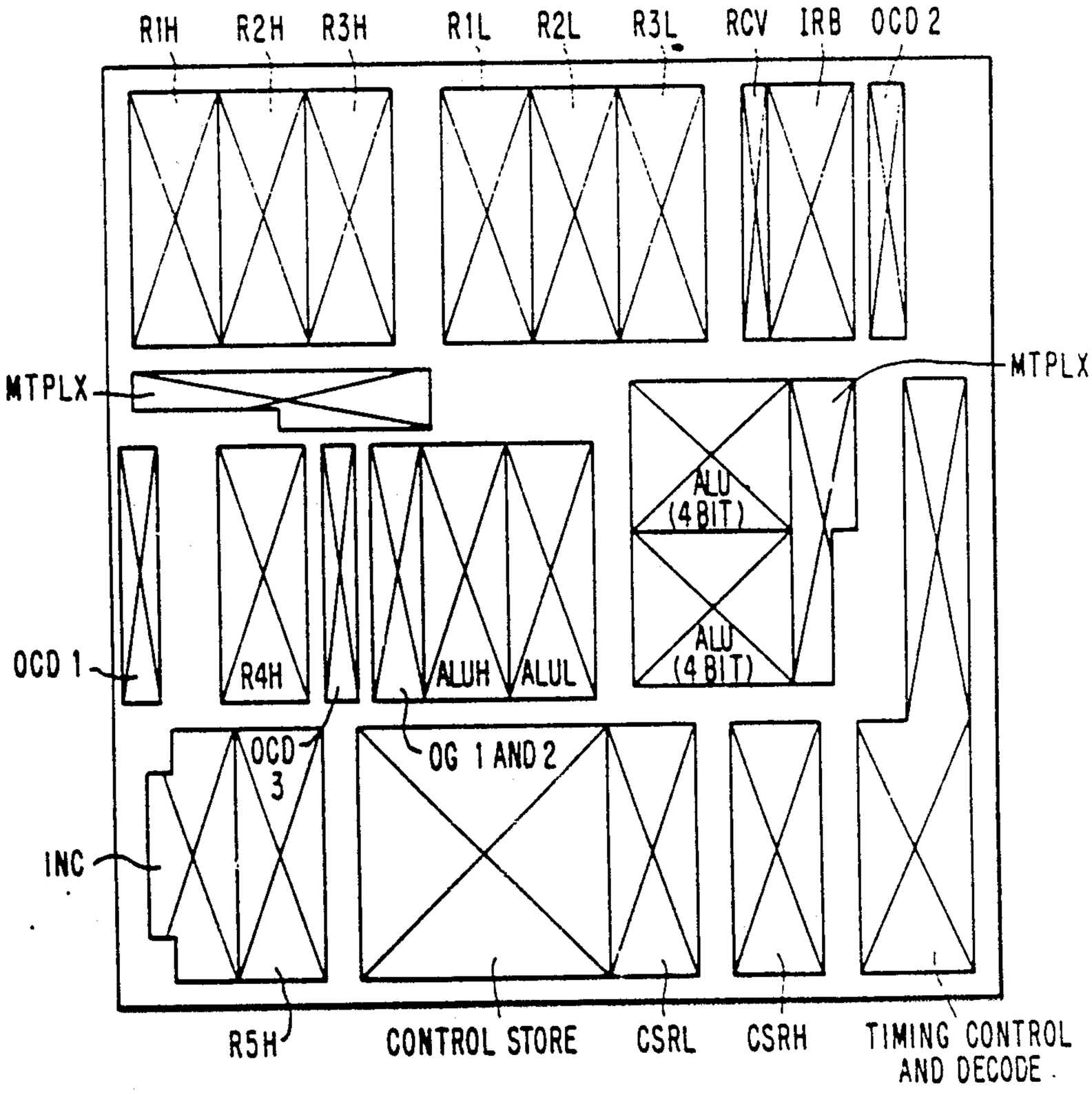


FIG.15



MICROPROCESSOR CHIP LAYOUT

FIG. 16