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(54) **MULTIPLE PLATED VIA ARRAYS OF DIFFERENT WIRE HEIGHTS ON A SAME SUBSTRATE**

(58) **Field of Classification Search**
CPC H01L 25/0657; H01L 21/4853; H01L 23/3675; H01L 23/42; H01L 23/481;
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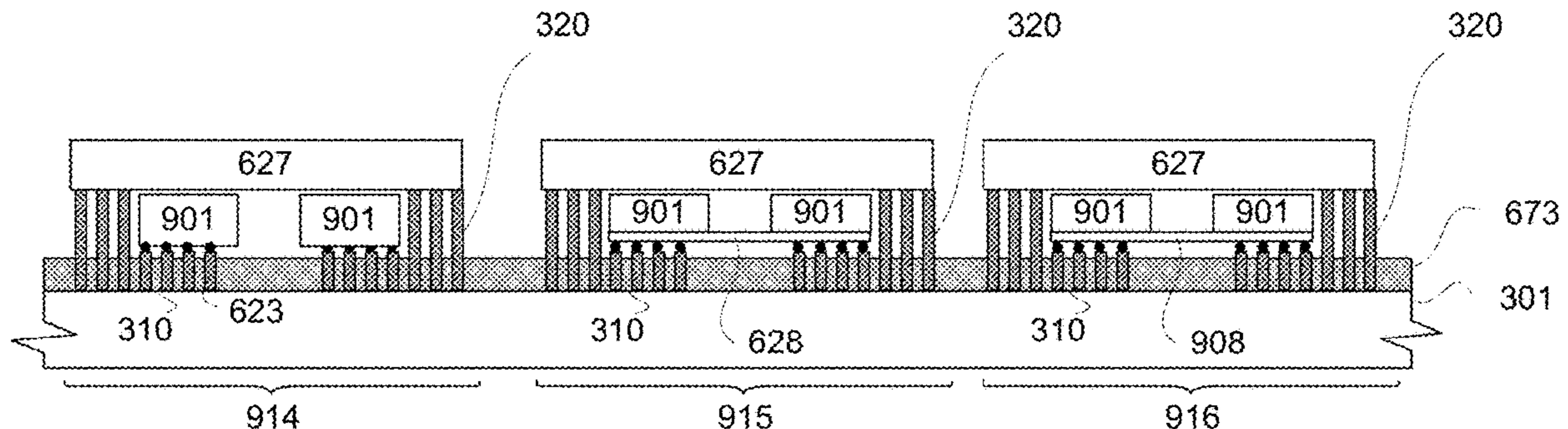
(63) Continuation of application No. 16/008,531, filed on Jun. 14, 2018, now Pat. No. 10,290,613, which is a
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(57) **ABSTRACT**

(51) **Int. Cl.**
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Apparatus(es) and method(s) relate generally to via arrays on a substrate. In one such apparatus, the substrate has a conductive layer. First plated conductors are in a first region extending from a surface of the conductive layer. Second plated conductors are in a second region extending from the surface of the conductive layer. The first plated conductors and the second plated conductors are external to the first substrate. The first region is disposed at least partially within the second region. The first plated conductors are of a first height. The second plated conductors are of a second height greater than the first height. A second substrate is coupled to first ends of the first plated conductors. The second substrate has at least one electronic component coupled thereto. A die
(Continued)

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is coupled to second ends of the second plated conductors.
The die is located over the at least one electronic component.

43 Claims, 20 Drawing Sheets

Related U.S. Application Data

continuation of application No. 15/430,943, filed on Feb. 13, 2017, now Pat. No. 10,026,717, which is a continuation of application No. 14/841,381, filed on Aug. 31, 2015, now Pat. No. 9,583,456, which is a continuation-in-part of application No. 14/087,252, filed on Nov. 22, 2013, now Pat. No. 9,263,394.

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See application file for complete search history.

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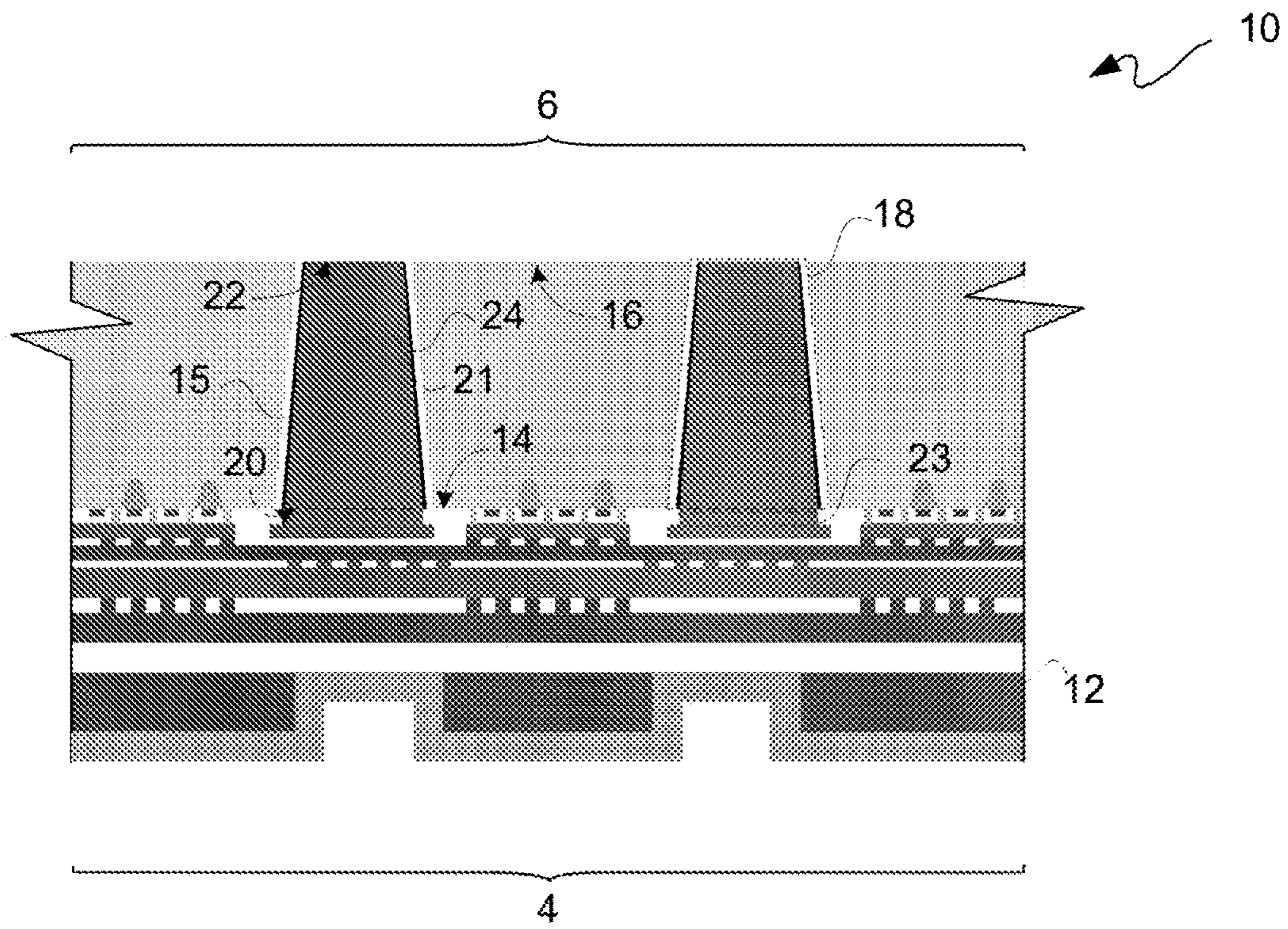


FIG. 1C

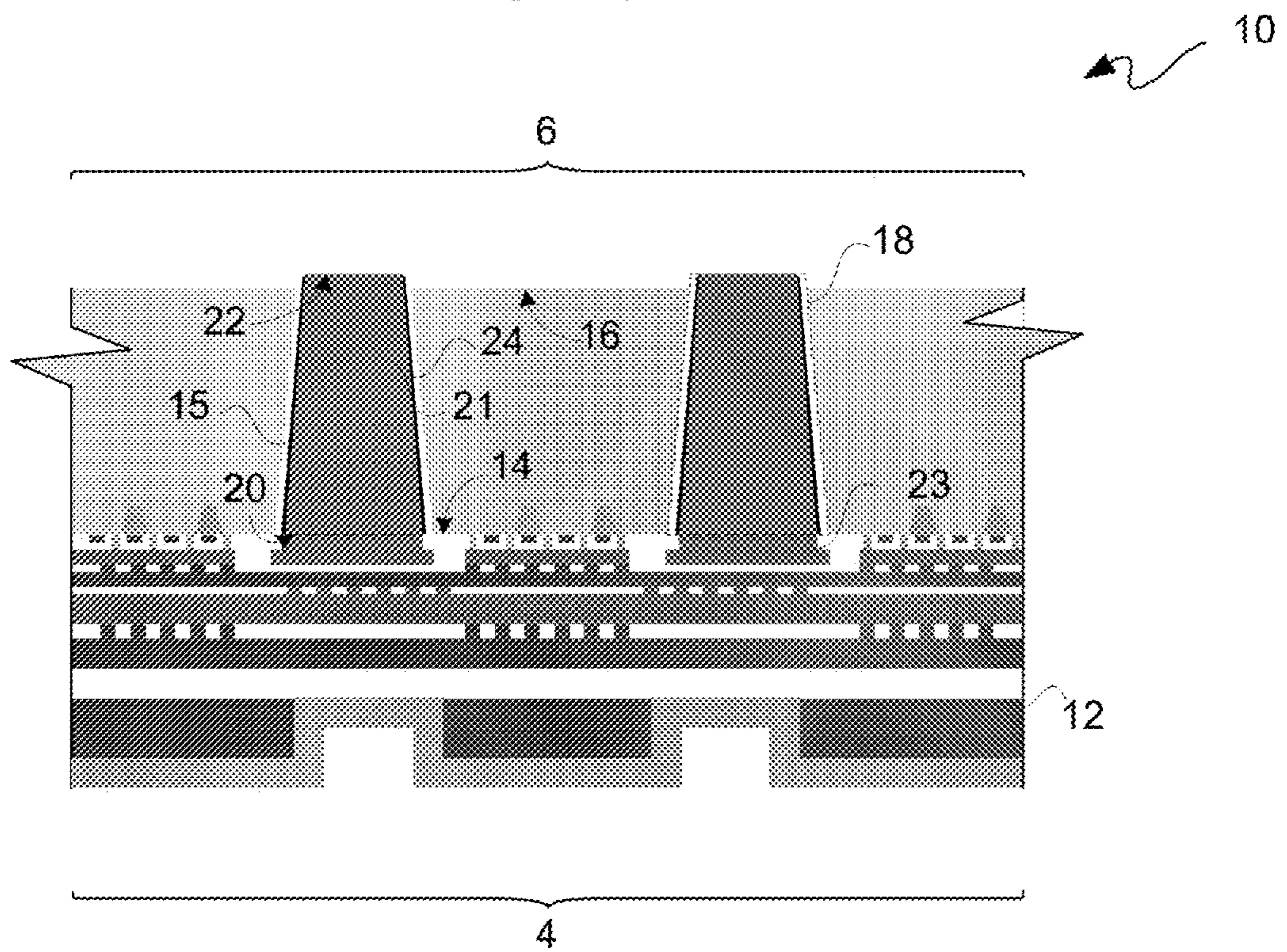


FIG. 1D

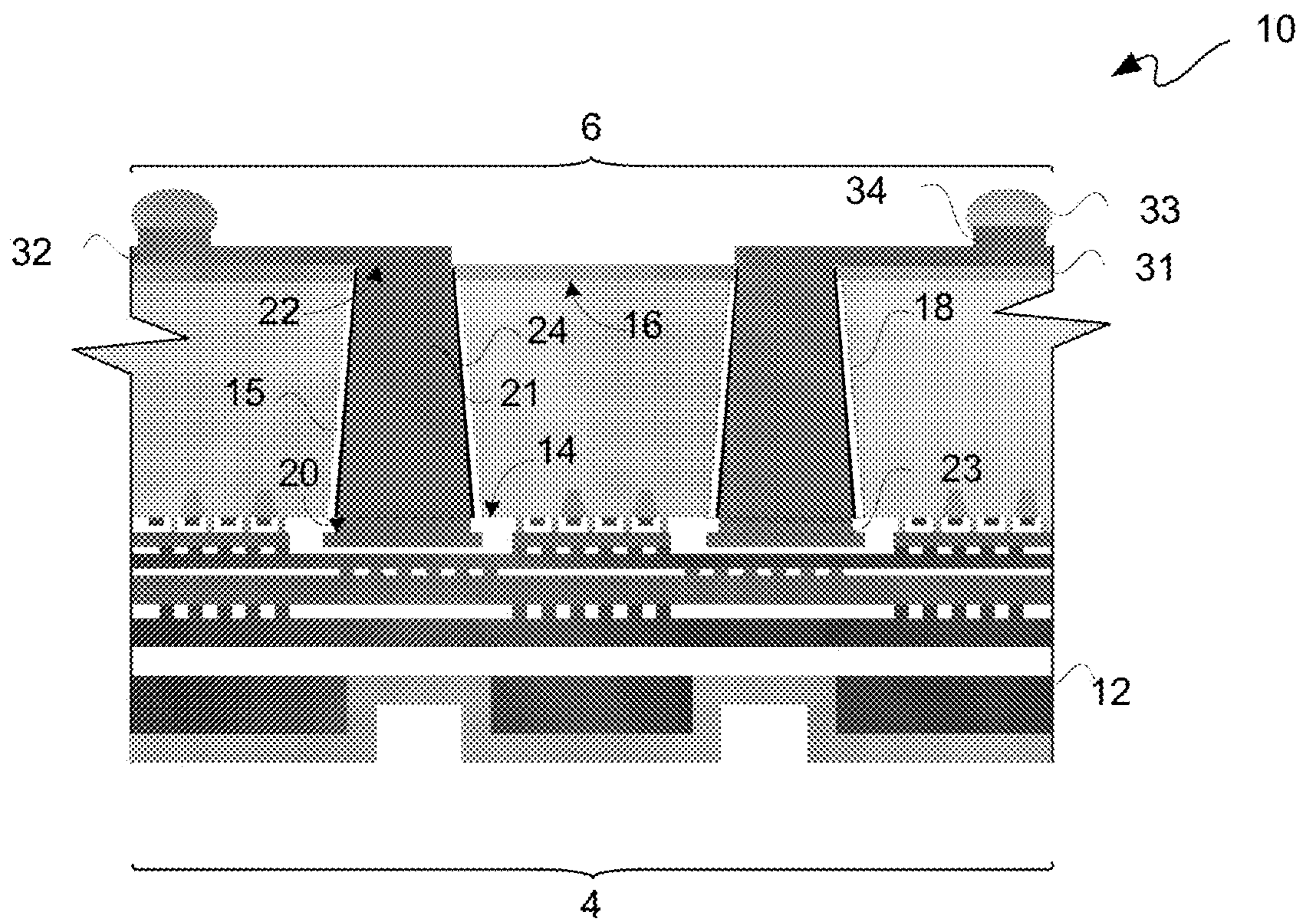


FIG. 1E

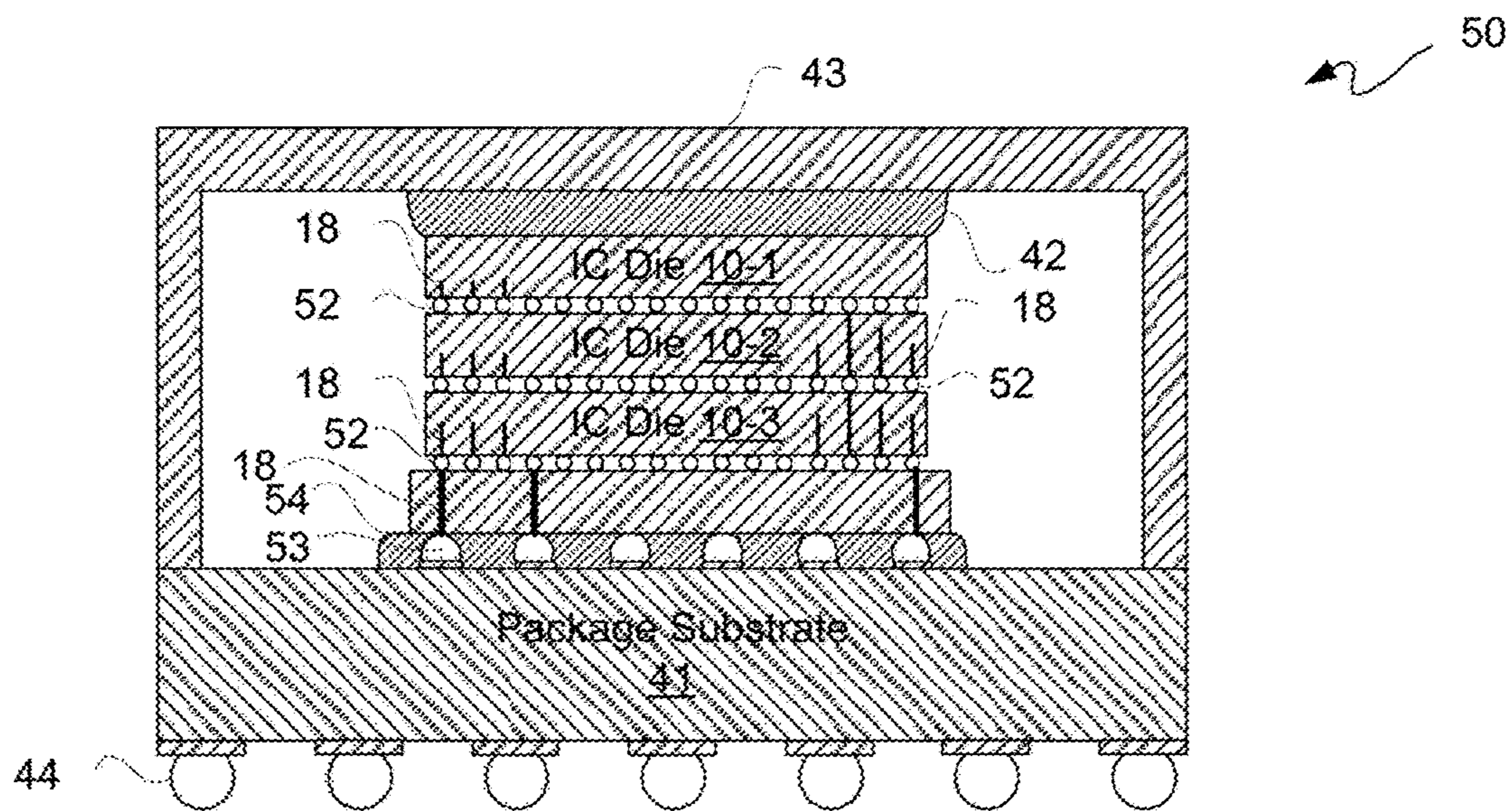


FIG. 2A

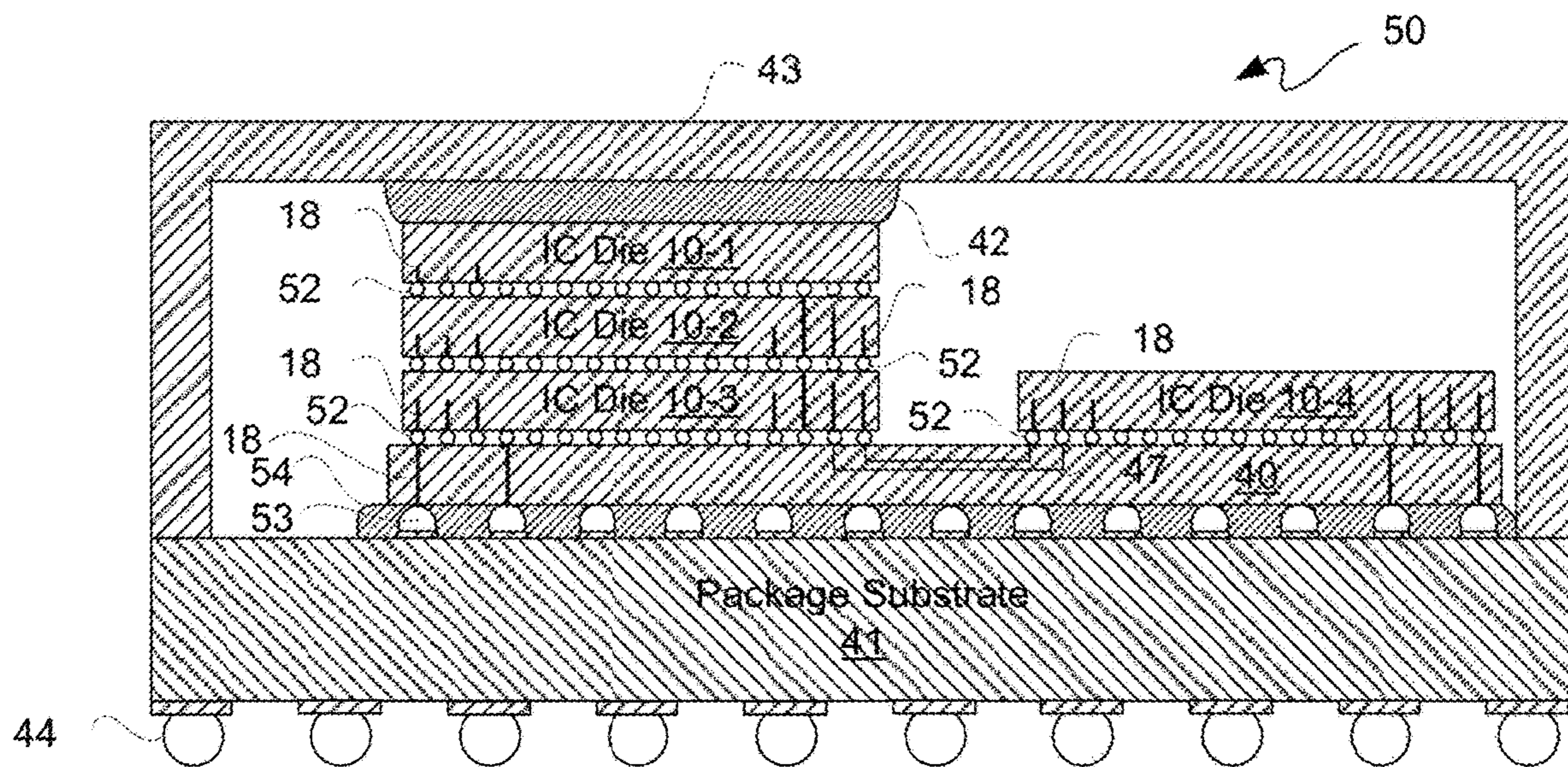


FIG. 2B

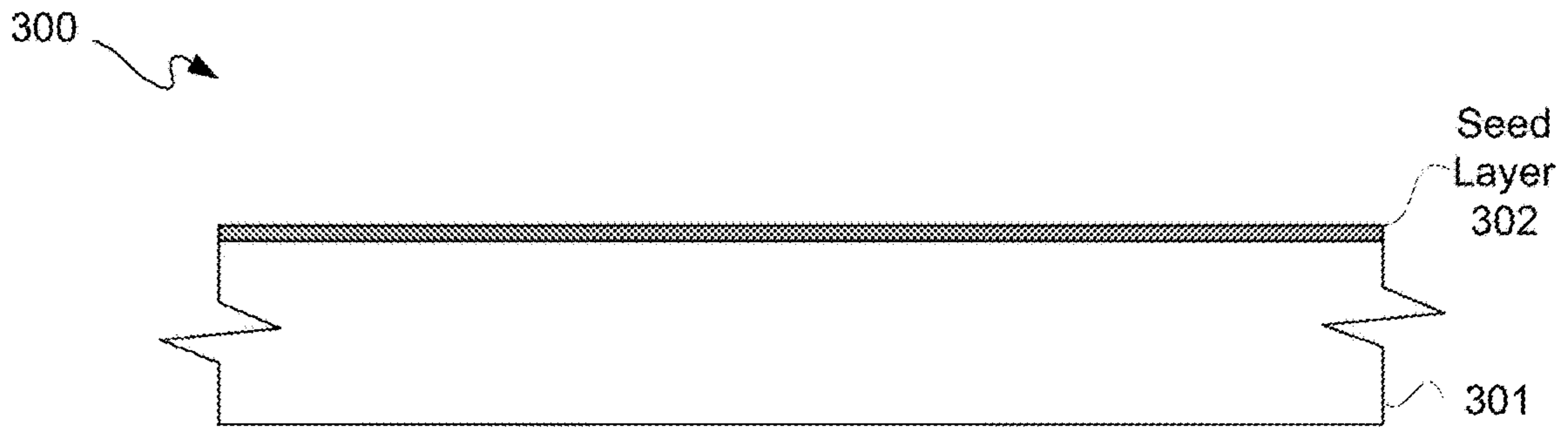


FIG. 3A

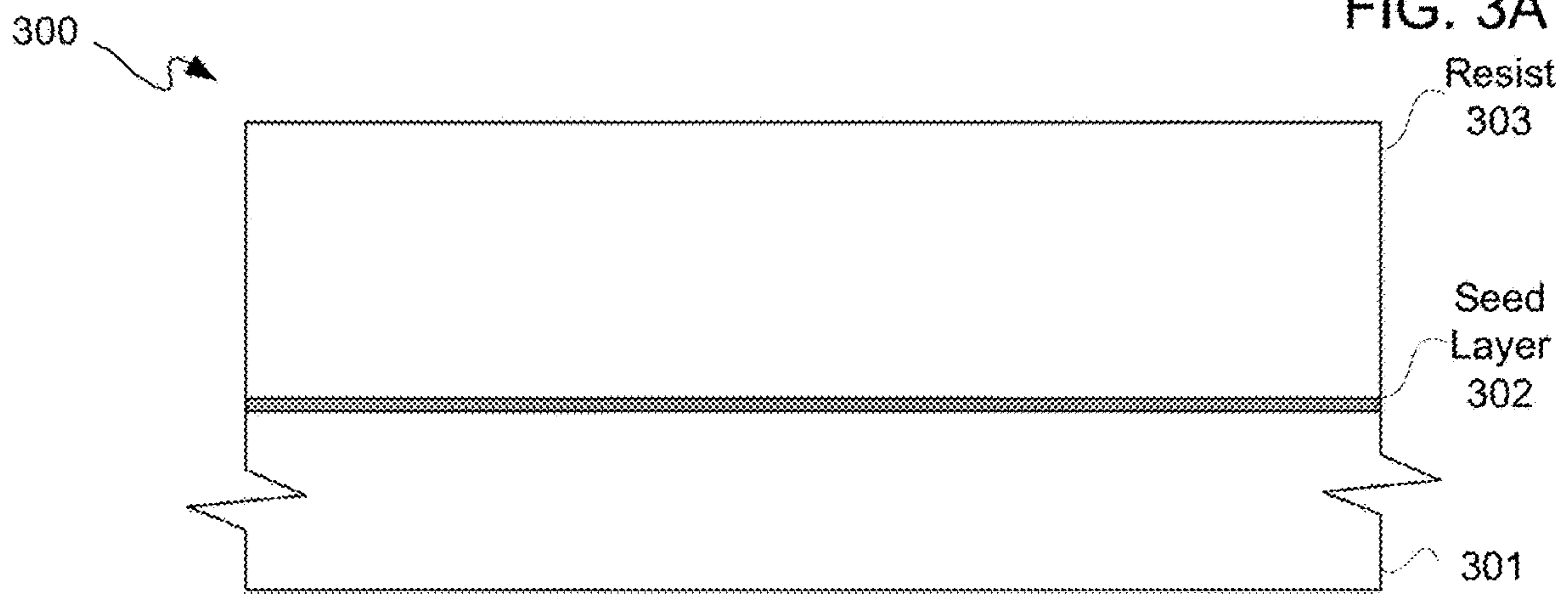


FIG. 3B

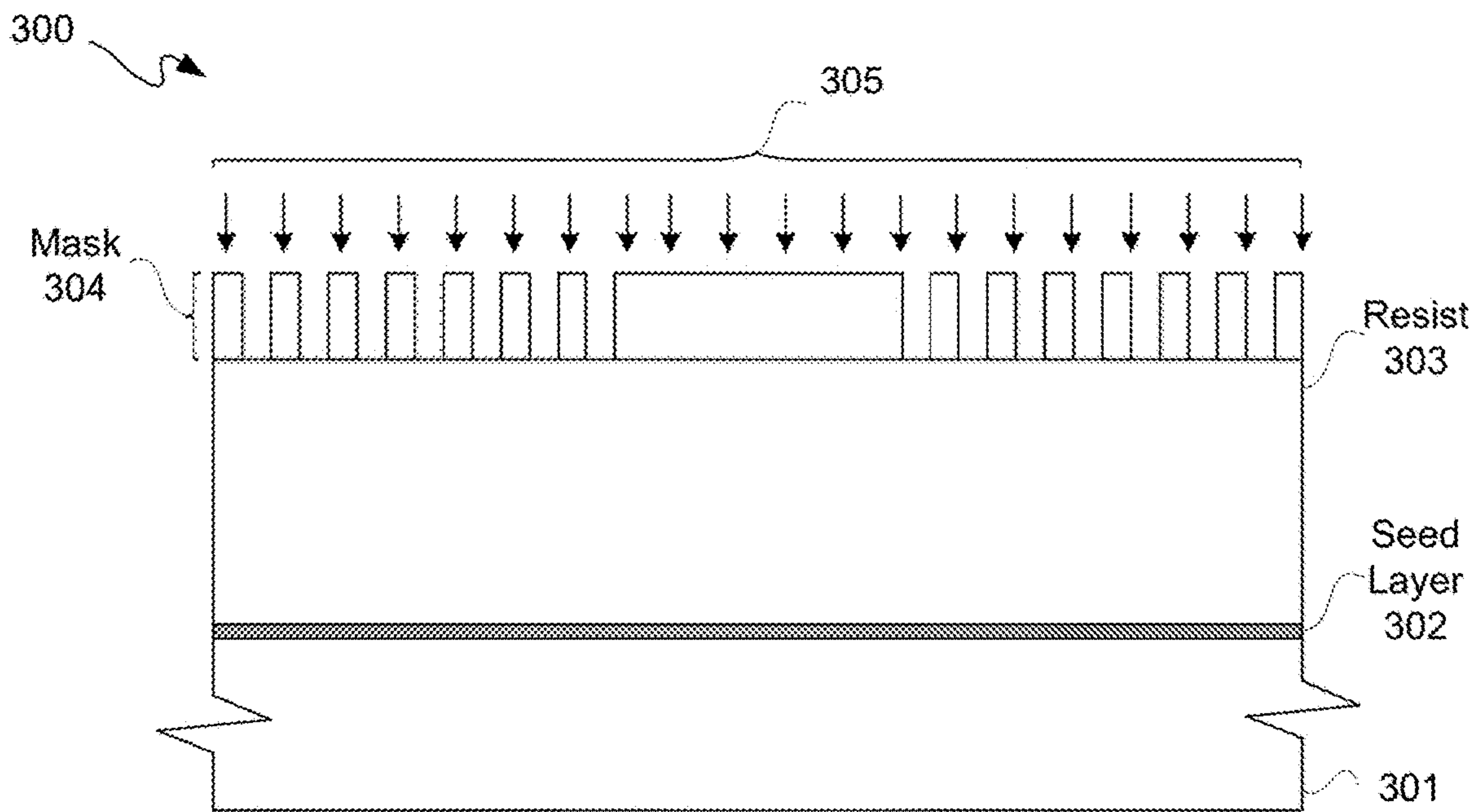


FIG. 3C

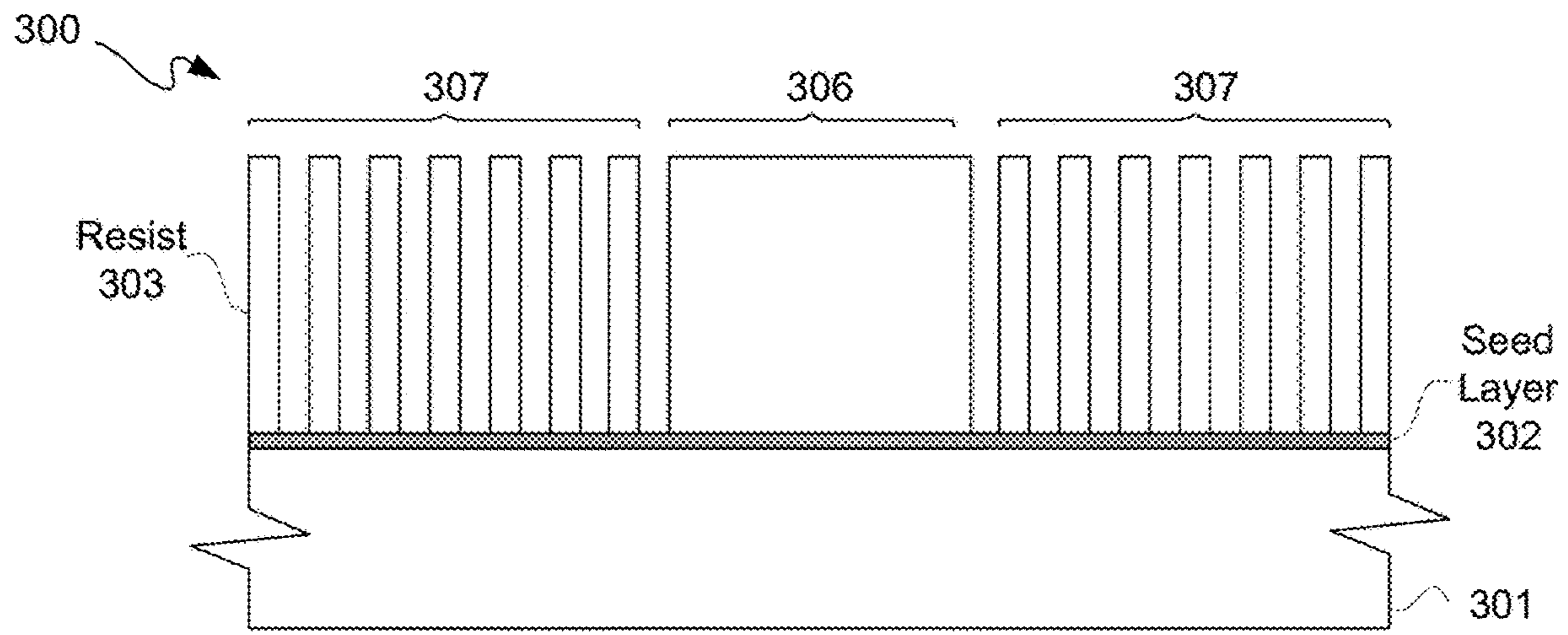


FIG. 3D

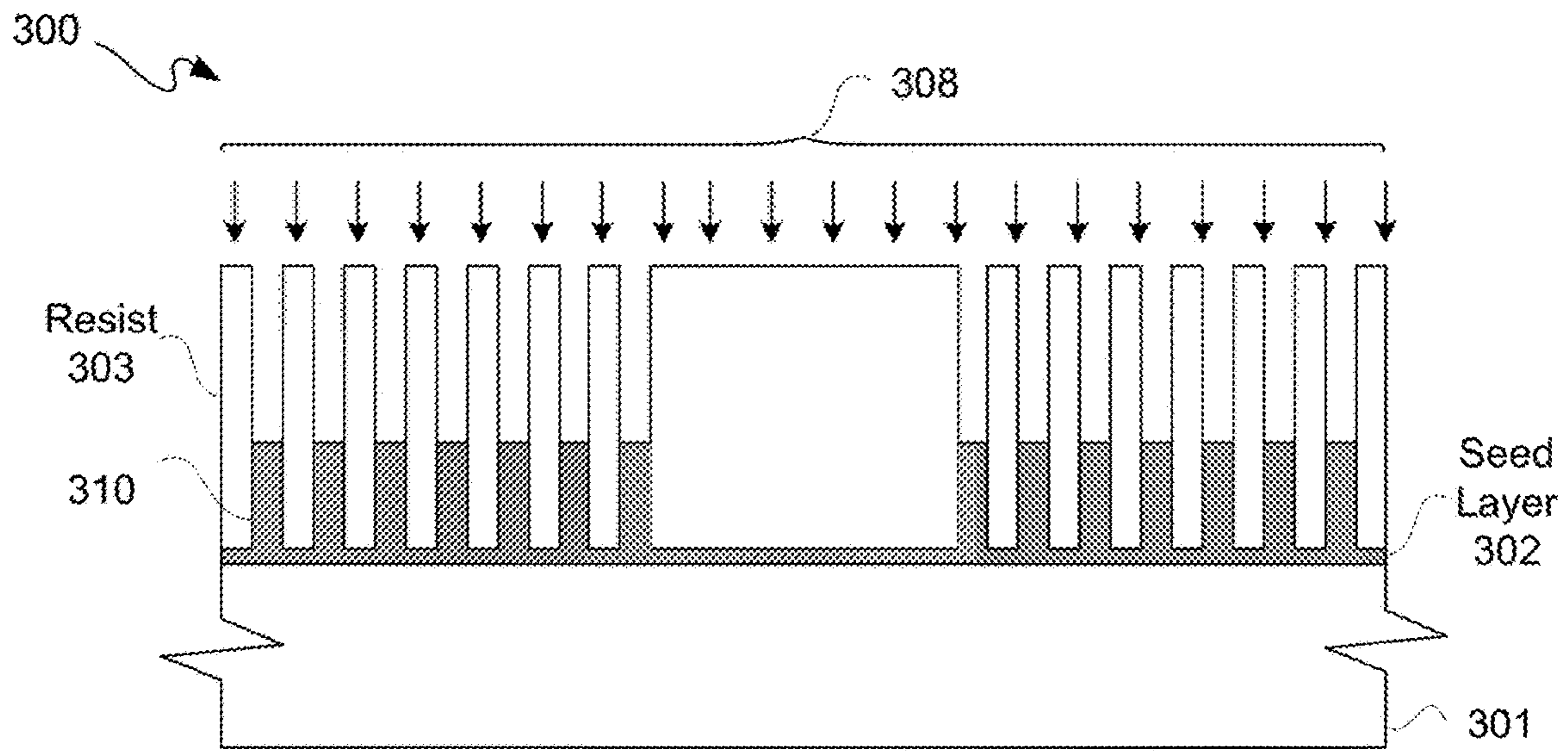


FIG. 3E

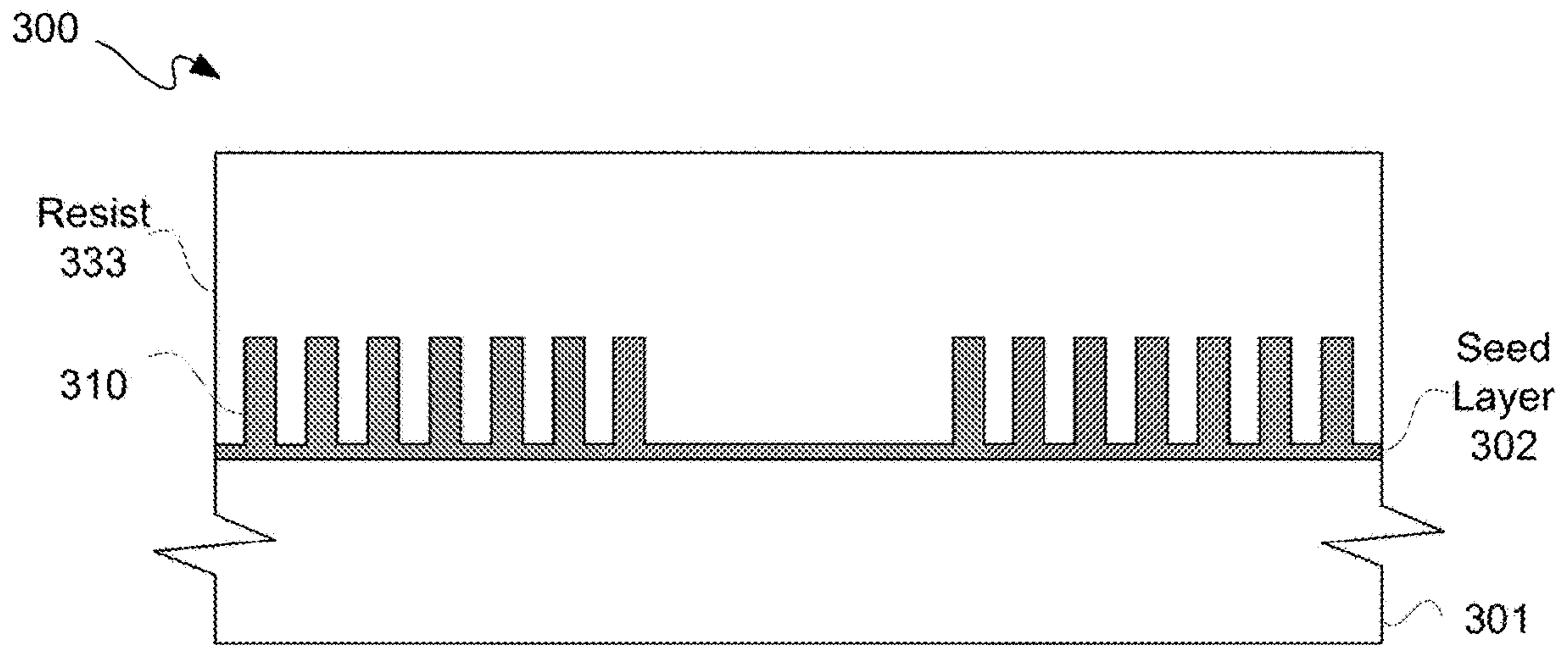


FIG. 3F

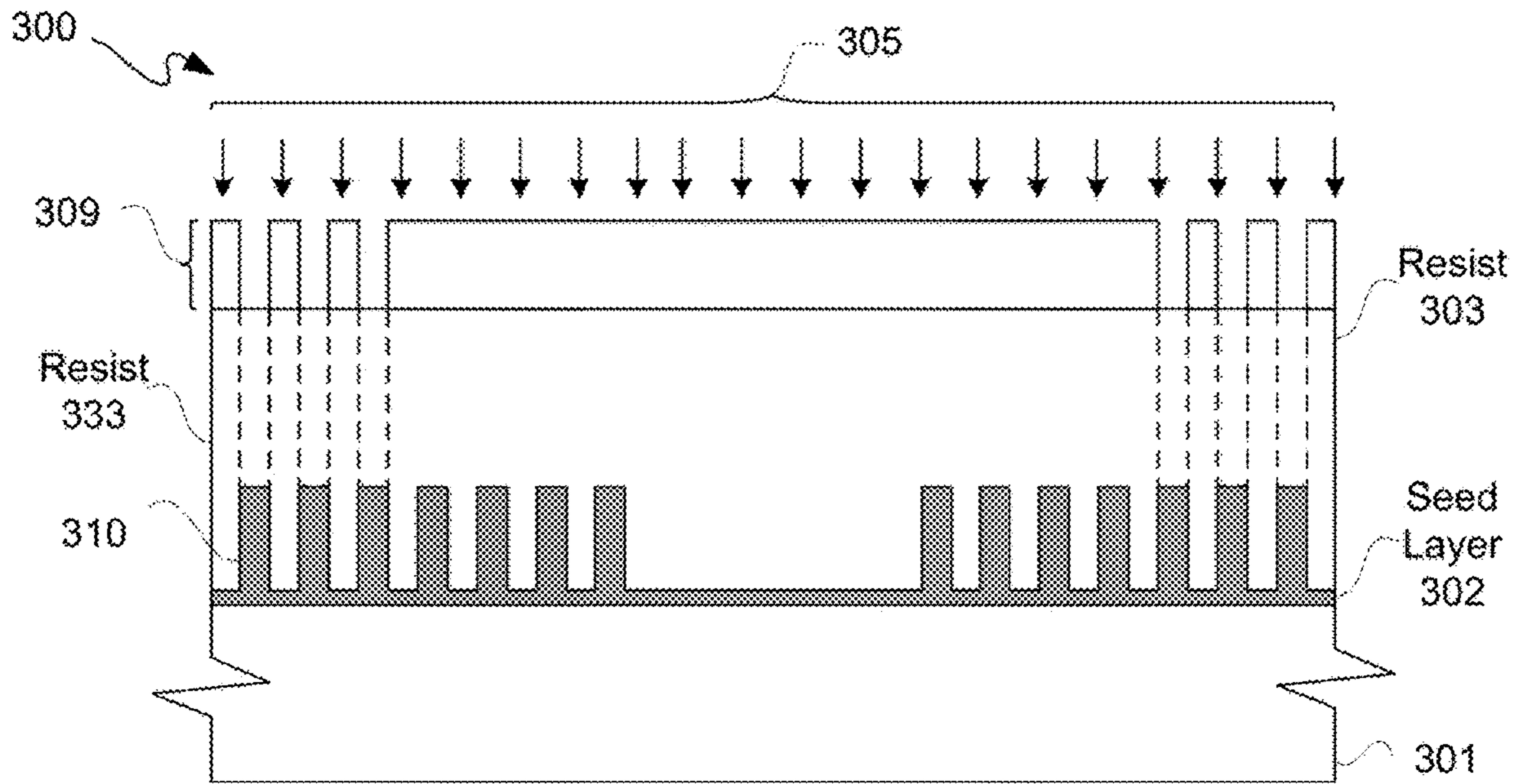


FIG. 3G

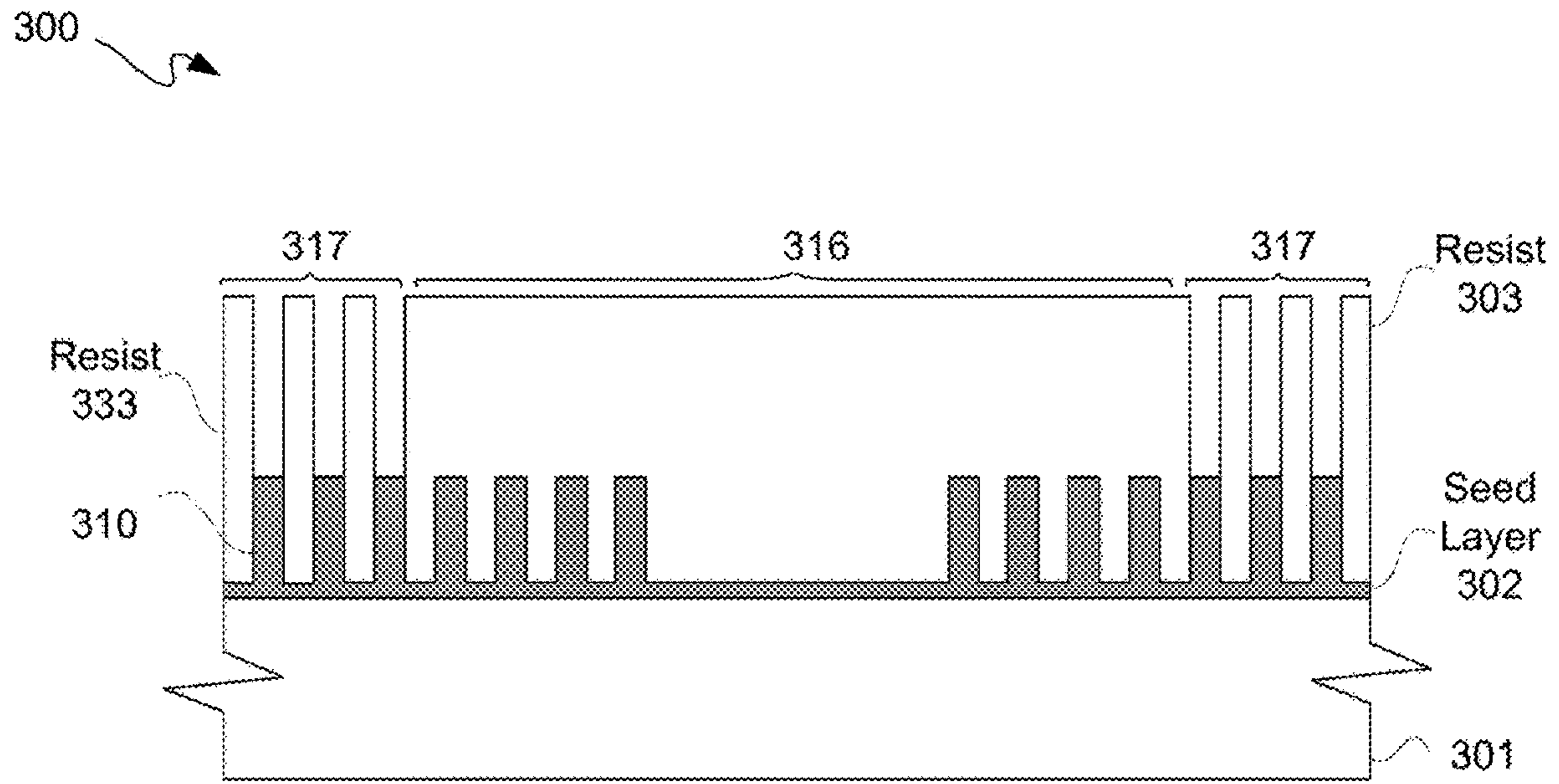


FIG. 3H

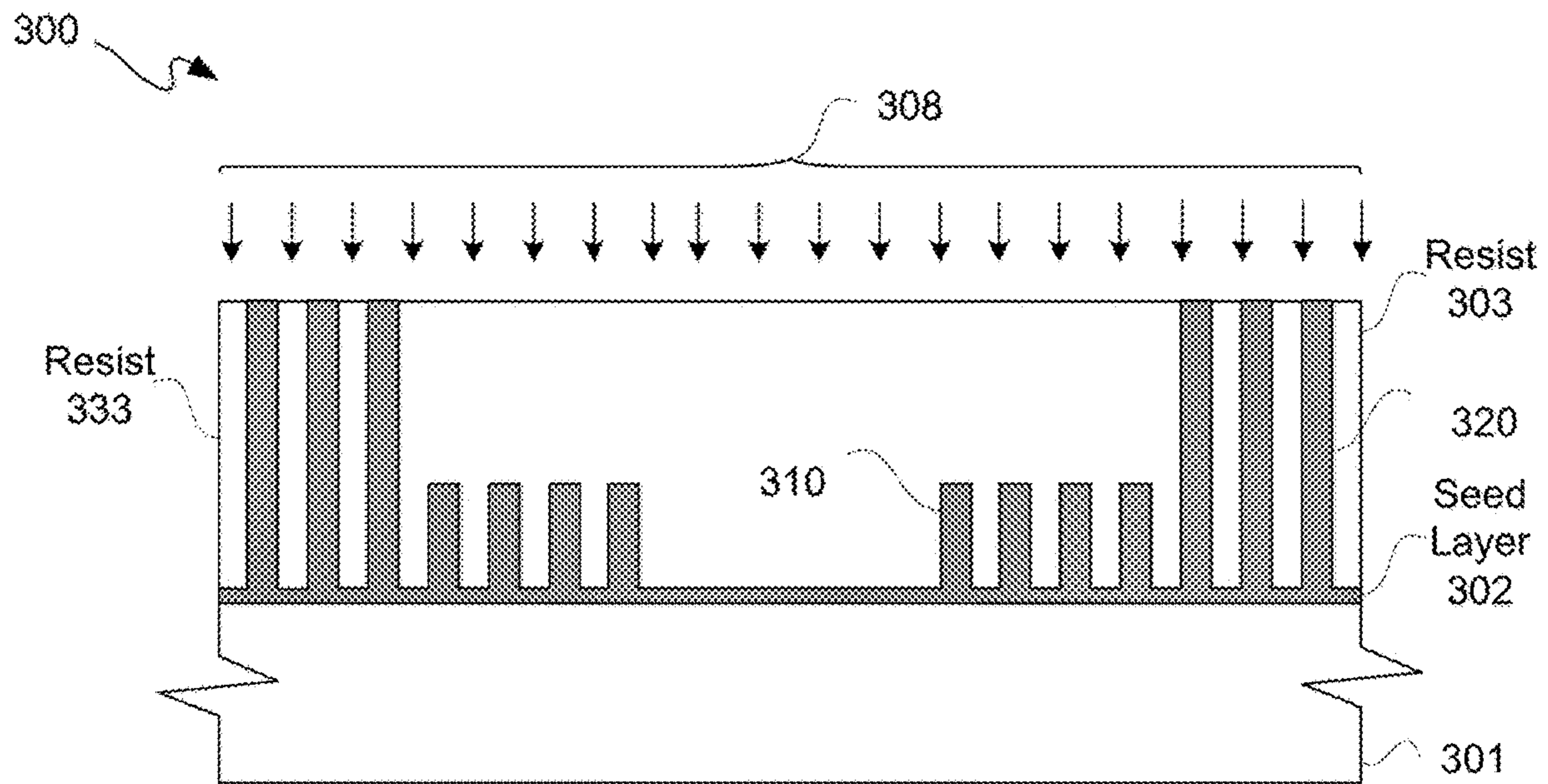


FIG. 3I

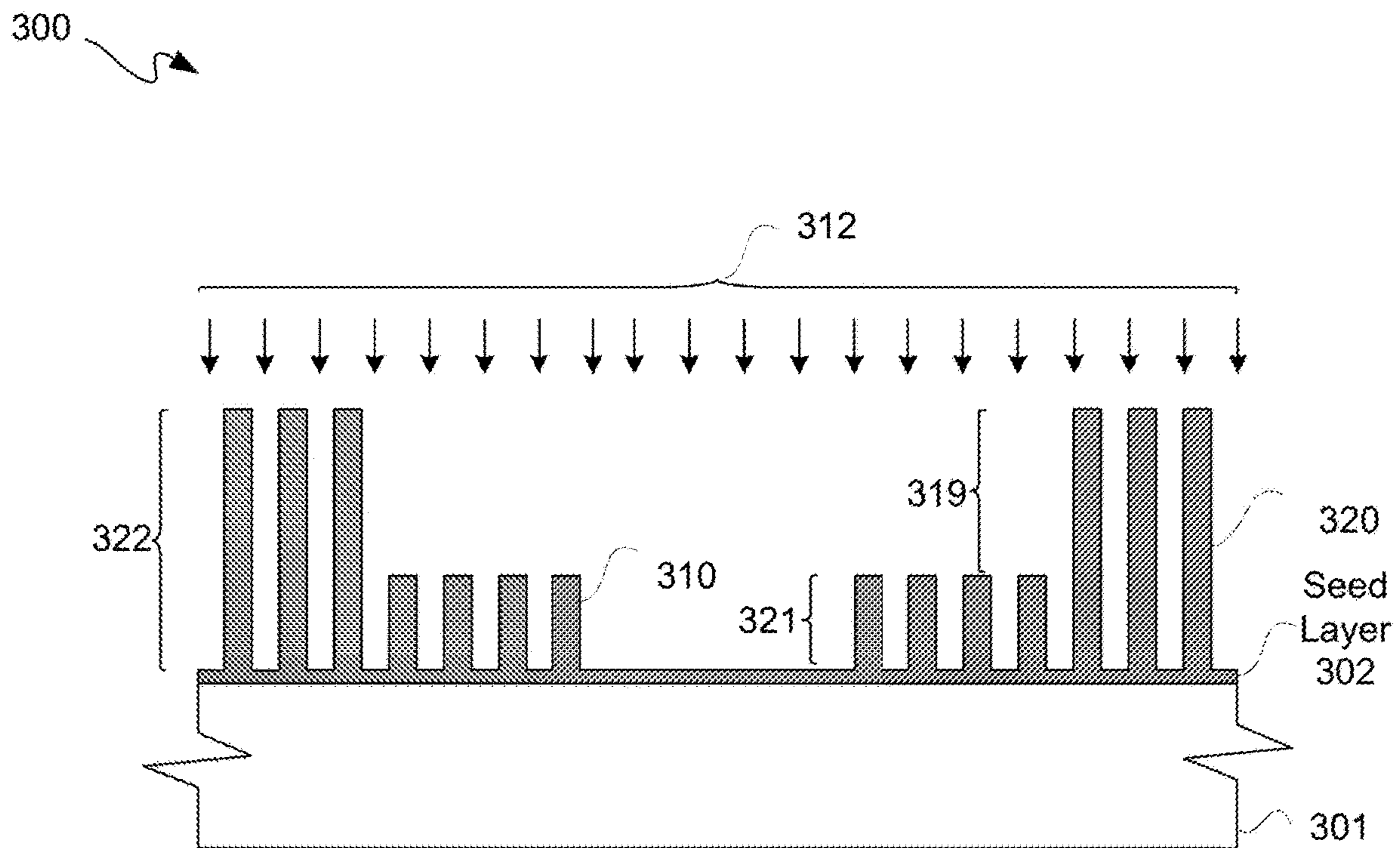


FIG. 3J

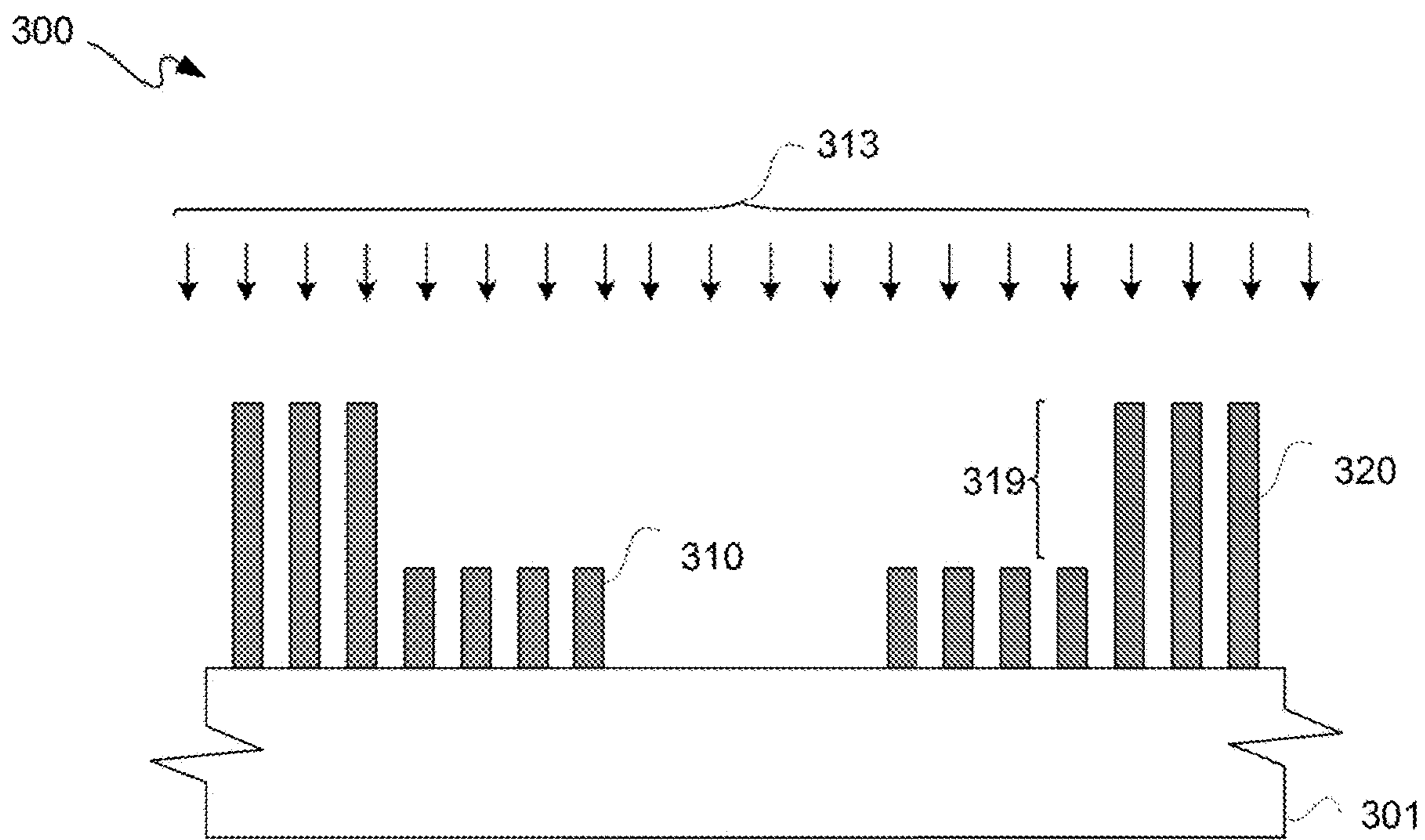


FIG. 3K

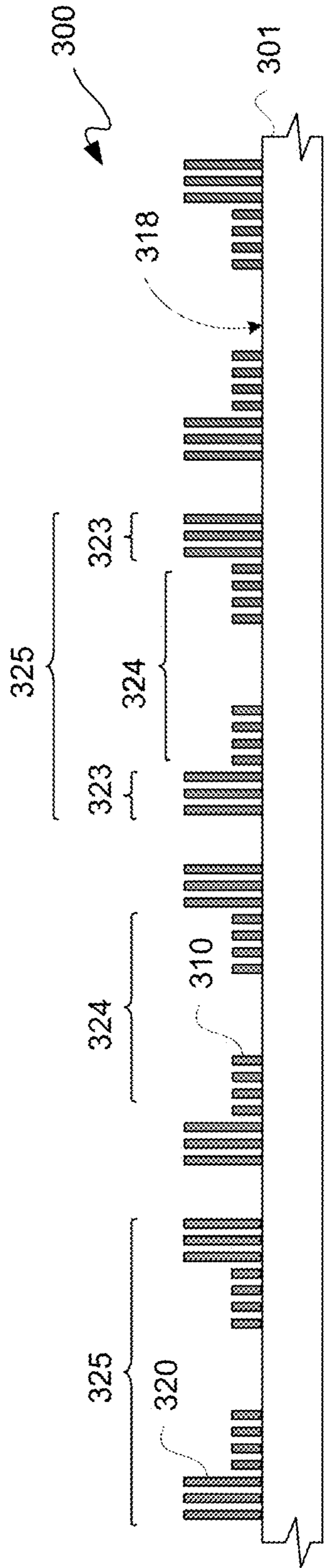


FIG. 3L

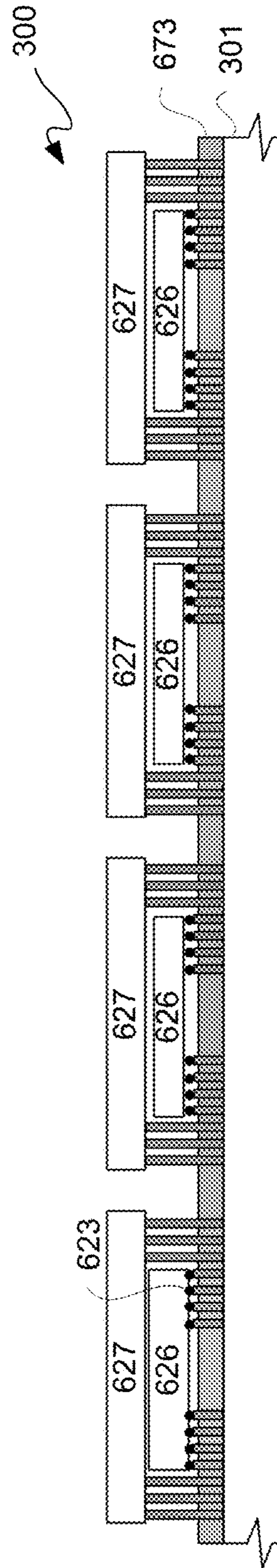


FIG. 3M

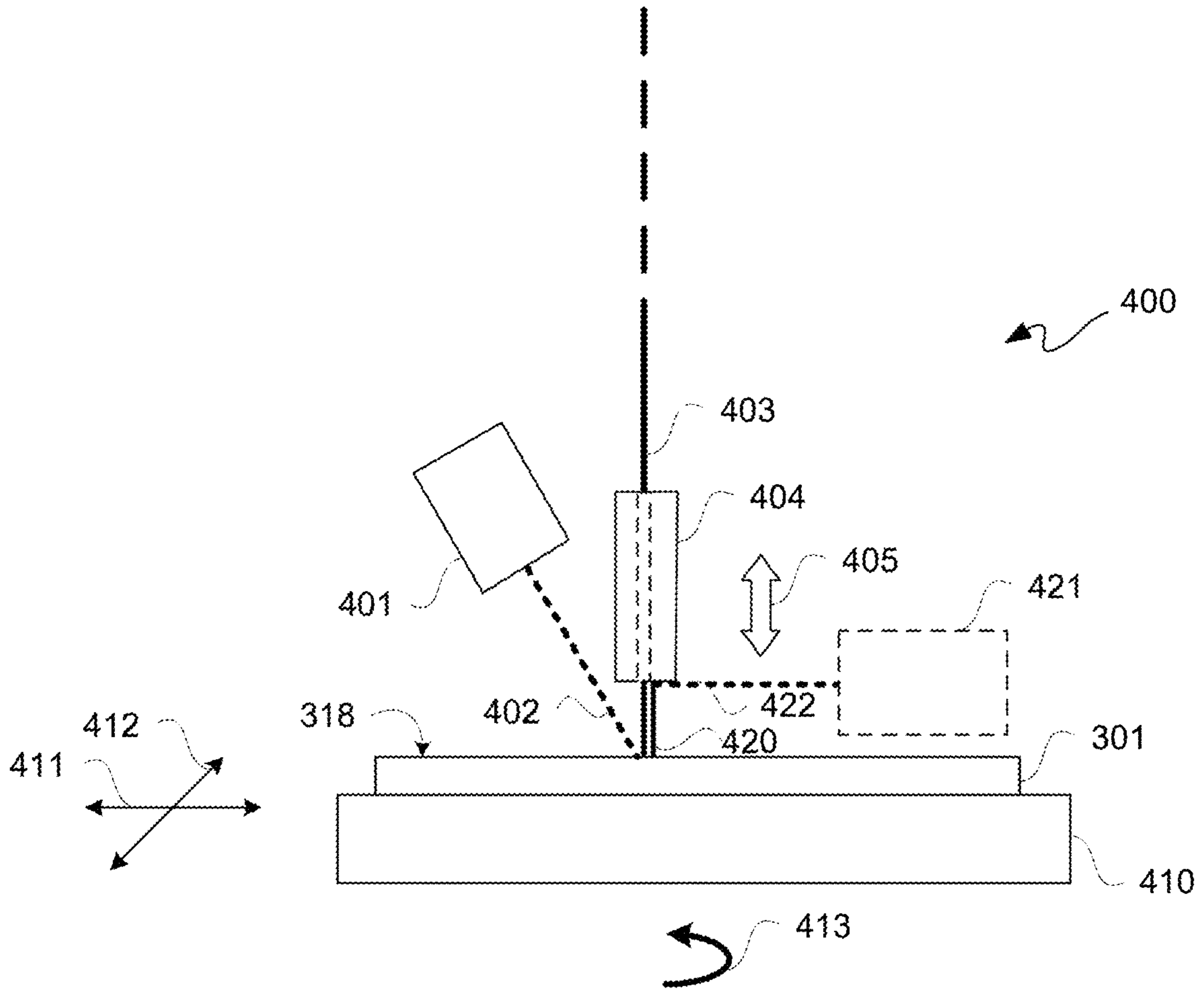


FIG. 4A

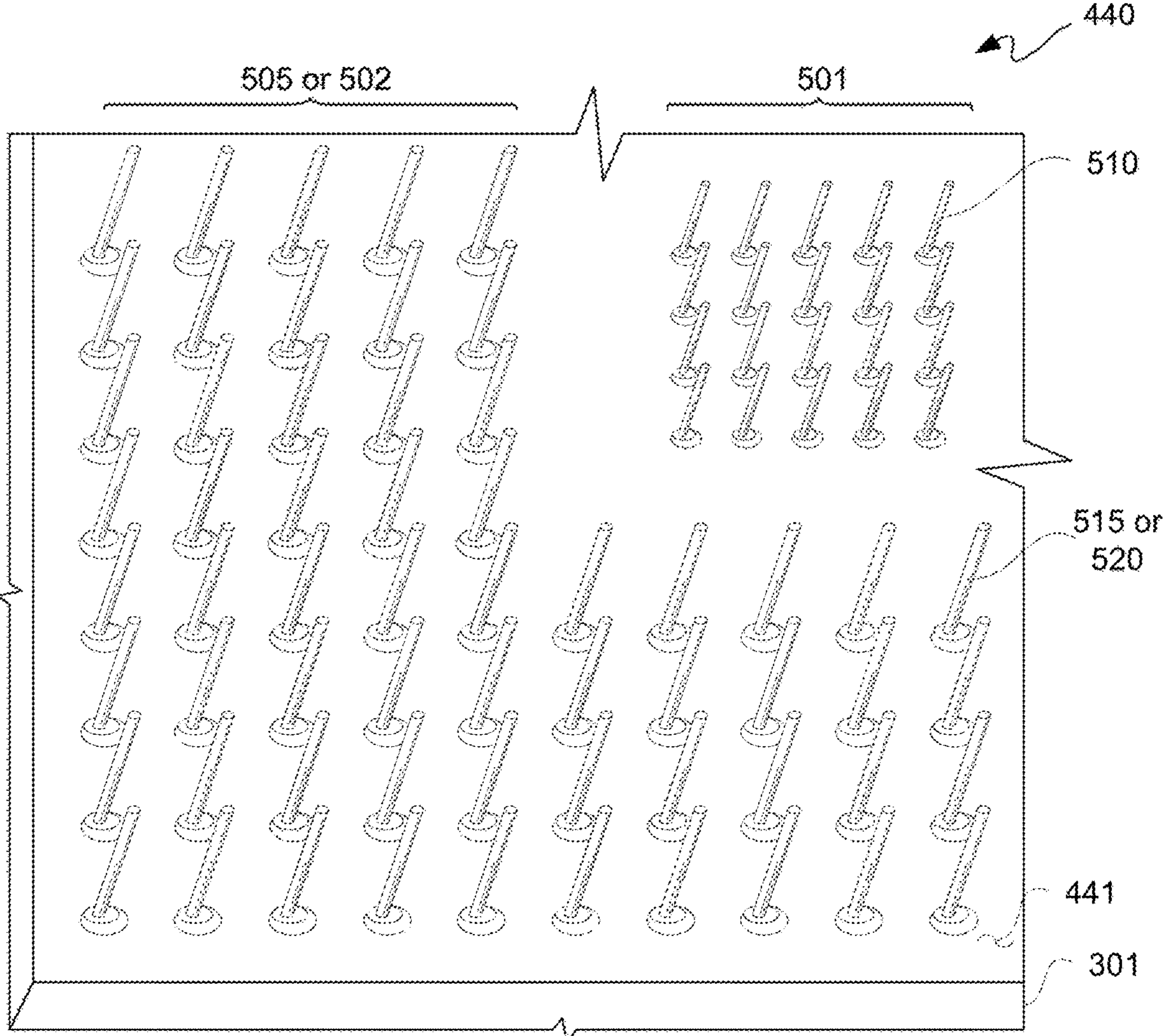


FIG. 4B

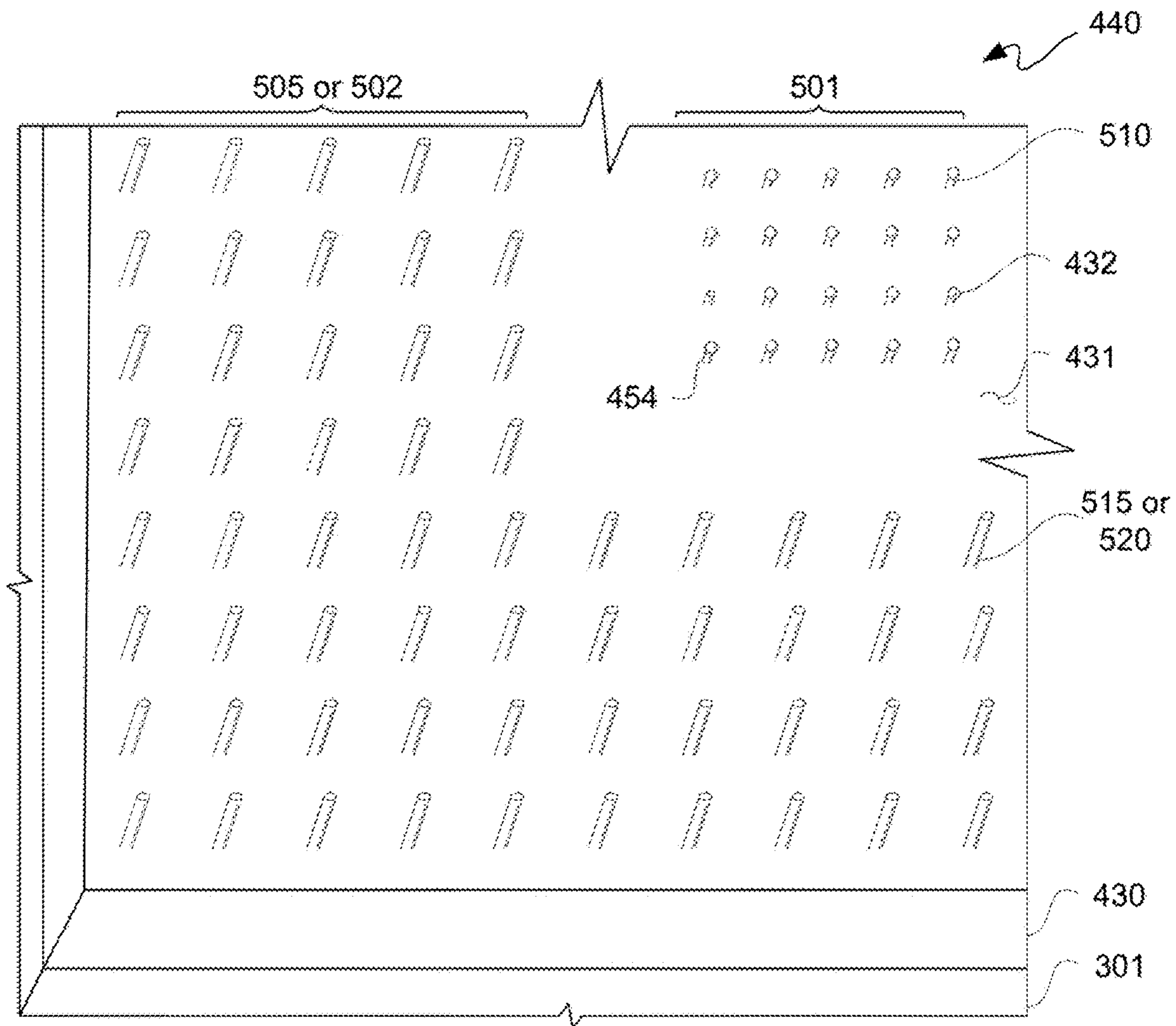


FIG. 4C

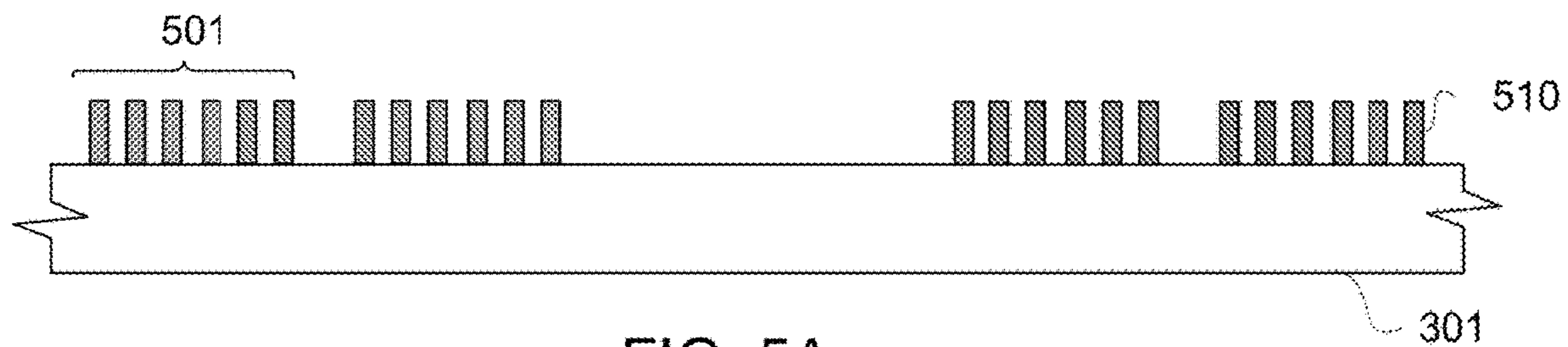


FIG. 5A

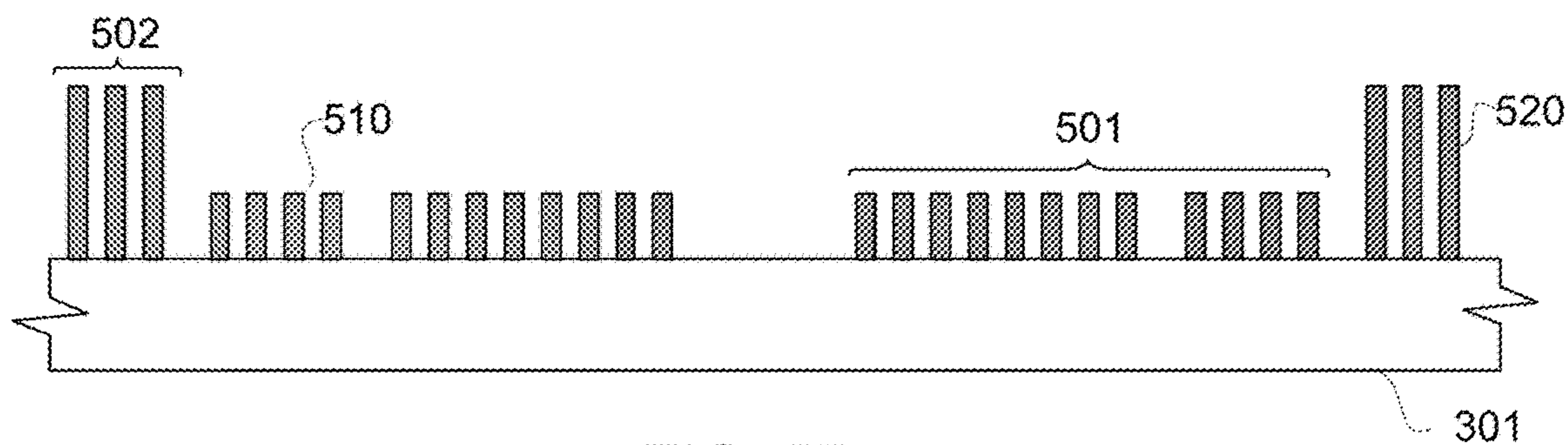


FIG. 5B

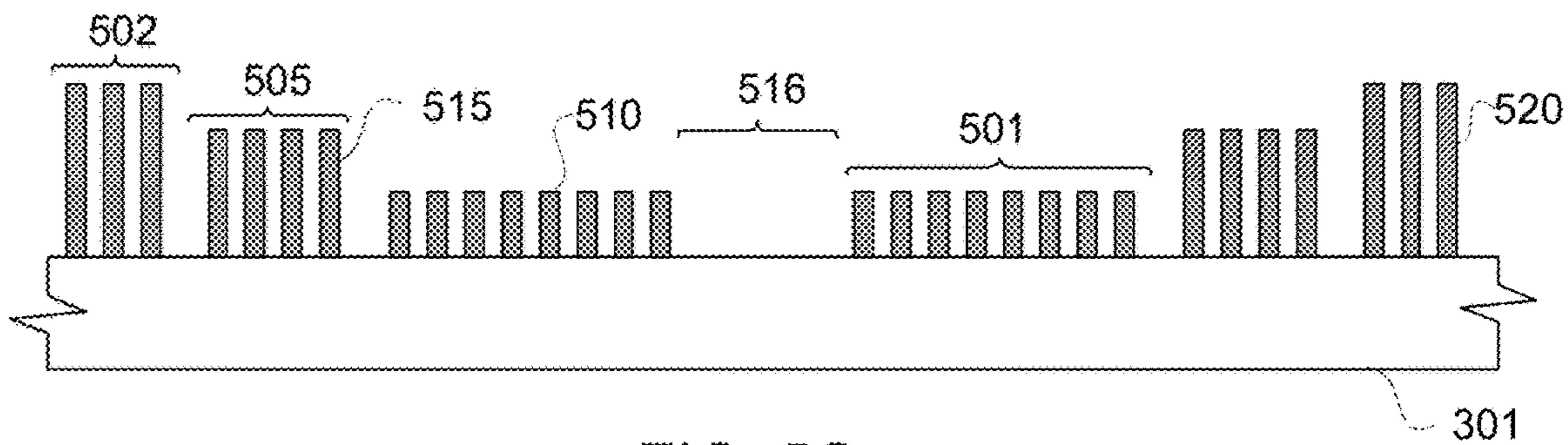


FIG. 5C

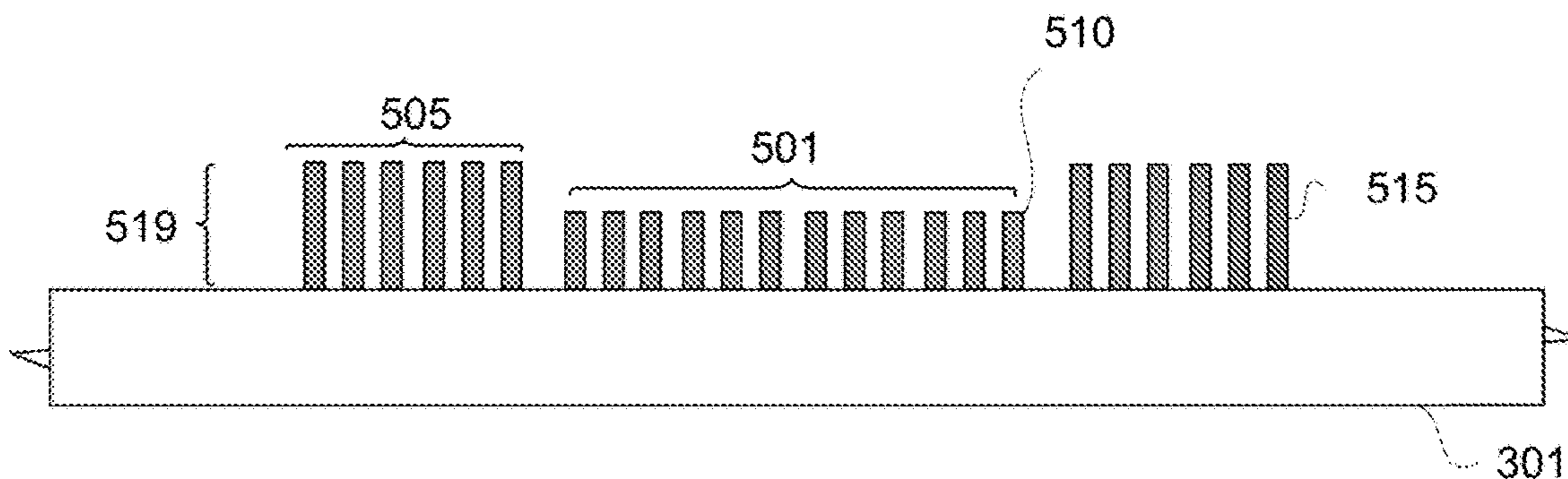


FIG. 5D

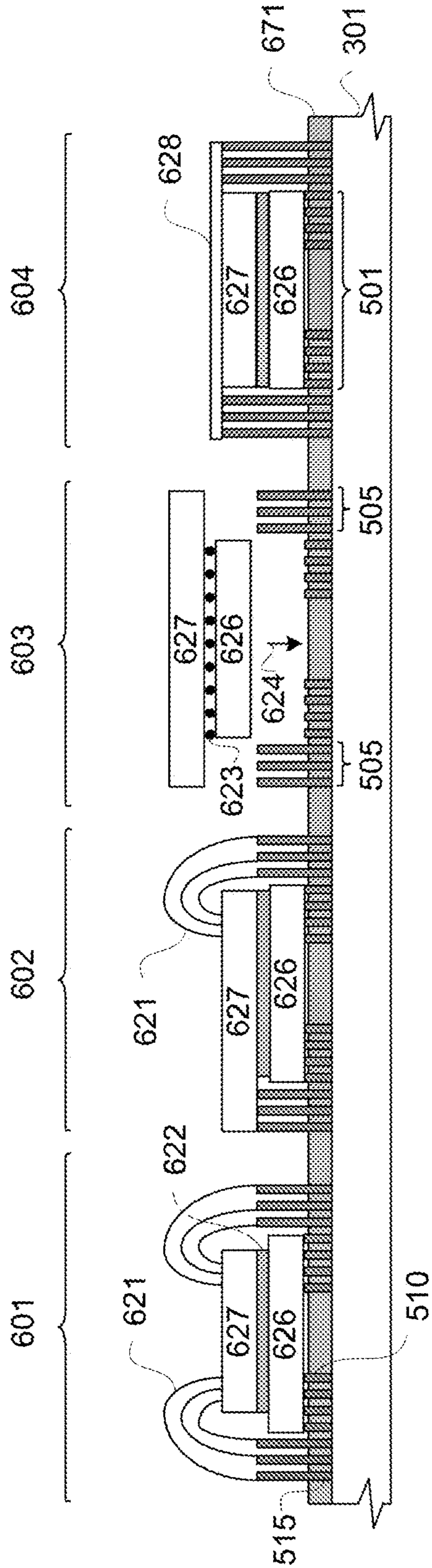


FIG. 6A

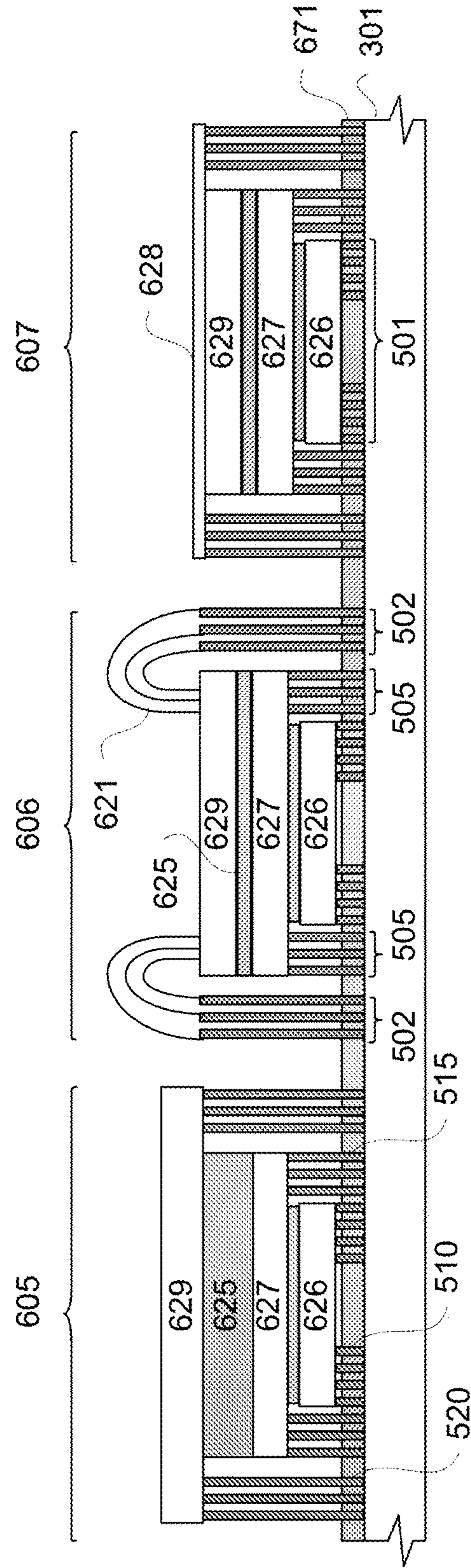


FIG. 6B

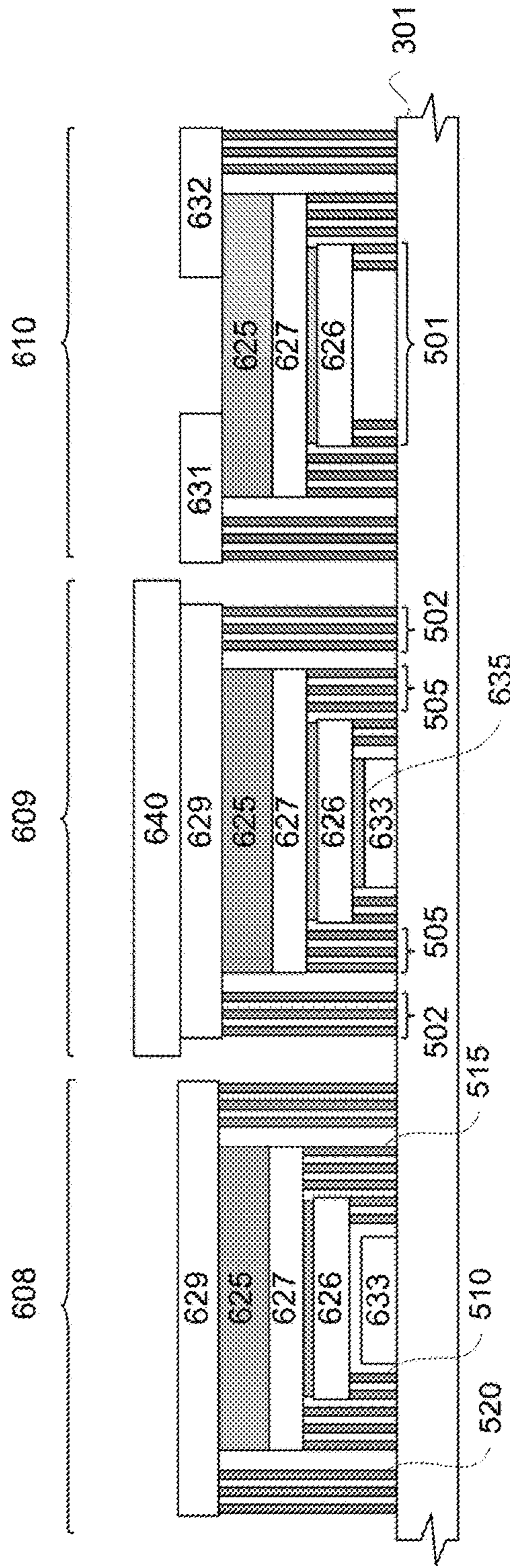


FIG. 6C

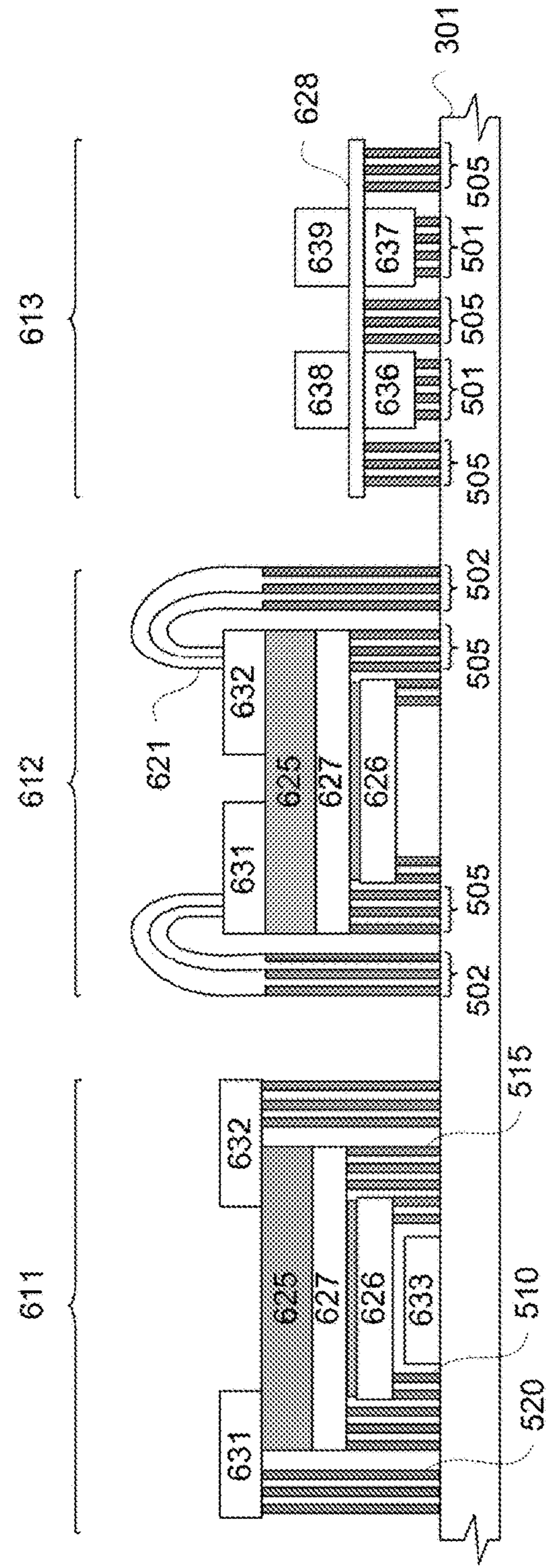


FIG. 6D

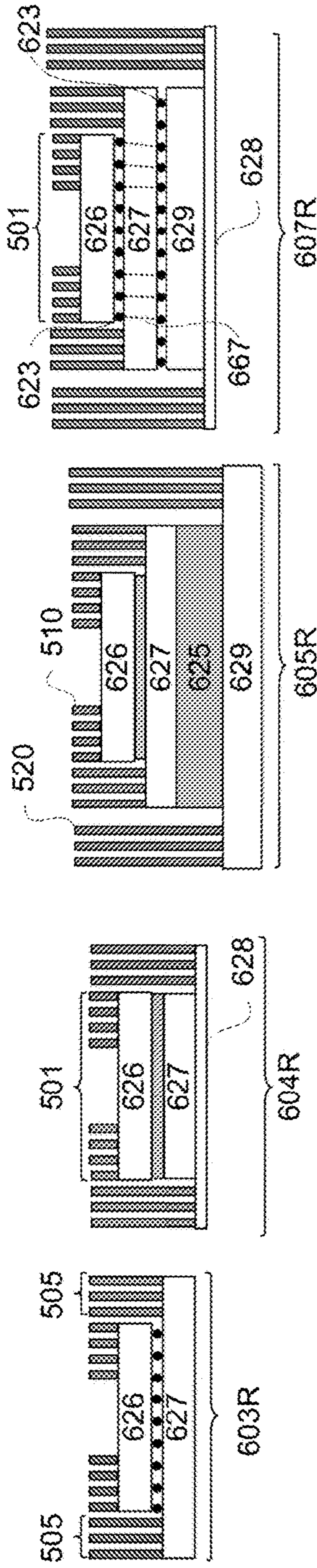


FIG. 6E-1

FIG. 6E-2

FIG. 6E-3

FIG. 6E-4

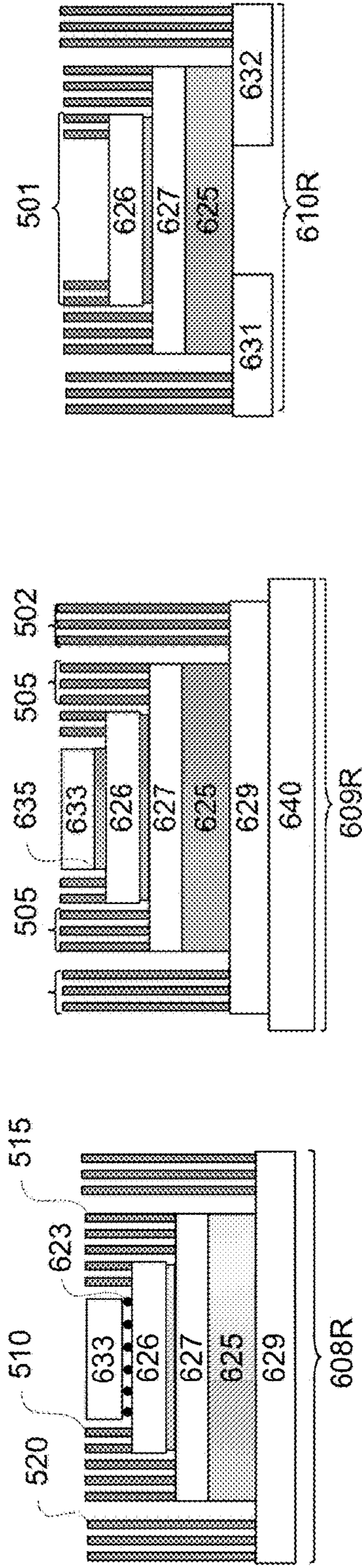


FIG. 6E-5

FIG. 6E-6

FIG. 6E-7

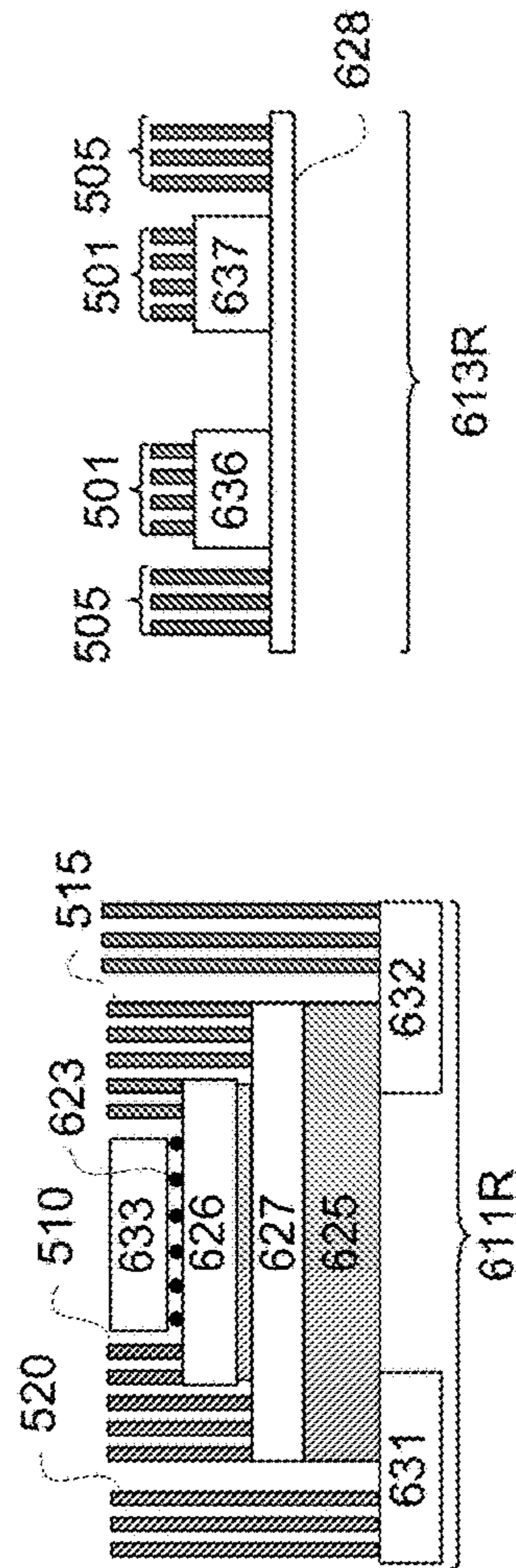


FIG. 6E-8

FIG. 6E-9

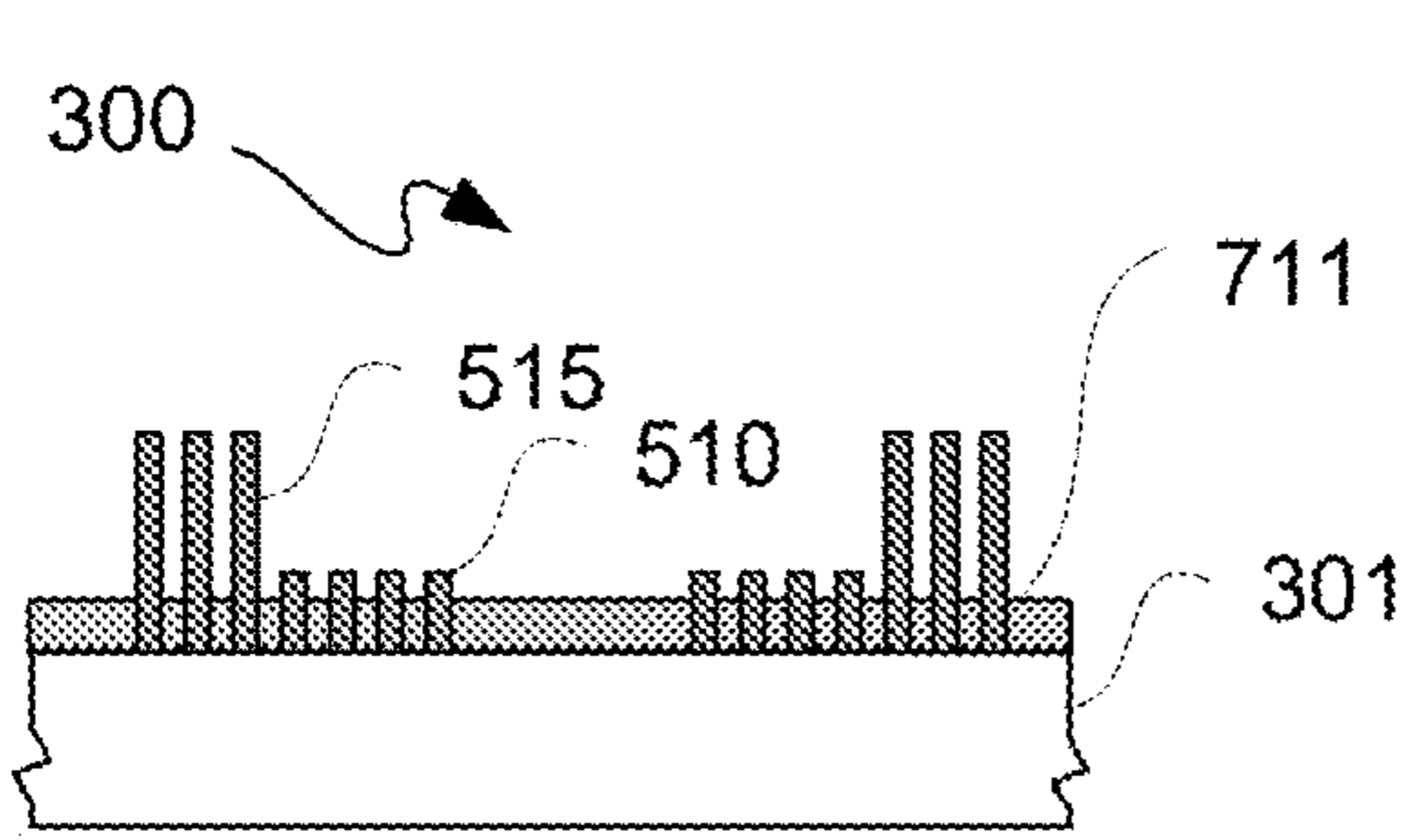


FIG. 7A

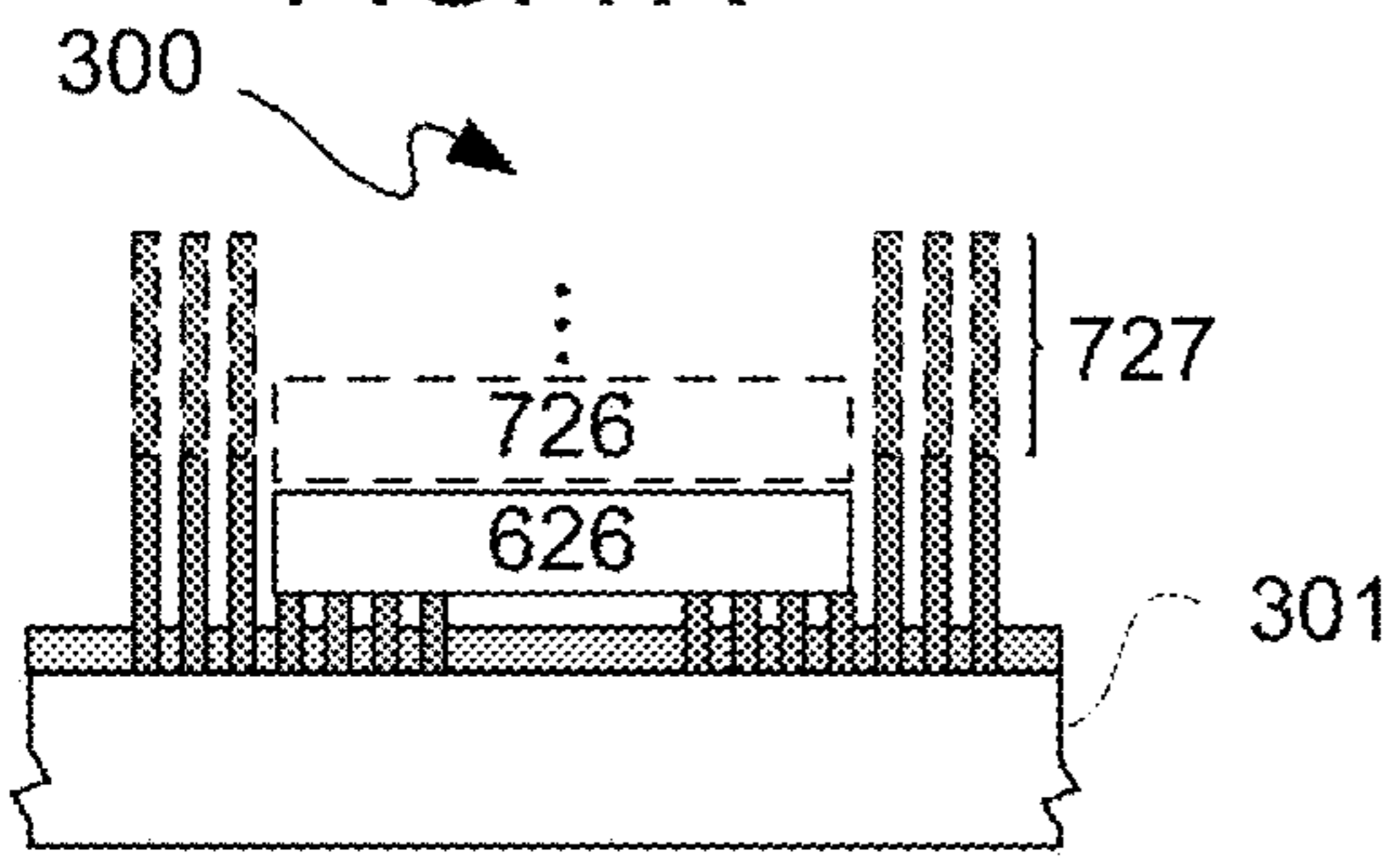


FIG. 7B

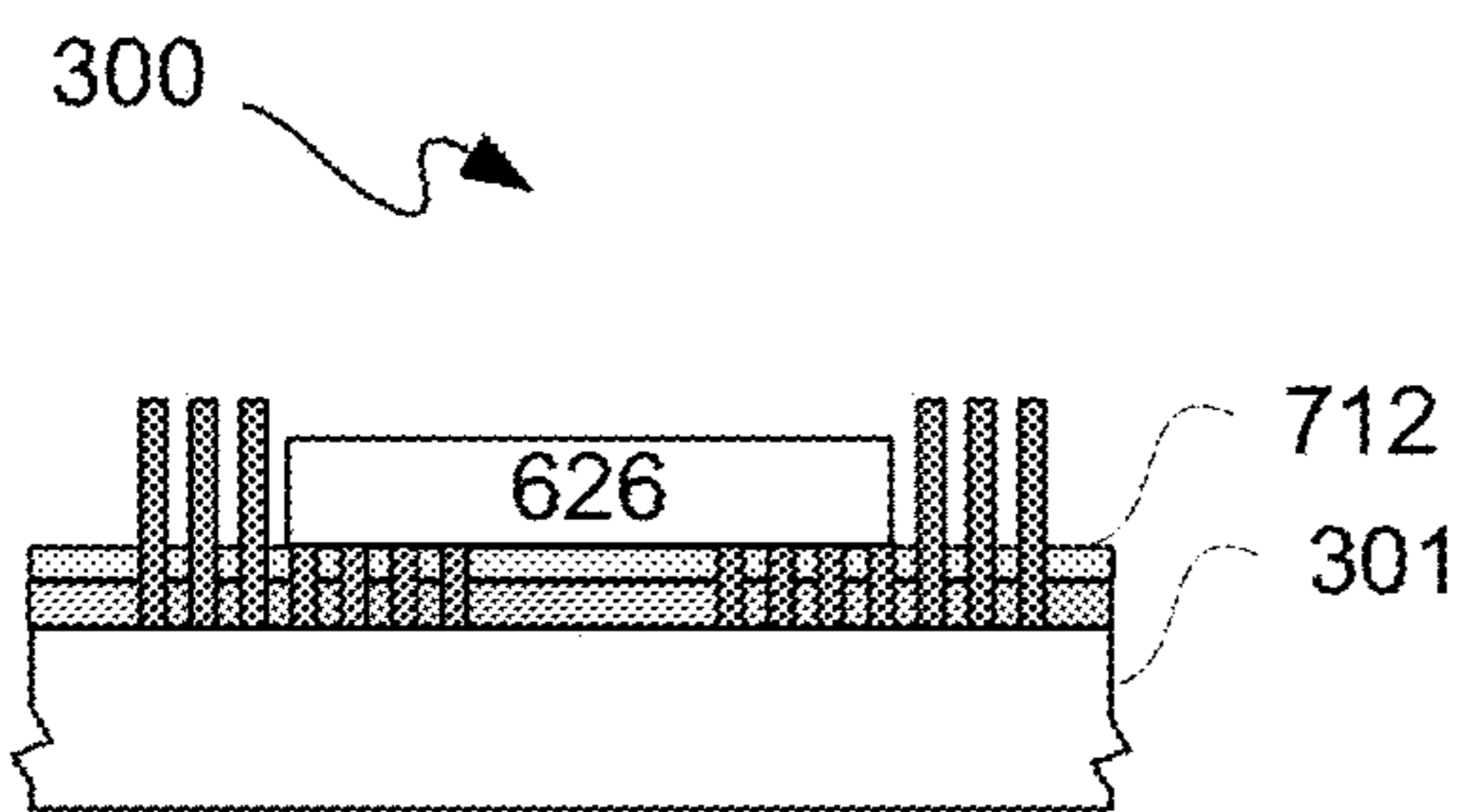


FIG. 7C

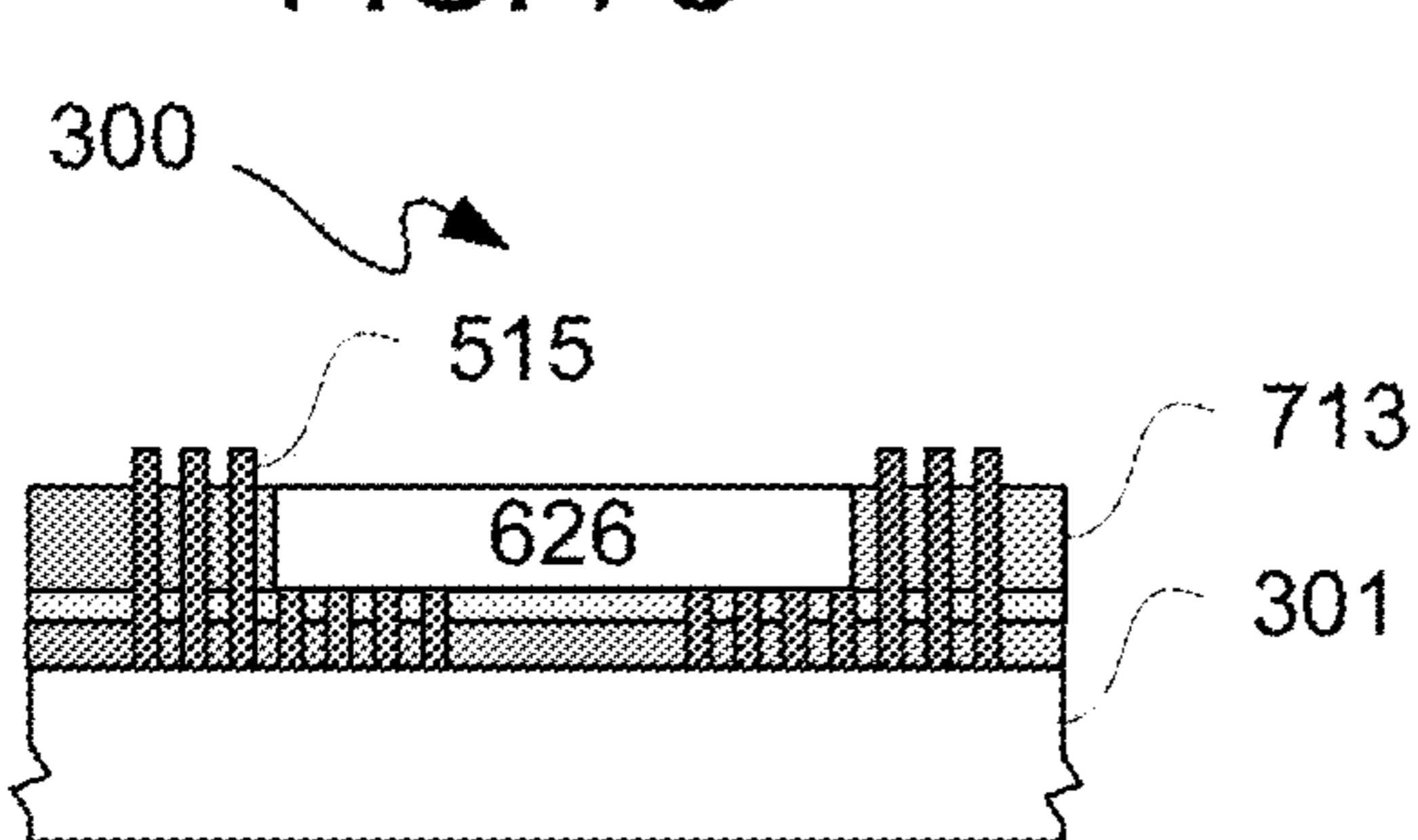


FIG. 7D

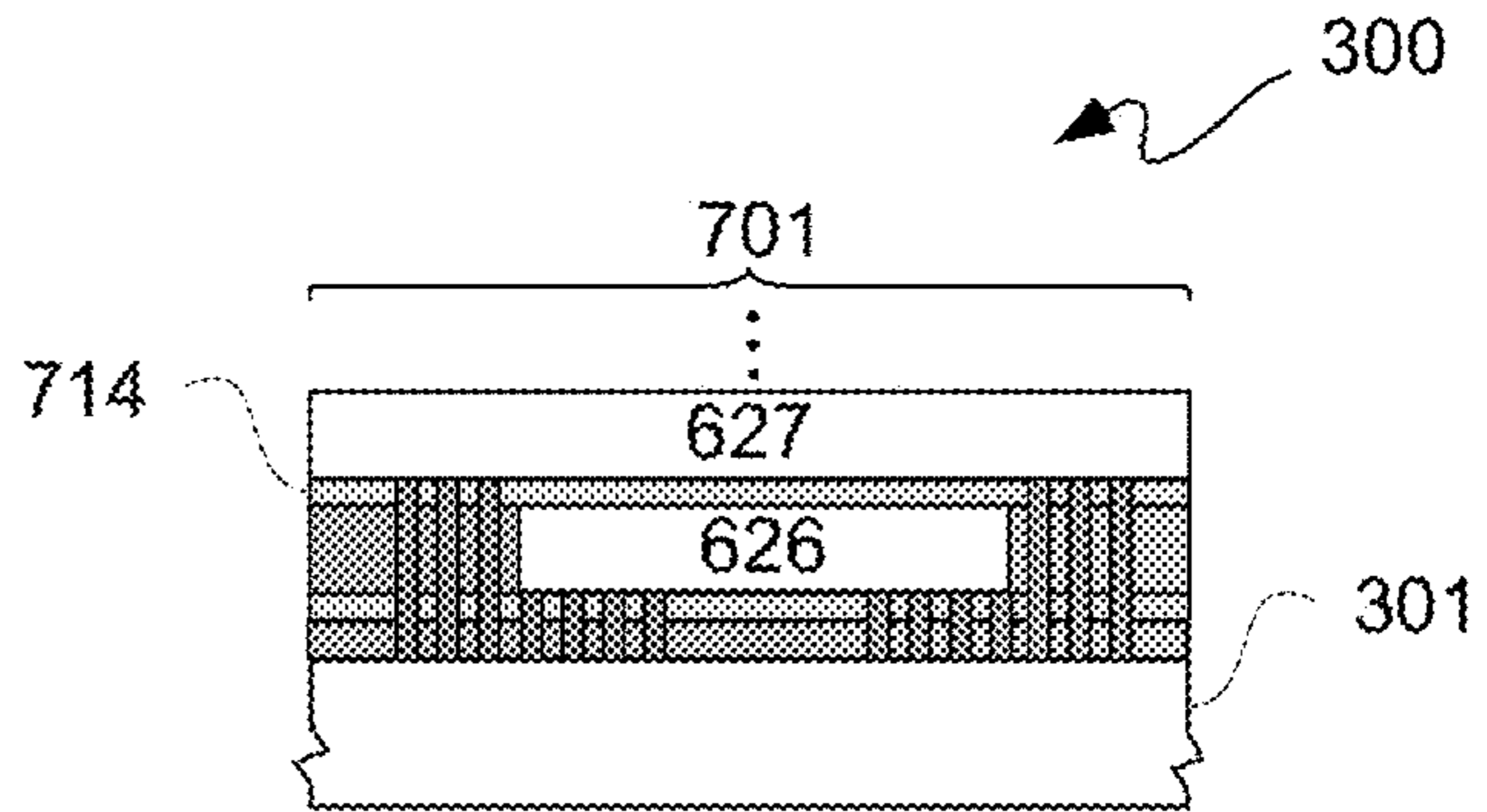


FIG. 7E-1

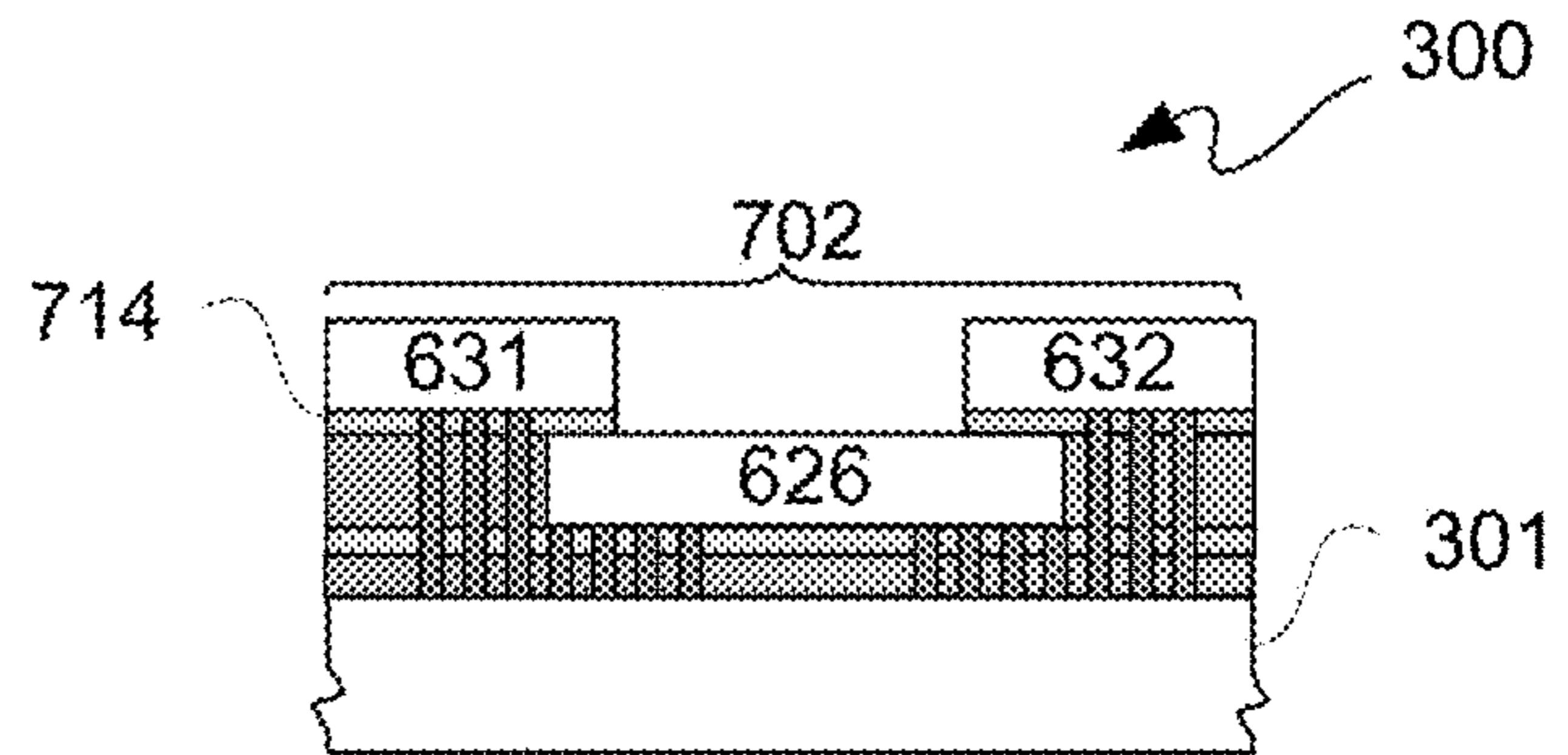


FIG. 7E-2

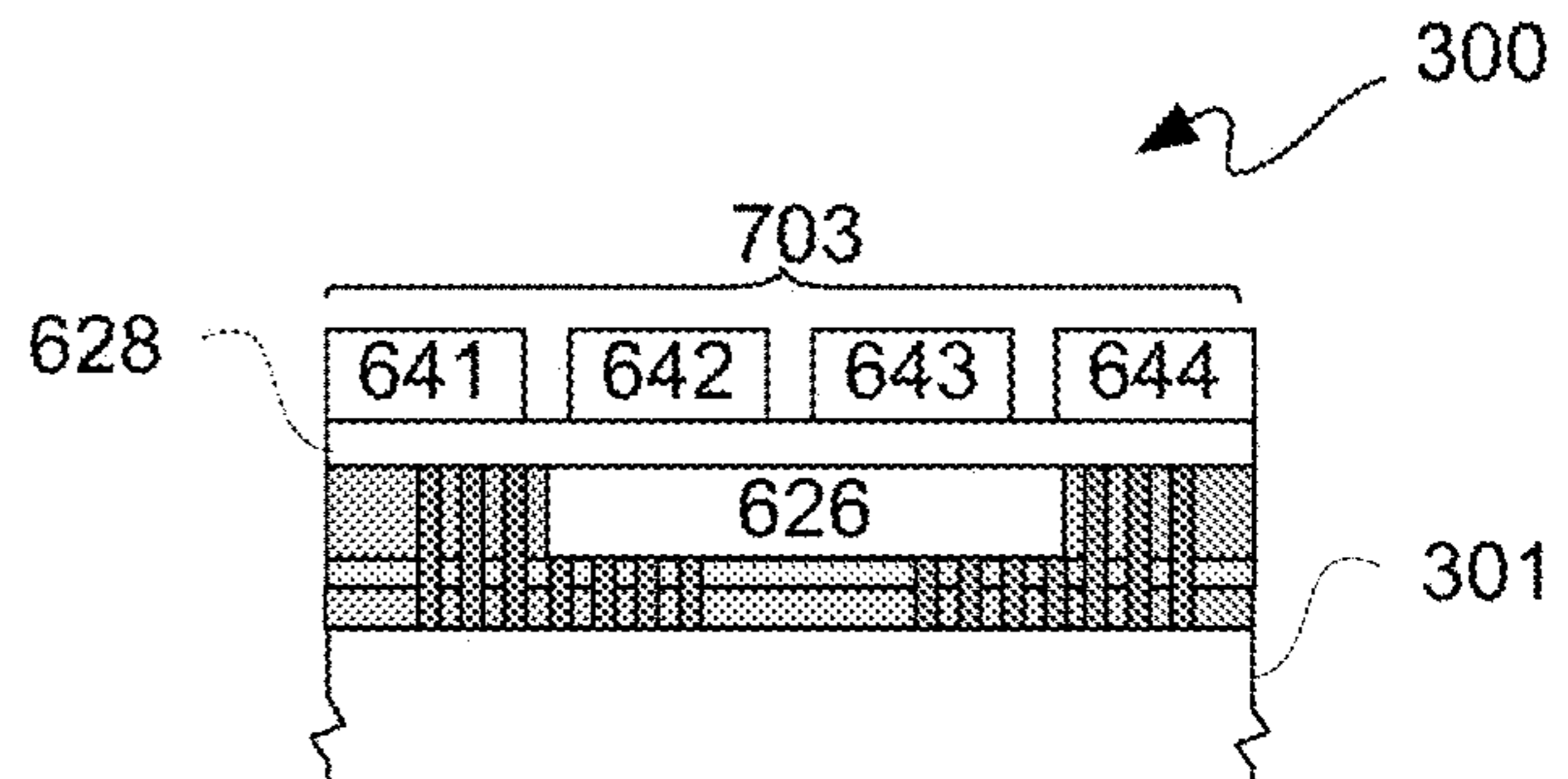


FIG. 7E-3

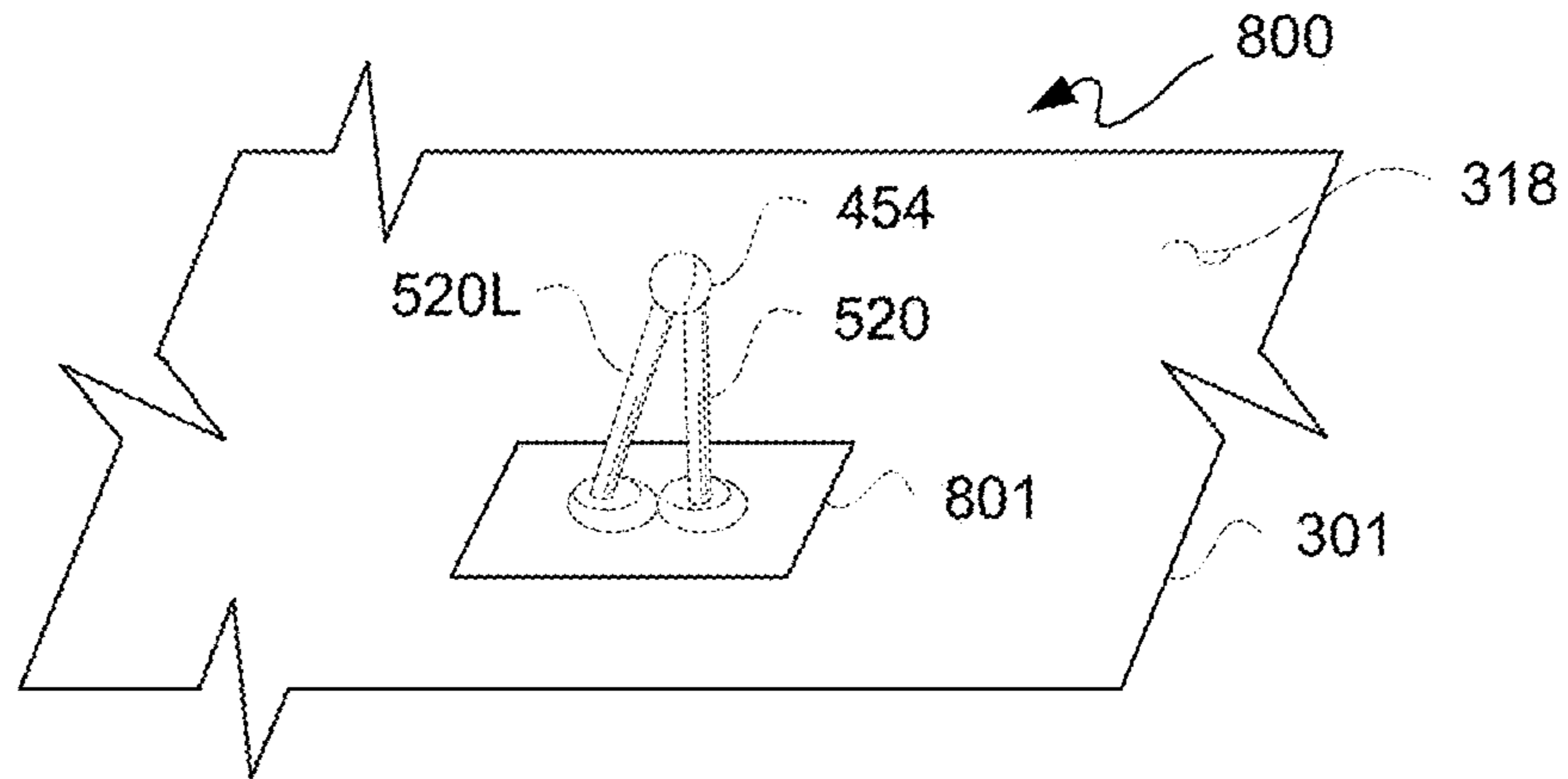


FIG. 8A

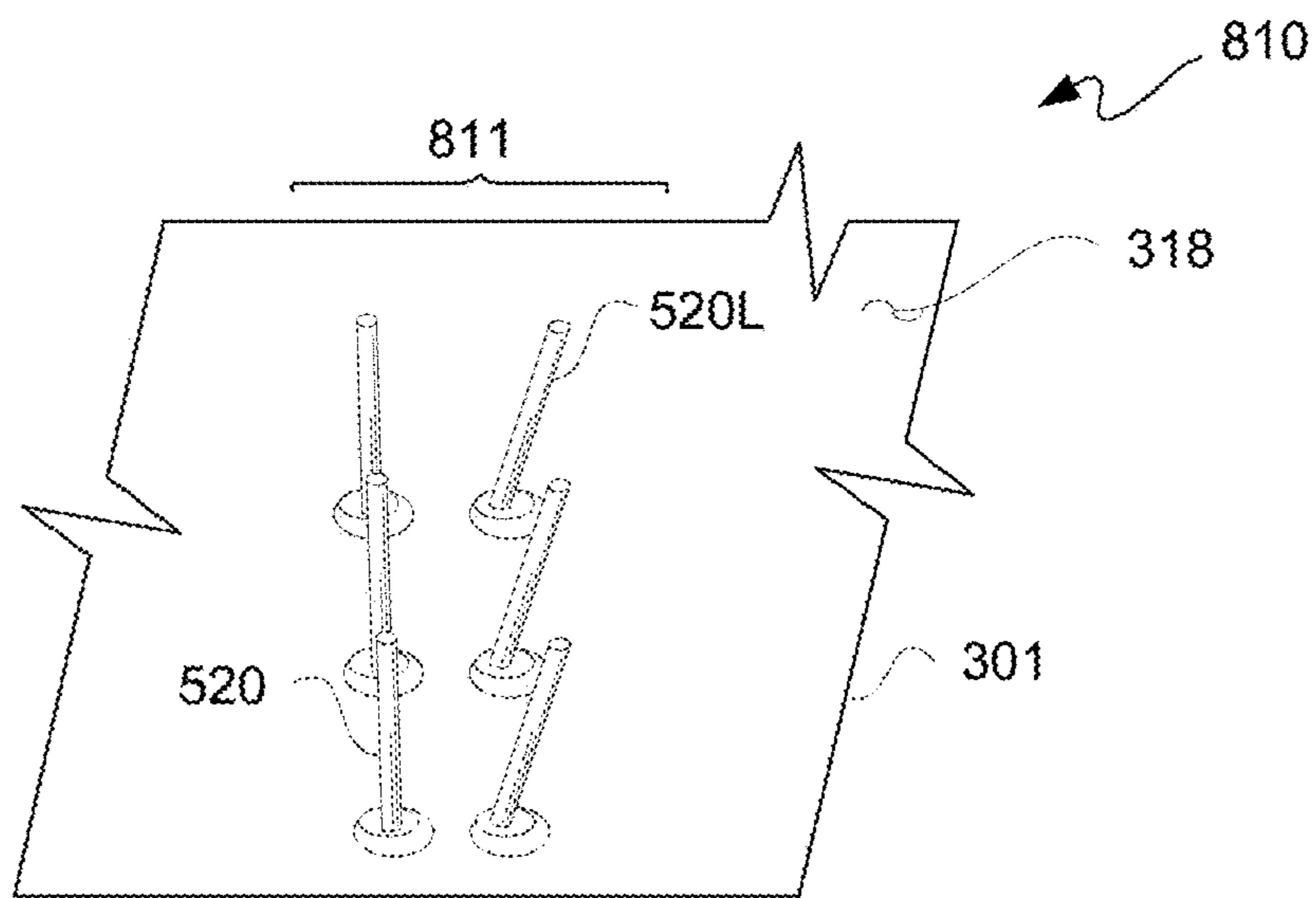


FIG. 8B

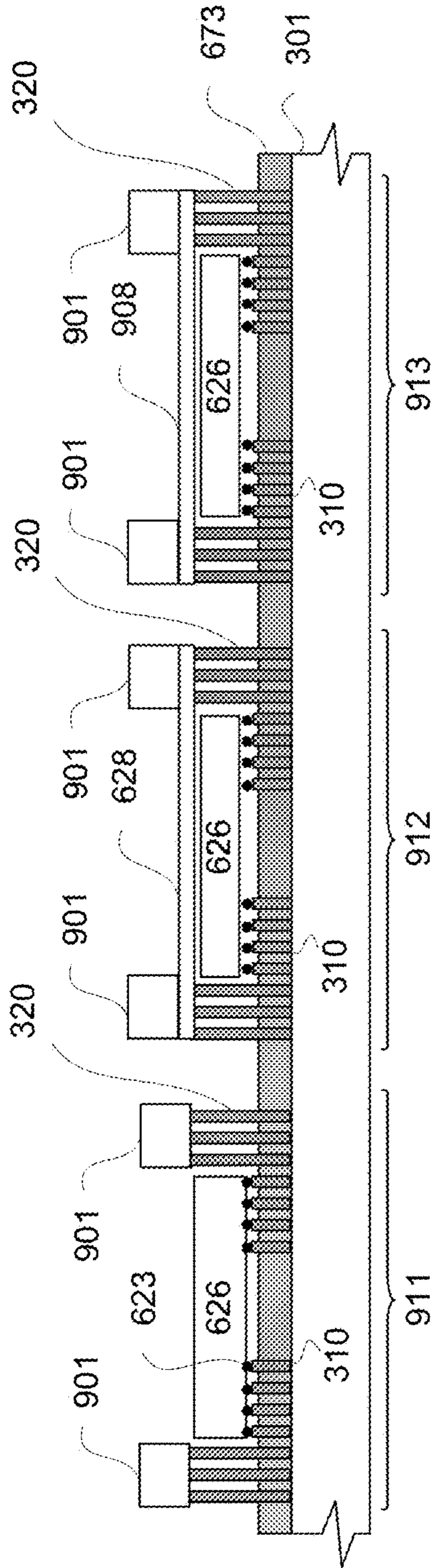


FIG. 9A

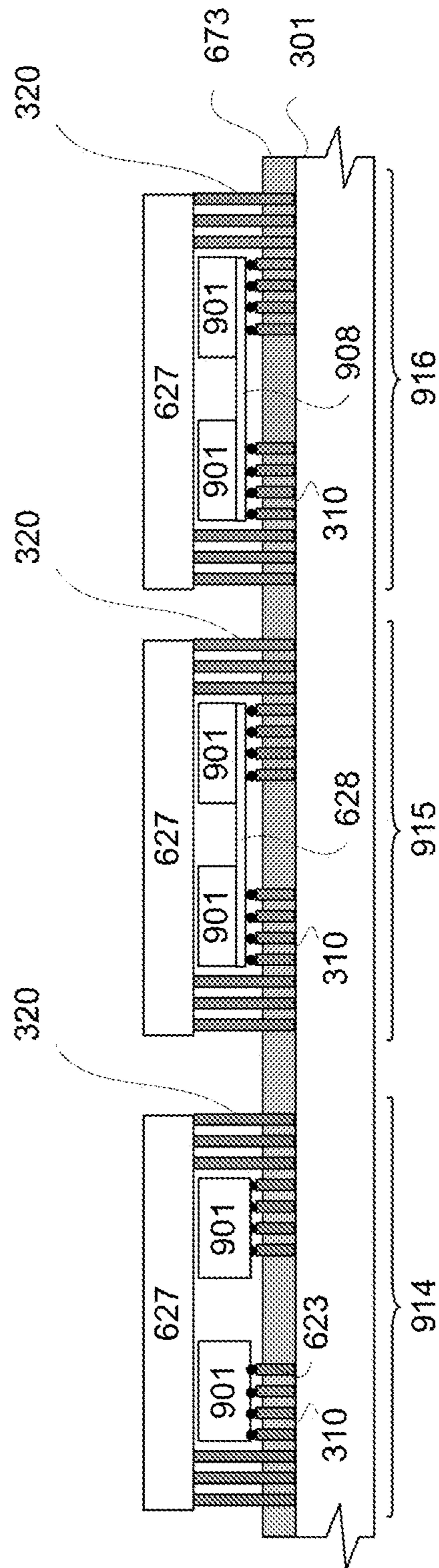


FIG. 9B

**MULTIPLE PLATED VIA ARRAYS OF
DIFFERENT WIRE HEIGHTS ON A SAME
SUBSTRATE**

Matter enclosed in heavy brackets [] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue; a claim printed with strikethrough indicates that the claim was canceled, disclaimed, or held invalid by a prior post-patent action or proceeding.

[CROSS-REFERENCE TO RELATED APPLICATION(S)] *CROSS-REFERENCE TO RELATED APPLICATIONS*

This application is a *reissue of U.S. patent application Ser. No. 16/245,116, filed Jan. 10, 2019 (now U.S. Pat. No. 10,629,567), which is a continuation of* [], and hereby claims priority to, *pending* U.S. patent application Ser. No. 16/008,531, filed on Jun. 14, 2018 (now U.S. Pat. No. 10,290,613), which is a continuation of U.S. patent application Ser. No. 15/430,943, filed on Feb. 13, 2017 (now U.S. Pat. No. 10,026,717), which is a continuation of U.S. patent application Ser. No. 14/841,381, filed on Aug. 31, 2015 (now U.S. Pat. No. 9,583,456), which is a continuation-in-part of U.S. patent application Ser. No. 14/087,252, filed on Nov. 22, 2013 (now U.S. Pat. No. 9,263,394), the entirety of each of which is hereby incorporated by reference herein for all purposes.

FIELD

The following description relates to integrated circuits (“ICs”). More particularly, the following description relates to multiple plated via arrays of different wire heights on a same substrate for an IC package.

BACKGROUND

Microelectronic assemblies generally include one or more ICs, such as for example one or more packaged dies (“chips”) or one or more dies. One or more of such ICs may be mounted on a circuit platform, such as a wafer such as in wafer-level-packaging (“WLP”), printed board (“PB”), a printed wiring board (“PWB”), a printed circuit board (“PCB”), a printed wiring assembly (“PWA”), a printed circuit assembly (“PCA”), a package substrate, an interposer, or a chip carrier. Additionally, one IC may be mounted on another IC. An interposer may be an IC or other type of electronic component, and an interposer may be a passive or an active IC, where the latter includes one or more active devices, such as transistors for example, and the former does not include any active device. Furthermore, an interposer may be formed like a PWB, namely without any circuit elements such as capacitors, resistors, or active devices. Additionally, an interposer includes at least one through-substrate-via.

An IC may include conductive elements, such as pathways, traces, tracks, vias, contacts, pads such as contact pads and bond pads, plugs, nodes, or terminals for example, that may be used for making electrical interconnections with a circuit platform. These arrangements may facilitate electrical connections used to provide functionality of ICs. An IC may be coupled to a circuit platform by bonding, such as bonding traces or terminals, for example, of such circuit platform to bond pads or exposed ends of pins or posts or the

like of an IC. Additionally, a redistribution layer (“RDL”) may be part of an IC to facilitate a flip-chip configuration, die stacking, or more convenient or accessible position of bond pads for example. Conventional interconnecting of an IC to another IC or to a circuit platform has issues with solder bridging. Accordingly, it would be desirable and useful to provide a structure for interconnection of an IC that mitigates against solder bridging.

BRIEF SUMMARY

An apparatus relates generally to via arrays on a substrate. In such an apparatus, the substrate has a conductive layer. First plated conductors are in a first region extending from a surface of the conductive layer. Second plated conductors are in a second region extending from the surface of the conductive layer. The first plated conductors and the second plated conductors are external to the first substrate. The first region is disposed at least partially within the second region. The first plated conductors are of a first height. The second plated conductors are of a second height greater than the first height. A second substrate is coupled to first ends of the first plated conductors. The second substrate has at least one electronic component coupled thereto. A die is coupled to second ends of the second plated conductors. The die is located over the at least one electronic component.

Another apparatus relates generally to via arrays on a substrate. In such an apparatus, the substrate has a conductive layer. First plated conductors are in a first region extending from a surface of the conductive layer. Second plated conductors are in a second region extending from the surface of the conductive layer. The first plated conductors and the second plated conductors are external to the first substrate. The first region is disposed at least partially within the second region. The first plated conductors are of a first height. The second plated conductors are of a second height greater than the first height. A die is coupled to first ends of the first plated conductors. A second substrate is coupled to second ends of the second plated conductors. The second substrate has at least one electronic component coupled thereto. The second substrate is located over the die.

A method relates generally to forming via arrays on a substrate. In such a method, a first substrate is obtained. A conductive layer is formed on an upper surface of the first substrate. A first resist layer is formed on the conductive layer. The first resist layer is patterned to provide a first mask with first vias from an upper surface of the first resist layer down to an upper surface of the conductive layer. Through-mask plating in the first vias provides first plated conductors in a first region extending from the upper surface of the conductive layer. A second resist layer is formed over the first plated conductors. The second resist layer is patterned to provide a second mask with second vias from an upper surface of the second resist layer down to upper surfaces of a subset of the first plated conductors. Through-mask plating in the second vias provides second plated conductors in a second region extending down to the upper surfaces of and including the subset of the first plated conductors. The first resist layer and the second resist layer are removed. Portions of the conductive layer between the first plated conductors and the second plated conductors are removed. The first plated conductors and the second plated conductors are external to the first substrate. The first region is disposed at least partially within the second region. The first plated conductors are of a first height. The second plated conductors are of a second height greater than the first height. A second substrate is coupled to first ends of the first plated

conductors. The second substrate has at least one electronic component coupled thereto. A die is coupled to second ends of the second plated conductors. The die is located over the at least one electronic component.

BRIEF DESCRIPTION OF THE DRAWING(S)

Accompanying drawing(s) show exemplary embodiment (s) in accordance with one or more aspects of exemplary apparatus(es) or method(s). However, the accompanying drawings should not be taken to limit the scope of the claims, but are for explanation and understanding only.

FIG. 1A is a schematic diagram of a cross-sectional view depicting an exemplary portion of an in-process wafer for providing an integrated circuit ("IC").

FIG. 1B is a schematic diagram of a cross-sectional view depicting an exemplary portion of an in-process wafer for providing another IC.

FIG. 1C is the diagram of FIG. 1A with the IC vertically flipped after chemical-mechanical-polishing of a lower surface of a substrate of the IC.

FIG. 1D is the diagram of FIG. 1A with the IC vertically flipped after a backside etch of a lower surface of a substrate of the IC to reveal a lower end contact surface of a via conductor thereof.

FIG. 1E is the diagram of FIG. 1D with a lower surface of the IC having formed thereon a passivation layer, which may be formed of one or more dielectric layers.

FIG. 2A is a block diagram of a cross-sectional view depicting an exemplary three-dimensional ("3D") IC packaged component with via structures.

FIG. 2B is a block diagram of a cross-sectional view depicting another exemplary 3D IC packaged component with via structures.

FIGS. 3A through 3M are respective block diagrams of side views depicting an exemplary portion of a process flow for processing a substrate to provide such substrate with two or more bond via arrays with wires of different heights.

FIG. 4A is a block diagram depicting an exemplary e-beam system.

FIG. 4B is a top-down angled perspective view depicting a portion of an exemplary in-process package for a die stack formed using the e-beam system of FIG. 4A.

FIG. 4C is the in-process package of FIG. 4B after deposition of a spacer or molding layer onto a top surface of a substrate.

FIGS. 5A through 5D are block diagrams of respective side views of substrates 301 with various exemplary configurations of wires that may be formed using the e-beam system of FIG. 4A or photolithography as generally described with reference to FIGS. 3A through 3M.

FIGS. 6A through 6D are block diagrams of side views of exemplary package-on-package assemblies ("die stacks") assembled using a substrate having two or more bond via arrays with wires of different heights.

FIGS. 6E-1 through 6E-9 are block diagrams of side views of exemplary package-on-package assemblies ("die stacks"), each of which may have two or more bond via arrays with wires of different heights.

FIGS. 7A through 7E-3 are block diagrams of side views depicting several exemplary die stacks, which may in part be commonly formed with reference to FIGS. 7A through 7D thereof.

FIGS. 8A and 8B are respective top-down perspective views depicting exemplary angled wire configurations.

FIGS. 9A and 9B are respective block diagrams of side views of exemplary in-process bond via array configurations.

DETAILED DESCRIPTION

In the following description, numerous specific details are set forth to provide a more thorough description of the specific examples described herein. It should be apparent, however, to one skilled in the art, that one or more other examples or variations of these examples may be practiced without all the specific details given below. In other instances, well known features have not been described in detail so as not to obscure the description of the examples herein. For ease of illustration, the same number labels are used in different diagrams to refer to the same items; however, in alternative examples the items may be different.

The following description generally relates to two or more bond via arrays (BVAs) on a same surface of a substrate. At least two of these bond via arrays have wires of distinctly different heights for accommodation of die stacking within at least one of such bond via arrays and in some applications vias or wires may have different electrical resistivities and/or elastic moduli.

FIG. 1A is a schematic diagram of a cross-sectional view depicting an exemplary portion of an in-process wafer for providing an IC 10 component. IC 10 includes a substrate 12 of a semiconductor material such as silicon (Si), gallium arsenide (GaAs), polymeric, ceramic, carbon-based substrates such as diamond, a silicon carbon (SiC), germanium (Ge), $\text{Si}_{1-x}\text{Ge}_x$, or the like. Even though a semiconductor substrate 12 as provided from an in-process wafer is generally described below, any sheet or layer semiconductor material or dielectric material, such as ceramic or glass for example, may be used as a substrate. Furthermore, even though an IC 10 is described, any microelectronic component that includes one or more through-substrate via structures may be used.

Substrate 12 includes an upper surface 14 and a lower surface 16 that extend in lateral directions and are generally parallel to each other at a thickness of substrate 12. Use of terms such as "upper" and "lower" or other directional terms is made with respect to the reference frame of the figures and is not meant to be limiting with respect to potential alternative orientations, such as in further assemblies or as used in various systems.

Upper surface 14 may generally be associated with what is referred to as a "front side" 4 of an in-process wafer, and lower surface 16 may generally be associated with what is referred to as a "backside" 6 of an in-process wafer. Along those lines, a front-side 4 of an in-process wafer may be used for forming what is referred to as front-end-of-line ("FEOL") structures 3 and back-end-of-line ("BEOL") structures 5. Generally, FEOL structures 3 may include shallow trench isolations ("STI") 7, transistor gates 8, transistor source/drain regions (not shown), transistor gate dielectrics (not shown), contact etch stop layer ("CESL"; not shown), a pre-metallization dielectric or pre-metal dielectric ("PMD") 11, and contact plugs 9, among other FEOL structures. A PMD 11 may be composed of one or more layers. Generally, BEOL structures 5 may include one or more inter-level dielectrics ("ILDs") and one or more levels of metallization ("M"). In this example, there are four ILDs, namely ILD1, ILD2, ILD3, and ILD4; however, in other configurations there may be fewer or more ILDs. Furthermore, each ILD may be composed of one or more dielectric layers. In this example, there are five levels of metallization,

namely M1, M2, M3, M4, and M5; however, in other configurations there may be fewer or more levels of metallization. Additionally, metal from a metallization level may extend through one or more ILDs, as is known. Furthermore, each level of metallization may be composed of one or more metal layers. A passivation level 13 may be formed on a last metallization layer. Such passivation level 13 may include one or more dielectric layers, and further may include an anti-reflective coating (“ARC”). Furthermore, a redistribution layer (“RDL”) may be formed on such passivation level. Conventionally, an RDL may include: a dielectric layer, such as a polyimide layer for example; another metal layer on such dielectric layer and connected to a bond pad of a metal layer of a last metallization level; and another dielectric layer, such as another polyimide layer for example, over such RDL metal layer while leaving a portion thereof exposed to provide another bond pad. A terminal opening may expose such other bond pad of such RDL metal layer. Thereafter, a solder bump or wire bond may be conventionally coupled to such bond pad.

As part of a FEOL or BEOL structure formation, a plurality of via structures 18 may extend within openings formed in substrate 12 which extend into substrate 12. Via structures 18 may be generally in the form of any solid of any shape formed by filling an opening formed in substrate 12. Examples of such solid shapes generally include cylindrical, conical, frustoconical, rectangular prismatic, cubic, or the like. Examples of openings for via structures, vias, and processes for the fabrication thereof, may be found in U.S. patent application Ser. No. 13/193,814 filed Jul. 29, 2011 (now U.S. Pat. No. 8,816,505), and U.S. patent application Ser. Nos. 12/842,717 and 12/842,651 both filed on Jul. 23, 2010 (now U.S. Pat. Nos. 8,791,575 and 8,796,135, respectively), and each of these patent applications (now patents) is hereby incorporated by reference herein for all purposes to the extent same is consistent with the description hereof.

Conventionally, via structures 18 may extend from upper surface 14 down toward lower surface 16, and after a backside reveal, via structures 18 may extend between surfaces 14 and 16, as effectively thickness of substrate 12 may be thinned so as to reveal lower end surfaces of via structures 18, as described below in additional detail. Via structures 18 extending through substrate 12 between surfaces 14 and 16, though they may extend above or below such surfaces, respectively, may be referred to as through-substrate-vias. As substrates are often formed of silicon, such through-substrate-vias are commonly referred to as TSVs, which stands for through-silicon-vias.

Such openings formed in substrate 12 may be conformally coated, oxidized, or otherwise lined with a liner or insulator 15. Conventionally, liner 15 is silicon dioxide; however, a silicon oxide, a silicon nitride, or another dielectric material may be used to electrically isolate via structures 18 from substrate 12. Generally, liner 15 is an insulating or dielectric material positioned between any and all conductive portions of a via structure 18 and substrate 12 such that an electronic signal, a ground, a supply voltage, or the like carried by such via structure 18 is not substantially leaked into substrate 12, which may cause signal loss or attenuation, shorting, or other circuit failure.

Overlying a liner 15 may be a barrier layer 24. Generally, barrier layer 24 is to provide a diffusion barrier with respect to a metallic material used to generally fill a remainder of an opening in which a via structure 18 is formed. Barrier layer 24 may be composed of one or more layers. Furthermore, a barrier layer 24 may provide a seed layer for subsequent

electroplating or other deposition, and thus barrier layer 24 may be referred to as a barrier/seed layer. Moreover, barrier layer 24 may provide an adhesion layer for adherence of a subsequently deposited metal. Thus, barrier layer 24 may be a barrier/adhesion layer, a barrier/seed layer, or a barrier/adhesion/seed layer. Examples of materials that may be used for barrier layer 24 include tantalum (Ta), tantalum nitride (TaN), palladium (Pd), titanium nitride (TiN), TaSiN, compounds of Ta, compounds of Ti, compounds of nickel (Ni), compounds of copper (Cu), compounds of cobalt (Co), or compounds of tungsten (W), among others.

Via structures 18 may generally consist of a metallic or other conductive material generally filling a remaining void in an opening formed in substrate 12 to provide a via conductor 21. In various examples, a via conductor 21 of a via structure 18 may generally consist of copper or a copper alloy. However, a via conductor 21 may additionally or alternatively include one or more other conductive materials such as tantalum, nickel, titanium, molybdenum, tungsten, aluminum, gold, or silver, including various alloys or compounds of one or more of the these materials, and the like. A via conductor 21 may include non-metallic additives to control various environmental or operational parameters of a via structure 18.

Via structures 18 may each include an upper end contact surface 20 which may be level with upper surface 14 of substrate 12 and a lower end contact surface 22 which may be level with lower surface 16 of substrate 12 after a backside reveal. End surfaces 20 and 22 may be used to interconnect via structures 18 with other internal or external components, as below described in additional detail.

In this example, upper end contact surface 20 of via conductors 21 are interconnected to M1 through a respective contact pad 23. Contact pads 23 may be formed in respective openings formed in PMD 11 in which M1 extends. However, in other configurations, one or more via conductors 21 may extend to one or more other higher levels of metallization through one or more ILDs. Furthermore, via structure 18 is what may be referred to as a front side TSV, as an opening used to form via structure is initially formed by etching from a front side of substrate 12.

However, a via structure may be a backside TSV, as generally indicated in FIG. 1B, where there is shown a schematic diagram of a cross-sectional view depicting an exemplary portion of an in-process wafer for providing another IC 10. Fabrication of a backside TSV is generally referred to as a “via last approach,” and accordingly fabrication of a front side TSV is generally referred to as a “via first approach.”

IC 10 of FIG. 1B includes a plurality of via structures 18, which are backside TSVs. For a backside TSV for via structure 18, liner 15 may be a deposited polymer into a “donut” silicon trench etch and deposited on lower surface 16 as a passivation layer 28, followed by a central silicon trench etch to remove an inner portion of the “donut” silicon trench, and followed by a seed layer deposition before patterning and electroplating to provide via conductors 21 having respective solder bump pads or landings 29. Optionally, a conventional anisotropic silicon etch may be used prior to depositing and patterning a polymer isolation layer as liner 15.

For purposes of clarity by way of example and not limitation, it shall be assumed that front side TSVs are used, as the following description is generally equally applicable to backside TSVs.

FIG. 1C is the diagram of FIG. 1A with IC 10 after a chemical-mechanical-polishing (“CMP”) of a lower surface

16 of a substrate 12. Such CMP may be performed to temporarily reveal lower end contact surface 22, and thus portions of liner 15 and barrier layer 24 previously underlying lower end contact surface 22 may be removed by CMP. Thus, in this example, lower end contact surface 22 may be coplanar and level with lower surface 16.

FIG. 1D is the diagram of FIG. 1A with IC 10 after a backside etch of a lower surface 16 of substrate 12 to temporarily reveal a lower end contact surface 22 of a via conductor 21. In this example, lower end contact surface 22 may be coplanar with lower surface 16; however, as via conductor 21, and optionally barrier layer 24, may protrude from substrate 12 after a backside reveal etch, lower end contact surface 22 in this example is not level with lower surface 16. For purposes of clarity and not limitation, IC 10 of FIG. 1D shall be further described, as the following description may likewise apply to IC 10 of FIG. 1C.

FIG. 1E is the diagram of FIG. 1D with a lower surface 16 of a substrate 12 having formed thereon a passivation layer 31, which may be formed of one or more dielectric layers. Furthermore, passivation layer 31 may be a polymer layer. For example, passivation layer 31 may be a benzocyclobutene ("BCB") layer or a combination of a silicon nitride layer and a BCB layer. In some applications, passivation layer 31 may be referred to as an inter-die layer. A metal layer 32, such as a copper, copper alloy, or other metal previously described, may be formed on passivation layer 31 and on lower end contact surfaces 22 of via conductors 21. This metal layer 32 may be an RDL metal layer. Balls 33 may be respectively formed on bonding pads 34, where such pads may be formed on or as part of metal layer 32. Balls 33 may be formed of a bonding material, such as solder or other bonding material. Balls 33 may be microbumps, C4 bumps, ball grid array ("BGA") balls, or some other die interconnect structure. In some applications, metal layer 32 may be referred to as a landing pad.

More recently, TSVs have been used to provide what is referred to as three-dimensional ("3D") ICs or "3D ICs." Generally, attaching one die to another using, in part, TSVs may be performed at a bond pad level or an on-chip electrical wiring level. ICs 10 may be diced from a wafer into single dies. Such single dies may be bonded to one another or bonded to a circuit platform, as previously described. For purposes of clarity by way of example and not limitation, it shall be assumed that an interposer is used for such circuit platform.

Interconnection components, such as interposers, may be in electronic assemblies for a variety of purposes, including facilitating interconnection between components with different connection configurations or to provide spacing between components in a microelectronic assembly, among others. Interposers may include a semiconductor layer, such as of silicon or the like, in the form of a sheet or layer of material or other substrate having conductive elements such as conductive vias extending within openings which extend through such layer of semiconductor material. Such conductive vias may be used for signal transmission through such interposer. In some interposers, ends of such vias may be used as contact pads for connection of such interposer to other microelectronics components. In other examples, one or more RDLs may be formed as part of such interposer on one or more sides thereof and connected with one or both ends of such vias. An RDL may include numerous conductive traces extending on or within one or more dielectric sheets or layers. Such traces may be provided in one level or in multiple levels throughout a single dielectric layer, sepa-

rated by portions of dielectric material within such RDL. Vias may be included in an RDL to interconnect traces in different levels of such RDL.

FIG. 2A is a block diagram of a cross-sectional view depicting an exemplary 3D IC packaged component 50 with via structures 18. While a stacked die or a package-on-package die may include TSV interconnects, use of via structures 18 for a 3D IC packaged component 50 is described for purposes of clarity by way of example. In this example of a 3D IC packaged component 50, there are three ICs 10, namely ICs 10-1, 10-2, and 10-3, stacked one upon the other. In other implementations, there may be fewer or more than three ICs 10 in a stack. ICs 10 may be bonded to one another using microbumps 52 or flip-chip solder bumps. Optionally, Cu pillars extending from a backside of a die may be used. Some of these microbumps 52 may be interconnected to via structures 18. For example, a Cu/Sn microbump transient liquid phase ("TLP") bonding technology may be used for bonding ICs to one another. Thus, interconnect layers may be on one upper or lower side or both upper and lower sides of an IC 10 of a 3D stack.

A bottom IC 10-3 of such ICs in a 3D stack optionally may be coupled to an interposer or interposer die 40. Interposer 40 may be an active die or a passive die. For purposes of clarity and not limitation, it shall be assumed that interposer 40 is a passive die. IC 10-3 may be coupled to interposer 40 by microbumps 52. Interposer 40 may be coupled to a package substrate. A package substrate may be formed of thin layers called laminates or laminate substrates. Laminates may be organic or inorganic. Examples of materials for "rigid" package substrates include an epoxy-based laminate such as FR4, a resin-based laminate such as bismaleimide-triazine ("BT"), a ceramic substrate, a glass substrate, or other form of package substrate. An under fill 54 for a flip chip attachment may encapsulate C4 bumps or other solder balls 53 used to couple interposer die 40 and package substrate 41. A spreader/heat sink ("heat sink") 43 may be attached to package substrate 41, and such heat sink 43 and substrate package 41 in combination may encase ICs 10 and interposer 40 of such 3D stack. A thermal paste 42 may couple an upper surface of IC 10-1 on top of such 3D stack to an upper internal surface of such heat sink 43. Ball grid array ("BGA") balls or other array interconnects 44 may be used to couple package substrate 41 to a circuit platform, such as a PCB for example.

FIG. 2B is a block diagram of a cross-sectional view depicting another exemplary 3D IC packaged component 50 with via structures 18. 3D IC packaged components 50 of FIGS. 2A and 2B are the same except for the following differences; in FIG. 2B, another IC 10-4 is separately coupled via microbumps 52 to interposer 40, where IC 10-4 is not coupled in the stack of ICs 10-1, 10-2, and 10-3. Furthermore, interposer 40 includes metal and via layers for providing wires 47 for interconnecting ICs 10-3 and 10-4. Furthermore, interposer 40 includes via structures 18 coupled to IC 10-4 through microbumps 52.

3D wafer-level packaging ("3D-WLP") may be used for interconnecting two or more ICs, one or more ICs to an interposer, or any combination thereof, where interconnects thereof may use via structures 18. Optionally, ICs may be interconnected die-to-die ("D2D") or chip-to-chip ("C2C"), where interconnects thereof may use via structures 18. Further, optionally, ICs may be interconnected die-to-wafer ("D2W") or chip-to-wafer ("C2W"), where interconnects thereof may use via structures 18. Accordingly, any of a variety of die stacking or chip stacking approaches may be used to provide a 3D stacked IC ("3D-SIC" or "3D-IC").

FIGS. 3A through 3M are respective block diagrams of side views depicting an exemplary portion process flow 300 for processing a substrate 301 to provide a substrate 301 with two or more bond via arrays with wires of different heights. Such wire heights may be sufficiently different for forming package-on-package components with one or more dies stacked within at least one of such bond via arrays. For purposes of clarity by way of example and not limitation, it shall be assumed that substrate 301 includes a fabricated multi-layered structure (“substrate”) with generally any and all BEOL and/or FEOL processing operations having been completed. In passive die configurations, such as a passive interposer for example, there may not be any FEOL processing operations. As used above, substrate 12 of FIG. 1A for example was a single layer. However, more generally a substrate 301 may be a single layer or multiple layers used to form a passive or active component. Along those lines, a semiconductor die may be referred to as a substrate 301. Generally, a substrate 301 may be any sheet, wafer or layer of semiconductor material or dielectric material, such as gallium-arsenide, silicon-germanium, ceramic, polymer, polymer composite, glass-epoxy, glass, or other suitable low-cost, rigid or semi-rigid material or bulk semiconductor material for structural support. Furthermore substrate 301 may be a printed circuit board (“PCB”) or a package substrate or a semiconductive or non-conductive material. For purposes of clarity by way of example and not limitation, it shall be assumed that substrate 301 is a package substrate, such as a logic package for a stacked die. However, substrate 301 in other examples may be an interposer or other form of substrate for providing an IC, including without limitation a 3D IC.

A conductor seed layer 302 is deposited onto an upper surface of substrate 301. Such seed layer 302 may be an adhesion layer and/or a seed layer (“seed/adhesion layer”). Seed/adhesion layer 302 may be a metal or metal compound, such as for example using one or more of copper (Cu), aluminum (Al), tin (Sn), platinum (Pt), nickel (Ni), gold (Au), tungsten (W), or silver (Ag), or other suitable conductive material. Furthermore, such seed layer may be deposited by plasma vapor deposition (PVD), chemical vapor deposition (CVD), sputtering, printing, plating, or other suitable form of deposition. For purposes of clarity and not limitation, it shall be assumed that seed/adhesion layer 302 is plated. A wet chemistry, such as for electrolytic plating or electroless plating, may be used.

At FIG. 3B, a resist layer 303 is deposited on seed/adhesion layer 302. Resist 303 may be a photoresist or other resist suitable for patterning. At FIG. 3C, a mask 304 is positioned over resist for exposure to light 305, such as in photolithography. Even though the example of a positive resist is used for purposes of clarity, a negative resist may be used in other implementations. For a positive resist 303, portions of such resist 303 exposed to light 305 become soluble to a photoresist developer. At FIG. 3D, such exposed portions of resist 303 are removed. In this example, a central block 306 of resist 303, along with right and left arrays of spaced-apart resist pins 307 to either side of central block 306 are left as disposed on seed/adhesion layer 302.

At FIG. 3E, through-mask plating 308 is used to form wires 310, namely “short” wires 310 extending from seed/adhesion layer 302 in gaps between wires of spaced-apart resist pins 307. Plating 308 may be an electrolytic or electroless plating as previously described. Furthermore, another form of conductive material deposition may be used instead of plating 308, such as described elsewhere herein.

As will be appreciated from the following description, alternatively “tall” wires 320 may be formed at FIG. 3E, with a subsequent masking and metal etch back to form “short” wires 310 from a portion of such “tall” wires 320. However, for purposes of clarity by way of example and not limitation, it shall be assumed that short wires 310 are formed at FIG. 3E.

At FIG. 3F, resist 333 is deposited. Optionally, in another implementation, such deposition of resist 333 may not be preceded by a prior removal of resist 303, such as by ashing, after formation of short wires 310. However, in this implementation, resist 303 is removed prior to deposition of resist 333. In one example, an injection printer nozzle maybe used to coat resist or mask at regions to prevent subsequent metal coating in such blocked regions.

At FIG. 3G, a mask 309 is positioned over resist for exposure to light 305, such as in photolithography. Again, even though the example of a positive resist is used for purposes of clarity, a negative resist may be used in other implementations. At FIG. 3H, such exposed portions of resist 303 are removed. In this example, a central block 316 of resist 303, along with right and left arrays of spaced-apart resist pins 317 to either side of central block 316 are left as disposed on seed/adhesion layer 302 and short wires 310.

At FIG. 3I, a through-mask plating 308 is used to form tall wires 320 from extending from exposed ends of short wires 310 in gaps between wires of spaced-apart resist pins 317. Again, plating 308 may be an electrolytic or electroless plating as previously described, or another form of conductive material deposition may be used instead of plating 308, such as described elsewhere herein.

At FIG. 3J, remaining resist 303 may be removed by ashing 312 or by wet resist selectively wet etched or by other known methods. Leaving short wires 310 and tall wires 320 respectively extending from seed/adhesion layer 302. From an upper surface of seed/adhesion layer 302 to distal ends of short wires 310, such short wires 310 may have a height 321. Likewise, from an upper surface of seed/adhesion layer 302 to distal ends of tall wires 320, such tall wires 320 may have a height 322. A difference 319 in heights 321 and 322 from distal ends of short wires 310 to distal ends of tall wires 320 may be at least approximately the thickness of a die to be coupled to such distal ends of short wires 310.

At FIG. 3K, a blanket metal etch 313 may be used to remove seed/adhesion layer 302 not located under and forming part of wires 310 and 320. For example, an anisotropic wet etch may be used. Such etch may remove upper portions of wires 310 and 320. However, a height 319 may be maintained after such blanket metal etch 313. After etching at 313, such assemblage of substrate 301 may be cleaned.

Substrate 301 may have multiple sets of bond via arrays as generally indicated in FIG. 3L. In a set 325, substrate 301 has a first bond via array 324 with short wires 310 extending from a top surface 318 of substrate 301, and a second bond via array 323 with tall wires 320 extending from a top surface 318 of substrate 301. First bond via array 324 is disposed at least partially within second bond via array 323. Short wires 310 of first bond via array 324 are of a first height, such as for example height 321, and tall wires of second bond via array 323 are of a second height, such as for example height 322, greater than such first height for a package-on-package (“PoP”) configuration. Attachment of one or more dies may include molding to provide sufficient support for such attachments. Even though generally PoP configurations are described herein, such PoP configurations may include one or more of through mold vias (“TMVs”),

TSVs, BGAs, flip-chip interconnects, or other forms of interconnects. Furthermore, configurations other than PoP may be used, including PiP and SiP configurations for example.

In FIG. 3M, a molding layer 673 may be deposited, such that tips of bond via arrays 324, as well as bond via arrays 323, extend above such molding layer 673. Dies 626 and 627, as described below in additional detail, may be respectively interconnected to bond via arrays 324 and 323 at a wafer-level, such as a silicon wafer for example, or other large substrate 301 level. Dies 626 may be interconnected to tips of corresponding bond via arrays 324 by bumps 623, as described below in additional detail, such as flip-chip bonded for example. Rather than bumps 623, optionally wire bonds may be used. However, for purposes of clarity and not limitation, generally bumps 623 are described hereinbelow. In another configuration, stacked or staggered or progressively larger overlapping dies, such as dies 626 and 627 in DRAM or NAND flash for example, may be interconnected using bond via arrays as described herein. In a staggered stacking, bond via array 324 may extend partially within bond via array 323, as bond via array 324 may extend in at least one direction, such as orthogonally with respect to the sheet of the drawing for example, beyond or outside of bond via array 323. For purposes of clarity by way of example and not limitation, it shall be assumed that bond via array 324 is disposed completely within bond via array 323.

Optionally, bond via arrays may be formed with e-beam. FIG. 4A is a block diagram depicting an exemplary e-beam system 400. Even though an e-beam is described below, another type of optically provided energy beam may be used, such as a laser beam for example, in other implementations. E-beam system 400 includes an e-beam optical subsystem 401 for controllably generating and projecting an e-beam 402. Wire 403, which may come from a spool housed inside or outside of an e-beam chamber, may be fed into a wire spool control head 404. Wire spool control head 404 may be vertically translated up or down in a z-direction 405 with respect to top surface 318 of substrate 301. Conventionally, e-beam system 400 is computer controlled for determining power level and time to fuse bond wires 420 at a contact zone on top surface 318 of substrate 301. Accordingly, spacing between wires 420 may vary from application to application. Spacing between such wires 420 for a bond via array may be as small as one-diameter of a wire 420 or even smaller.

Wire spool control head 404 may feed wires 403 of various lengths to form bond via arrays of wires 420 of various heights. E-beam 402 may be used to heat ends of such wires 420 for attachment to top surface 318 of substrate 301. Because an e-beam 402 is used for wire bonding, heating is localized so as not to adversely affect other circuitry of substrate 301 or adjacent wire bonds. In other words, a heat affected zone may be so small as to be practically non-existent. Wire spool control head 404 may be configured to precision cut wire 403 for providing such wires 420 of various heights. In this example, a copper wire with a lead (Pb) coating is used for wire 403.

A platen or platform 410, upon which substrate 301 is placed, may be laterally translated in an x-direction 411 and/or y-direction 412. Such translation may be used to provide rows or columns of wires to form bond via arrays with wires of various heights. Furthermore, platform 410 may be rotated 413 for such lateral translation. Optionally, another e-beam optical subsystem 421 or a beam splitting optical subsystem 421 may be used to provide an e-beam 422 for cutting wire 403. With respect to the latter subsys-

tem, such beam splitting optical subsystem 421 may be positioned to split e-beam 402 output from e-beam optical subsystem 401 for providing such optional cutting capability.

FIG. 4B is a top-down angled perspective view depicting a portion of an exemplary in-process package 440 for a die stack formed using e-beam system 400 of FIG. 4A. A bond via array 505, or bond via array 502, and 501 may be respectively formed of medium wires 515, or tall wires 520, and short wires 510. In this example, wires 510 and 515 or 520 are fusion bonded to substrate 301 using an e-beam, such as of FIG. 4A. Even though wires 510, 515, and 520 may be at a non-perpendicular angle with respect to surface 441 of a substrate of package 440 to which they are attached or coupled, such as illustratively depicted, in other embodiments such wires may be perpendicular to such surface. Short wires 510 may correspond to short wires 310 of FIG. 3L, and tall wires 520 may correspond to tall wires 320 of FIG. 3L. Medium wires 515 may be between short and tall wires 510 and 520 in height, as described below in additional detail. Wires 510, 515, or 520 may be ball bonded to planar surface 441, such as by EFO wire bonding. Additionally, there may be pads, as well as pad openings, (not shown for purposes of clarity and not limitation) along surface 441.

Even though wire bond wires 510, 515, and 520 are illustratively depicted as being in corresponding arrays, such wires may or may not be in a corresponding array. Accordingly, wire bond wires 510, 515, and/or 520 may be unevenly spaced with respect to corresponding wire bond wires 510, 515, and/or 520. Moreover, wire bond wires 510 and/or wire bonds therefor may have generally different or same dimensions with reference to diameters or widths or cross sections ("cross sectional dimensions") with respect to one another. Likewise, wire bond wires 515 and 520, as well as wire bonds therefor, may have generally different or same diameters or widths or cross sections with respect to one another. Wire bonds of such wire bond wires 510, 515, and/or 520 may be disposed externally on a surface of a substrate and extend away from such surface.

FIG. 4C is the in-process package 440 of FIG. 4B after deposition of a spacer or molding layer 430 onto a top surface of substrate 301. After such deposition, such as described below in additional detail, only top portions of short wires 510, as well as top portions of wires 515 or 520, may extend above a top surface 431 of such spacer layer 430. Along those lines, top ends 432, such as of short wires 510, may be accessible for metallurgical attachment of a die, such as by deposition of solder balls or bumps 454 onto such top ends 432 for reflow for example. In one implementation, a bond structure or structures may be disposed on a die side to be connected or coupled with various wires as described herein.

FIGS. 5A through 5D are block diagrams of respective side views of substrates 301 with various exemplary configurations of wires that may be formed using e-beam system 400 of FIG. 4A or photolithography as generally described with reference to FIGS. 3A through 3L. In FIG. 5A, an ultra-high density input/output pitch for a bond via array 501 of short wires 510 extending from substrate 301 is illustratively depicted. Generally, such pitch may be approximately -0.5 mm or less; though larger pitches than this upper limit may be used in some implementations. Additionally, for example, a pitch as small as 10 microns may be used in some implementations. In FIG. 5B, in addition to bond via arrays 501 as in FIG. 5A, substrate 301 has extending therefrom tall wires 520 to provide a bond via

array 502. One or more bond via arrays 501 may be located inside of bond via array 502, which may be used for example by a peripheral I/O. Furthermore, tall wires 520 may be formed of a different material than short wires 510. For example, tall wires 520 may be formed of nickel or tungsten (W) and/or their respective alloys, and short wires may be formed another conductive material as described elsewhere herein.

Furthermore, wires of various heights as well as various conductive materials may be used, as generally indicated with reference to FIG. 5C. FIG. 5C includes wires 510 and 520 respectively for bond via arrays 501 and 502 as in FIG. 5B, as well as bond via arrays 505 of "medium" wires 515. Medium wires 515 may have a height 519 which is between heights of wires 510 and 520. Differences in heights as between wires 510, 515, and/or 520 may be to accommodate different thicknesses of one or more dies and/or packages, as well as one or more interfaces therebetween, disposed within an outer bond via array. In the example of FIG. 5C, an inner bond via array 501 has an open middle section 516, and such inner bond via array 501 is within a middle bond via array 505, and such middle bond via array 505 is within an outer bond via array 502. However, bond via arrays may be positioned for close compact stacking too, as illustratively depicted in FIG. 5D, where bond via array 501 has no open middle section 516 and resides within an outer bond via array 505 formed of "middle" wires 515.

FIGS. 6A through 6D are block diagrams of side views of exemplary package-on-package assemblies ("die stacks") 601 through 613 assembled using a substrate 301 having two or more bond via arrays with wires of different heights. Wires of such bond via arrays of die stacks 601 through 613 may be formed using e-beam fusion bonded wires. Optionally, an underfill layer 671 may be deposited on an upper surface of substrate 301 after formation of wires of one or more bond via arrays, as described below in additional detail, such as to provide additional structural support. One or more other underfill layers may follow such underfill layer 671, though they may not be illustratively depicted for purposes of clarity and not limitation. Optionally, underfill layer 671 may be omitted, such as to have a dielectric constant of air and/or to provide for airflow through a package for cooling. FIGS. 6A through 6D are further described with simultaneous reference to FIGS. 5A through 5D, as well as simultaneous reference to FIGS. 6A through 6D.

For die stack 601, short wires 510 of a bond via array 501 coupled to substrate 301 are coupled to a backside surface of a die 626. A front side surface of die 626 may have coupled thereto a spacer layer 622, such as a layer of polymer or an epoxy used for molding and/or encapsulation. A front side surface of a die 627 may be placed on top of such spacer layer 622. A backside surface of die 627 may be wire bonded with wire bonds 621 to top ends of medium wires 515 of a bond via array 505 coupled to substrate 301. In this example, both of dies 626 and 627 are disposed within bond via array 505. In this configuration, die 626 may be referred to as an up or upward facing die, and die 627 may be referred to as a down or downward facing die.

For die stack 602, short wires 510 of a bond via array 501 coupled to substrate 301 are coupled to a backside surface of a die 626. A front side surface of die 626 may have coupled thereto a spacer layer 622. A right side portion of a backside surface of a die 627 may be placed on top of such spacer layer 622 and a left side portion of such backside surface of die 627 may be placed on tops of top ends of a left portion of a bond via array 505 of medium wires 515. A right side

portion of a front side surface of die 627 may be wire bonded with wire bonds 621 to top ends of medium wires 515 of a right side portion of bond via array 505 coupled to substrate 301. In this example, both of dies 626 and 627 are upward facing.

For die stack 603, dies 626 and 627 may be attached to one another with intervening bumps or balls ("bumps") 623, such as micro bumps for example. Again, rather than bumps 623, wire bonds may optionally be used. Material for bumps 623 may include one or more of solder, Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, Pt, or the like. For example, bump material may be eutectic Sn/Pb solder, lead-free solder, or high-lead solder. An under bump metallization ("UBM") layer (not shown) and an insulating layer (not shown), as well as other known details for die-to-die interconnect, may be included, though not particularly shown here for purposes of clarity and not limitation. Thus, for example, dies 626 and 627 may be interconnected with a flip-chip, ball grid array ("BGA") or other die-to-die interconnect technology prior to being coupled to substrate 301, as generally indicated by arrow 624. In this example, backside surfaces of dies 626 and 627 face one another. Accordingly, a front side surface of die 626 may be coupled to a bond via array 501, and an un-interconnected portion of such backside surface of die 627 may be coupled to a bond via array 505.

For die stack 604, short wires 510 of a bond via array 501 coupled to substrate 301 are coupled to a backside surface of a die 626. A front side surface of die 626 may have coupled thereto a spacer layer 622. A front side surface of a die 627 may be placed on top of such spacer layer 622. A backside surface of die 627 may be coupled to a redistribution layer ("RDL") 628, which may include one or more metal layers and one or more dielectric layers. Top ends of medium wires 515 of a bond via array 505 coupled to substrate 301 may be coupled to RDL 628 on a same side of die 627 to which RDL 628 is coupled. In this example, both of dies 626 and 627 are disposed within bond via array 505. In this configuration, die 626 is upward facing die, and die 627 is downward facing die.

For die stack 605, short wires 510 of a bond via array 501 coupled to substrate 301 are coupled to a backside surface of a die 626. A front side surface of die 626 may have coupled thereto a spacer layer 622. A backside surface of a die 627 may be placed on top of such spacer layer 622. Top ends of medium wires 515 of a bond via array 505 coupled to substrate 301 may be coupled to such backside surface of die 627, and a front side surface of die 627 may have disposed thereon another spacer layer 625. On top of spacer layer 625 may be disposed a backside surface of a die 629. Top ends of tall wires 520 of a bond via array 502 coupled to substrate 301 may be coupled to such backside surface of die 629. In this example, both of dies 626 and 627 are disposed within bond via array 502. In this configuration, dies 626, 627 and 629 are all upward facing.

Die stack 606 is similar to die stack 605, except generally for the following differences. A backside surface of die 629 may be coupled to RDL 628, and another portion of RDL 628 may be coupled to top ends of tall wires 520 of a bond via array 502 coupled to substrate 301.

Die stack 607 is similar to die stack 606, except generally for the following differences. Rather than wire bonding via wires 621 to top ends of tall wires 520 of a bond via array 502 coupled to substrate 301, and RDL 628 is disposed on an coupled to a top of die 629 and on top ends of wires 520, which coupling may be metallurgical. In this configuration, dies 626 and 627 are upward facing, and die 629 is downward facing.

Die stack **608** is similar to die stack **605**, except generally for the following differences. A die **633** is coupled to substrate **301** using a low-profile die-to-die interconnect technology (not shown), such as flip-chip for example. Die **633** is positioned under die **626** and is located within a bond via array **501**.

Die stack **609** is similar to die stack **608**, except generally for the following differences. A spacer layer **635** is disposed between dies **633** and **626**, and a cold plate or other heat sink **640** is coupled to a front side surface of die **629**.

Die stack **610** is similar to die stack **608**, except generally for the following differences. Die **629** is replaced with dies **631** and **632**. A portion of a backside surface of each of dies **631** and **632** is disposed on a spacer layer **625**. A left side portion of such backside surface of die **631** is coupled to top ends of tall wires **520** of a left side portion of a bond via array **502**, and a right side portion of such backside surface of die **632** is coupled to top ends of tall wires **520** of a right side portion of bond via array **502**.

Die stack **611** is similar to die stack **610**, except generally for the following differences. A die **633** is added, such as previously described with reference to die stack **608**.

Die stack **612** is similar to die stack **610**, except generally for the following differences. Dies **631** and **632** have respective front sides thereof on spacer layer **625**. Backsides of dies **631** and **632** are respectively wire bonded via wires **621** to top ends of tall wires **520** of a bond via array **502** on left and right side portions respectively thereof.

For die stack **613**, separate dies **636** and **637** are coupled to short wires **510** of a bond via array **501**. Bond via array **501** is disposed within a bond via array **505**; however, in this example a portion of bond via array **505**, or a separate bond via array **505**, is disposed within bond via array **501**. Dies **636** and **637** may have their respective front side surfaces coupled to bond via array **501**. An RDL **628** is metallurgically coupled to top ends of bond via array or arrays **505**, as well as to respective backside surfaces of dies **636** and **637**. A top surface of RDL **628** has metallurgically coupled thereto respective backside surfaces of dies **638** and **639**. Dies **638** and **639** may be positioned above dies **636** and **637**, respectively.

FIGS. **6E-1** through **6E-9** are block diagrams of side views of exemplary package-on-package assemblies ("die stacks") **603R**, **604R**, **605R**, **607R**, **608R**, **609R**, **610R**, **611R**, and **613R**, each of which may have two or more bond via arrays with wires of different heights. With simultaneous reference to FIGS. **6A** through **6D** and **6E-1** through **6E-9**, die stacks **603R**, **604R**, **605R**, **607R**, **608R**, **609R**, **610R**, **611R**, and **613R** are further described. Generally, die stacks **603R**, **604R**, **605R**, **607R**, **608R**, **609R**, **610R**, **611R**, and **613R** respectively correspond to **603**, **604**, **605**, **607**, **608**, **609**, **610**, **611**, and **613**, except that die stacks **603R**, **604R**, **605R**, **607R**, **608R**, **609R**, **610R**, **611R**, and **613R** may be assembled in a reverse direction or order ("upside down"). Additionally, die stack **607R** may have dies **626**, **627** and **629** sequentially interconnected using bumps **623**, and die stacks **608R** and **611R** may have dies **633** and **626** interconnected using bumps **623**. Additionally, optionally die **627** may include TSVs **667** for interconnect dies **626** and **629** through such TSVs **667**. Along those lines, even though bond via arrays or bumps are illustratively depicted in die stacks as described herein, in some implementations such bumps or balls may be switched for bond via arrays, and vice versa. Additionally, in die stack **613R**, a bond via array **505** between dies **636** and **637** in die stack **613** may be omitted in die stack **613R**. An initial or base die or dies in one or

more of die stacks **603R**, **604R**, **605R**, **607R**, **608R**, **609R**, **610R**, **611R**, and **613R** may be an interposer.

Die stacks **603R**, **604R**, **605R**, **607R**, **608R**, **609R**, **610R**, **611R**, and **613R** may be assembled before or after singulation. Furthermore, one or more of die stacks **603R**, **604R**, **605R**, **607R**, **608R**, **609R**, **610R**, **611R**, and **613R** may be coupled to a substrate, such as substrate **301** for example.

FIGS. **7A** through **7E-3** are block diagrams of side views depicting several exemplary die stacks **701** through **703**, which may in part be commonly formed with reference to FIGS. **7A** through **7D**. Processing of such die stacks **701** through **703** may be included as part of process flow **300**. With simultaneous reference to FIGS. **7A** through **7E-3**, exemplary die stacks **701** through **703** are further described.

At FIG. **7A**, to provide a spacer layer **711**, an adhesive, encapsulant or molding compound, such as used to provide a spacer layer as previously described, may be deposited, such as by any of a variety of paste printing, transfer molding, liquid encapsulant molding, vacuum laminating, spin coating or other suitable application. Spacer layer **711** may be formed over substrate **301** such that such molding compound surrounds wires **510** and **515**, with top portions thereof extending above an upper surface of spacer layer **711**. Spacer layer **711** may provide additional support for wires **510**, as well as subsequently wires **515**, for attachment of a die.

At FIG. **7B**, a die **626** may be attached to top ends of short wires **510**. Even though attachment of a single die **626** is described below in additional detail, a stack of dies, such as die **626** and another die **726**, as well as other die, may optionally be coupled to one another in a stack. In such an implementation, longer outer BVA wires, as generally indicated by optional lengths **727**, may be used to accommodate a die stack. In one implementation, the stack of dies over die **626** may be couple to another via through die connectors or electrodes or TSVs.

At FIG. **7C**, an underfill layer **712** may be deposited so as to be disposed over spacer layer **711**, as well as under die **626**. Optionally, underfill layer **712** may be deposited after spacer layer **711** is deposited but before attachment of die **626**. At FIG. **7D**, another spacer layer **713** may be deposited, such as previously described with reference to spacer layer **711**, so as to surround a sidewall or sidewalls of die **626**, as well as to be disposed around medium wires **515**. Top portions of medium wires **515** extend above an upper surface of spacer layer **713**.

For die stack **701**, at FIG. **7E-1** a die **627** may be coupled to such top portions of medium wires of FIG. **7D**, and subsequent thereto another underfill layer **714** may be deposited under die **627**. Optionally, one or more other dies **627** may be part of such die stack **701**.

For die stack **702**, at FIG. **7E-2** dies **631** and **632** may respectively be coupled to such top portions of medium wires of FIG. **7D**, and subsequent thereto an underfill layer **714** may be deposited under dies **631** and **632**.

For die stack **703**, at FIG. **7E-3** an RDL **628** may respectively be coupled to top portions of medium wires of FIG. **7D**, and be metallurgically coupled to die **626**. One or more dies **641** through **644** may be metallurgically coupled to a top surface of RDL **628**.

Accordingly, it should be understood that substrate **301** may be a wafer for wafer-level packaging, or substrate **301** may be an individual package substrate for chip-level packaging. It should further be understood that multiple wires of varying diameters and lengths may be used. Along those lines, generally short wires may have a length in a range of approximately 0.01 to 0.1 mm, a diameter in a range of

approximately 0.01 to 0.1 mm, and a pitch in a range of approximately less than 0.5 mm. Generally medium wires may have a length in a range of approximately 0.05 to 0.5, a diameter in a range of approximately 0.01 to 0.1 mm, and a pitch in a range of approximately 0.01 to 0.5. Generally tall wires may have a length in a range of approximately 0.1 to 1 mm, a diameter in a range of approximately 0.01 to 0.2, and a pitch in a range of approximately 0.01 to 0.5. Additionally, such short, medium and tall wires may be made of different materials for different conductivities and/or varying e-moduli. Such wires may be formed with e-beam may have minimal intermetallic formation with fast fusion bonding, minimal thermal preload on a package, and/or reduced stress in a package. Furthermore, such wires formed with e-beam or with photolithography may be vertical wires for densely packed bond via arrays.

Generally, wires, such as wires **510**, **515**, and **520** are vertical within ± 3 degrees with respect to being perpendicular to a top surface **318** of substrate **301**. However, such wires need not be formed with such verticality in other implementations.

FIGS. **8A** and **8B** are respective top-down perspective views depicting exemplary angled wire configurations **800** and **810**. In angled wire configuration **800**, an angled tall wire **520L** and a tall wire **520** are fuse bonded to a same landing pad **801** on a top surface **318** of substrate **301**. A solder ball or bump **454** may be commonly deposited on top ends of such wires **520L** and **520**. In this angled wire configuration **800**, which may be used for a high-power, a robust ground or supply, or other application, angled tall wire **520L** may generally be in a range of approximately less than 90 degrees with respect to top surface **318**. In angled wire configuration **810**, a bond via array **811** includes angled tall wires **520L**, as well as vertical tall wires **520**. Angled tall wires **520** may be used to extend to a different die than tall wires **520**, to provide a wire bonding surface separate from vertical tall wires **520** which may be coupled to a die or RDL, or other application. Along the above lines, at least one bond via array, whether for tall, medium, or short wires, may have a portion of such wires thereof being angled wires, such as angled wires **520L** for example.

FIGS. **9A** and **9B** are block diagrams of side views of exemplary in-process bond via array configurations **911** through **913** and **914** through **916**, respectively. FIGS. **9A** and **9B** are described together, as portions of each may be used in a device.

Along those lines, two or more of same instances or combinations of different instances of bond via array configurations **911** through **916** may be disposed on a common substrate **301**. Each of bond via array configurations **911** through **916** includes two bond via arrays with wires **310** and **320** of different heights, as previously described. In these examples, short wires **310** and tall wires **320** are used; however, other combinations of wires may be used in other examples in accordance with the above description.

Bond via array configuration **911** includes a die **626** coupled to an inner bond via array formed of wires **310**. An outer bond via array formed of wires **320**, in which such inner bond via array is located, has coupled thereto one or more electronic components **901**. Die **626** may be coupled to one or more electronic components **901** via wires **310** and **320**, as well as by bumps **623** and substrate **301** such as previously described. Electronic components **901** may be above die **626**.

Electronic components **901** are discrete components or devices. Electronic components **901** may be active, passive, or electromechanical components. For purposes of clarity by

way of example and not limitation, it shall be assumed that electronic components **901** are passive components. Examples of passive components include one or more capacitors ("C") including arrays and networks thereof, one or more resistors ("R") including arrays and networks thereof, one or more magnetic devices including inductors ("L"), RC networks, LC networks, RLC networks, transducers, sensors, detectors, and antennas, among others. Examples of active components include transistors, optoelectronic devices, and diodes, among others.

Bond via array configuration **912** includes a die **626** coupled to an inner bond via array formed of wires **310**. An outer bond via array formed of wires **320**, in which such inner bond via array is located, has coupled thereto an RDL **628**. Coupled to RDL **628** may be one or more electronic components **901**. Die **626** may be coupled to one or more electronic components **901** via wires **310** and **320** and RDL **628**, as well as by bumps **623** and substrate **301** such as previously described. Electronic components **901** may be above die **626**, and RDL **628** may be over die **626** by bridging wires **320** of a bond via array thereof.

Bond via array configuration **913** includes a die **626** coupled to an inner bond via array formed of wires **310**. An outer bond via array formed of wires **320**, in which such inner bond via array is located, has coupled thereto an interposer **908**. Coupled to interposer **908** may be one or more electronic components **901**. Again, die **626** may be coupled to one or more electronic components **901** via wires **310** and **320** and interposer **908**, as well as by bumps **623** and substrate **301** such as previously described. Electronic components **901** may be above die **626**, and interposer **908** may be over die **626** by bridging wires **320** of a bond via array thereof.

In bond via array configurations **911** through **913**, electronic components **901** are disposed outside of a perimeter of an inner die **626**. With respect to bond via array configurations **911** through **913**, at least one electronic component **901** is at least partially disposed outside of an inner bond via array, and a die **626** is at least partially disposed within an outer bond via array. However, in bond via array configurations **914** through **916**, at least one electronic component **901** is disposed at least partially within an outer bond via array, as well as disposed within an outside perimeter of upper die **627**.

Bond via array configuration **914** includes a die **627** coupled to an outer bond via array formed of wires **320**. An inner bond via array formed of wires **310**, located within such outer bond via array, may have coupled thereto one or more electronic components **901**. Die **627** may be coupled to one or more electronic components **901** via wires **310** and **320**, as well as by bumps **623** and substrate **301** such as previously described. Electronic components **901** may be below die **627**, and die **627** may be over one or more electronic components **901** by bridging wires **320** of a bond via array thereof.

Bond via array configuration **915** includes a die **627** coupled to an outer bond via array formed of wires **320**. An inner bond via array formed of wires **310**, located within such outer bond via array, may have coupled thereto an RDL **628**. RDL **628** may have coupled thereto one or more electronic components **901**. Die **627** may be coupled to one or more electronic components **901** via wires **310** and **320** and RDL **628**, as well as by bumps **623** and substrate **301** such as previously described. Electronic components **901** may be below die **627**, and die **627** may be over one or more electronic components **901** by bridging wires **320** of a bond via array thereof.

Bond via array configuration **916** includes a die **627** coupled to an outer bond via array formed of wires **320**. An inner bond via array formed of wires **310**, located within such outer bond via array, may have coupled thereto an interposer **908**. Interposer **908** may have coupled thereto one or more electronic components **901**. Die **627** may be coupled to one or more electronic components **901** via wires **310** and **320** and interposer **908**, as well as by bumps **623** and substrate **301** such as previously described. Electronic components **901** may be below die **627**, and die **627** may be over one or more electronic components **901** by bridging wires **320** of a bond via array thereof.

While the foregoing describes exemplary embodiment(s) in accordance with one or more aspects of the invention, other and further embodiment(s) in accordance with the one or more aspects of the invention may be devised without departing from the scope thereof, which is determined by the claim(s) that follow and equivalents thereof. Claim(s) listing steps do not imply any order of the steps. Trademarks are the property of their respective owners.

What is claimed is:

1. An apparatus, comprising:
 - a first substrate having a conductive layer;
 - first plated conductors in a first region extending from a surface of the conductive layer;
 - second plated conductors in a second region extending from the surface of the conductive layer;
 - wherein the first plated conductors and the second plated conductors are external to the first substrate;
 - wherein the first region is disposed at least partially within the second region;
 - wherein the first plated conductors are of a first height;
 - wherein the second plated conductors are of a second height greater than the first height;
 - a second substrate coupled to first ends of the first plated conductors;
 - the second substrate having at least one electronic component coupled thereto;
 - a die coupled to second ends of the second plated conductors; and
 - the die located over the at least one electronic component.
2. The apparatus according to claim 1, wherein the at least one electronic component includes a discrete passive component.
3. The apparatus according to claim 2, wherein the second substrate includes a redistribution layer.
4. The apparatus according to claim 2, wherein the second substrate includes an interposer.
5. The apparatus according to claim 1, wherein the second substrate includes a redistribution layer.
6. The apparatus according to claim 5, wherein the at least one electronic component includes a network of two discrete passive components selected from a resistor, a capacitor, or an inductor coupled to the redistribution layer.
7. The apparatus according to claim 1, wherein the second substrate includes an interposer.
8. The apparatus according to claim 7, wherein the at least one electronic component includes a network of two discrete passive components selected from a resistor, a capacitor, or an inductor coupled to the interposer.
9. The apparatus according to claim 1, wherein:
 - the first plated conductors include a first plated layer; and
 - the second plated conductors include the first plated layer and a second plated layer thereover.
10. An apparatus, comprising:
 - a first substrate having a conductive layer;

first plated conductors in a first region extending from a surface of the conductive layer;

second plated conductors in a second region extending from the surface of the conductive layer;

wherein the first plated conductors and the second plated conductors are external to the first substrate;

wherein the first region is disposed at least partially within the second region;

wherein the first plated conductors are of a first height;

wherein the second plated conductors are of a second height greater than the first height;

a die coupled to first ends of the first plated conductors;

a second substrate coupled to second ends of the second plated conductors;

the second substrate having at least one electronic component coupled thereto; and

the second substrate located over the die.

11. The apparatus according to claim 10, wherein the at least one electronic component includes a discrete passive component.

12. The apparatus according to claim 11, wherein the second substrate includes a redistribution layer.

13. The apparatus according to claim 11, wherein the second substrate includes an interposer.

14. The apparatus according to claim 10, wherein the second substrate includes a redistribution layer.

15. The apparatus according to claim 14, wherein the at least one electronic component includes a network of two discrete passive components selected from a resistor, a capacitor, or an inductor coupled to the redistribution layer.

16. The apparatus according to claim 10, wherein the second substrate includes an interposer.

17. The apparatus according to claim 16, wherein the at least one electronic component includes a network of two discrete passive components selected from a resistor, a capacitor, or an inductor coupled to the interposer.

18. The apparatus according to claim 10, wherein:

- the first plated conductors include a first plated layer; and
- the second plated conductors include the first plated layer and a second plated layer thereover.

19. A method, comprising:

- obtaining a first substrate;
- forming a conductive layer on an upper surface of the first substrate;

forming a first resist layer on the conductive layer;

patterning the first resist layer to provide a first mask with first vias from an upper surface of the first resist layer down to an upper surface of the conductive layer;

through-mask plating in the first vias to provide first plated conductors in a first region extending from the upper surface of the conductive layer;

forming a second resist layer over the first plated conductors;

patterning the second resist layer to provide a second mask with second vias from an upper surface of the second resist layer down to upper surfaces of a subset of the first plated conductors;

through-mask plating in the second vias to provide second plated conductors in a second region extending down to the upper surfaces of and including the subset of the first plated conductors;

removing the first resist layer and the second resist layer;

removing portions of the conductive layer between the first plated conductors and the second plated conductors;

wherein the first plated conductors and the second plated conductors are external to the first substrate;

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wherein the first region is disposed at least partially within the second region;
 wherein the first plated conductors are of a first height;
 wherein the second plated conductors are of a second height greater than the first height;
 coupling a second substrate to first ends of the first plated conductors;
 the second substrate having at least one electronic component coupled thereto;
 coupling a die to second ends of the second plated conductors; and
 wherein the die is located over the at least one electronic component.

20. The method according to claim 19, wherein:
 the first conductive layer is a seed layer or an adhesion layer; and
 the removing of the first resist layer precedes the forming of the second resist layer.

21. An apparatus, comprising:
 a first substrate;

first plated conductors on a first region of a surface of the first substrate, the first plated conductors directly coupled to the surface of the first substrate;
 second plated conductors on a second region of the surface of the first substrate, the second plated conductors directly coupled to the surface of the first substrate;

wherein:

the first plated conductors and the second plated conductors are external to the first substrate;
 the first region is disposed at least partially within the second region;
 the first plated conductors are of a first height; and
 the second plated conductors are of a second height greater than the first height;

a first electronic component coupled to ends of the first plated conductors;

a second substrate coupled to ends of the second plated conductors, the second substrate comprising a laminate substrate; and

a second electronic component coupled to the second substrate and located over the first electronic component.

22. The apparatus of claim 21, further comprising a support layer or molding layer disposed on the surface of the first substrate, wherein at least a portion of the second plated conductors is within the support layer or molding layer.

23. The apparatus of claim 21, further comprising an underfill layer disposed between the first electronic component and the second electronic component.

24. The apparatus of claim 21, further comprising an underfill layer disposed between the first electronic component and the second substrate.

25. The apparatus of claim 21, wherein the first electronic component is connected to the second electronic component via at least the first and second plated conductors.

26. The apparatus of claim 21, wherein the second substrate is coupled to the second electronic component via at least one wire.

27. The apparatus of claim 21, further comprising bump or ball interconnects disposed between and coupling the second substrate and the ends of the second plated conductors.

28. The apparatus of claim 21, wherein the first substrate comprises an interposer or a redistribution layer.

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29. The apparatus of claim 21, wherein the second electronic component comprises a network of two discrete circuit elements.

30. An apparatus, comprising:
 an interconnection component;

first plated conductors on a first region of a surface of the interconnection component, the first plated conductors directly coupled to the surface of the interconnection component;

second plated conductors on a second region of the surface of the interconnection component, the second plated conductors directly coupled to the surface of the interconnection component;

wherein:

the first plated conductors and the second plated conductors are external to the interconnection component;

the first region is disposed at least partially within the second region;

the first plated conductors are of a first height; and
 the second plated conductors are of a second height greater than the first height;

a die coupled to ends of the first plated conductors;

a laminate substrate coupled to ends of the second plated conductors; and

an electronic component electrically connected to at least some of the second plated conductors and located over the die.

31. The apparatus of claim 30, further comprising a support layer or molding layer disposed on the surface of the interconnection component, wherein at least a portion of the second plated conductors is within the support layer or molding layer.

32. The apparatus of claim 30, further comprising an underfill layer disposed between the die and the electronic component.

33. The apparatus of claim 30, further comprising an underfill layer disposed between the die and the laminate substrate.

34. The apparatus of claim 30, wherein the laminate substrate is coupled to the die via at least one wire.

35. The apparatus of claim 30, wherein the electronic component is connected to the die via at least the first plated conductors.

36. The apparatus of claim 30, further comprising bump or ball interconnects disposed between and coupling the laminate substrate and the ends of the second plated conductors.

37. The apparatus of claim 30, wherein the interconnection component comprises an interposer or a redistribution layer.

38. The apparatus of claim 30, wherein the electronic component comprises a network of two discrete circuit elements.

39. The apparatus of claim 30, wherein the electronic component is a first electronic component, and wherein the apparatus further comprises a second electronic component electrically connected to at least some of the second plated conductors and located over the die.

40. The apparatus of claim 39, wherein the die is connected to the first and second electronic components via at least the first plated conductors.

41. The apparatus of claim 40, wherein the first and second electronic components are disposed at least partially outside of the first region.

42. The apparatus of claim 30, wherein a back surface of the die is at a third height between the first and second heights.

43. The apparatus of claim 42, further comprising a spacer over the back surface of the die, the spacer having a thickness substantially equal to the difference between the second and third heights. 5

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