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(54) **MASKS FORMED BASED ON INTEGRATED CIRCUIT LAYOUT DESIGN HAVING CELL THAT INCLUDES EXTENDED ACTIVE REGION**

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***H01L 27/02*** (2006.01)
***H01L 27/092*** (2006.01)
***G06F 30/392*** (2020.01)

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CPC ........ ***G06F 30/392*** (2020.01); ***H01L 27/0207*** (2013.01)

(58) **Field of Classification Search**
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See application file for complete search history.

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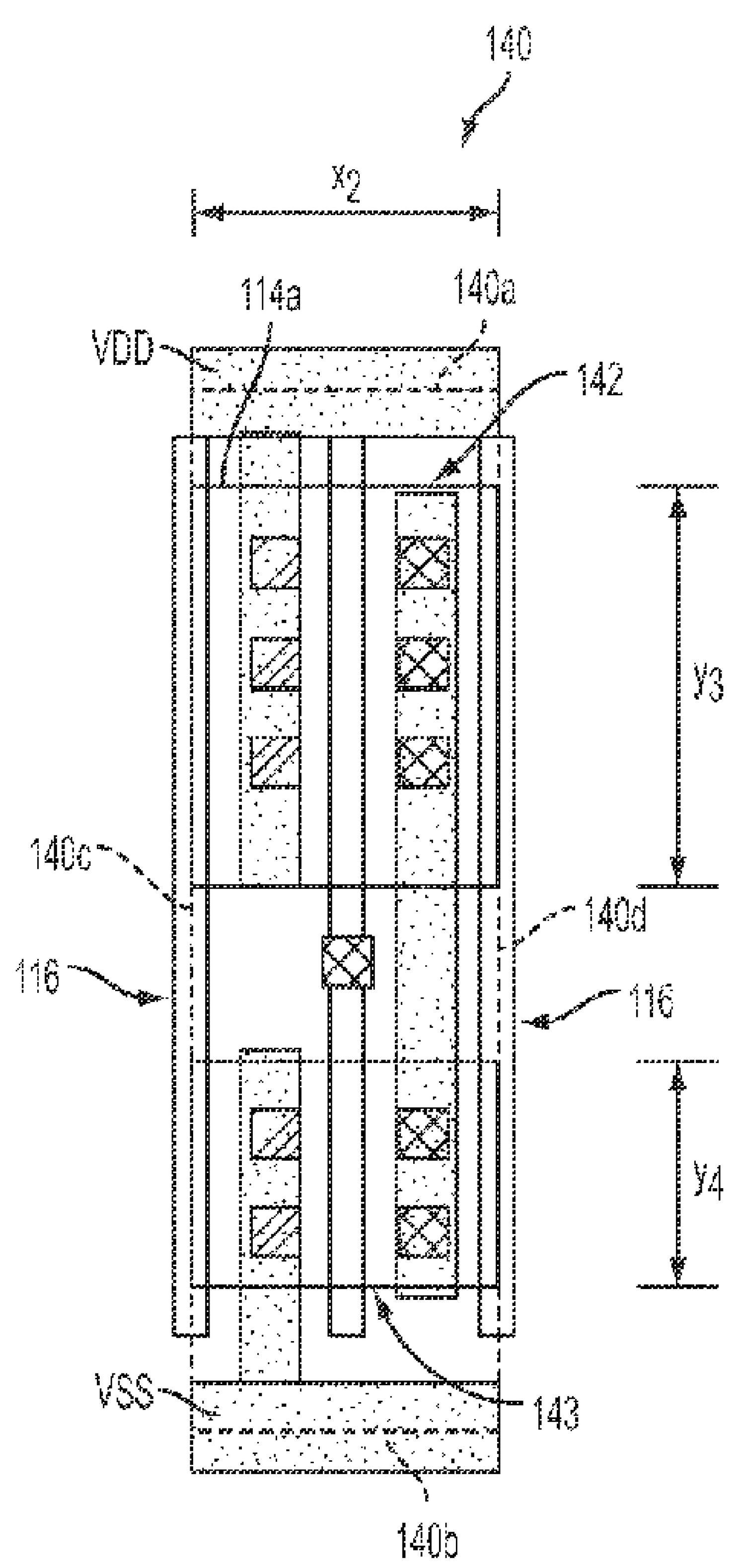
(57) **ABSTRACT**

A set of masks corresponds to an integrated circuit layout. The integrated circuit layout includes a first cell having a first transistor region and a second transistor region, and a second cell having a third transistor region and a fourth transistor region. The first cell and the second cell adjoin each other at side cell boundaries thereof, the first transistor region and the third transistor region are formed in a first continuous active region, and the second transistor region and the fourth transistor region are formed in a second continuous active region. The set of masks is formed based on the integrated circuit layout.

**38 Claims, 8 Drawing Sheets**



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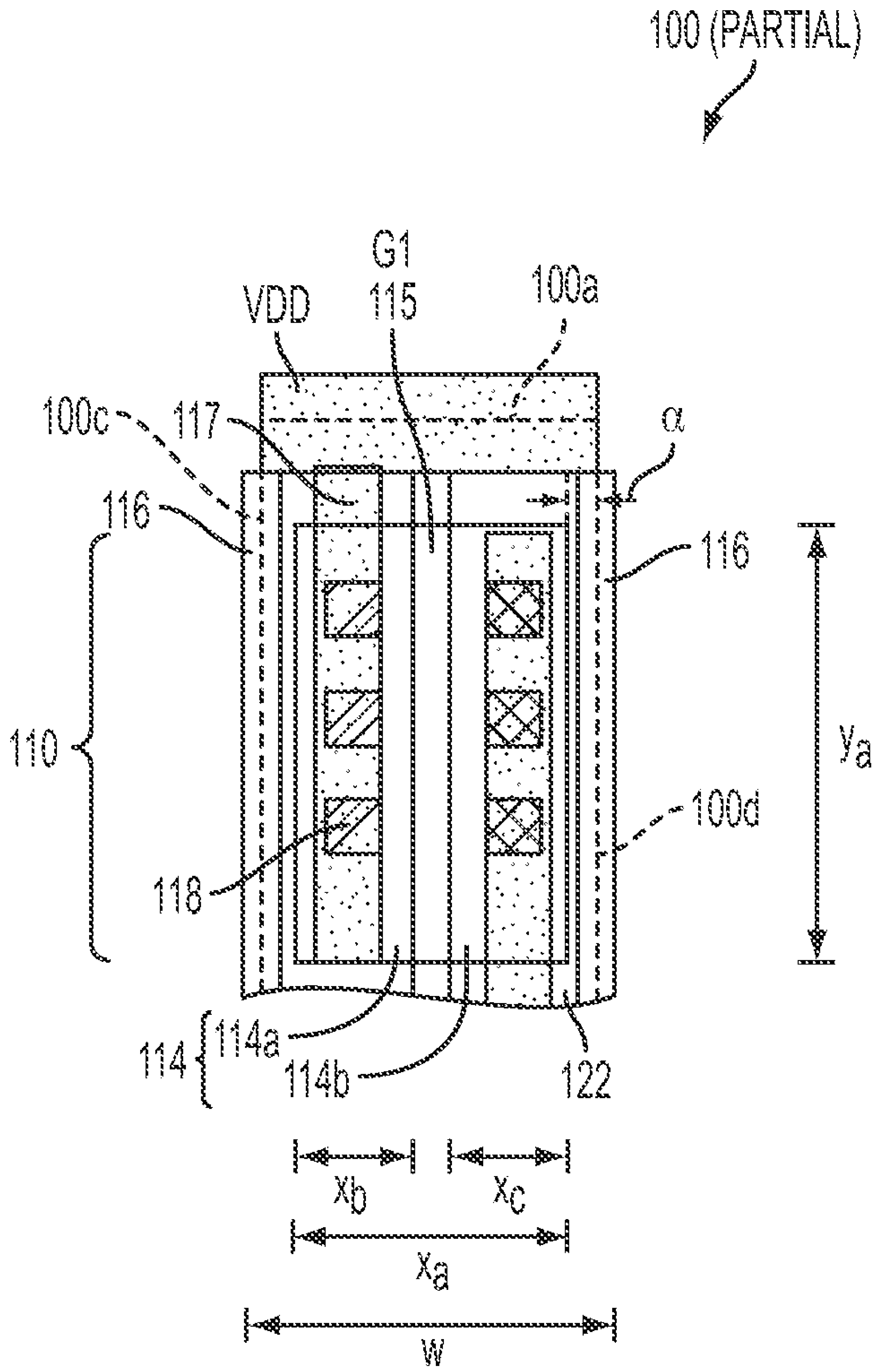

100 (PARTIAL)
G1
115
VDD
100a
100c
117
α
116
116
110
$y_a$
100d
118
114
114a
114b
122
$x_b$
$x_c$
$x_a$
w

FIG. 1A

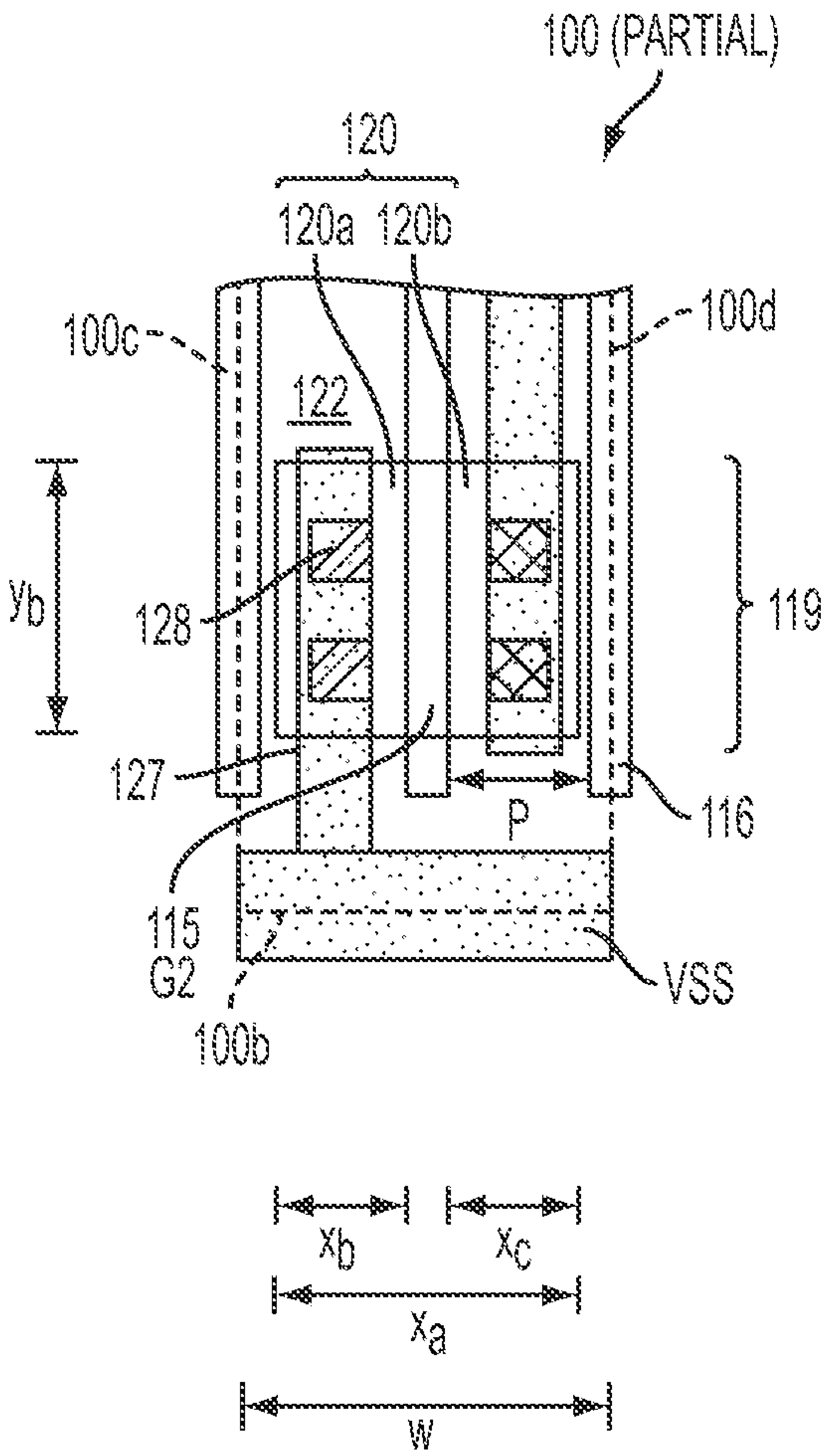
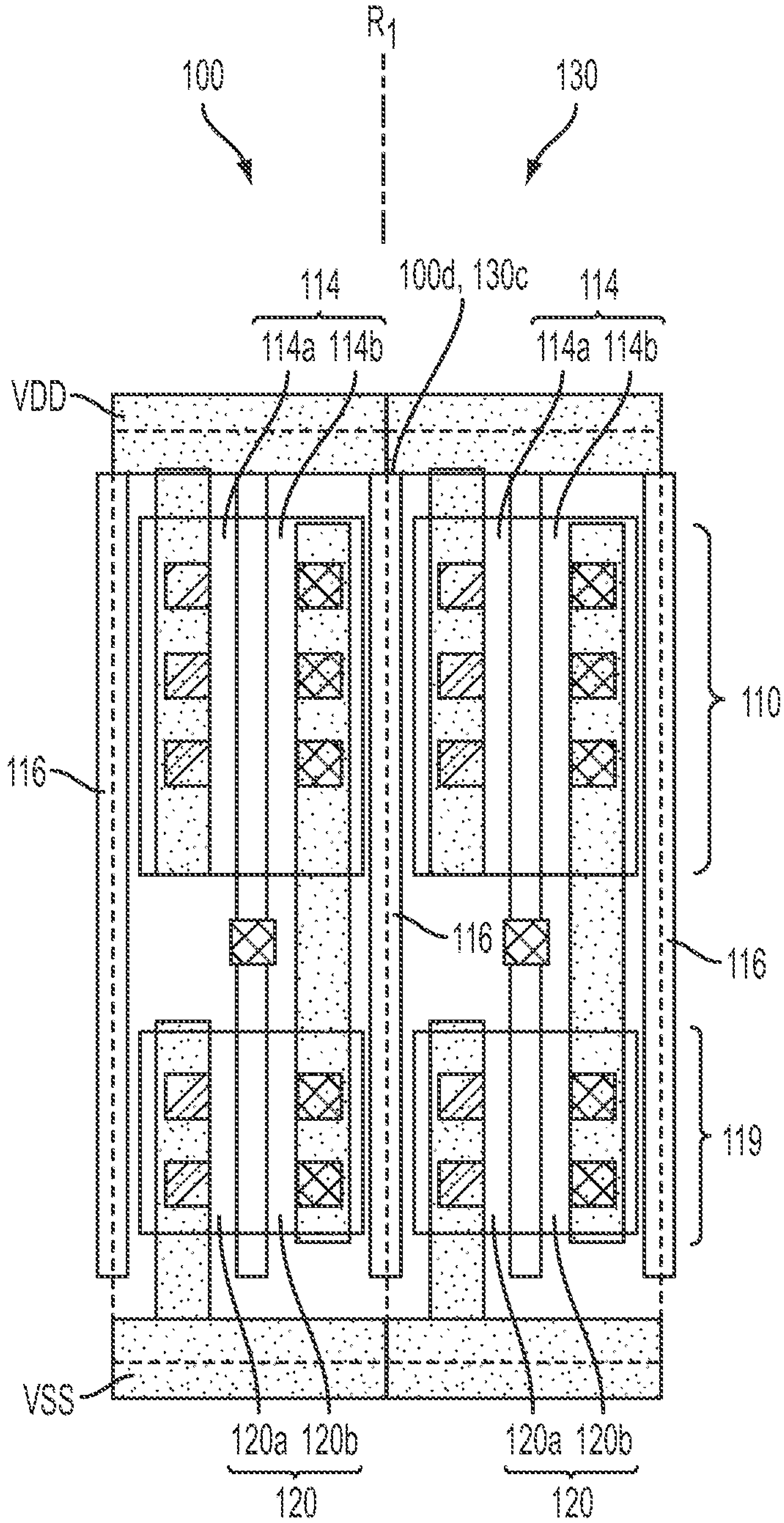

100 (PARTIAL)
120
120a
120b
100c
100d
122
yb
128
119
127
P
116
115
G2
VSS
100b
xb
xc
xa
w

FIG. 1B



R1
100
130
114
100d, 130c
114
114a 114b
114a 114b
VDD
116
110
116
116
119
VSS
120a 120b
120
120a 120b
120


FIG. 2A

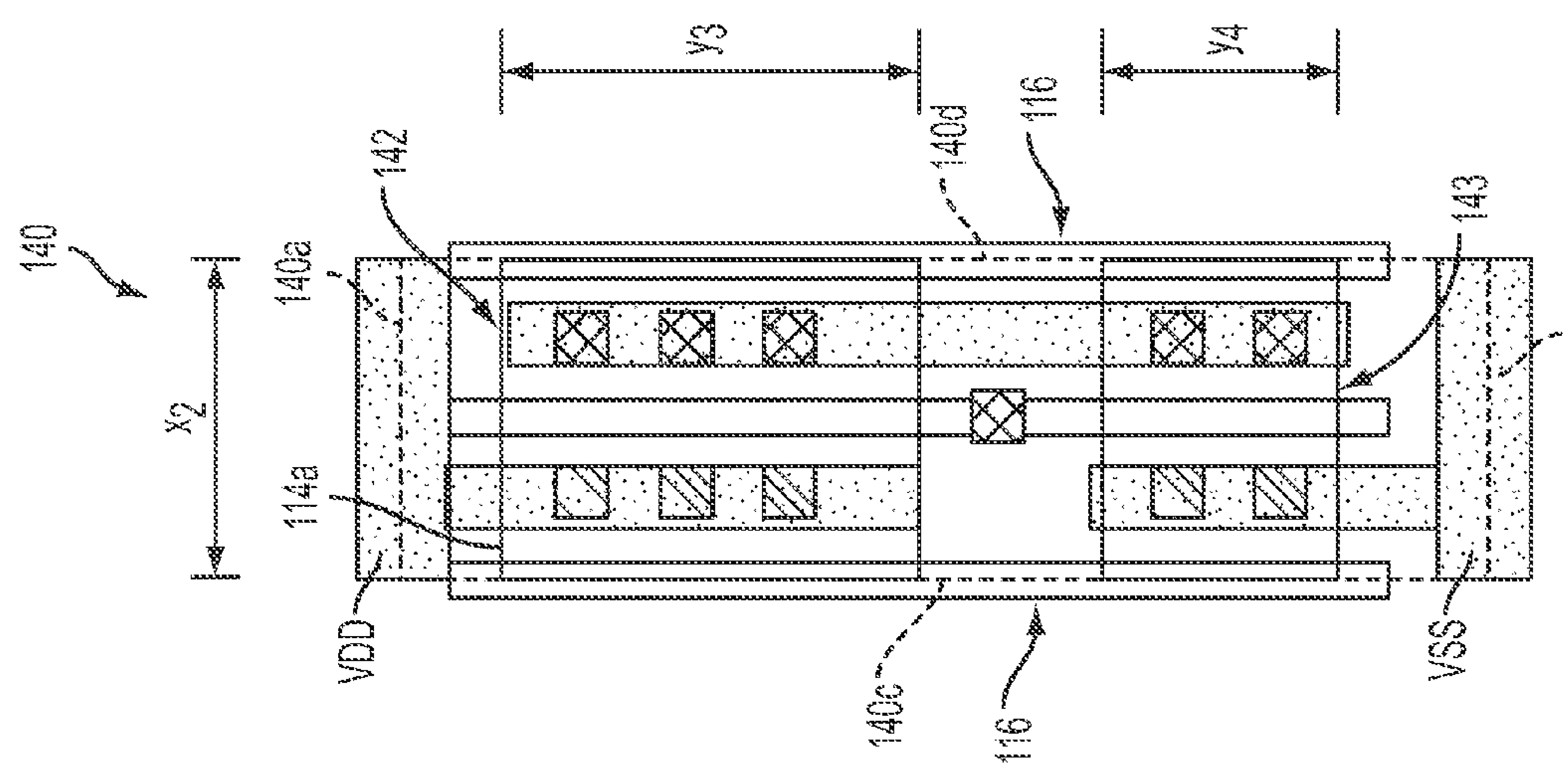

140
142
140a
x2
114a
VDD
Y3
140d
116
Y4
143
140b
140c
116
VSS

FIG. 2C

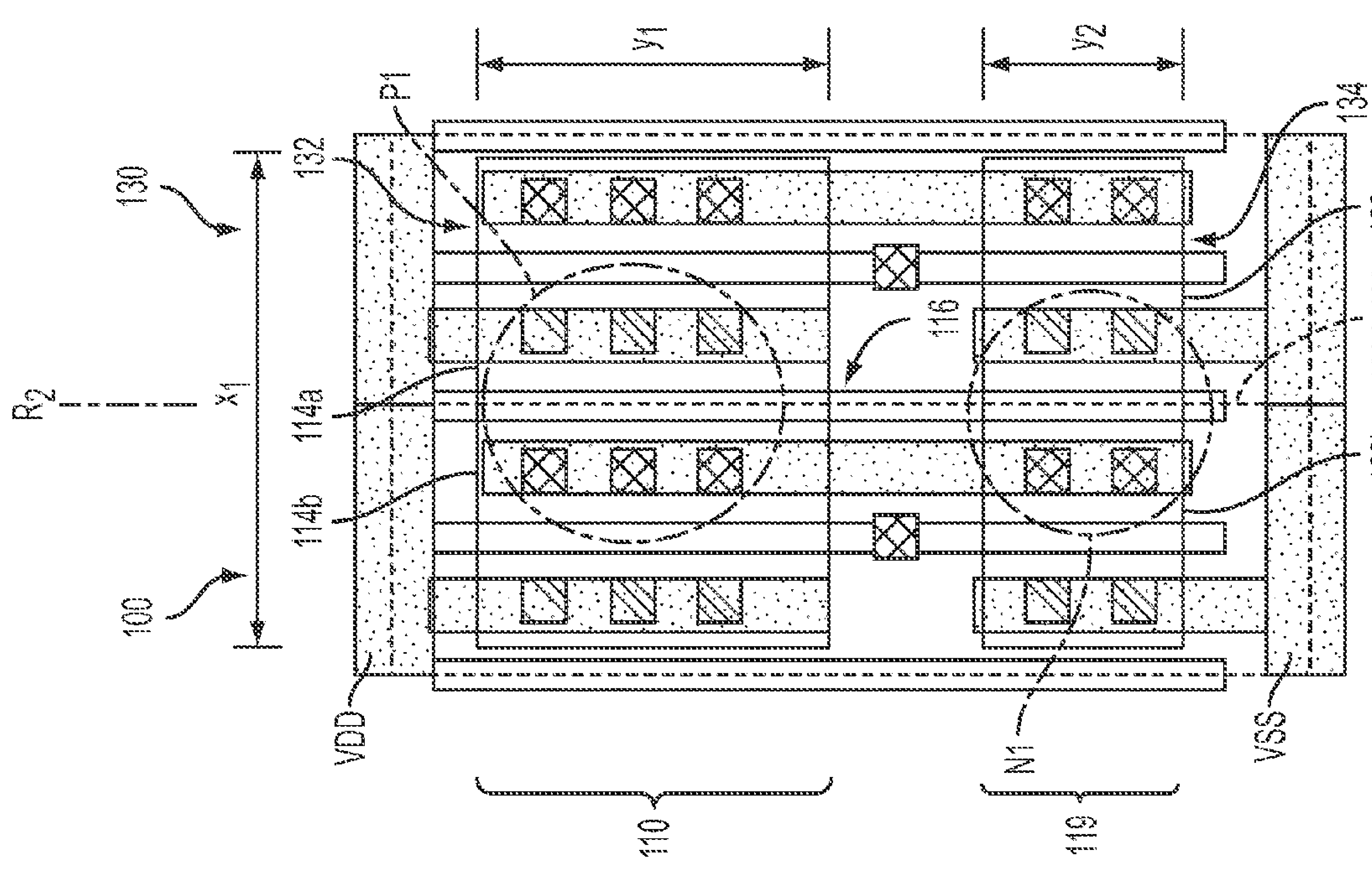

R2
x1
130
100
132
P1
Y1
Y2
134
120a
116
114a
114b
100d, 130c
120b
VDD
N1
VSS
110
119

FIG. 2B

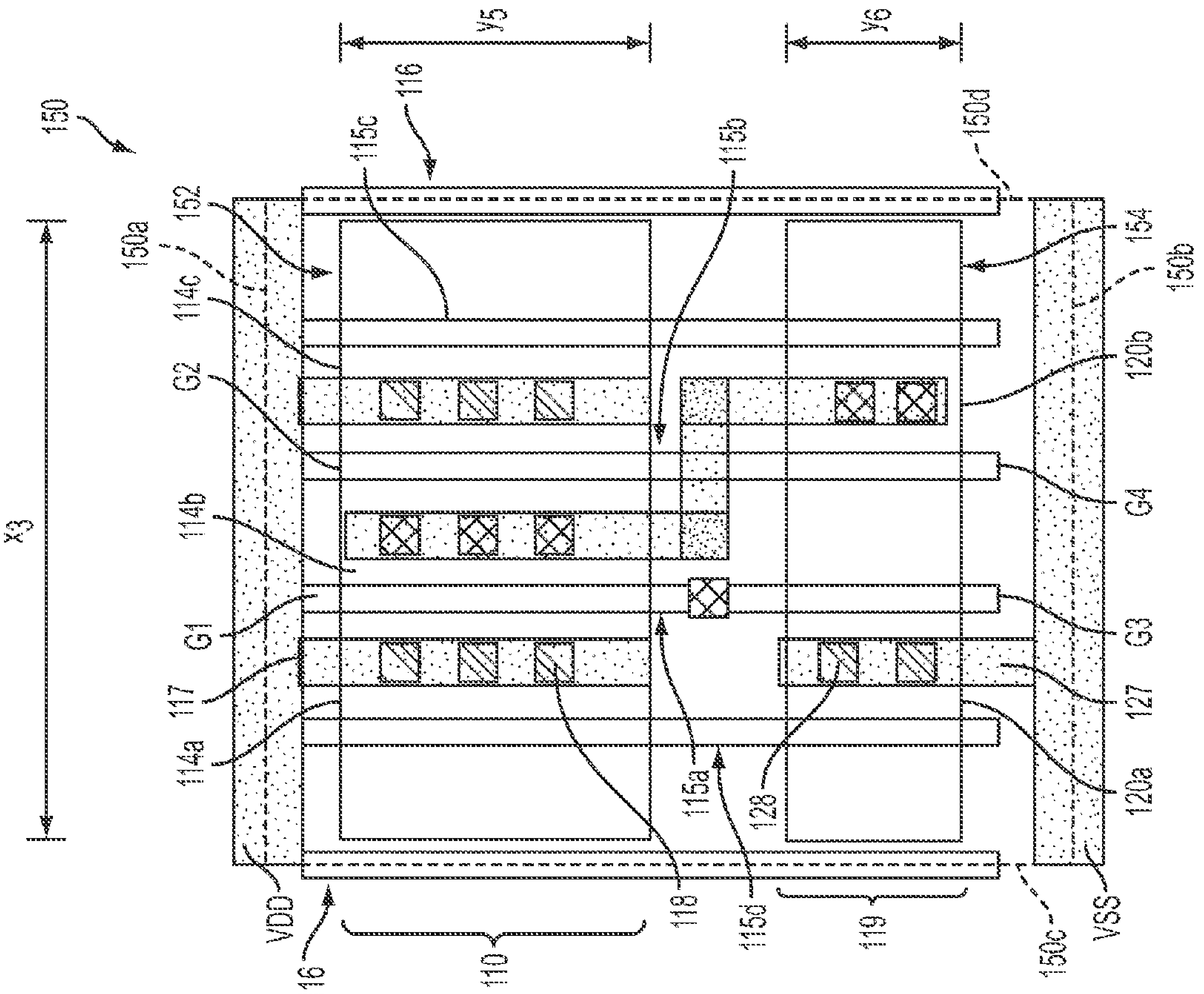

150
X3
Y5
Y6
116
115c
115b
150d
152
150a
114c
G2
114b
G1
117
114a
154
150b
120b
G4
G3
127
120a
128
115a
118
115d
119
150c
VDD
VSS
110

FIG. 4

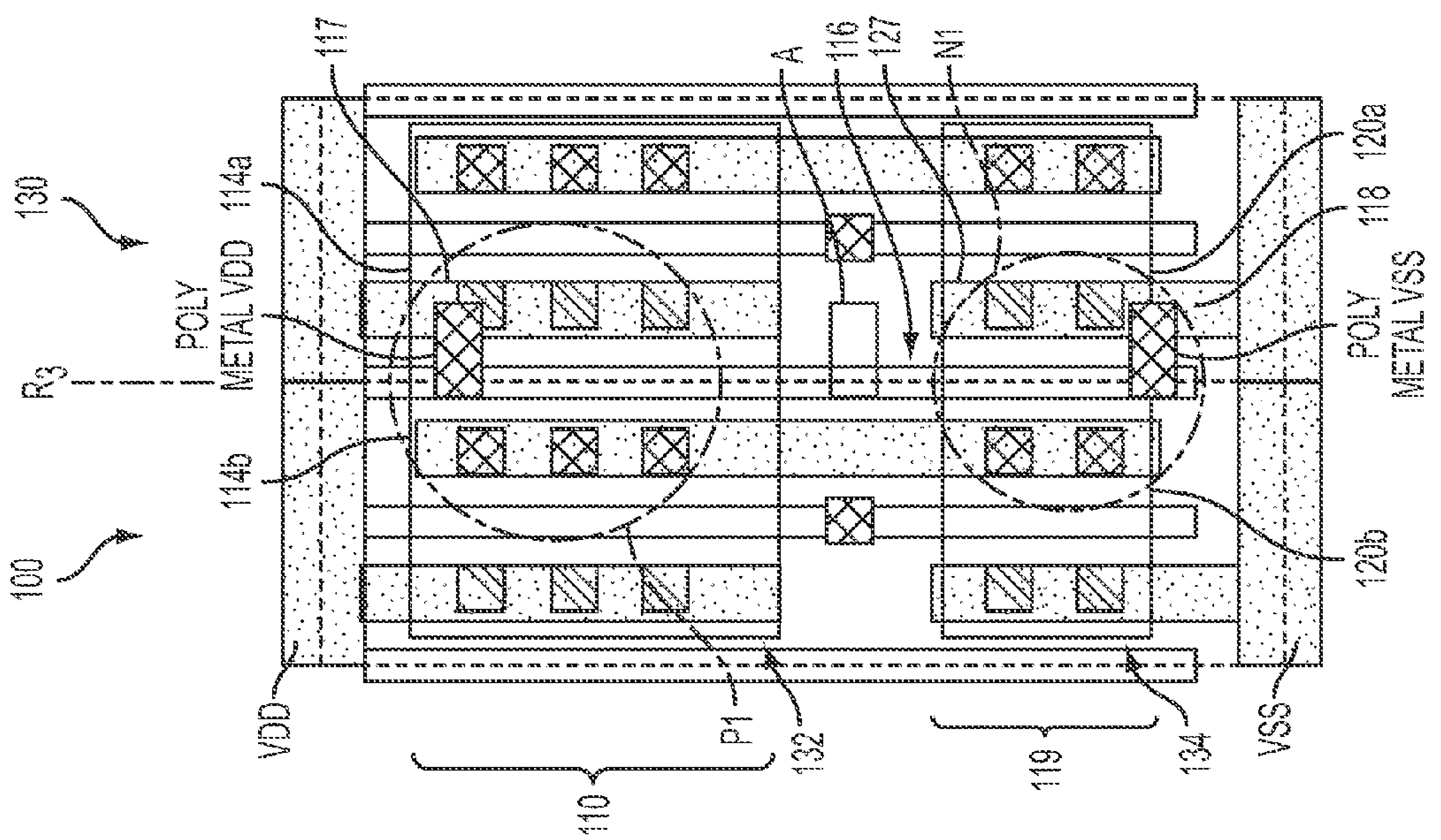

130
100
R3
POLY
METAL VDD
114a
114b
117
A
116
127
N1
120a
118
POLY
METAL VSS
120b
VDD
P1
132
110
119
134
VSS

FIG. 3

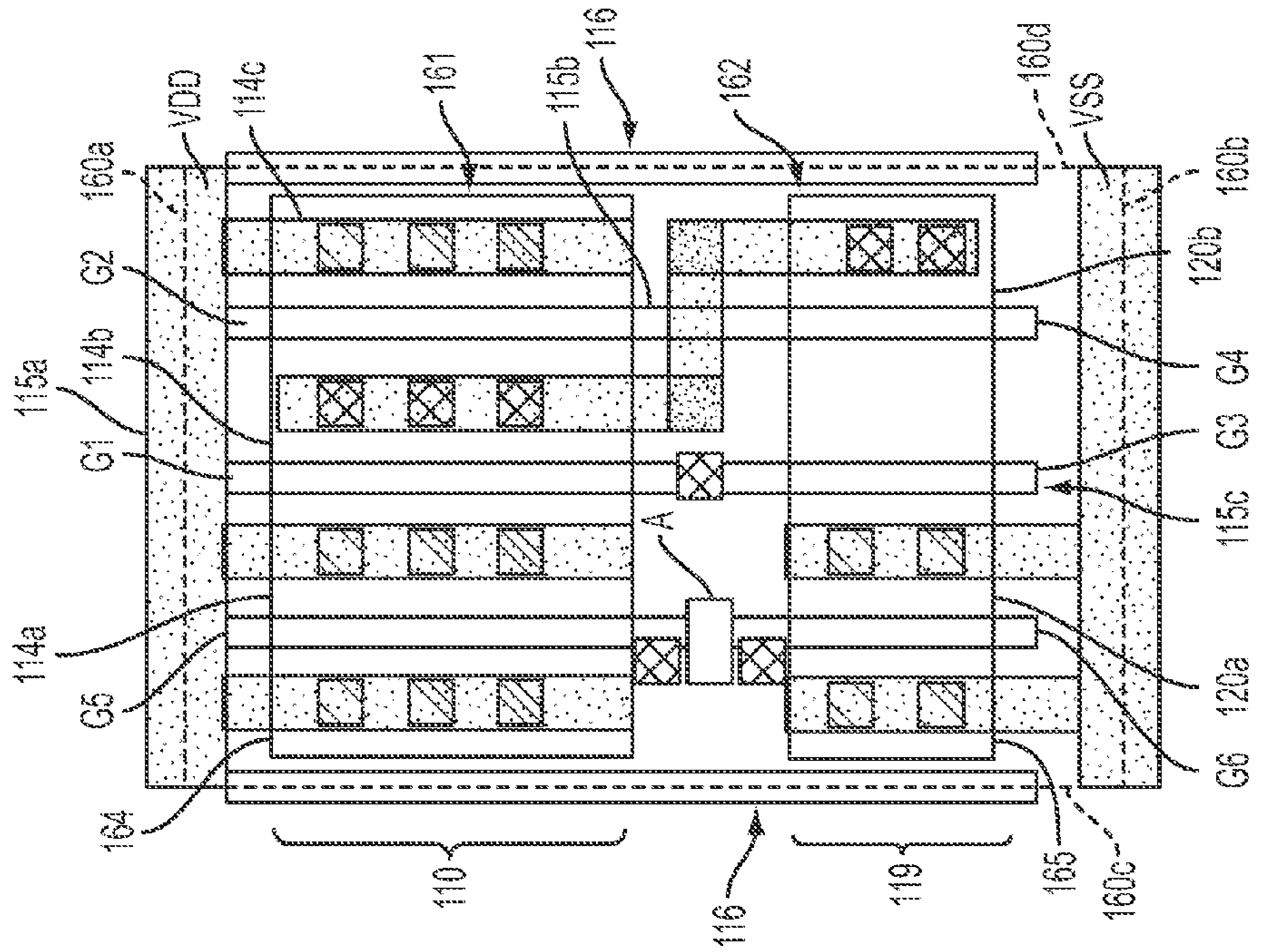

160'
VDD
160a
114c
161
115b
116
162
160d
VSS
160b
G2
114b
115a
G1
114a
G5
164
110
116
119
165
160c
A
120b
G4
G3
115c
120a
G6

FIG. 6

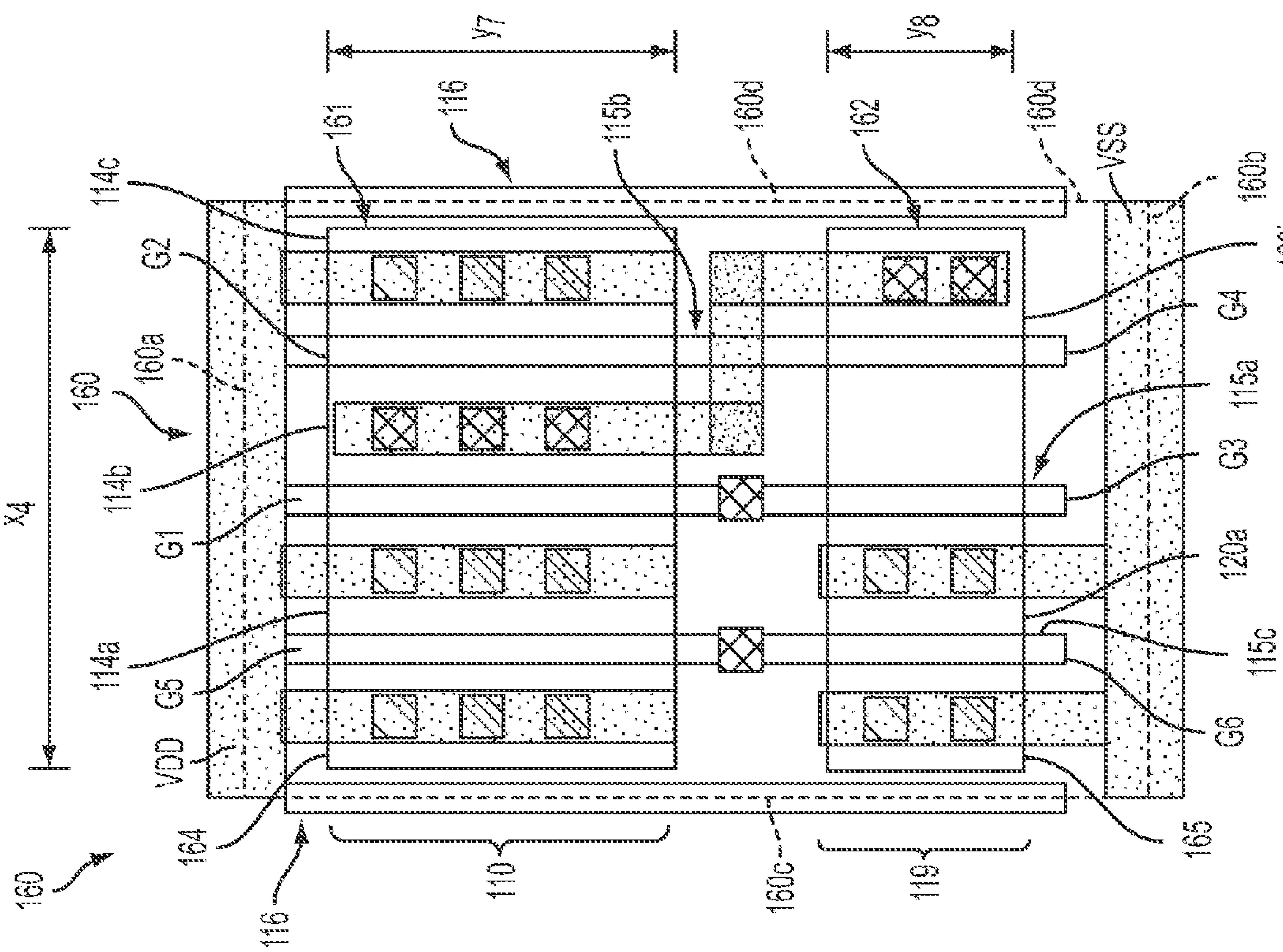
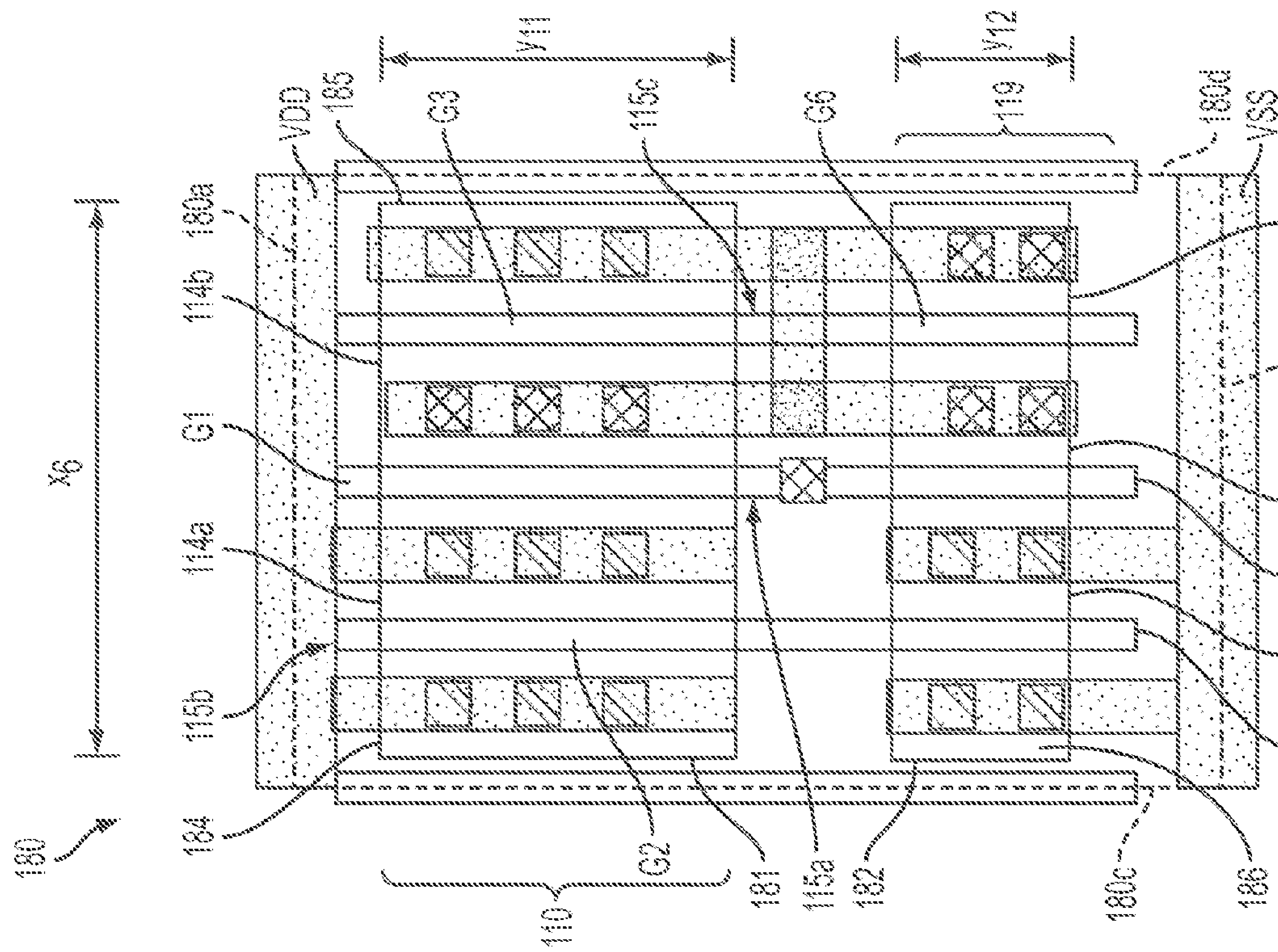
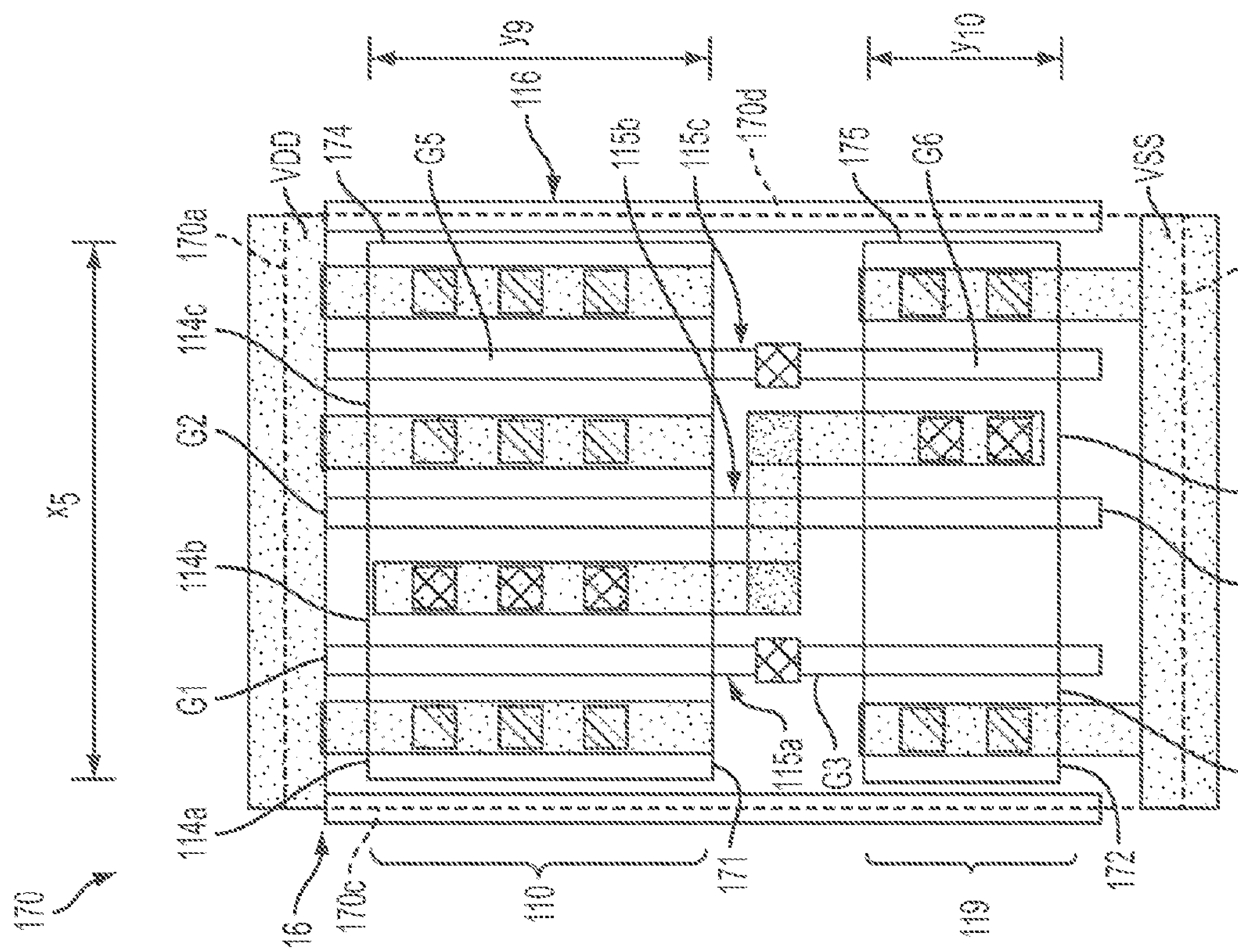

Y7
Y8
114c
161
116
115b
160d
162
160d
VSS
160b
X4
G2
160
160a
114b
G1
114a
G5
VDD
164
160
116
110
160c
119
165
120b
G4
115a
G3
120a
115c
G6

FIG. 5



180
X6
Y11
Y12
VDD
VSS
180a
180b
180c
180d
184
185
186
181
182
110
119
115a
115b
115c
114a
114b
120a
120b
120c
G1
G2
G3
G4
G5
G6


FIG. 8



170
X5
Y9
Y10
VDD
VSS
170a
170b
170c
170d
116
174
175
171
172
110
119
115a
115b
115c
114a
114b
114c
120a
120b
G1
G2
G3
G4
G5
G6


FIG. 7

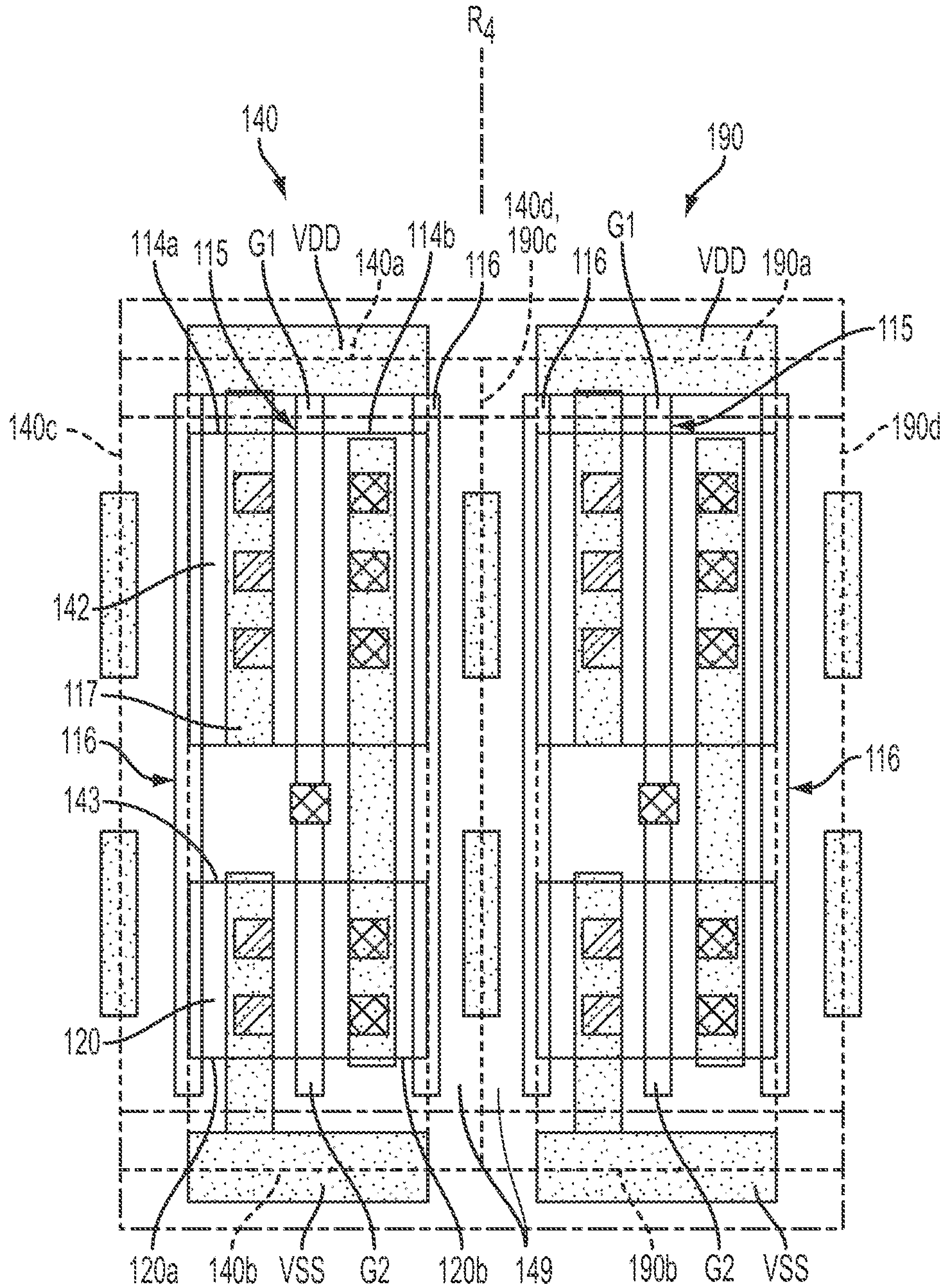

R4
140
190
114a
115
G1
VDD
140a
114b
116
140d,
190c
116
G1
VDD
190a
115
140c
190d
142
117
116
143
116
120
120a
140b
VSS
G2
120b
149
190b
G2
VSS

FIG. 9

# MASKS FORMED BASED ON INTEGRATED CIRCUIT LAYOUT DESIGN HAVING CELL THAT INCLUDES EXTENDED ACTIVE REGION

**Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue; a claim printed with strikethrough indicates that the claim was canceled, disclaimed, or held invalid by a prior post-patent action or proceeding.**

## PRIORITY CLAIM

The present application is a divisional of U.S. application Ser. No. 13/779,104, filed Feb. 27, 2013, which claims the priority of U.S. Provisional Application No. 61/747,751, filed Dec. 31, 2012, which are incorporated herein by reference in their entireties.

## BACKGROUND

In the design of integrated circuits, particularly digital circuits, standard cells having fixed functions are widely used. Standard cells are typically pre-designed and saved in cell libraries. During an integrated circuit design process, the standard cells are retrieved from the cell libraries and placed into desired locations. Routing is then performed to connect the standard cells with each other and with other circuits on the chip.

Pre-defined design rules are followed when placing the standard cells into the desired locations. For example, spacing the active regions apart from the cell boundaries, so that when neighboring cells are abutted, the active regions of neighboring cells will not adjoin each other. The precaution associated with the active regions; however, incurs area penalties. The reserved space between the active regions and the cell boundaries results in a significant increase in the areas of the standard cells. In addition, because the active regions are spaced apart from the cell boundaries, when the standard cells are placed abutting each other, the active regions will not be joined, even if some of the active regions in the neighboring cells need to be electrically coupled. The spaced apart active regions have to be electrically connected using metal lines. The performance of the resulting device is worse than if the active regions are continuous.

Layout patterns and configurations can affect yield and design performance of the standard cells.

## BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the embodiments, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGS. **1**A and **1**B are a first transistor region and a second transistor region of a single standard cell in accordance with one or more embodiments;

FIGS. **2**A through **2**C are layouts of different arrangements and types of standard cells in accordance with one or more embodiments.

FIG. **3** is a layout of a pair of standard cells having continuous active regions in accordance with one or more embodiments;

FIG. **4** is a layout of a single standard cell having an extended active region in accordance with one or more embodiments;

FIG. **5** is a layout of a single standard cell having an extended active region and dummy poly biasing in accordance with one or more embodiments;

FIG. **6** is a layout of a single standard cell having an extended active region with active region biasing and separate dummy poly biasing in accordance with one or more embodiments;

FIG. **7** is a layout of a single standard cell having an extended active region and biasing at a drain region in accordance with one or more embodiments; and

FIG. **8** is a layout of a single standard cell having an extended active region and biasing at a source region in accordance with one or more embodiments.

FIG. **9** is a layout of a pair of standard cells in accordance with one or more embodiments.

## DETAILED DESCRIPTION

The making and using of the embodiments of the disclosure are discussed in detail below. It should be appreciated, however, that the embodiments provide many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative, and do not limit the scope of the disclosure.

One or more embodiments of integrated circuit design layouts including standard cells are shown. Throughout the various views and embodiments, like reference numbers are used to designate like elements. In some embodiments, an integrated circuit is manufactured by performing one or more lithographic processes, growing processes, etching processes, or other processes based on a set of masks. In some embodiments, a set of masks is fabricated based on an integrated circuit design layout that depicts a plurality of features of the integrated circuit in various component layers.

FIGS. **1**A and **1**B are a first transistor region and a second transistor region of a single standard cell in accordance with one or more embodiments.

In FIGS. **1**A and **1**B, according to one or more embodiments, portions of a single standard cell **100** (e.g., an inverter cell) are depicted separately for facilitating the illustration of the present disclosure. The present disclosure is not limited to generating layouts of inverter cells and is applicable for generating layouts of other types of circuits including, for example, AND, OR, XOR, XNOR gates, and the like.

The standard inverter cell **100** includes upper and lower boundaries **100**a and **100**b and left and right cell boundaries **100**c and **100**d as indicated by the dashed lines shown in FIGS. **1**A and **1**B. The first transistor region (e.g., a PMOS transistor **110**) of the standard inverter cell **100** as shown in FIG. **1**A includes a p-type active region **114** (as indicated by the dimensions $X_a$ by $Y_a$) including source region **114**a (as indicated by the dimensions $X_b$ by $Y_a$) and drain region **114**b (as indicated by the dimensions $X_c$ by $Y_a$) and a first portion of an active gate strip **115** as a gate $G_1$. The source and drain regions **114**a and **114**b are on opposite sides of gate $G_1$. Further, dummy gate strips **116** are placed at left and right boundaries **100**c and **100**d. Dummy gate strips **116** do not act as a gate to any transistors. Each dummy gate strip **116** has only one-half a width inside the standard inverter cell **100** and the other half is outside the standard inverter cell **100**. Active gate strip **115** and dummy gate strips **116** are parallel to each other and equally spaced apart. Gate strip

115 and dummy gate strips 116 are formed of polysilicon or other conductive materials such as metals, metal alloys and metal silicides. Further, a VDD power supply line is connected to source region 114a by a metal connection (e.g., a metal line 117 and contact plug 118), and supplies a voltage level VDD.

The second transistor region (e.g., an NMOS transistor 119) of the standard inverter cell 100 as shown in FIG. 1B includes a second portion of gate strip 115 as a gate $G_2$ and an n-type active region (i.e., oxide-dimensioned region (OD)) 120 (as indicated by the dimensions $X_a$ by $Y_b$) including a source region 120a (as indicated by the dimensions $X_b$ by $Y_b$) and a drain region 120b (as indicated by the dimensions $X_c$ by $Y_b$). Active regions 114 and 120 are spaced apart from each other by an isolation region 122 (e.g., a shallow trench isolation (STI) region) as shown in FIG. 1B. A VSS power supply line is connected to source region 120a by a metal connection (e.g., a metal line 127 and a contact plug 128) and supplies a ground level or negative voltage level. Gate strip 115 includes a gate pitch P which is measured from an edge of gate strip 115 to a respective edge of a neighboring gate strip (e.g., dummy gate 116).

A width "w" of standard inverter cell 100 is defined by a measurement from left to right boundaries 100c and 100d. The cell width is also referred to as the cell pitch. A length of standard inverter cell 100 is defined by the measurement from upper to lower boundaries 100a and 100b. In one or more embodiments, edges of active regions 114 and 120 are spaced apart from the right and left boundaries 100c and 100d by a distance a as shown in FIG. 1A.

FIGS. 2A through 2C are layouts of different arrangements and types of standard cells in accordance with one or more embodiments.

In FIG. 2A, the single standard inverter cell 100 (on the left of reference line $R_1$) abuts another standard inverter cell 130 (on the right of reference line $R_1$). The standard cell 130 includes the same features as that of standard inverter cell 100 and therefore a detailed description thereof is omitted. The adjoining cells 100 and 130 are adjoined at their side boundaries (i.e., the right side boundary 100d of cell 100 and the left side boundary 130c of the cell 130). A dummy gate strip 116 is at the adjoining cell boundaries 100d and 130c, between the active regions 114 of the PMOS transistor regions 110 of both cells 100 and 130 and between the active regions 120 of the NMOS transistor regions 119 of both cells 100 and 130. As such, drain regions 114b and 120b of cell 100 are disposed to the left of the dummy gate strip 116, and source regions 114a and 120a of cell 130 are disposed to the right of the dummy gate strip 116.

Further, in one or more embodiments, the active regions 114 of the cells 100 and 130 are discrete (i.e., spaced apart from each other), and the active regions 120 of cells 100 and 130 are also discrete. In one or more embodiments, active regions of adjoining cells are continuous in FIG. 2B as explained below, to prevent area penalties, i.e., increased area usage, during a layout design process, and to increase gate density and the long OD region (LOD) effect. LOD effect refers the improved performance and reduced process variation as a result of a long, continuous OD region in comparison with a shorter, discrete OD region.

In FIG. 2B, standard inverter cells 100 (on the left of reference line $R_2$) and 130 (on the right of reference line $R_2$) are adjoined at side boundaries 100d and 130c. Further, the standard inverter cells 100 and 130 include a continuous active region 132 (as indicated by the dimensions $X_1$ by $Y_1$) in the PMOS transistor regions 110 and a continuous active region 134 (as indicated by dimensions $X_1$ by $Y_2$) in the NMOS transistor 119. The dummy gate strip 116 and adjacent drain region 114b of the standard inverter cell 100 and adjacent source region 114a of the standard inverter cell 130 together form a parasitic transistor (e.g., transistor P1 in the PMOS transistor region 110). The dummy gate strip 116 and adjacent drain region 120b and adjacent source region 120a together form a parasitic transistor (e.g., transistor N1 in the NMOS transistor region 119). As a result, unwanted capacitance exists between the parasitic transistors P1 and N1 because of these parasitic transistors P1 and N1 are within close proximity to each other. The resulting unwanted capacitance affects circuit performance.

FIG. 2C is another example of a standard cell 140 according to one or more embodiments. The standard cell 140 is similar to the standard cell 100; however, in standard cell 140, an extended active region 142 (as indicated by the dimensions $X_2$ by $Y_3$) is included in the PMOS transistor region 110 and an extended active region 143 (as indicated by the dimensions $X_2$ by $Y_4$) is included in the NMOS transistor region 119. The standard cell 140 is referred to as a poly on OD edge (PODE) cell. As shown, extended active regions 142 and 143 extend over an edge of dummy gate strips 116 at side boundaries 140c and 140d of the standard cell 140. When two PODE type standard cells are abutted (as depicted in FIG. 9), a blank region 149 exists between the two cells such that the cells have discrete OD regions similar to that shown in FIG. 1B. In cases with devices where the edge of the OD regions have some sinking or recess effect, the use of PODE type standard cells resolve this issue by extending the poly to the OD edge. When the OD is recessed at the edge and other layers need to be placed above the recess, the device performance is potentially degraded. Thus, in order to avoid the OD recess, a poly is used to block the OD edge. If two PODE type standard cells abut each other, the devices should be separated (as depicted in FIG. 9).

FIG. 3 is a layout of an example variation of a combination of the standard cells 100 (on the left of reference line $R_3$) and 130 (on the right of reference line $R_3$) as similarly shown in FIG. 2B. The layout of FIG. 3 includes continuous active regions 132 and 134 and is used for illustrating an operation for eliminating parasitic capacitance within the continuous active regions 132 and 134.

As shown in FIG. 3, the standard cells 100 and 130 are the same as shown in FIG. 2B, therefore a description of the elements is omitted. In one or more embodiments, a poly cut is performed (as depicted by box A) to separate upper and lower portions of the dummy gate strip 116. The upper portion (i.e., the portion above box A) is electrically connected to the VDD power supply line and the lower portion (i.e., the portion below box A) is electrically connected to the VSS power supply line. The electrical connection to VDD and VSS is made by metal connections to turn off the parasitic transistors (P1 and N1). For example, poly metal VDD connection is used to electrically couple the VDD power supply line to a metal line 117 at the source region 114a of the second standard cell 130. Also, poly metal VSS connection is used to electrically couple the VSS power supply line to a metal line 127 at the source region 120a of the second standard cell 130.) The use of the continuous active regions 132 and 134 provides the benefit of regaining gate density and the LOD effect.

FIG. 4 is a layout of a standard cell 150 having an oxide diffusion (OD) extension layers including extended active regions 152 and 154 in accordance with one or more embodiments. The standard cell 150 in FIG. 4 is a single standard cell having OD extension layers and is similar to the standard cell **100** shown in FIGS. **1**A and **1**B except in the PMOS transistor region **110** includes three additional gate strips (**115**b, **115**c, and **115**d) and an additional source region **114**c. The gate strip **115**b is between and functions as the gate electrode for the drain region **114**b and the additional source region **114**c. The gate strip **115**c can be used for connection with another device or as a dummy gate strip.

The standard cell **150** includes the first gate strip **115**a, the second gate strip **115**b, and the third gate strip **115**c are in parallel with each other. Upper and lower boundaries **150**a and **150**b are at opposite ends of the standard cell **150**, and left and right side boundaries **150**c and **150**d are parallel to the plurality of gate strips **115**a, **115**b and **115**c. The PMOS transistor **110** comprises a first portion of the first gate strip **115**a as a first gate $G_1$ and a first portion of the second gate strip **115**b as a second gate $G_2$.

The PMOS transistor **110** further includes the extended active region **152** (as indicated by dimensions $X_3$ by $Y_5$) including a first source region **114**a and a first drain region **114**b at opposite sides of the first gate $G_1$, and the first drain region **114**b and a second source region **114**c at opposite sides of the second gate $G_2$. The active region **152** is extended by two gate pitches (i.e., one gate pitch on each side). The use of an extended active region allows the metal (M**0**) poly to be positioned in the active OD region and therefore there is no degradation regarding the device size.

Standard cell **150** further includes a NMOS transistor **119** including a second portion of the first gate strip **115**a as a third gate $G_3$ and a second portion of the second gate strip **115**b as a fourth gate $G_4$, the second extended active region **154** (as indicated by dimensions $X_3$ by $Y_6$) includes a third source region **120**a opposite first source region **114**a of the PMOS transistor **110** and adjacent to third gate $G_3$, and a second drain region **120**b opposite second source region **114**c and adjacent to fourth gate $G_4$.

First and second source regions **114**a and **114**c of PMOS transistor **110** are connected with VDD power supply line by metal connections (e.g., metal line **117** and contact plugs **118**). Further, third source region **120**a of NMOS transistor **119** is connected with VSS power supply line by a metal connection (e.g., metal line **127** and contact plug **128**). In one or more embodiments, first gate strip **115**a is an active gate strip and second gate strip **116** is a dummy gate strip. Further, according to one or more embodiments, gate strip **115**d is a non-operative floating poly and gate strip **115**c is an active gate strip for other devices (not shown).

In one or more embodiments, first drain region **114**b of PMOS transistor **110** is electrically connected with second drain region **120**b of NMOS transistor **119** by a metal connection.

FIG. **5** is a layout of a single standard cell **160** having extended active regions and dummy poly biasing to prevent parasitic capacitance in accordance with one or more embodiments. The layout of standard cell **160** is similar to the layout of standard cell **150** shown in FIG. **5**. Compared with standard cell **150**, PMOS transistor **110** and NMOS transistor **119** include extended active region **161** (as indicated by dimensions $X_4$ and $Y_7$) and extended active region **162** (as indicated by dimensions $X_4$ and $Y_8$) which are extended by one gate pitch at one side (e.g., a left side boundary **160**c) of standard cell **160** instead of both sides. In the example depicted in FIG. **5**, the active regions **161** and **162** are not extended beyond the third source region **114**c of PMOS transistor **110** of standard cell **160** and second drain region **120**b of NMOS transistor **119**. Therefore, third source region **114**c of PMOS transistor **110** of standard cell **160** and second drain region **120**b of NMOS transistor **119** align near the side cell boundary **160**d.

Standard cell **160** further includes a third gate strip **115**c parallel to first gate strip **115**a and includes an upper portion as a fifth gate $G_5$ and a lower portion as a sixth gate $G_6$. First and second dummy source regions **164** and **165** corresponding to PMOS transistor **110** and NMOS transistor **119** are defined within the extension of the active regions **161** and **162**. First and second dummy source regions **164** and **165** are disposed to the left of the third gate strip **115**c and adjacent to a side boundary (e.g., the left side boundary **160**c). VDD power supply line is electrically connected to first dummy source region **164** and VSS power supply line is electrically connected to second dummy source region **165** by metal connections. Use of first and second dummy source regions **164** and **165** at boundary **160**c prevents the generation of parasitic capacitance, and protects the source region **114**a and the LOD effect as a result of the extended active regions **161** and **162**.

In one or more embodiments, third gate strip **115**c is a dummy gate strip and is biased at VDD power supply line or the VSS power supply line.

In some embodiments, some or all layouts of standard cells for NOT, AND, OR, XOR, or XNOR gates, and/or the like are arranged in a manner that the source regions are positioned adjacent to the cell side boundaries, such as side boundaries **160**c and **160**d of cell **160**. Accordingly, generation of parasitic transistors at the side boundaries **160**c and **160**d when abutting another cell is prevented.

FIG. **6** is a layout of single standard cell **160'** with active region biasing and separate dummy poly biasing in accordance with one or more embodiments. In FIG. **6**, compared with the standard cell **160** in FIG. **5**, a poly cut is performed (as depicted box "A") at fifth gate $G_5$ and sixth gate $G_6$ and fifth gate $G_5$ is electrically connected with VDD power supply line by a metal connection, and sixth gate $G_6$ is electrically connected with VSS power supply line by a metal connection. Since the fifth gate $G_5$ and the sixth gate $G_6$ are cut, and the fifth gate $G_5$ which corresponds to a parasitic transistor, is connected to power, the connection of fifth gate $G_5$ to power disables the fifth gate $G_5$ Further, sixth gate $G_6$ is connected to ground and is not used as a transistor.

FIG. **7** is a layout of a single standard cell **170** having extended active region **171** (as indicated by dimensions $X_5$ by $Y_9$) and extended active region **172** (as indicated by dimensions $X_5$ by $Y_{10}$) in accordance with one or more embodiments. Active regions **171** and **172** are extended by one gate pitch at a right side of standard cell **170**. Some of the elements within standard cell **170** are the same as standard cell **160** therefore a description thereof is omitted.

In FIG. **7**, third gate strip **115**c is parallel to and adjacent to second gate strip **115**b and includes the upper portion as the fifth gate $G_5$ and the lower portion as the sixth gate $G_6$. First and second dummy source regions **174** and **175** are defined within the corresponding active regions **171** and **172** and are disposed to the right of the gate strip **115**c along a side boundary **170**d of standard cell **170**. First dummy source region **174** and second source region **114**c are at opposite sides of fifth gate $G_5$, and second dummy source region **175** and second drain region **120**b are at opposite sides of sixth gate $G_6$. VDD power supply line is electrically connected to first dummy source region **174** and VSS power supply line is electrically connected to second dummy source region **175**. As shown in FIG. **7**, in one or more embodiments, source region **175** is electrically coupled to VSS (i.e., also referred to as biasing performed at a drain side of NMOS transistor **119**). Third gate strip **115**c is connected with VSS power supply line to effectively disable the parasitic transistor formed by the drain region **120**b, the source region **175**, and the gate $G_6$.

FIG. **8** is a layout of a single standard cell **180** having an extended active region **181** (as indicated by dimensions $X_6$ by $Y_{11}$) and an extended active region **182** (as indicated by dimensions $X_6$ by $Y_{12}$) and performing biasing at a source region in accordance with one or more embodiments.

In FIG. **8**, standard cell **180** is an inverter, for example, and includes first, second and third gate strips **115**a, **115**b and **115**c parallel with each other. Upper and lower boundaries **180**a and **180**b on opposite ends of standard cell **180** and left and right side boundaries **180**c and **180**d parallel to first, second and third gates **115**a, **115**b and **115**c. A PMOS transistor **110** includes a first portion of first gate strip **115**a as a first gate $G_1$, first extended active region **181** including a first source region **114**a and a first drain region **114**b at opposite sides of first gate $G_1$, a first portion of second gate strip **115**b as a second gate $G_2$, a first dummy source region **184** and first source region **114**a disposed opposite second gate $G_2$, and a first portion of third gate strip **115**c as a third gate $G_3$ and a second dummy source region **185** and first drain region **114**b disposed opposite third gate $G_3$.

Standard cell **180** further includes NMOS transistor **119** including a second portion of first gate strip **115**a as a fourth gate $G_4$, second extended active region **182** including a second source region **120**a opposite first source region **114**a and second source region **120**a and second drain region **120**b disposed at opposite sides of the fourth gate $G_4$. A second portion of second gate strip **115**b as a fifth gate $G_5$, and a third dummy source region **186** and second source region **120**a are disposed at opposite sides of the fifth gate $G_5$, and a second portion of third gate strip **120**c as a sixth gate $G_6$, the second drain region **120**b and a third drain region **120**c are disposed at opposite sides of sixth gate $G_6$. First dummy source region **184**, second dummy source region **185** and first source region **114**a are connected with VDD power supply line by metal connections, and third dummy source region **186**, and second source region **120**a are connected with the VSS power supply line by metal connections. As shown, first, second and third source regions **184**, **185** and **186** are disposed along the side boundaries **180**c and **180**d of standard cell **180**. Biasing is performed on the source side of the standard cell **180**. The first, second and third drain regions **114**b, **120**b and **120**c are connected together and act as an output of the inverter.

FIG. **9** illustrates a pair of PODE type standard cells according to one or more embodiments. As shown in FIG. **9**, two PODE type standard cells **140** (on the left of reference line $R_4$) and **190** (on the right of reference line $R_4$) are provided. Details regarding the standard cell **140** are discussed above with regards to FIG. **2**C. Standard cell **190** has cell boundaries **190**a, **190**b, **190**c and **190**d and further comprises the same components as that of standard cell **140**, therefore a detailed description of standard cell **190** is omitted to avoid unnecessary repetition. As mentioned above, when PODE type standard cells **140** and **190** are abutted as shown in FIG. **9**, blank region **149** exists between the two cells such that the cells have discrete OD regions similar to that shown in FIG. **2**A.

One or more embodiments include a set of masks corresponding to an integrated circuit layout. The integrated circuit layout comprises a first cell comprising a first transistor region and a second transistor region, and a second cell comprising a third transistor region and a fourth transistor region. The first cell and the second cell adjoin each other at side cell boundaries thereof, the first transistor region and the third transistor region are formed in a first continuous active region, and the second transistor region and the fourth transistor region are formed in a second continuous active region. The set of masks is formed based on the integrated circuit layout.

One or more embodiments include a set of masks corresponding to an integrated circuit layout. The integrated circuit layout comprises a first cell comprising a first active region and a first side boundary, and a second cell comprising a second active region and a second side boundary along the first side boundary. The integrated circuit layout further comprises a first gate strip in the first cell parallel to the first side boundary and overlying the first active region, a second gate strip in the second cell parallel to the second side boundary and overlying the second active region, and a dummy gate strip parallel to and between the first gate strip and the second gate strip, wherein the dummy gate strip overlies at least one of the first active region or the second active region. The set of masks is formed based on the integrated circuit layout.

One or more embodiments include a set of masks corresponding to an integrated circuit layout. The integrated circuit layout comprises a first cell comprising a first active region and a first side boundary, and a second cell comprising a second active region and a second side boundary along the first side boundary. The integrated circuit layout further comprises a first gate strip in the first cell parallel to the first side boundary and overlying the first active region, a second gate strip in the second cell parallel to the second side boundary and overlying the second active region, a blank region abutting the first active region and the second active region, a first dummy gate strip in the first cell between the first gate strip and the first side boundary, and overlying the first active region and the blank region, and a second dummy gate strip in the second cell between the second gate strip and the second side boundary, and overlying the second active region and the blank region. The set of masks is formed based on the integrated circuit layout.

Although the embodiments and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the embodiments as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps. In addition, each claim constitutes a separate embodiment, and the combination of various claims and embodiments are within the scope of the disclosure.

What is claimed is:

**1**. A set of masks corresponding to an integrated circuit layout, the integrated circuit layout comprising:

a first cell comprising a first transistor region and a second transistor region;

a second cell comprising a third transistor region and a fourth transistor region, wherein

the first cell and the second cell adjoin each other at side cell boundaries thereof,

the first transistor region and the third transistor region are formed in a first continuous active region, and

the second transistor region and the fourth transistor region are formed in a second continuous active region; and

a middle gate strip *electrically continuously* extending from the first transistor region to the second transistor region, along a line at which the first cell adjoins the second cell,

wherein the set of masks is formed based on the integrated circuit layout.

**2**. The set of masks of claim **1**, wherein the first cell further comprises:

a first gate strip; and

upper and lower cell boundaries on opposite ends of the first cell,

wherein

the side cell boundaries are parallel to the first gate strip;

the first transistor region comprises a first PMOS transistor comprising a first portion of the first gate strip as a first gate, a first source region and a first drain region adjacent to the first gate, and

the second transistor region comprises a first NMOS transistor comprising a second portion of the first gate strip as a second gate, and a second source region and a second drain region adjacent to the second gate.

**3**. The set of masks of claim **2**, wherein the second cell further comprises:

a second gate strip parallel to the first gate strip; and

upper and lower cell boundaries on opposite sides of the second cell,

wherein

the third transistor region comprises a second PMOS transistor comprising a first portion of the second gate strip as a third gate, and a third source region and a third drain region adjacent to the third gate, and

the fourth transistor region comprises a second NMOS transistor comprising a second portion of the second gate strip as a fourth gate, and a fourth source region and a fourth drain region adjacent to the fourth gate.

**4**. The set of masks of claim **3**, wherein the first gate strip [and] *is an active gate strip,* the second gate [strips are] *strip is an* active gate [strips] *strip* and the middle gate strip is a dummy gate strip.

**5**. The set of masks of claim **3**, wherein the integrated circuit layout further comprises:

a first power supply line extending across the upper cell boundaries of the first cell and the second cell; and

a second power supply line extending across the lower cell boundaries of the first cell and the second cell,

wherein the first power supply line is electrically coupled to the first source region and the third source region and the second power supply line is electrically coupled to the second source region and the fourth source region.

[**6**. The set of masks of claim **5**, wherein:

an upper portion of the middle gate strip, the first drain region, and the third source region form a parasitic transistor;

a lower portion of the middle gate strip, the second drain region, and the fourth source region form a parasitic transistor;

the upper portion of the middle gate strip is electrically coupled to the first power supply line; and

the lower portion of the middle gate strip is electrically coupled to the second power supply line.]

**7**. The set of masks of claim **1**, wherein:

the first cell further comprises a first dummy gate strip along the side cell boundary opposite to the middle gate strip and the second cell further comprises a second dummy gate strip along the side cell boundary opposite to the middle gate strip.

**8**. The set of masks of claim **1**, wherein:

the first continuous active region extends to the side cell boundaries of the first cell, and the second continuous active region extends to the side cell boundaries of the second cell.

**9**. A set of masks corresponding to an integrated circuit layout, the integrated circuit layout comprising:

a first cell comprising a first active region and a first side boundary;

a second cell comprising a second active region and a second side boundary along the first side boundary;

a first gate strip in the first cell parallel to the first side boundary and overlying the first active region;

a second gate strip in the second cell parallel to the second side boundary and overlying the second active region; and

a dummy gate strip parallel to and between the first gate strip and the second gate strip,

wherein the dummy gate strip overlies [one of] the first active region [or] *and* the second active region*, and the dummy gate strip is electrically continuous*,

wherein the set of masks is formed based on the integrated circuit layout.

**10**. The set of masks of claim **9**, wherein:

the first cell further comprises a third active region,

the second cell further comprises a fourth active region[,

when the dummy gate strip overlies the first active region, the dummy gate strip also overlies the third active region, and

when the dummy gate strip overlies the second active region, the dummy gate strip also overlies the fourth active region].

**11**. The set of masks of claim **9**, wherein the integrated circuit layout further comprises a first power supply line along a direction perpendicular to the dummy gate strip, wherein the first active region comprises a first source region electrically coupled to the first power supply line.

**12**. The set of masks of claim **11**, wherein the integrated circuit layout further comprises a second power supply line along the direction perpendicular to the dummy gate strip, wherein the second active region comprises a second source region electrically coupled to the second power supply line.

**13**. The set of masks of claim **12**, wherein the first power supply line is electrically coupled to the second power supply line.

**14**. The set of masks of claim **12**, wherein the first power supply line is [electrically] separate from the second power supply line.

**15**. A set of masks corresponding to an integrated circuit layout, the integrated circuit layout comprising:

a first cell comprising a first active region and a first side boundary;

a second cell comprising a second active region and a second side boundary along the first side boundary;

a first gate strip in the first cell parallel to the first side boundary and overlying the first active region;

a second gate strip in the second cell parallel to the second side boundary and overlying the second active region;

a blank region abutting the first active region and the second active region;

a first dummy gate strip [in the first cell] between the first gate strip and the first side boundary, and overlying the first active region and the blank region; and

a second dummy gate strip [in the second cell between the second gate strip and the second side boundary, and] overlying the second active region and the blank region*, wherein the second dummy gate strip is electrically continuous with the first dummy gate strip*,

wherein the set of masks is formed based on the integrated circuit layout.

**16**. The set of masks of claim **15**, wherein the first dummy gate strip overlies a border between the first active region and the blank region.

**17**. The set of masks of claim **15**, wherein:

the first cell further comprises a third active region,

the second cell further comprises a fourth active region[,

the first dummy gate strip overlies the third active region, and

the second dummy gate strip overlies the fourth active region].

**18**. The set of masks of claim **17**, wherein:

the first dummy gate strip overlies a first edge of the blank region[, and

the first active region and the third active region abut the first edge of the blank region].

**19**. The set of masks of claim **18**, wherein:

the second dummy gate strip overlies a second edge of the blank region[, and

the second active region and the fourth active region abut the second edge of the blank region].

**20**. The set of masks of claim **15**, wherein the second side boundary is along the first side boundary in the blank region.

*21. A device, the device comprising:*

*a first cell comprising a first transistor region and a second transistor region;*

*a second cell comprising a third transistor region and a fourth transistor region,*

*wherein*

*the first cell and the second cell adjoin each other at side cell boundaries thereof,*

*the first transistor region and the third transistor region are formed in a first continuous active region, and*

*the second transistor region and the fourth transistor region are formed in a second continuous active region; and*

*a middle gate strip electrically continuously extending from the first transistor region to the second transistor region, along a line at which the first cell adjoins the second cell.*

*22. The device of claim 21, wherein the first cell further comprises:*

*a first gate strip; and*

*upper and lower cell boundaries on opposite ends of the first cell,*

*wherein*

*the side cell boundaries are parallel to the first gate strip;*

*the first transistor region comprises a first PMOS transistor comprising a first portion of the first gate strip as a first gate, a first source region and a first drain region adjacent to the first gate, and*

*the second transistor region comprises a first NMOS transistor comprising a second portion of the first gate strip as a second gate, and a second source region and a second drain region adjacent to the second gate.*

*23. The device of claim 22, wherein the second cell further comprises:*

*a second gate strip parallel to the first gate strip; and*

*upper and lower cell boundaries on opposite sides of the second cell,*

*wherein*

*the third transistor region comprises a second PMOS transistor comprising a first portion of the second gate strip as a third gate, and a third source region and a third drain region adjacent to the third gate, and*

*the fourth transistor region comprises a second NMOS transistor comprising a second portion of the second gate strip as a fourth gate, and a fourth source region and a fourth drain region adjacent to the fourth gate.*

*24. The device of claim 23, wherein the first gate strip and the second gate strip are active gate strips and the middle gate strip is a dummy gate strip.*

*25. The device of claim 23, wherein the device further comprises:*

*a first power supply line extending across the upper cell boundaries of the first cell and the second cell; and*

*a second power supply line extending across the lower cell boundaries of the first cell and the second cell,*

*wherein the first power supply line is electrically coupled to the first source region and the third source region and the second power supply line is electrically coupled to the second source region and the fourth source region.*

*26. The device of claim 21, wherein:*

*the first cell further comprises a first dummy gate strip along the side cell boundary opposite to the middle gate strip and the second cell further comprises a second dummy gate strip along the side cell boundary opposite to the middle gate strip.*

*27. The device of claim 21, wherein:*

*the first continuous active region extends to the side cell boundaries of the first cell, and*

*the second continuous active region extends to the side cell boundaries of the second cell.*

*28. A device, the device comprising:*

*a first cell comprising a first active region and a first side boundary;*

*a second cell comprising a second active region and a second side boundary along the first side boundary;*

*a first gate strip in the first cell parallel to the first side boundary and overlying the first active region;*

*a second gate strip in the second cell parallel to the second side boundary and overlying the second active region; and*

*a dummy gate strip parallel to and between the first gate strip and the second gate strip,*

*wherein the dummy gate strip is electrically continuous and overlies the first active region and the second active region.*

*29. The device of claim 28, wherein:*

*the first cell further comprises a third active region,*

*the second cell further comprises a fourth active region.*

*30. The device of claim 28, wherein the device further comprises a first power supply line along a direction perpendicular to the dummy gate strip, wherein the first active region comprises a first source region electrically coupled to the first power supply line.*

*31. The device of claim 30, wherein the device further comprises a second power supply line along the direction perpendicular to the dummy gate strip, wherein the second active region comprises a second source region electrically coupled to the second power supply line.*

*32. The device of claim 28, wherein the first power supply line is electrically coupled to the second power supply line.*

*33. The device of claim 28, wherein the first power supply line is separate from the second power supply line.*

*34. A device, the device comprising:*

*a first cell comprising a first active region and a first side boundary;*

*a second cell comprising a second active region and a second side boundary along the first side boundary;*

*a first gate strip in the first cell parallel to the first side boundary and overlying the first active region;*

*a second gate strip in the second cell parallel to the second side boundary and overlying the second active region;*

*a blank region abutting the first active region and the second active region;*

*a first dummy gate strip between the first gate strip and the first side boundary, and overlying the first active region and the blank region; and*

*a second dummy gate strip overlying the second active region and the blank region, wherein the second dummy gate strip is electrically continuous with the first dummy gate strip.*

*35. The device of claim 34, wherein the first dummy gate strip overlies a border between the first active region and the blank region.*

*36. The device of claim 34, wherein:*

*the first cell further comprises a third active region,*

*the second cell further comprises a fourth active region.*

*37. The device of claim 36, wherein:*

*the first dummy gate strip overlies a first edge of the blank region, and*

*the first active region and the third active region abut the first edge of the blank region.*

*38. The device of claim 37, wherein:*

*the second dummy gate strip overlies a second edge of the blank region, and*

*the second active region and the fourth active region abut the second edge of the blank region.*

*39. The device of claim 34, wherein the second side boundary is along the first side boundary in the blank region.*

* * * * *