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(54) **ORGANIC LIGHT-EMITTING DISPLAY DEVICE AND MANUFACTURING METHOD OF THE SAME**

(71) Applicant: **SAMSUNG DISPLAY CO., LTD.**, Yongin-si (KR)

(72) Inventor: **Hyun-Tae Kim**, Yongin (KR)

(73) Assignee: **SAMSUNG DISPLAY CO., LTD.**, Yongin (KR)

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H01L 21/02 (2006.01)
H01L 27/32 (2006.01)

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USPC 345/39, 44, 46, 82, 87, 92, 212
See application file for complete search history.

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Primary Examiner — Henry N Tran

(74) *Attorney, Agent, or Firm* — F. Chau & Associates, LLC

(57) **ABSTRACT**

An organic light-emitting display device and a related manufacturing method of the organic light-emitting display device are disclosed. In one aspect, the organic light-emitting display device includes a plurality of pixels which are formed between a plurality of scan lines and a plurality of data signal lines. It also includes a plurality of initialization voltage lines which are formed in parallel with the plurality of scan lines and are shared between two adjacent pixels of a row to supply an initialization voltage to the two adjacent pixels. It also includes a driving voltage line which supplies a driving voltage to the plurality of pixels and includes a first voltage line formed in a vertical direction and a second voltage line that is connected between the two adjacent pixels and formed in a horizontal direction.

42 Claims, 13 Drawing Sheets

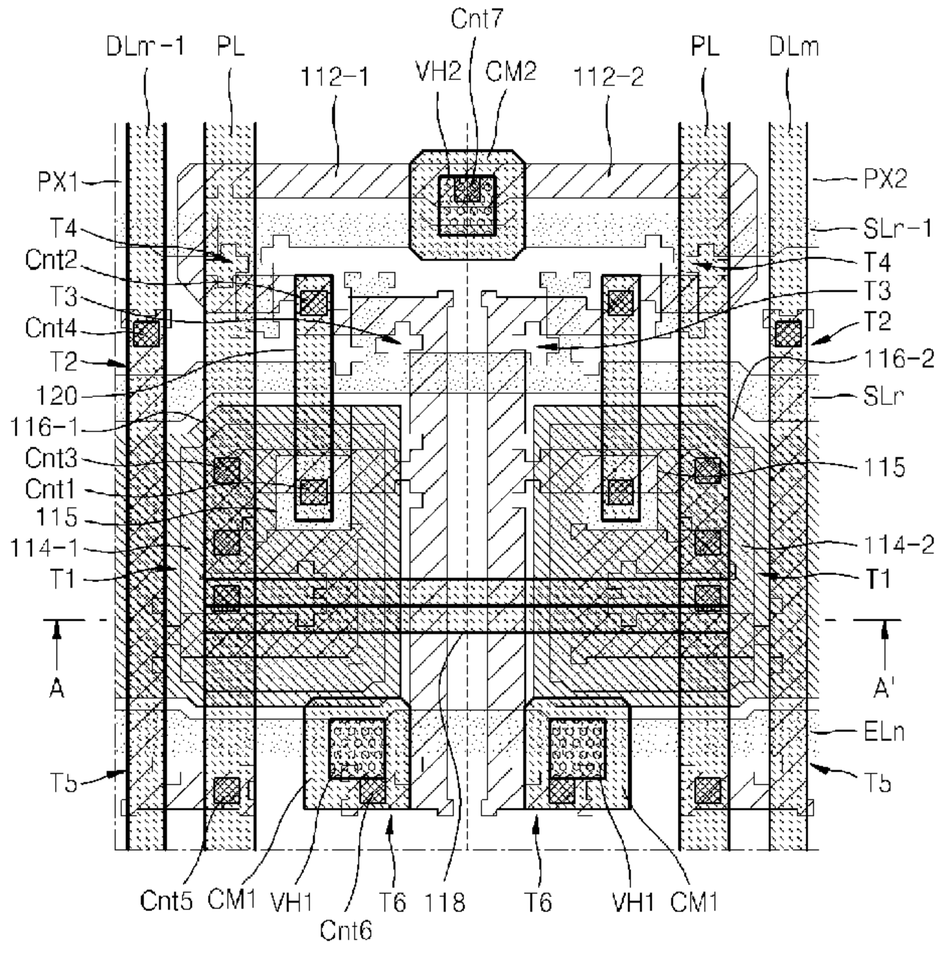

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FIG. 1

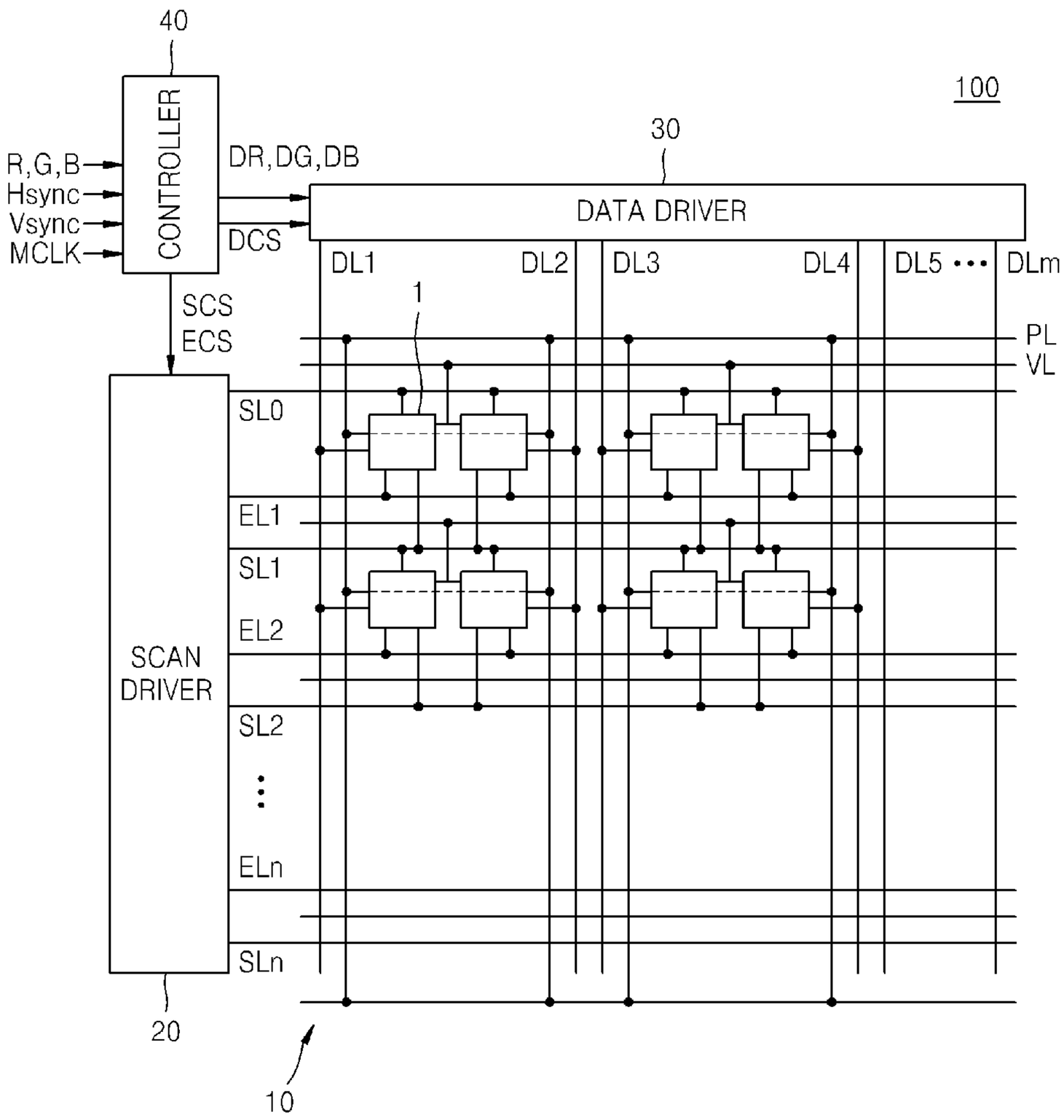
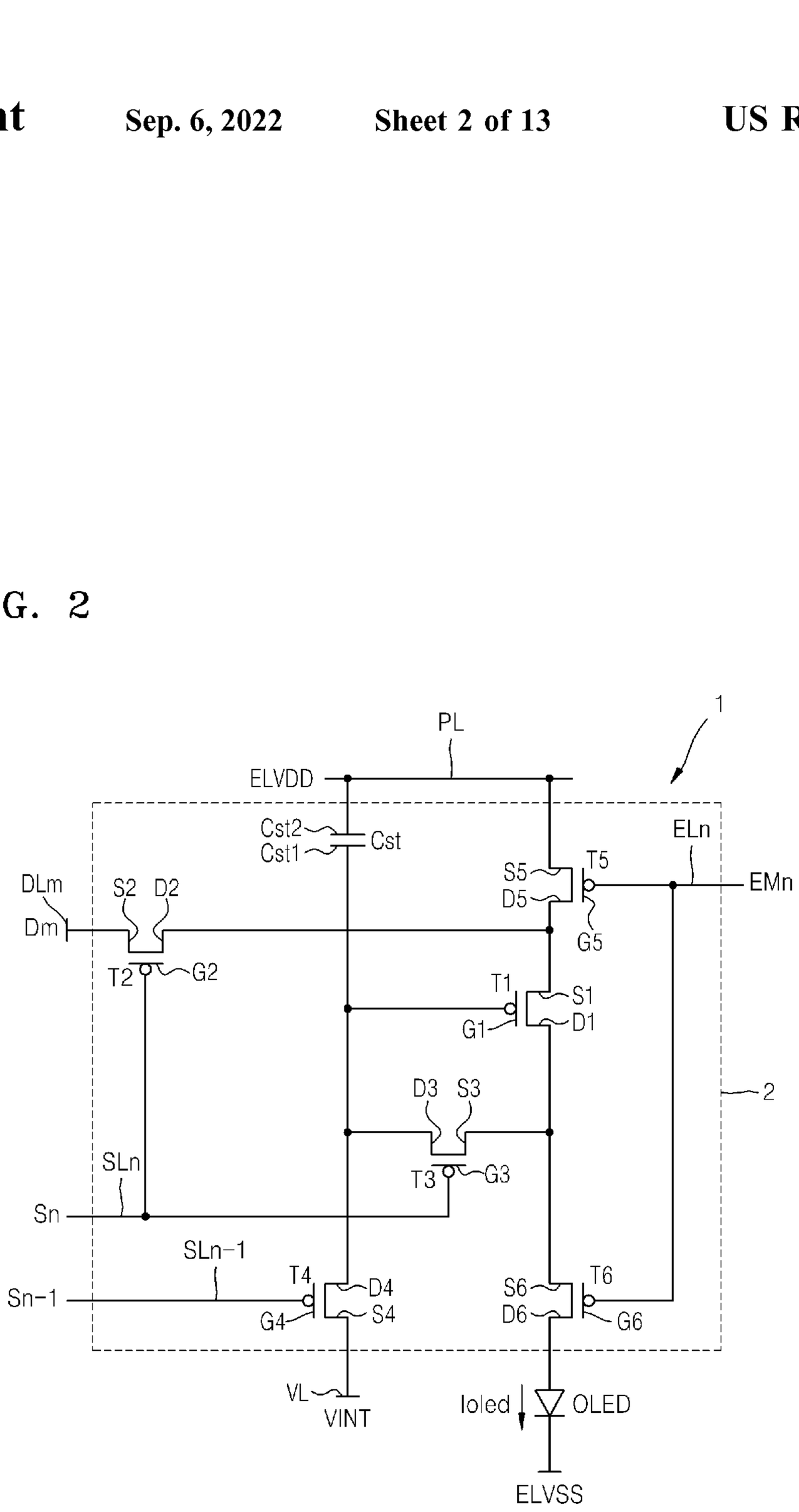

40
100
30
CONTROLLER
R,G,B
Hsync
Vsync
MCLK
DR,DG,DB
DCS
DATA DRIVER
DL1
DL2
DL3
DL4
DL5 • • •
DLm
1
SCS
ECS
PL
VL
SL0
EL1
SL1
EL2
SCAN DRIVER
SL2
ELn
SLn
20
10

FIG. 2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PL
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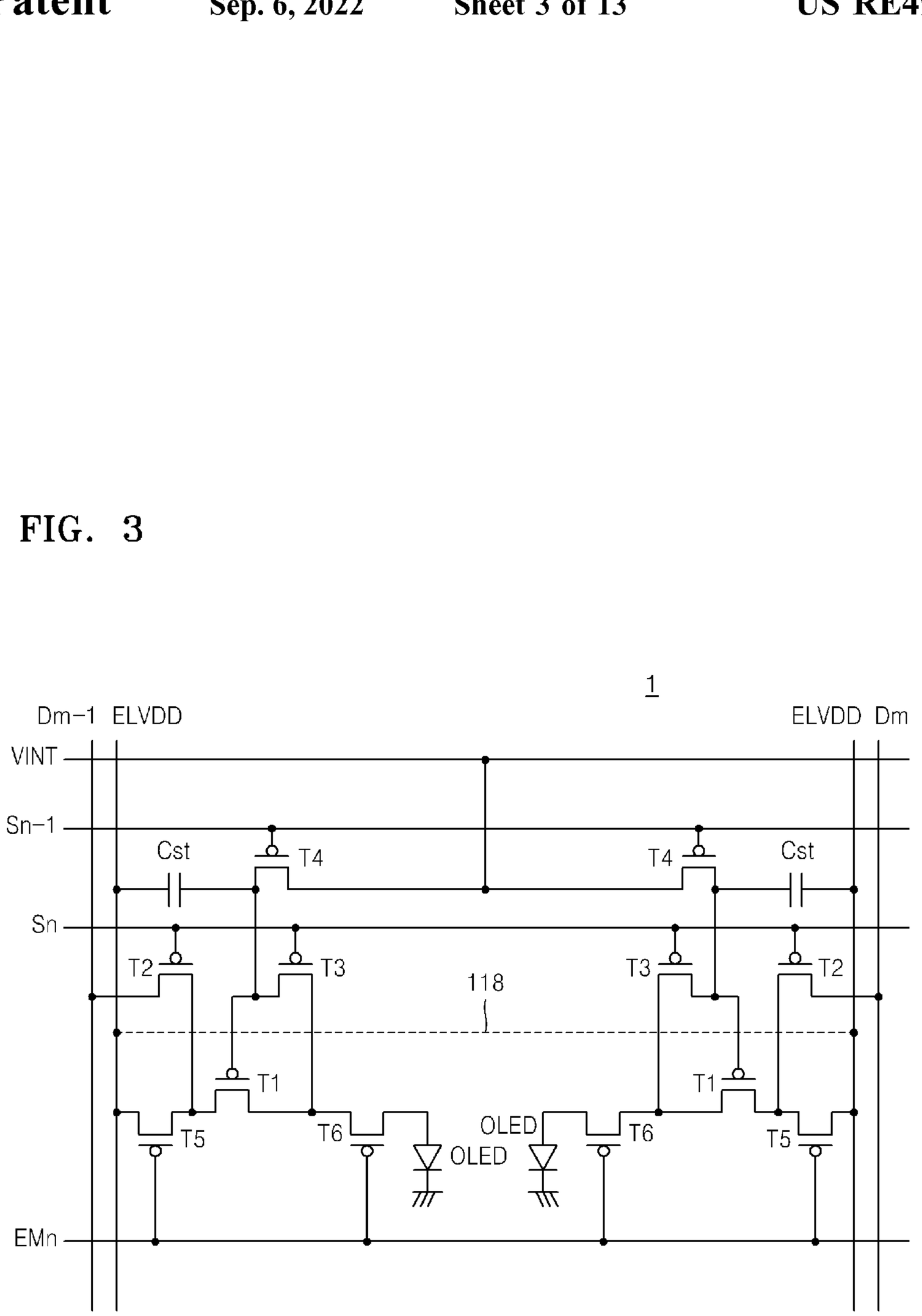
Cst2
Cst1
Cst
ELn
T5
S5
D5
G5
EMn
DLm
Dm
S2
D2
T2
G2
T1
S1
D1
G1
D3
S3
T3
G3
2
SLn
Sn
SLn-1
Sn-1
T4
D4
S4
G4
S6
D6
T6
G6
VL
VINT
Ioled
OLED
ELVSS

FIG. 3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ELVDD
Dm
VINT
Sn-1
Sn
EMn
Cst
T4
T4
Cst
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T3
T3
T2
118
T1
T1
T5
T6
OLED
OLED
T6
T5

FIG. 4

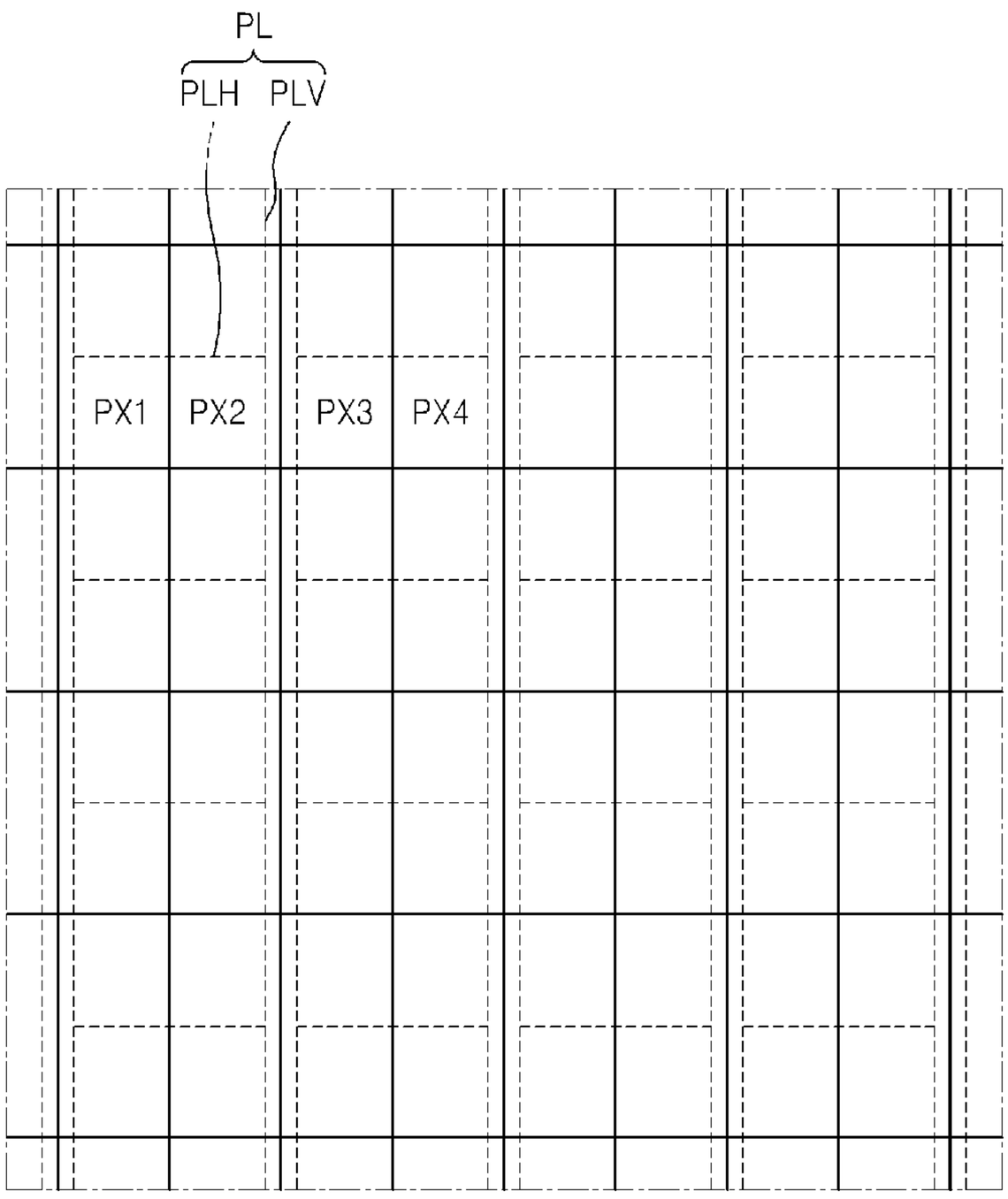


FIG. 5

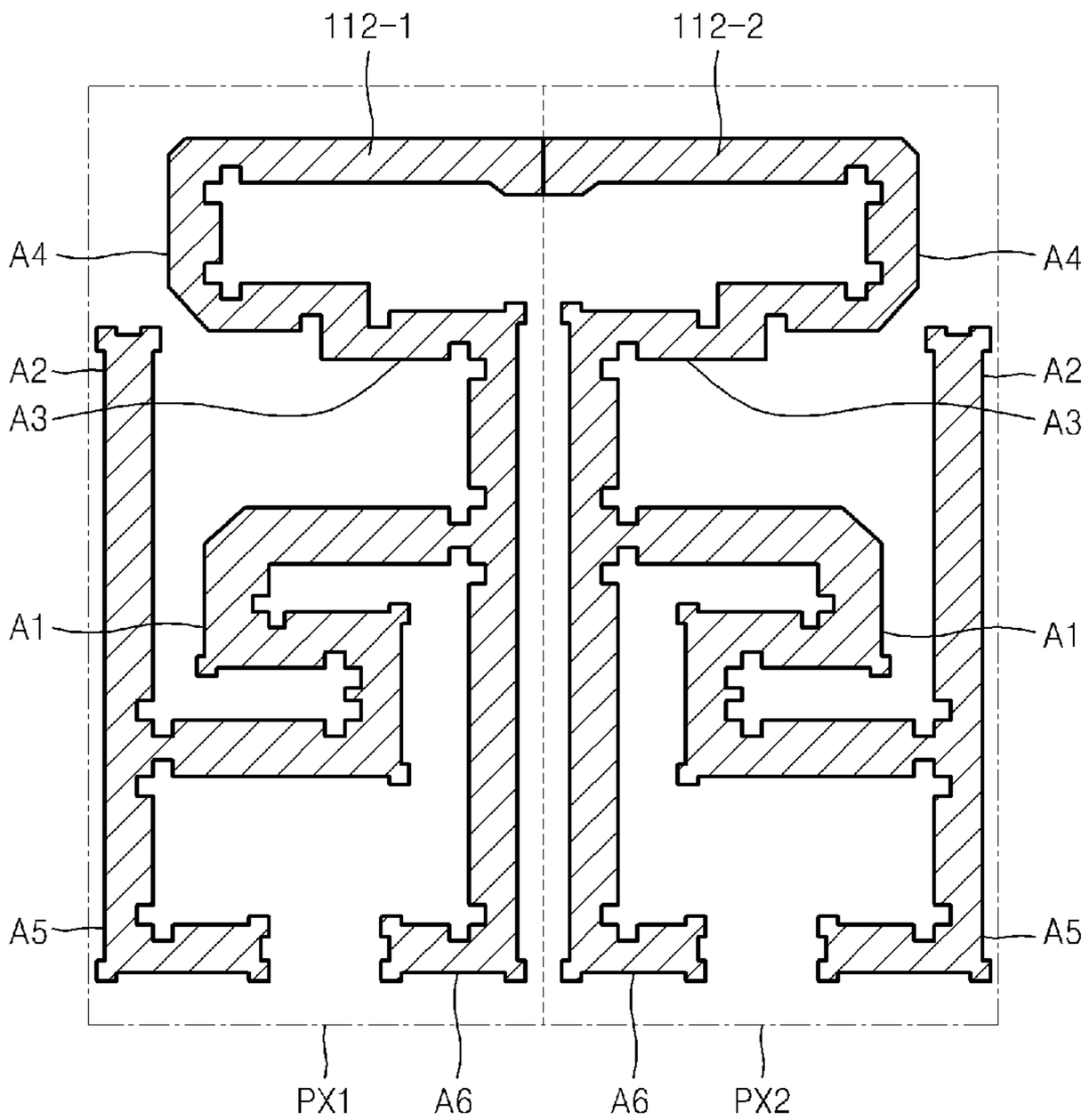
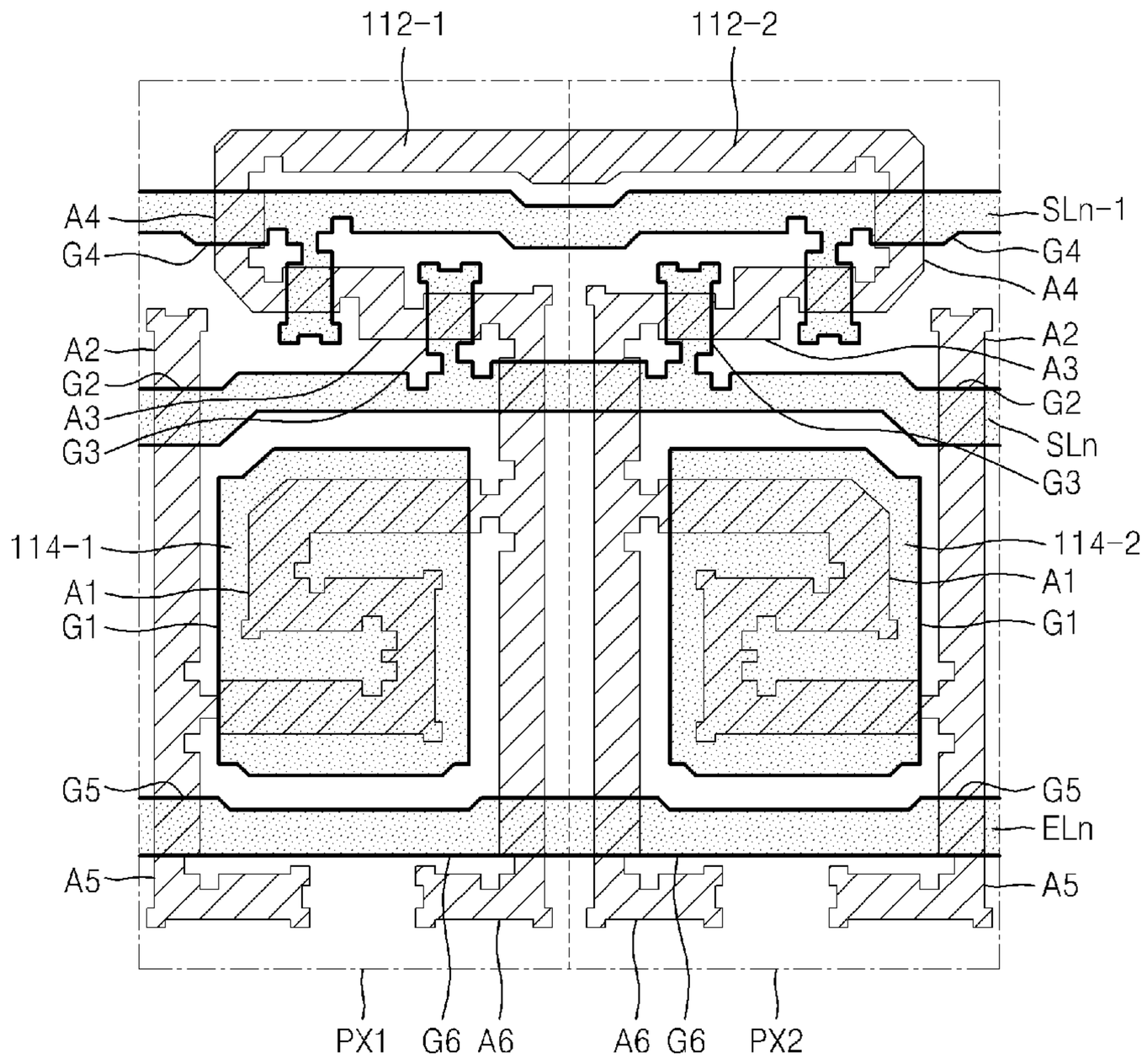


FIG. 6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112-2
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G4
SLn-1
G4
A4
A2
G2
A3
G3
A2
A3
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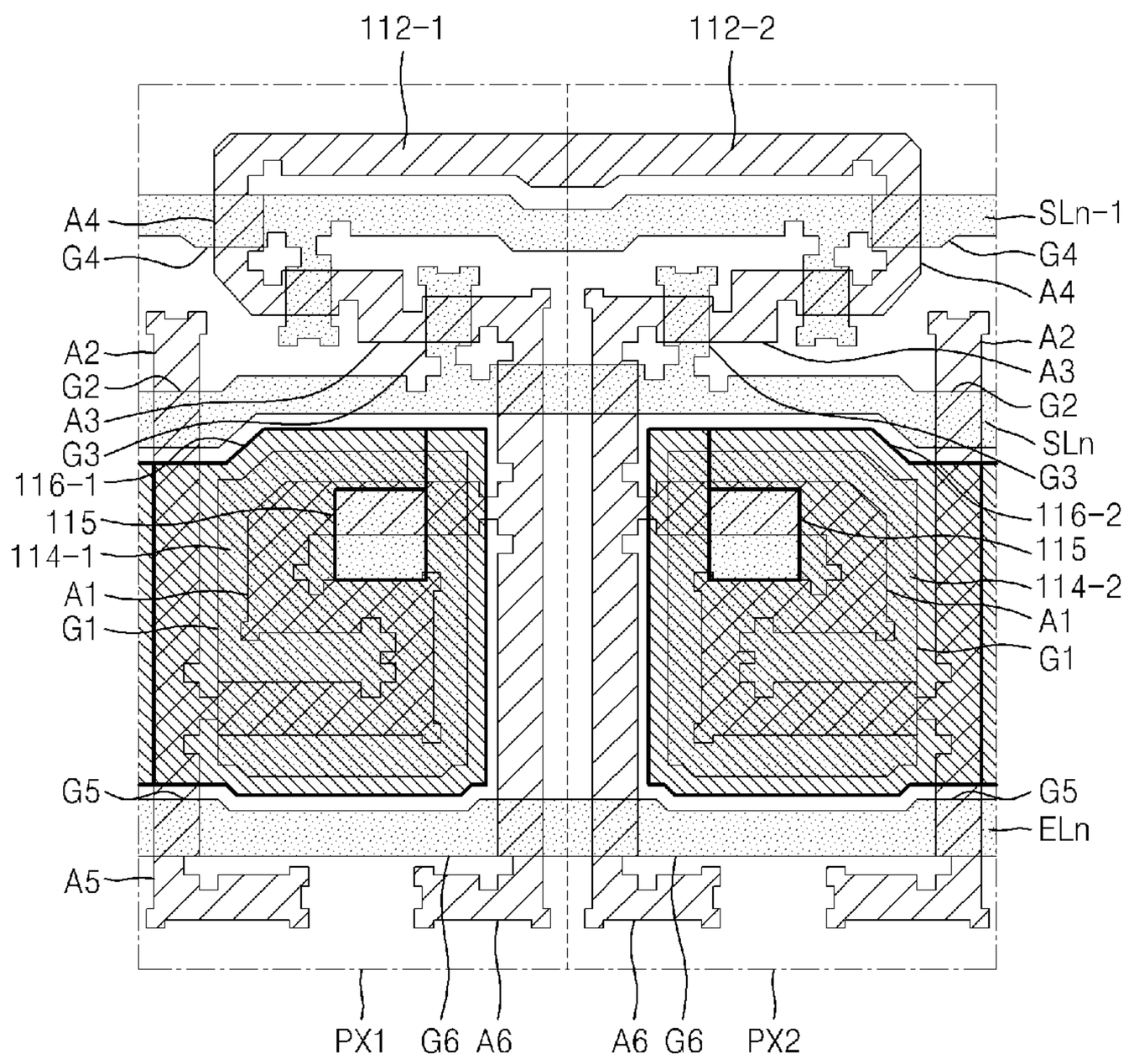
SLn
G3
114-1
A1
G1
114-2
A1
G1
G5
G5
ELn
A5
A5
PX1
G6
A6
A6
G6
PX2

FIG. 7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112-2
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G4
SLn-1
G4
A4
A2
G2
A3
G3
116-1
115
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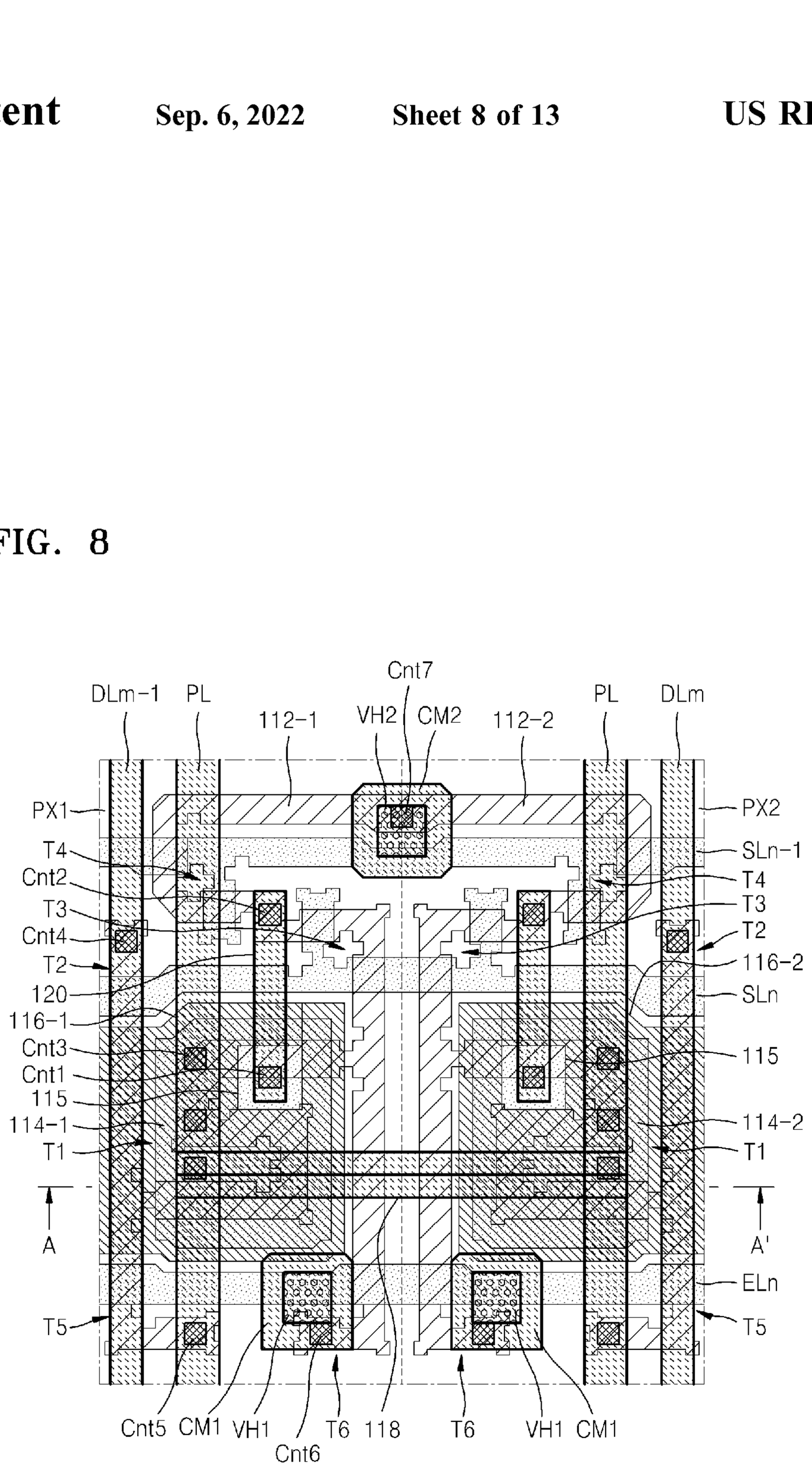
A1
G1
A2
A3
G2
SLn
G3
116-2
115
114-2
A1
G1
G5
G5
ELn
A5
PX1
G6
A6
A6
G6
PX2

FIG. 8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DLm-1
PL
112-1
VH2
CM2
112-2
PL
DLm
PX1
PX2
T4
SLn-1
Cnt2
T4
T3
T3
Cnt4
T2
T2
116-2
120
SLn
116-1
Cnt3
115
Cnt1
115
114-1
114-2
T1
T1
A
A'
ELn
T5
T5
Cnt5
CM1
VH1
Cnt6
T6
118
T6
VH1
CM1

FIG. 9

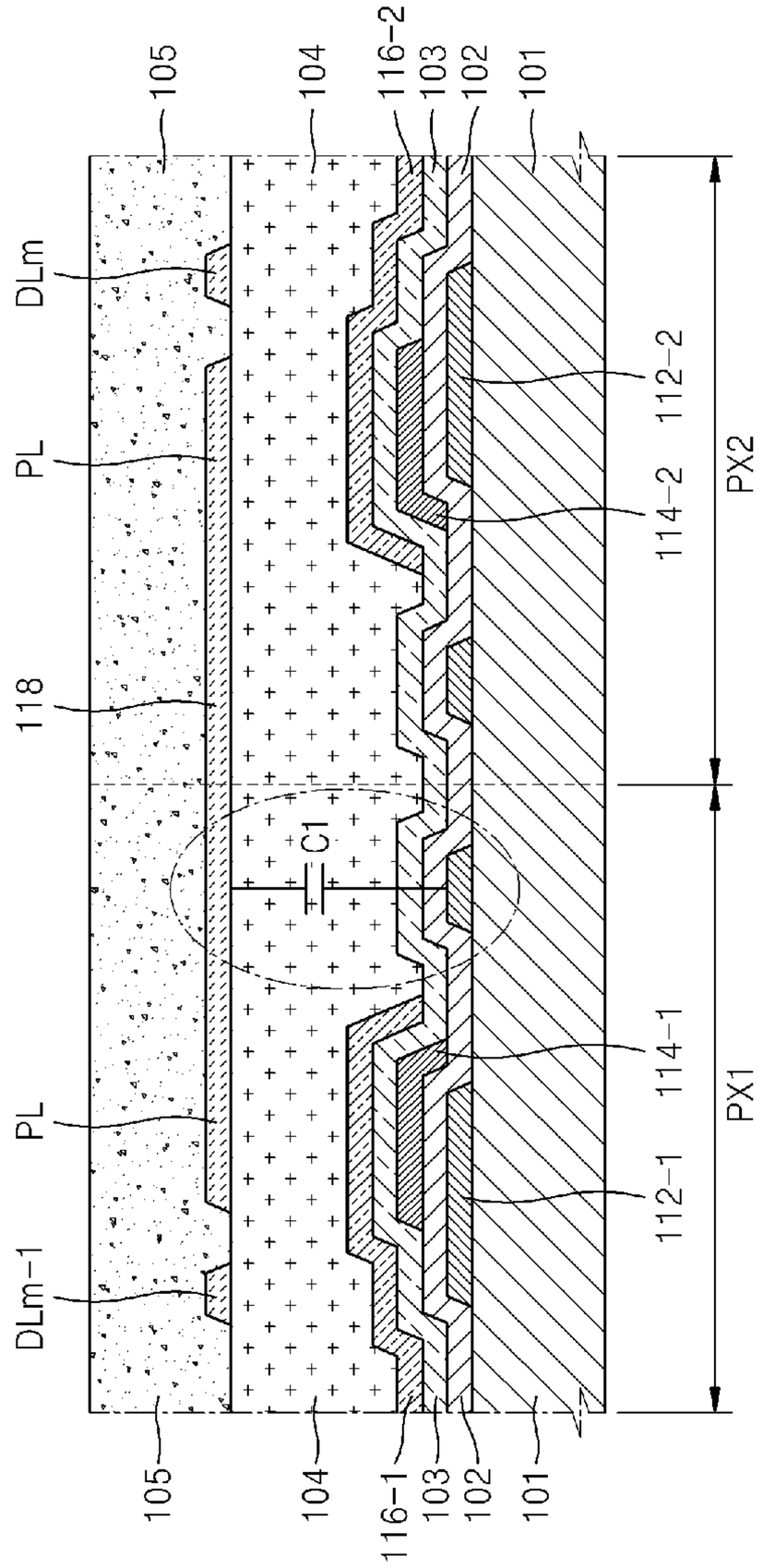

DLm-1
PL
118
PL
DLm
C1
112-1
114-1
PX1
114-2
112-2
PX2
105
104
116-1
103
102
101

FIG. 10

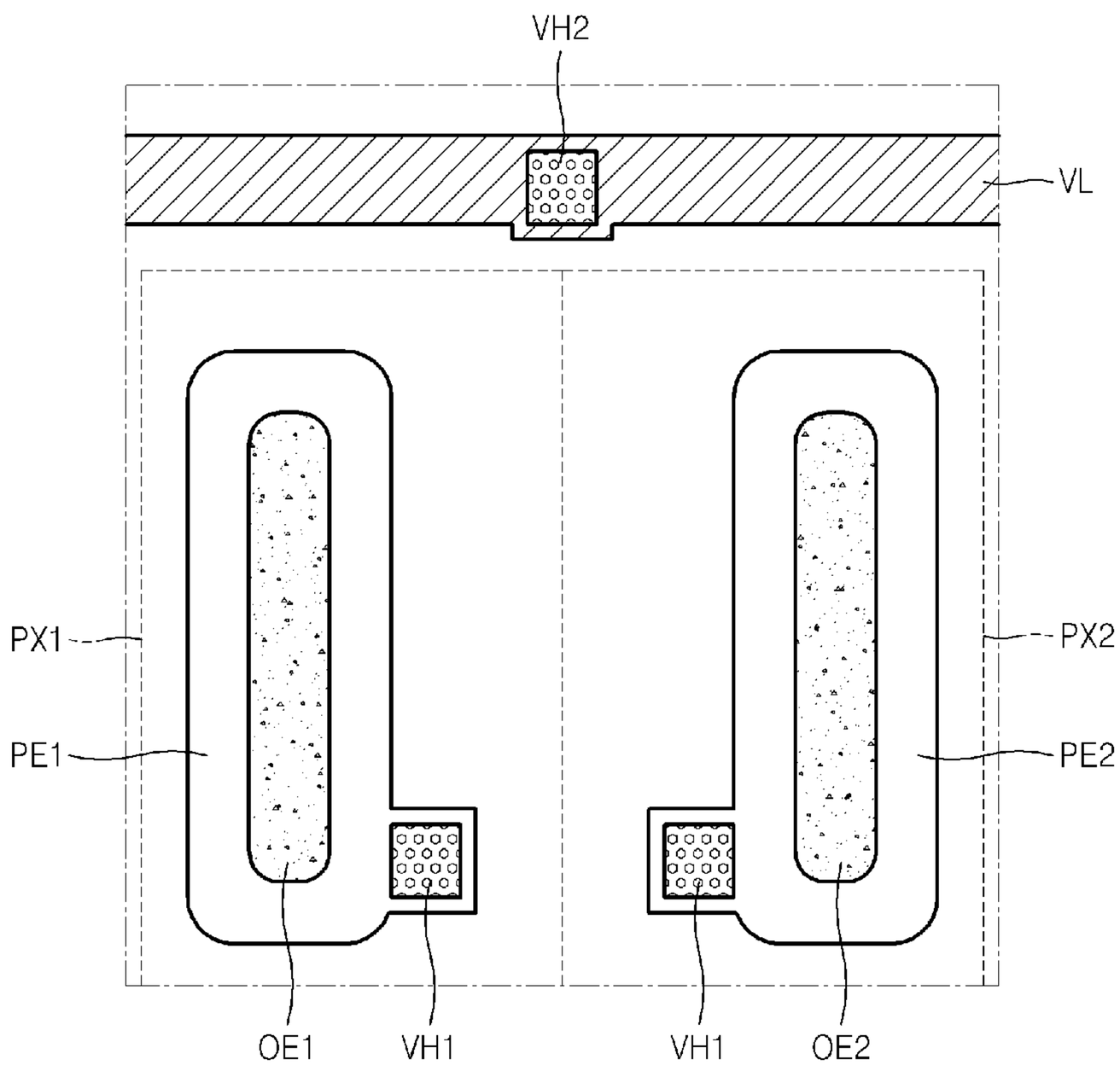


FIG. 11

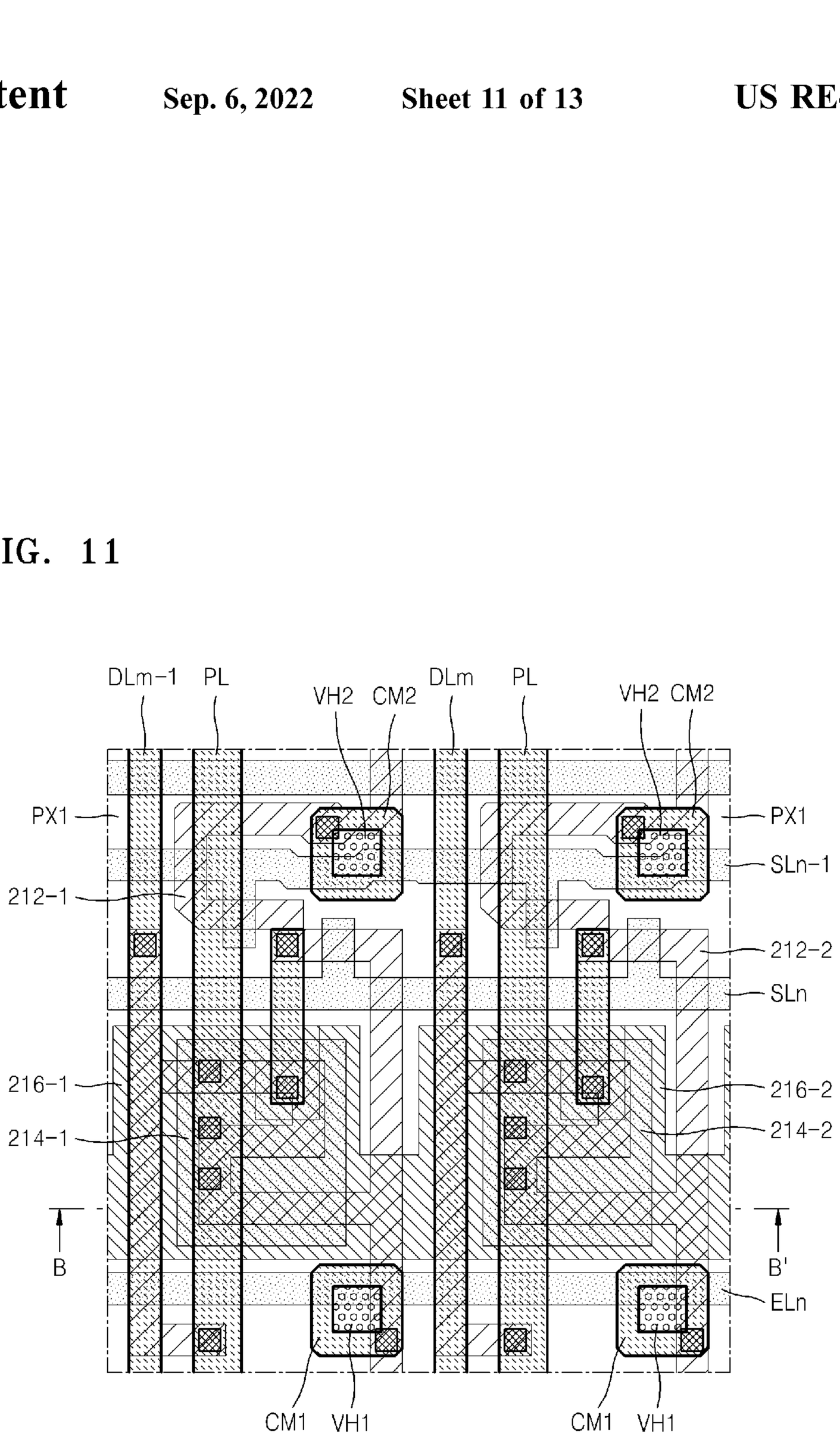

DLm-1
PL
VH2
CM2
DLm
PL
VH2
CM2
PX1
212-1
216-1
214-1
B
PX1
SLn-1
212-2
SLn
216-2
214-2
B'
ELn
CM1
VH1
CM1
VH1

FIG. 12

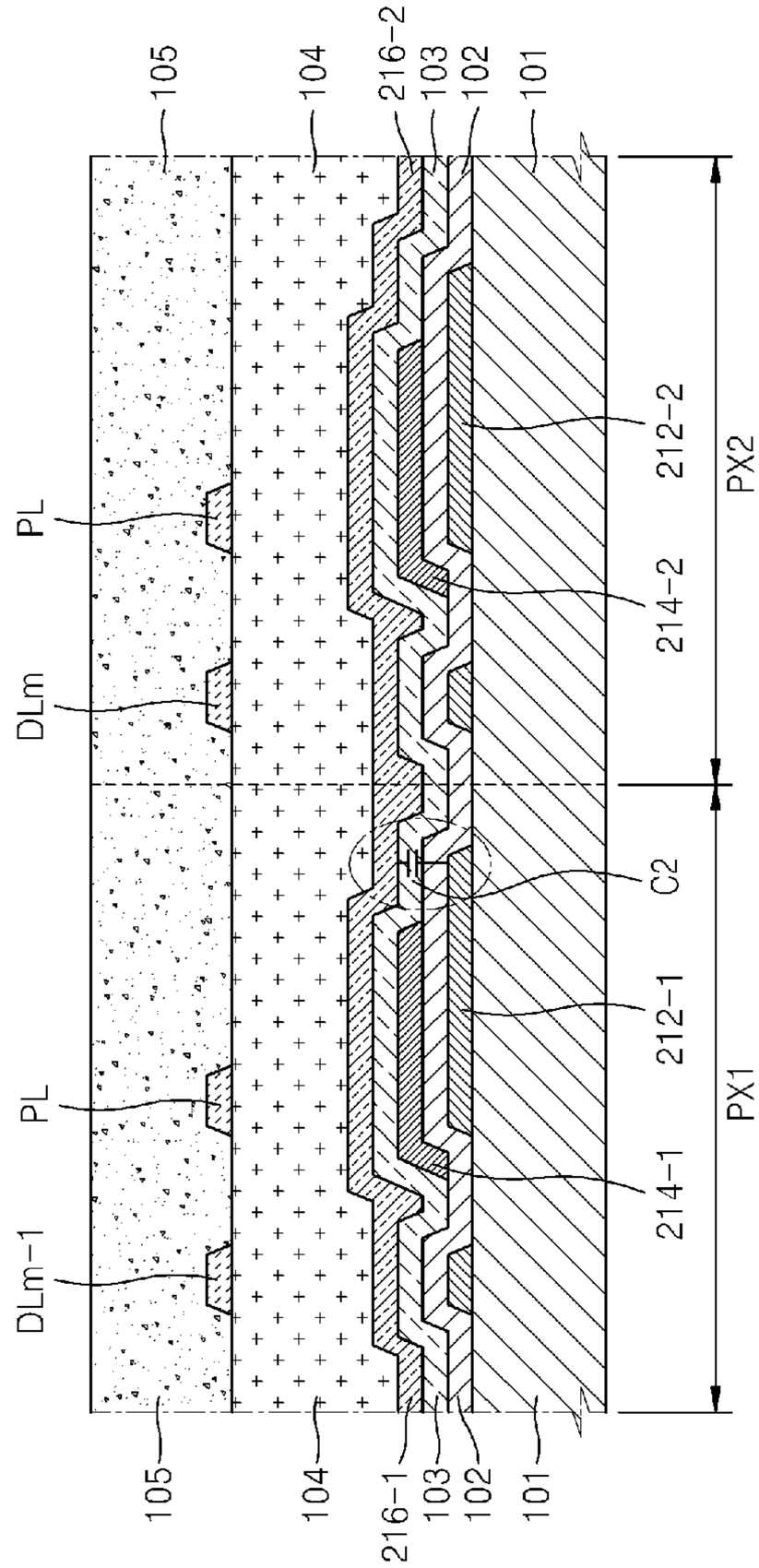
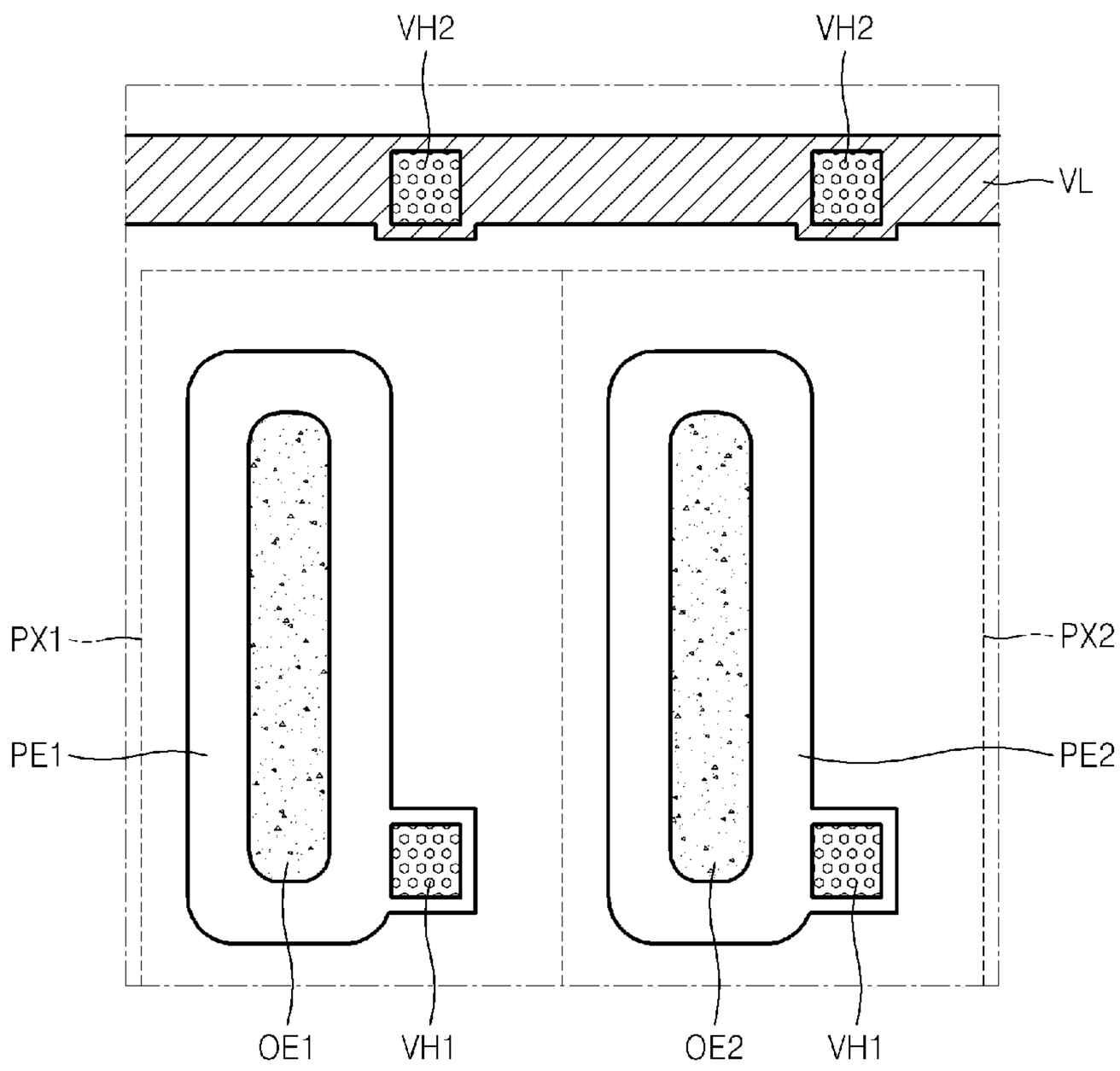

DLm-1
PL
DLm
PL
105
104
216-1
103
102
101
214-1
212-1
C2
214-2
212-2
PX1
PX2

FIG. 13



ORGANIC LIGHT-EMITTING DISPLAY DEVICE AND MANUFACTURING METHOD OF THE SAME

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue; a claim printed with strikethrough indicates that the claim was canceled, disclaimed, or held invalid by a prior post-patent action or proceeding.

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of Korean Patent Application No. 10-2012-0128371, filed on Nov. 13, 2012, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein in its entirety by reference.

BACKGROUND

1. Field

The disclosed technology relates to an organic light-emitting display device and a manufacturing method of the same.

2. Description of the Related Technology

A display device displays an image, and an organic light-emitting diode (OLED) display has particularly generated interest for use in commercializing a variety of products.

An OLED display has a self-emission characteristic by which, differently from a liquid crystal display (LCD), the OLED display does not need an additional light source such as a backlight. Therefore, the thickness and weight of an OLED display are comparatively reduced. Also, OLED displays have high-quality characteristics of low power consumption, high luminance, and high response speeds, and so on.

A panel of the OLED display includes a plurality of pixels which are arranged in an N×M matrix, and a data signal Dm, a scan signal Sn, and a power supply voltage ELVDD are selectively applied to each of the pixels in the matrix. The power supply voltage ELVDD may be commonly supplied to all pixel circuits. Unfortunately, wires for respectively supplying the power supply voltage ELVDD to the pixels have parasitic resistance components. If the power supply voltage ELVDD is supplied through the wires, a voltage drop occurs due to the parasitic resistance components.

SUMMARY OF CERTAIN INVENTIVE ASPECTS

In some aspects, the disclosed technology relates to a display device in which wires for supplying a power supply voltage ELVDD are formed in a mesh structure to prevent a voltage drop of the power supply voltage ELVDD and minimize leakage current.

According to an aspect of the disclosed technology, there is provided an organic light-emitting display device comprising: a plurality of pixels which are formed between a plurality of scan lines and a plurality of data lines; a plurality of initialization voltage lines which are formed in parallel with the plurality of scan lines and are shared between two adjacent pixels of a row to supply an initialization voltage to the two adjacent pixels; and a driving voltage line which supplies a driving voltage to the plurality of pixels and

comprises a first volatage line formed in a vertical direction and a second voltage line that is connected between the two adjacent pixels and formed in a horizontal direction.

In some embodiments, the driving voltage line is formed in a mesh structure in which the first and second voltage lines are connected to each other. The first voltage lines of the two adjacent pixels are spaced a distance apart from each other so as to parallel each other. The driving voltage line is formed on a layer on which the plurality of data lines are formed.

In some embodiments, the initialization voltage line is formed to be parallel with the second voltage. The initialization voltage line is formed on a layer on which pixel electrodes are formed. The initialization voltage line is electrically connected to initialization thin film transistors (TFTs) of the two adjacent pixels through a via hole commonly formed in the two adjacent pixels.

According to another aspect of the disclosed technology, there is provided an organic light-emitting display device comprising: active layers which have a connection area connected to each other between two adjacent pixels in a row; a first gate insulating layer, a second gate insulating layer, and an interlayer insulating layer which are sequentially formed on the active layers; a contact holes which is formed in the first and second gate insulating layers and the interlayer insulating layer and exposes the connection area of the active layers; a driving voltage line which is formed on the interlayer insulating layer; a contact metal which contacts the contact hole on the interlayer insulating layer; a protective layer which is formed on the driving voltage line and the contact metal; a via hole which is formed in protective layer and exposes part of the contact metals and are formed in the protective layer; and an initialization voltage line which is connected to the active layers through the via hole.

In some embodiments, the driving voltage line comprises a first voltage line formed in a vertical direction and a second voltage connected between the two adjacent pixels in a horizontal direction. The driving voltage line is formed in a mesh structure in which the first and second voltage lines are connected to each other. The first voltage lines are respectively formed in the two adjacent pixels and spaced a distance apart from each other so as to parallel each other. The driving voltage line is formed on a layer on which the plurality of data lines are formed.

In some embodiments, the initialization voltage line is disposed to be parallel with the second voltage line. The initialization voltage line is formed on a layer on which pixel electrodes are formed.

In some embodiments, the active layers may be symmetrical to each other between the two adjacent pixels based on the connection area. Parts of the active layers are formed to be orthogonal to the second voltage line and overlap with the second voltage line.

According to another aspect of the disclosed technology, there is provided a method of manufacturing an organic light-emitting display device, comprising: forming active layers that have a connection area connected between two adjacent pixels of a row on a substrate; sequentially forming first and second gate insulating layers and an interlayer insulating layer on the active layers; forming a contact hole in the first and second gate insulating layers and the interlayer insulating layer to expose a part of the connection area of the active layers; forming a contact metal contacting a driving voltage line and the contact holes on the interlayer insulating layer; forming a protective layer on the driving voltage line and the contact metal; forming a via hole in the

protective layer to expose part of the contact metal; and forming an initialization voltage line that is connected to the active layers through the via hole.

In some embodiments, the driving voltage line comprises a first voltage line disposed in a vertical direction and a second voltage line that is connected between the two adjacent pixels in a horizontal direction, and is formed in a mesh structure in which the first and second voltage lines are connected to each other.

In some embodiments, the initialization voltage line is formed to be parallel with the second voltage line.

In some embodiments, the active layers are symmetrical to each other between the two adjacent pixels based on the connection area, and parts of the active layers are disposed to be orthogonal to the second voltage line and overlap with the second voltage line.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other features and advantages of the disclosed technology will become more apparent by describing in detail exemplary embodiments thereof with reference to the attached drawings in which:

FIG. **1** is a schematic block diagram illustrating a display device according to an embodiment of the disclosed technology;

FIG. **2** is an equivalent circuit diagram of one pixel of a display device, according to an embodiment of the disclosed technology;

FIG. **3** is a schematic circuit diagram of two adjacent pixels of a display device, according to an embodiment of the disclosed technology;

FIG. **4** is a view illustrating a mesh structure of a driving power line PL of a display device, according to an embodiment of the disclosed technology;

FIGS. **5** through **10** are views illustrating a method of forming pixel circuits of two adjacent pixels, according to an embodiment of the disclosed technology; and

FIGS. **11** through **13** are views illustrating a comparison example with respect to the disclosed technology.

DETAILED DESCRIPTION OF CERTAIN INVENTIVE EMBODIMENTS

The disclosed technology will now be described more fully with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. The invention may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the concept of the invention to one of ordinary skill in the art. In the drawings, the thicknesses of layers and regions are exaggerated for clarity.

It will also be understood that when a layer is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present.

It will be further understood that the terms "comprises," "comprising," "includes," and/or "including," when used herein, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

FIG. **1** is a schematic block diagram illustrating a display device **100** according to an embodiment of the disclosed technology.

Referring to FIG. **1**, the display device **100** includes a display unit **10** including a plurality of pixels, a scan driver **20**, a data driver **30**, and a controller **40**. The scan driver **20**, the data driver **30**, and the controller **40** may be respectively formed on separate semiconductor chips or may be integrated on one semiconductor chip. The scan driver **20** and the display unit **10** are often formed on the same substrate.

The display unit **10** is located at intersections of a plurality of scan lines SL**0** through SLn, a plurality of data signal lines DL**1** through DLm, and a plurality of emission control lines EL**1** through ELn to include the pixels that are arranged in a matrix form.

Each of the pixels is connected to two of the plurality of scan lines SL**0** through SLn. Each of the pixels is also connected to a scan line corresponding to the corresponding pixel and a scan line of a previous pixel line in FIG. **1** but is not limited thereto. For example, each of the pixels is connected to two scan lines and the two adjacent pixels arranged in column lines do not share one scan line. In this case, pixels in first row line are connected to a first scan line SL**0** and a second scan line SL**1**, and pixels in second row line are connected to a third scan line SL**2** and a fourth scan line SL**3**.

Also, each of the pixels is connected to one of the plurality of data signal lines DL**1** through DLm and one of the plurality of emission control lines EL**1** through ELn.

Each of the pixels is connected to one of a plurality of initialization voltage lines VL for supplying an initialization voltage and one of a plurality of driving voltage lines PL) for supplying a first power supply voltage ELVDD.

Two adjacent pixels are symmetrical to one another in a direction extending across the scan lines SL**0** through SLn, i.e., a row line (or a pixel line, a width direction, or a horizontal direction). Two adjacent pixels having symmetrical structures share the initialization voltage lines VL arranged in a row line. The driving voltage lines PL that are arranged in column lines of the two adjacent pixels having the symmetrical structures are kept a predetermined distance from each other in parallel. The driving voltage lines PL that are arranged in column lines are connected to each other through the driving voltage lines PL that are arranged in row lines to form a mesh structure.

The scan driver **20** generates two corresponding scan signals and transmits the two corresponding scan signals to the pixels through the scan lines SL**0** through SLn. In other words, the scan driver **20** transmits a first scan signal through a scan line corresponding to a row line in which each pixel is included and transmits a second scan signal through a scan line corresponding to a previous row line of the corresponding row line. For example, the scan driver **20** transmits a first scan signal Sn to a pixel arranged in an m^{th} column line of an n^{th} row line through an nth scan line SLn and transmits a second scan signal Sn−1 to the pixel through an $n-1^{th}$ scan line SLn−1. The scan driver **20** generates emission control signals EM**1** through EMn and respectively transmits the emission control signals EM**1** through EMn to the pixels through the plurality of emission control lines EL**1** through ELn. Scan signals S_0 through Sn and emission control signals EM**1** through EMn are generated by the same scan driver **20** in the present embodiment but are not limited thereto. The display device **100** may further include an emission control driver by which the emission control signals are generated.

The data driver **30** respectively transmits data signals D**1** through Dm to the pixels through the data signal lines DL**1** through DLm.

The controller **40** converts a plurality of image signals R (red), G (green), and B (blue) transmitted from an external source into a plurality of image data signals DR, DG, and DB and transmits the image data signals DR, DG, and DB to the data driver **30**. The controller **40** also receives a vertical sync signal Vsync, a horizontal sync signal Hsync, and a clock signal MCLK to generate control signals for controlling driving of the scan driver **20** and the data driver **30** and transmits the control signals to the scan driver **20** and the data driver **30**. In other words, the controller **40** generates and transmits a scan driving control signal SCS and an emission driving control signal ECS for controlling the scan driver **20** and a data driving control signal DCS for controlling the data driver **30**.

Each pixel respectively emits light having a predetermined luminance through a driving current Ioled supplied to an organic light-emitting diode (OLED) according to the data signals D**1** through DM transmitted through the plurality of data signal lines DL**1** through DLm.

FIG. **2** is an equivalent circuit diagram of one pixel **1** of the display device, according to an embodiment of the disclosed technology. FIG. **3** is a schematic circuit diagram of two adjacent pixels **1** of a display device, according to an embodiment of the disclosed technology.

The pixel **1** shown in FIGS. **2** and **3** is one of a plurality of pixels included in an n^{th} row line and is connected to a scan line SLn corresponding to the n^{th} row line and a scan line SLn−1 corresponding to an $n-1^{th}$ row line before the n^{th} row line.

The pixel **1** of the display device according to an embodiment of the disclosed technology includes a pixel circuit **2** including a plurality of thin film transistors (TFTs), and a storage capacitor Cst. The pixel **1** also includes an OLED which receives a driving current from the pixel circuit **2** to emit light.

The TFTs include a driving TFT T**1**, a switching TFT T**2**, a compensation TFT T**3**, a initialization TFT T**4**, a first emission control TFT T**5**, and a second emission control TFT T**6**.

The pixel **1** includes a first scan line SLn, a second scan line SLn−1, an emission control line ELn, a data signal line DLm, a driving voltage line PL, and an initialization voltage line VL. The first scan line SLn transmits a first scan signal Sn to the switching TFT **2** and the compensation TFT T**3**. The second scan line SLn−1 transmits a second scan signal Sn−1 as a previous scan signal to the initialization TFT T**4**. The emission control line ELn transmits an emission control signal EMn to the first and second emission control TFTs T**5** and T**6**. The data signal line DLm intersects with the first scan line SLn and transmits a data signal Dm. The driving voltage line PL transmits a first power supply voltage ELVDD and is substantially parallel with the data signal line DLm. The initialization voltage line VL transmits an initialization voltage VINT for initializing the driving TFT T**1** and is substantially parallel with the second scan line SLn−1.

A gate electrode G**1** of the driving TFT T**1** is connected to a first electrode Cst**1** of the storage capacitor Cst. A source electrode S**1** of the driving TFT T**1** is connected to the driving voltage line PL through the first emission control TFT T**5**. A drain electrode D**1** of the driving TFT T**1** is electrically connected to an anode electrode of the OLED through the second emission control TFT T**6**. The driving

TFT T**1** receives the data signal Dm according to a switching operation of the switching TFT T**2** to supply the driving current Ioled to the OLED.

A gate electrode G**2** of the switching TFT T**2** is connected to the first scan line SLn. A source electrode S**2** of the switching TFT T**2** is connected to the data signal line DLm. A drain electrode D**2** of the switching TFT T**2** is connected to the source electrode S**1** of the driving TFT T**1** and is connected to the driving voltage line PL through the first emission control TFT T**5**. The switching TFT T**2** is turned on according to the first scan signal Sn received through the first scan line SLn to perform a switching operation which is to transmit the data signal Dm transmitted to the data signal line DLm to the source electrode S**1** of the driving TFT T**1**.

A gate electrode G**3** of the compensation TFT T**3** is connected to the first scan line SLn. A source electrode S**3** of the compensation TFT T**3** is connected to the drain electrode D**1** of the driving TFT T**1** and is connected to the anode electrode of the OLED through the second emission control TFT T**6**. A drain electrode D**3** of the compensation TFT T**3** is connected to the first electrode Cst**1** of the storage capacitor Cst, a drain electrode D**4** of the initialization TFT T**4**, and the gate electrode G**1** of the driving TFT T**1**. The compensation TFT T**3** is turned on according to the first scan signal Sn received through the first scan line SLn to connect the gate electrode G**1** and the drain electrode D**1** of the driving TFT T**1** to each other for diode-connection of the driving TFT T**1**.

A gate electrode G**4** of the initialization TFT T**4** is connected to the second scan line SLn−1. A source electrode S**4** of the initialization TFT T**4** is connected to the initialization voltage line VL. A drain electrode D**4** of the initialization TFT T**4** is connected to the first electrode Cst**1** of the storage capacitor Cst, the drain electrode D**3** of the compensation TFT T**3**, and the gate electrode G**1** of the driving TFT T**1**. The initialization TFT T**4** is turned on according to the second scan signal Sn−1 received through the second scan line SLn−1 to transmit the initialization voltage VINT to the gate electrode G**1** of the driving TFT T**1** in order to perform an initialization operation of initializing a voltage of the gate electrode G**1** of the driving TFT T**1**.

A gate electrode G**5** of the first emission control TFT T**5** is connected to an emission control line ELn. A source electrode S**5** of the first emission control TFT T**5** is connected to the driving voltage line PL. A drain electrode D**5** of the first emission control TFT T**5** is connected to the source electrode S**1** of the driving TFT T**1** and the drain electrode D**2** of the switching TFT T**2**.

A gate electrode G**6** of the second emission control TFT T**6** is connected to the emission control line ELn. A source electrode S**6** of the second emission control TFT T**6** is connected to the drain electrode D**1** of the driving TFT T**1** and the source electrode S**3** of the compensation TFT T**3**. A drain electrode D**6** of the second emission control TFT T**6** is electrically connected to the anode electrode of the OLED. The first and second emission control TFTs T**5** and T**6** are simultaneously turned on according to the emission control signal EMn received through the emission control line ELn to transmit the first power supply voltage ELVDD to the OLED in order to allow the driving current Ioled to flow in the OLED.

A second electrode Cst**2** of the storage capacitor Cst is connected to the driving voltage line PL. The first electrode Cst**1** of the storage capacitor Cst is connected to the gate electrode G**1** of the driving TFT T**1**, the drain electrode D**3** of the compensation TFT T**3**, and the drain electrode D**4** of the initialization TFT T**4**.

A cathode electrode of the OLED is connected to a second power supply voltage ELVSS. The OLED receives the driving current Ioled from the driving TFT T**1** to emit light in order to display an image. The first power supply voltage ELVDD may be a predetermined high level voltage, and the second power supply voltage ELVSS may be a voltage lower than the first power supply voltage ELVDD or a ground voltage.

Referring to FIG. **3**, an initialization voltage line VL supplying an initialization voltage VINT, a first scan line SLn supplying a first scan signal Sn, a second scan line SLn−1 supplying a second scan line Sn−1, and an emission control line ELn supplying an emission control signal EMn are formed in parallel in a horizontal direction. Data signal lines DLm−1 and DLm and a driving voltage line PL are formed in parallel in a vertical direction orthogonal to the horizontal direction.

Two adjacent pixels **1** share the initialization voltage line VL and are formed so that the data signal lines DLm−1 and DLm and the driving voltage lines PL keep a predetermined distance from each other to face each other. The adjacent driving voltage lines PL are connected to each other through a connection line **118** formed in the horizontal direction, thus creating a mesh structure, in order to supply power in the horizontal and vertical directions. Therefore, the area of a power supply line is further extended to reduce the voltage drop caused by resistance of the line.

In the present embodiment, the two adjacent pixels **1** may share the initialization voltage line VL to be symmetrical to each other. Therefore, the data signal line DLm−1 and the driving voltage line PL in the vertical direction of the left pixel **1** are formed at the left side of the left pixel **1**. The data signal line DLm and the driving voltage line PL in the vertical direction of the right pixel **1** are formed at the right side of the right pixel **1**. As a result, another signal line on the same layer is not formed between the driving voltage lines PL of the left and right pixels **1** in the vertical direction, and thus the two driving voltage lines PL in the vertical direction are connected to each other through the connection line **118** formed on the same layer as the driving voltage lines PL in the vertical direction.

FIG. **4** is a view illustrating a mesh structure of a driving voltage line PL of a display device, according to an embodiment of the disclosed technology.

Referring to FIG. **4**, the driving voltage line PL of the display device includes vertical driving voltage lines PLV extending in a vertical direction in column lines and horizontal driving voltage lines PLH each connecting two adjacent pixels (e.g., first and second pixels PX**1** and PX**2**) in row lines. The driving voltage line PL is also formed in a mesh structure. The horizontal driving voltage lines PLH are formed by a connection line **118** connecting two vertical driving voltage lines PLV. The connection line **118** may extend from the vertical driving voltage lines PLV to form a single body with the vertical driving voltage lines PLV. Or the connection line **118** may be formed as a separate line and connected to the vertical driving voltage lines PLV directly or through contact hole.

The horizontal driving voltage lines PLH are arranged at appropriate position according to arrangements of a pixel circuit. The vertical driving voltage lines PLV of two pixels (e.g., the first and second pixels PX**1** and PX**2**) sharing the horizontal driving voltage line PLH keep a distance from each other to face each other. Vertical driving voltage lines PLV of two adjacent pixels (e.g. second and third pixels PX**2** and PX**3**) which do not share the horizontal driving voltage line PLH are adjacent to each other with the data line in between. That is, the horizontal driving voltage line PLH is not formed between the two adjacent pixels (e.g., the second and third pixels PX**2** and PX**3**) of which the vertical driving voltage lines PLV are adjacent to each other.

FIGS. **5** through **10** are views illustrating a method of forming pixel circuits of two adjacent pixels, according to an embodiment of the disclosed technology. FIG. **9** is a cross-sectional view taken along line A-A' of FIG. **8**.

Referring to FIGS. **5** and **9**, first and second active layers **112-1** and **112-2** of first and second pixels PX**1** and PX**2** are formed on a substrate **101**. The first active layer **112-1** of the first pixel PX**1** and the second active layer **112-2** of the second pixel PX**2** are connected to each other. The first and second active layers **112-1** and **112-2** are symmetrical to each other based on an active area connection between the first and second pixels PX**1** and PX**2**. The active area connection between the first and second pixels PX**1** and PX**2** is connected to an initialization voltage line VL later.

The first and second active layers **112-1** and **112-2** may be formed as amorphous silicon layers, polycrystalline silicon layers, or oxide semiconductor layers such as G-I-Z layers [(In2O3)a(Ga2O3)b(ZnO)c layer] (wherein a, b, and c are real numbers satisfying a condition of a≥0, b≥0, and c>0). According to certain embodiments, the first and second active layers **112-1** and **112-2** are connected to each other and thus transmit an initialization voltage VINT applied to the initialization voltage line VL to the first and second pixels PX**1** and PX**2**.

TFTs of a pixel circuit are formed along the first and second active layers **112-1** and **112-2**. Active layers A**1**, A**2**, A**3**, A**4**, A**5**, and A**6** of a driving TFT T**1**, a switching TFT T**2**, a compensation TFT T**3**, an initialization TFT T**4**, a first emission control TFT T**5**, and a second emission control TFT T**6** are formed on each of the first and second active layers **112-1** and **112-2**. An active layer of each TFT includes a channel area which is not doped with impurities, and source and drain areas which are formed by doping both sides of the channel area with impurities. Here, the impurities vary according to a type of a TFT and may be N-type or P-type impurities.

The first and second active layers **112-1** and **112-2** are curved in various shapes. In particular, each of the active layers A**1** of the driving TFTs T**1** has a plurality of curved parts having zigzag shapes, "S" shapes, or "ㄹ" shapes. Therefore, the channel areas are formed to be long, and thus, the driving range of the gate voltage widens. As a result, widening of the driving range of the gate voltage changes the intensity of the gate voltage, and thus, gradations of light emitted from OLEDs are further precisely controlled. Thereby the resolution and image quality of the organic light-emitting display device are improved.

Referring to FIGS. **6** and **9**, a first gate insulating layer **102** is formed on the substrate **101** on which the first and second active layers **112-1** and **112-2** are formed. The first gate insulating layer **102** may be formed of an organic insulating material, an inorganic insulting material, or in a multilayer structure in which organic insulating materials alternate with inorganic insulating materials.

A first gate lines are formed on the first gate insulating layer **102**. The first gate lines may include a first scan line SLn, a second scan line SLn−1, an emission control line ELn, and first capacitor electrodes **114-1** and **114-2**. The first gate lines may include at least one metal material in the group of aluminum (Al), platinum (Pt), palladium (Pd), silver (Ag), magnesium (Mg), gold (Au), nickel (Ni), neodymium (Nd), iridium (Ir), chromium (Cr), lithium (Li), calcium (Ca), molybdenum (Mo), titanium (Ti), tungsten

(W), and copper (Cu), and preferably, a low resistance metal material such as aluminum (Al), copper (Cu), or the like.

The first capacitor electrodes **114-1** and **114-2** operate as gate electrodes G**1** of the driving TFTs T**1**. The first capacitor electrodes **114-1** and **114-2** are separated from the first scan line SLn, the second scan line SLn−1, and the emission control line ELn and overlap with the channel areas of the active areas A**1** of the driving TFTs T**1** in floating electrode shapes. The first capacitor electrodes **114-1** and **114-2** are separated from each other between adjacent pixels to be formed in square shapes. The first scan line SLn operates as gate electrodes G**2** of the switching TFTs T**2** and gate electrodes G**3** of the compensation TFTs T**3**. The second scan line SLn−1 operates as gate electrodes G**4** of the initialization TFT T**4**. The emission control line ELn operates as gate electrodes G**5** of the first emission control TFTs T**5** and gate electrodes G**6** of the second emission control TFTs T**6**.

Referring to FIGS. **7** and **9**, a second gate insulating layer **103** is formed on the substrate **101** on which the first gate line are formed. The second gate insulating layer **103** operates a dielectric of a storage capacitor Cst. The second gate insulating layer **103** may be formed of an organic insulating material, an inorganic insulating material, or in a multilayer structure in which organic insulating materials alternate with inorganic insulating materials.

Second gate lines are formed on the second gate insulating layer **103**. The second gate lines include second capacitor electrodes **116-1** and **116-2**. The second gate lines may be formed of at least one metal material in the group of aluminum (Al), platinum (Pt), palladium (Pd), silver (Ag), magnesium (Mg), gold (Au), nickel (Ni), neodymium (Nd), iridium (Ir), chromium (Cr), lithium (Li), calcium (Ca), molybdenum (Mo), titanium (Ti), tungsten (W), and copper (Cu), and preferably, a low resistance metal material such as aluminum (Al), copper (Cu), or the like, like a material of the first gate line GL**1**.

The second capacitor electrodes **116-1** and **116-2** overlap with the first capacitor electrodes **114-1** and **114-2** to form the storage capacitor Cst. The second capacitor electrodes **116-1** and **116-2** are separated from each other between adjacent pixels sharing an initialization voltage VINT and having symmetrical structures, and each are connected to the second capacitor electrodes of adjacent pixels not sharing an initialization voltage VINT. Or the second capacitor electrodes **116-1** and **116-2** may be separated from each other in floating electrode shapes. The second capacitor electrodes **116-1** and **116-2** include storage openings **115**. The storage openings **115** may have closed curve shapes. Here, a closed curve refers to a figure in which when one dot is marked on a straight line or a curve, start and end dots are closed like a polygon or a circle. The second capacitor electrodes **116-1** and **116-2** including the storage openings **115** may have doughnut shapes. Although an overlay deviation occurs between the first capacitor electrodes **114-1** and **114-2** and the second capacitor electrodes **116-1** and **116-2** in the manufacturing process of the display device, the capacitance of the storage capacitor Cst may be maintained as constant due to the shapes of the second capacitor electrodes **116-1** and **116-2**. The overlay deviation refers to a difference between two or more overlapping layers which are shifted in up, down, left, and right directions and thus become different from their initial designed states. The overlay deviation may occur due to a misalignment between a substrate and a mask or a misalignment between the substrate and an exposure when a conductive layer is formed on a whole surface of the substrate and then patterned through a photolithography. It is likely that the overlay deviation will occur within an error range of a process apparatus in a system for making large panels and simultaneously producing a mass of panels. Even if the first capacitor electrodes **114-1** and **114-2** are shifted in up, down, left, and right directions, the second capacitor electrodes **116-1** and **116-2** overlap completely with the first capacitor electrodes **114-1** and **114-2**, and the storage openings **115** of the second capacitor electrodes **116-1** and **116-2** constantly overlap with the first capacitor electrodes **114-1** and **114-2** at all times. Therefore, capacitance is kept constant.

Referring to FIGS. **8** and **9**, an interlayer insulating layer **104** is formed on the substrate **101** on which the second gate lines are formed. Like the first and second gate insulating layers **102** and **103**, the interlayer insulating layer **104** may be formed of an organic insulating material, an inorganic insulating material, or in a multilayer structure in which organic insulating materials alternate with inorganic insulating layers.

First contact holes Cnt**1** are formed in the second gate insulating layer **103** and the interlayer insulating layer **104** through the openings **115** of the second capacitor electrodes **116-1** and **116-2** to expose the first capacitor electrodes **114-1** and **114-2**. Third contact holes Cnt**3** are formed in the interlayer insulating layer **104** to expose the second capacitor electrodes **116-1** and **116-2**. Second contact holes Cnt**2** are formed in the first and second gate insulating layers **102** and **103** and the interlayer insulating layer **104** to expose drain areas of the active layers A**3** of the compensation TFTs T**3** and drain areas of the active layers A**4** of the initialization TFTs T**4**. Fourth contact holes Cnt**4** are formed in the first and second gate insulating layers **102** and **103** and the interlayer insulating layer **104** to expose source areas of the active layers A**2** of the switching TFTs T**2**. Fifth contact holes Cnt**5** are formed in the first and second gate insulating layers **102** and **103** and the interlayer insulating layer **104** to expose the active layers A**5** of the first emission control TFTs T**5**. Sixth contact holes Cnt**6** are formed in the first gate insulating layers **102** and **103** and the interlayer insulating layer **104** to expose the active layers A**6** of the second emission control TFTs T**6**. Seventh contact holes Cnt**7** are formed in the first and second gate insulating layers **102** and **103** and the interlayer insulating layer **104** to expose an active area connection in which the first active layer **112-1** of the first pixel PX**1** and the second active layer **112-2** of the second pixel PX**2** are connected to each other.

First contact metals CM**1** are formed on the interlayer insulating layer **104** to cover data signal lines DLm−1 and DLm, the driving voltage line PL in a vertical direction, the connection line **118**, a connection line **120** connecting the first and second contact holes Cnt**1** and Cnt**2**, and the sixth contact holes Cnt**6**. Second contact metals CM**2** are formed on the interlayer insulating layer **104** to cover the seventh contact holes Cnt**7**.

The data signal lines DLm−1 and DLm are disposed at a side edge of every one pixel in the vertical direction. The data signal lines DLm−1 and DLm are connected to the switching TFTs T**2** through the fourth contact holes Cnt**4**.

The driving voltage lines PL include the vertical driving voltage line PLV in the vertical direction and the horizontal driving voltage line PLH formed by the connection line **118** in a horizontal direction. One vertical driving voltage lines PLV is disposed at a side edge of every one pixel in the vertical direction to be adjacent to the data signal lines DLm−1 and DLm. Two vertical driving voltage lines PLV face each other between the first and second pixels PX**1** and PX**2**. The connection line **118** crosses the first and second

pixels PX1 and PX2 in the horizontal direction and connects the vertical driving voltage lines PLV of the first and second pixels PX1 and PX2 to operate as the horizontal driving voltage line PLH. Therefore, a mesh structure of the driving voltage lines PL is realized. The driving voltage lines PL are connected to the second capacitor electrodes **116-1** and **116-2** through the third contact holes Cnt3.

The connection line **120** connects the first capacitor electrodes **114-1** and **114-2**, the compensation TFTs T3, and the initialization TFTs T4.

The data signal lines DLm−1 and DLm, the driving voltage lines PL including the connection line **118**, the connection line **120**, the first contact metals CM1, and the second contact metals CM2 may be formed of the same material on the same layer.

A protective layer **105** is formed on the substrate **101** on which the data signal lines DLm−1 and DLm, the driving voltage lines PL including the connection line **118**, the connection line **120**, the first contact metals CM1, and the second contact metals CM2 are formed. First and second via holes VH1 and VH2 are formed in the protective layer **105** to expose parts of the first and second contact metals CM1 and CM2.

The second via hold VH2 is commonly formed in the two adjacent first and second pixels PX1 and PX2 to improve an aperture of the two adjacent first and second pixels PX1 and PX2 more than when the second via hole VH2 is formed in each pixels first and second PX1 and PX2.

Referring to FIG. **10**, pixel electrodes PE1 and PE2 and the initialization voltage line VL are formed on the protective layer **105**. The pixel electrodes PE1 and PE2 are respectively connected to the second emission control TFTs T6 through the first vial holes VH1. The initialization voltage line VL is connected to the initialization TFTs T4 of the first and second pixels PX1 and PX2 through the second via hole VH2 commonly formed in the first and second pixels PX1 and PX2 in order to simultaneously transmit an initialization voltage VINT to the first and second pixels PX1 and PX2. The initialization voltage line VL may be formed of the same material as the pixel electrodes PE1 and PE2 on the same layer.

Although not shown, a pixel-defining layer (PDL) is formed on edges of the pixel electrodes PE1 and PE2 and the protective layer **105** and has a pixel opening exposing the pixel electrodes PE1 and PE2. The PDL may be formed of an organic material such as polyacrylate resin and polyimides or a silica-based inorganic material. Organic layers OE1 and OE2 and opposing electrodes (not shown) are formed on the pixel electrodes PE1 and PE2 exposed through the pixel opening. Here, the opposing electrodes cover the organic layers OE1 and OE2 and are formed on a whole surface of the substrate **101**. Therefore, OLEDs of the first and second pixels PX1 and PX2, including the pixel electrodes PE1 and PE2, the organic layers OE1 and OE2 disposed on the pixel electrodes PE1 and PE2, and opposing electrodes covering the organic layers OE1 and OE2 and formed on the whole surface of the substrate **101**, are formed.

If the display device has a front emission type structure, the pixel electrodes PE1 and PE2 may be included as reflective electrodes, and the opposing electrodes may be included as transmissive electrodes. In this case, the opposing electrodes may include transflective layers formed of Mg, Al, Pt, Pd, Au, Ni, Nd, Ir, Cr, Li, Ca, or the like or transmissive metal oxides such as ITO, IZO, ZnO, or the like. If the display device has a bottom emission type structure, Ag, Mg, Al, Pt, Pd, Au, Ni, Nd, Ir, Cr, Li, Ca, or the like may be deposited so that the opposing electrodes have reflective functions. If the pixel electrodes PE1 and PE2 are used as anode electrodes, the pixel electrodes PE1 and PE2 may include layers formed of a metal oxide such as ITO, IZO, ZnO, or the like having a high work function (an absolute value). If the pixel electrodes PE1 and PE2 are used as cathode electrodes, the pixel electrodes PE1 and PE2 may use high conductive metals having low work functions (absolute values) such as Ag, Mg, Al, Pt, Pd, Au, Ni, Nd, Ir, Cr, Li, Ca, or the like. If the pixel electrodes PE1 and PE2 are used as anode electrodes, the opposing electrodes are used as cathode electrodes. If the pixel electrodes PE1 and PE2 are used as cathode electrodes, the opposing electrodes are used as anode electrodes.

One or more functional layers, such as emissive layers (EMLs), hole transport layers (HTLs), hole injection layers (HILs), electron transport layers (ETLs), and electron injection layers (EILs), may be stacked in a single or multilayer structure to form the organic layers OE1 and OE2 of the first and second pixels PX1 and PX2. The organic layers OE1 and OE2 may be low or high molecular organic materials. If the organic layers OE1 OE2 emit R, G, and B lights, the EMLs may be patterned as R, G, and B emissive layers according to R, G, and B sub-pixels. If the organic layers OE1 and OE2 emit white light, the EMLs may have multilayer structures in which R, G, and B emissive layers are stacked, or single layer structures including R, G and B emissive materials to emit white light.

FIGS. **11** through **13** are views illustrating a comparison example with respect to the disclosed technology. FIG. **12** is a cross-sectional view taken along line B-B' of FIG. **11**.

Referring to FIGS. **11** through **13**, an active layer **212-1** of a first pixel PX1 and an active layer **212-2** of a second pixel PX2 are formed separately on a substrate **101**. A first gate insulating layer **102**, a first gate lines, a second gate insulating layer **103**, a second gate lines, and an interlayer insulating layer **104** are sequentially formed on the active layers **212-1** and **212-2**. The first gate lines include a first scan line SLn, a second scan line SLn−1, an emission control line ELn, and first capacitor electrodes **214-1** and **214-2**. The second gate lines include second capacitor electrodes **216-1** and **216-2**. The second capacitor electrode **216-1** of the first pixel PX1 and the second capacitor electrode **216-2** of the second pixel PX2 are connected to each other.

Data signal lines DL and driving voltage lines PL are formed on the interlayer insulating layer **104**. The second capacitor electrodes **216-1** and **216-2** of the first and second pixels PX1 and PX2 are connected to the driving voltage lines PL through contact holes and thus operate to realize a mesh structure of the driving voltage lines PL. First and second contact metals CM1 and CM2 are formed on the interlayer insulating layer **104**.

A protective layer **105** is formed on the substrate **101** on which the data signal lines DLm−1 and DLm, the driving voltage lines PL, the first contact metals CM1, and the second contact metals CM2 are formed. First and second via holes VH1 and VH2 are formed in the protective layer **105** of the first and second pixels PX1 and PX2 to expose parts of the first and second contact metals CM1 and CM2.

Pixel electrodes PE1 and PE2 and an initialization voltage line VL are formed on the protective layer **105**. The pixel electrodes PE1 and PE2 are connected to second emission control TFTs T6 of the first and second pixels PX1 and PX2 through the first via holes vH1. The initialization voltage line VL is connected to initialization TFTs T4 of the first and second pixels PX1 and PX2 through the second via holes VH2 formed in the each first and second pixels PX1 and PX2.

As described with reference to FIG. **9**, in certain embodiments, driving voltage lines PL having a mesh structure including vertical driving voltage lines PLV and horizontal driving voltage lines PLH may be formed of the same material on the same layer. Therefore, the first gate insulating layer **102**, the second gate insulating layer **103**, and the interlayer insulating layer **104** are formed between the connection line **118** constituting the horizontal driving voltage lines PLH and the first and second active layers **112-1** and **112-2** formed to be approximately orthogonal to the connection line **118**.

In the comparison example of FIG. **12**, the driving voltage lines PL having the mesh structure are formed of the second capacitor electrodes **216-1** and **216-2**. Therefore, the first gate insulating layer **102** and the second gate insulating layer **103** are formed between a connection part of the second capacitor electrodes **216-1** and **216-2** and the active layers **212-1** and **212-2**.

In a comparison between FIGS. **9** and **12**, a capacitance of a parasitic capacitor C**1** occurring between the driving voltage lines PL and the first and second active layers **112-1** and **112-2** according to certain embodiments of the disclosed technology is smaller than a capacitance of a parasitic capacitor C**2** occurring between the driving voltage lines PL and the active layers **212-1** and **212-2** in the comparison example.

A parasitic capacitor occurring between the driving voltage lines PL having the mesh structure and active layers increase a leakage current flowing in pixel electrodes of OLEDs through the second emission control TFTs T**6**, thereby increasing a black luminance.

The horizontal driving voltage lines PLH are formed on the same layer on which the vertical driving voltage lines PLV are formed on the same layer as the data signal lines DLm−1 and DLm to form a thicker insulating layer between the driving voltages PL and the first and second active layers **112-1** and **112-2** in the embodiment of the disclosed technology than in the comparison example. Therefore, a parasitic capacitor of the driving voltage lines PL is reduced to prevent the black luminance from increasing, thereby reducing an image distortion of a screen.

Also, in certain embodiments of the disclosed technology, the driving voltage lines PL are formed in the mesh structure to supply a first power supply voltage ELVDD having a predetermined and constant intensity to thereby reduce voltage drop.

According to the above-described embodiments, an active matrix (AM) type organic light-emitting display device having a 6Tr-1Cap structure includes six TFTs and one capacitor in one pixel. However, the disclosed technology is not limited thereto, and a display device may include a plurality of TFTs and capacitors in one pixel. Also, an additional line may be further formed or an existing line may be omitted so that the display device has various structures.

As described above, a display device according to embodiments of the disclosed technology a voltage drop due to an increase in a size of a panel can be compensated.

Also, various embodiments of the display device minimize a parasitic capacitance to prevent increasing a black luminance.

While the disclosed technology has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope of the disclosed technology as defined by the following claims.

What is claimed is:

1. An organic light-emitting display device comprising:

a first pixel having a first active layer and a second pixel having a second active layer, the first pixel and the second pixel formed as two adjacent pixels in a row of pixels;

a connection area between the first pixel and the second pixel, the connection area including direct, physical contact between the first active layer and the second active layer;

at least one insulating layer formed on the first active layer and the second active layer;

a contact hole which is formed in the insulating layer and exposes the connection area;

a driving voltage line which is formed on the insulating layer;

a contact metal which is formed on the insulating layer and contacts the connection area through the contact hole;

a protective layer which is formed on the driving voltage line and the contact metal;

a via hole which is formed in the protective layer and exposes part of the contact metal; and

an initialization voltage line which is connected to the contact metal to electrically connect to the first active layer and the second active layer through the via hole.

2. The organic light-emitting display device of claim **1**, wherein the driving voltage line for the two adjacent pixels comprises two first voltage lines formed in a vertical direction and a second voltage line that is connected to the two first voltage lines in a horizontal direction.

3. The organic light-emitting display device of claim **2**, wherein the two first voltage lines are spaced a distance apart from each other so as to parallel each other.

4. The organic light-emitting display device of claim **1**, wherein the driving voltage line is formed on a layer on which a plurality of data signal lines are formed.

5. The organic light-emitting display device of claim **2**, wherein the initialization voltage line is disposed to be parallel with the second voltage line.

6. The organic light-emitting display device of claim **1**, wherein the initialization voltage line is formed on a layer on which pixel electrodes are formed.

7. The organic light-emitting display device of claim **1**, wherein the first active layer and the second active layer are symmetrical based on the connection area.

8. The organic light-emitting display device of claim **2**, wherein parts of the first and second active layers are formed to be orthogonal to the second voltage line and overlap with the second voltage line.

9. A method of manufacturing an organic light-emitting display device, the method comprising:

forming a first active layer *for* a first pixel and a second active layer for a second pixel, the first and second pixels formed as two adjacent pixels in a row of pixels on a substrate, the first and second active layers having a connection area between the first and second pixels, the connection area including direct, physical contact between the first active layer and the second active **[**law**]** *layer*;

forming at least one insulating layer on the first and second active layers;

forming a contact hole in the insulating layer to expose a part of the connection area;

forming a contact metal and a driving voltage line on the insulating layer, wherein the contact metal contacts the connection area through the contact hole;

forming a protective layer on the driving voltage line and the contact metal;

forming a via hole in the protective layer to expose part of the contact metal; and

forming an initialization voltage line that is connected to the contact metal to electrically connect to the first and second active layers through the via hole.

10. The method of claim **9**, wherein the driving voltage line for the first and second pixels comprises two first voltage lines formed in a vertical direction and a second voltage line that is connected to the two first voltage lines in a horizontal direction.

11. The method of claim **10**, wherein the initialization voltage line is formed to be parallel with the second voltage line.

12. The method of claim **10**, wherein the first and second active layers are symmetrical based on the connection area, and parts of the first and second active layers are disposed to be orthogonal to the second voltage line and overlap with the second voltage line.

13. An organic light emitting diode display comprising:

a scan line extended to a first direction;

a first data line extended to a second direction different from the first direction;

a first driving voltage line extended to the second direction;

an initialization voltage line extended to the first direction;

a first thin film transistor comprising a first gate electrode and a first active layer being curved under the first gate electrode, and coupled to the first driving voltage line;

a second thin film transistor coupled to the first data line and the scan line;

a third thin film transistor coupled to the initialization voltage line and the first thin film transistor;

a first organic light emitting diode coupled to the first thin film transistor;

a first insulating layer covering the first thin film transistor; and

a first storage capacitor electrically coupled to the first gate electrode of the first thin film transistor,

wherein the first storage capacitor comprises a first capacitor electrode including a portion of the first gate electrode of the first thin film transistor, and a second capacitor electrode overlapping the first capacitor electrode, and

wherein a portion of the first insulating layer is between the first capacitor electrode and the second capacitor electrode, and

wherein one end of the first active layer is extended to the second thin film transistor, and the other end of the first active layer is extended to the third thin film transistor.

14. The organic light emitting diode display of claim 13, further comprising: a fourth thin film transistor coupled to the first driving voltage line and the first thin film transistor.

15. The organic light emitting diode display of claim 14, wherein the first active layer is extended to and coupled to the fourth thin film transistor.

16. The organic light emitting diode display of claim 14, further comprising:

a second insulating layer over the second capacitor electrode.

17. The organic light emitting diode display of claim 16, further comprising:

a first pixel electrode on the second insulating layer, and coupled to the first organic light emitting diode and the first thin film transistor.

18. The organic light emitting diode display of claim 16, wherein the initialization voltage line is on the second insulating layer.

19. The organic light emitting diode display of claim 18, wherein the first active layer is extended to and coupled to the fourth thin film transistor.

20. The organic light emitting diode display of claim 19, further comprising; a contact metal coupled to the initialization voltage line and the third thin film transistor.

21. The organic light emitting diode display of claim 13, further comprising;

a second data line extended to the second direction;

a second driving voltage line extended to the second direction;

a fifth thin film transistor comprising a second gate electrode and a second active layer being curved under the second gate electrode, and coupled to the second driving voltage line;

a sixth thin film transistor coupled to the second data line and the scan line;

a seventh thin film transistor coupled to the initialization voltage and the third thin film transistor;

a second organic light emitting diode coupled to the fifth thin film transistor; and

a second storage capacitor electrically coupled to the second gate electrode of the fifth thin film transistor,

wherein the second storage capacitor comprises a third capacitor electrode including a portion of the second gate electrode of the fifth thin film transistor, and a fourth capacitor electrode overlapping the third capacitor electrode,

wherein a portion of the first insulating layer between the third storage capacitor electrode and the fourth storage capacitor electrode,

wherein one end of the second active layer is extended to the sixth thin film transistor, and the other end of the second active layer is extended to the seventh thin film transistor, and

wherein the second active layer is symmetric to the first active layer.

22. The organic light emitting diode display of claim 21, further comprising; a eighth thin film transistor coupled to the second driving voltage line and the fifth thin film transistor.

23. The organic light emitting diode display of claim 22, wherein the second active layer is extended to and coupled to the eighth thin film transistor.

24. The organic light emitting diode display of claim 21, further comprising:

a second insulating layer over the first storage capacitor and the second storage capacitor.

25. The organic light emitting diode display of claim 24, comprising;

a second pixel electrode on the second insulating layer, and coupled to the second organic light emitting diode and the fifth thin film transistor.

26. The organic light emitting diode display of claim 25, wherein the initialization voltage line is on the second insulating layer.

27. The organic light emitting diode display of claim 26, Wherein the first active layer is extended to and electrically coupled to the second active layer.

28. An organic light emitting diode display comprising:

substrate;

a plurality of scanning lines on the substrate;

a plurality of data lines;

a first thin film transistor coupled to a first scan line of the scan lines and a first data line of the data lines;

a plurality of driving voltage lines;

a second thin film transistor comprising a first gate electrode and a first active layer and electrically coupled to a first driving voltage line of the driving voltage lines;

a plurality of initialization voltage lines;

a third thin film transistor comprising a second gate electrode and coupled to a first initialization voltage line of the initialization voltage lines and the second thin film transistor;

a first organic light emitting diode electrically coupled to the second thin film transistor;

a first insulating layer covering the second thin film transistor; and

a first storage capacitor coupled to the first gate electrode and comprising a first capacitor electrode and a second capacitor electrode over the first capacitor electrode, wherein the first capacitor electrode includes a portion of the first gate electrode of the second thin film transistor, and a portion of the first insulating layer is between the first capacitor electrode and the second capacitor electrode,

wherein the first active layer is coupled to an active layer of the third thin film transistor, and

wherein the first active layer under the first gate electrode is curved.

29. The organic light emitting diode display of claim 28, further comprising a fourth thin film transistor comprises a third gate electrode and is electrically coupled to the first driving voltage line and the second thin film transistor.

30. The organic light emitting diode display of claim 29, wherein the first active layer is coupled to an active layer of the fourth thin film transistor.

31. The organic light emitting diode display of claim 29, further comprising a second insulating layer over the first capacitor electrode.

32. The organic light emitting diode display of claim 31, wherein the first organic light emitting diode comprises a first pixel electrode that is formed on the second insulating layer.

33. The organic light emitting diode display of claim 32, wherein the initialization voltage lines are formed on the second insulating layer.

34. The organic light emitting diode display of claim 33, wherein the first active layer is coupled to an active layer of the fourth thin film transistor.

35. The organic light emitting diode display of claim 34, further comprising a contact metal coupled to the first initialization voltage line and the third thin film transistor.

36. The organic light emitting diode display of claim 28, further comprising;

a fourth thin film transistor coupled to the first scan line and a second data line of the data lines;

a fifth thin film transistor comprising a third gate electrode and a second active layer, and electrically coupled to a second driving voltage line of the driving voltage lines;

a sixth thin film transistor comprising a fourth gate electrode and coupled to the first initialization voltage line and the fifth thin film transistor;

a second organic light emitting diode electrically coupled to the fifth thin film transistor; and

a second storage capacitor electrically coupled to the third gate electrode and comprising a third capacitor electrode and a fourth capacitor electrode over the third capacitor electrode, wherein the third capacitor electrode includes a portion of the third gate electrode of the fifth thin film transistor, and a portion of the first insulating layer is between the third storage capacitor electrode and the fourth storage capacitor electrode,

wherein the second active layer is coupled an active layer of the sixth transistor,

wherein the second active layer curved under the third gate electrode, and

wherein the second active layer is symmetric to the first active layer.

37. The organic light emitting diode display of claim 36, further comprising a seventh thin film transistor comprises a fifth gate electrode and is electrically coupled to the second driving voltage line and the fifth thin film transistor.

38. The organic light emitting diode display of claim 37, wherein the second active layer is coupled to an active layer of the seventh thin film transistor.

39. The organic light emitting diode display of claim 36, further comprising;

a second insulating layer over the first storage capacitor and the second storage capacitor.

40. The organic light emitting diode display of claim 39, wherein the second organic light emitting diode comprises a second pixel electrode that is formed on the second insulating layer.

41. The organic light emitting diode display of claim 40, wherein the first initialization voltage line formed on the second insulating layer.

42. The organic light emitting diode display of claim 41, wherein the first active layer is coupled to the second active layer.

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