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(54) **FLIP CHIP AND METHOD OF MAKING FLIP CHIP**

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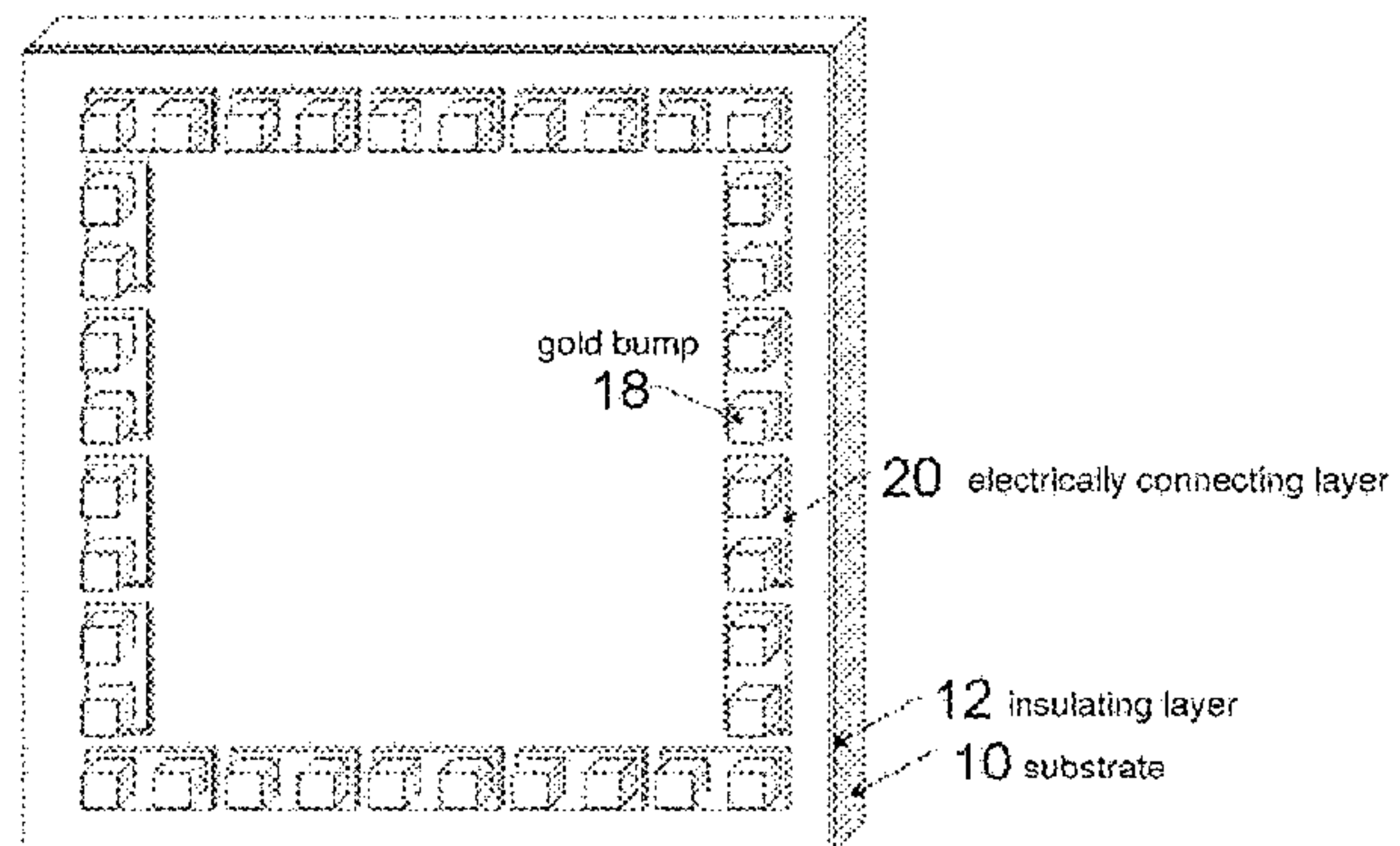
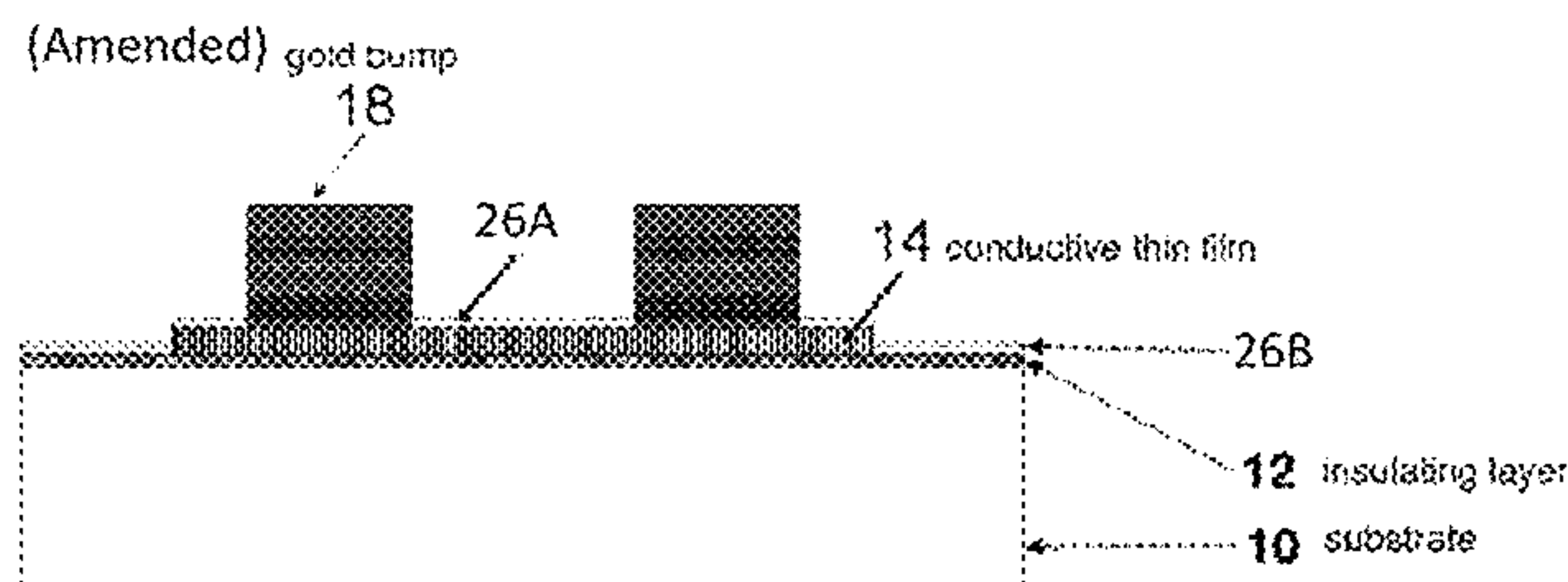
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(57) **ABSTRACT**

Disclosed is a method for manufacturing a flip chip, in which a gold typically used in a flip chip manufacturing is adhered by conductive adhesives, wherein the method comprises steps of depositing a metal seed layer on a substrate; applying and patterning a photoresist or a dry film; forming a gold bump by electroplating; patterning the seed layer; forming an insulating layer on the seed layer and upper end of the gold bump; and patterning an insulating layer. Accordingly, it is possible to manufacture a flip chip, in which electrical function between bumps can be evaluated, with less cost.

**19 Claims, 6 Drawing Sheets**

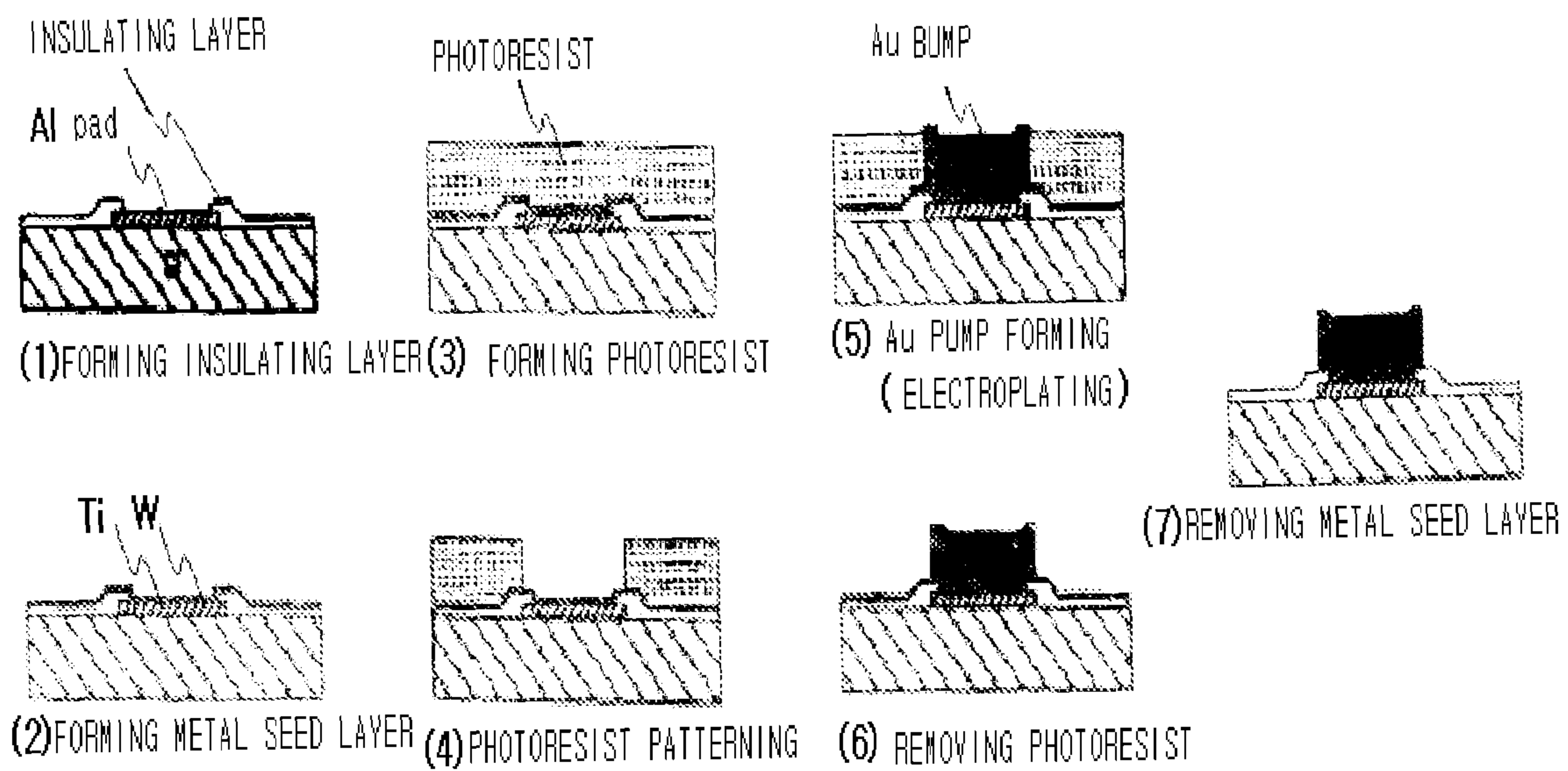


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Fig. 1



Prior Art



Fig. 2

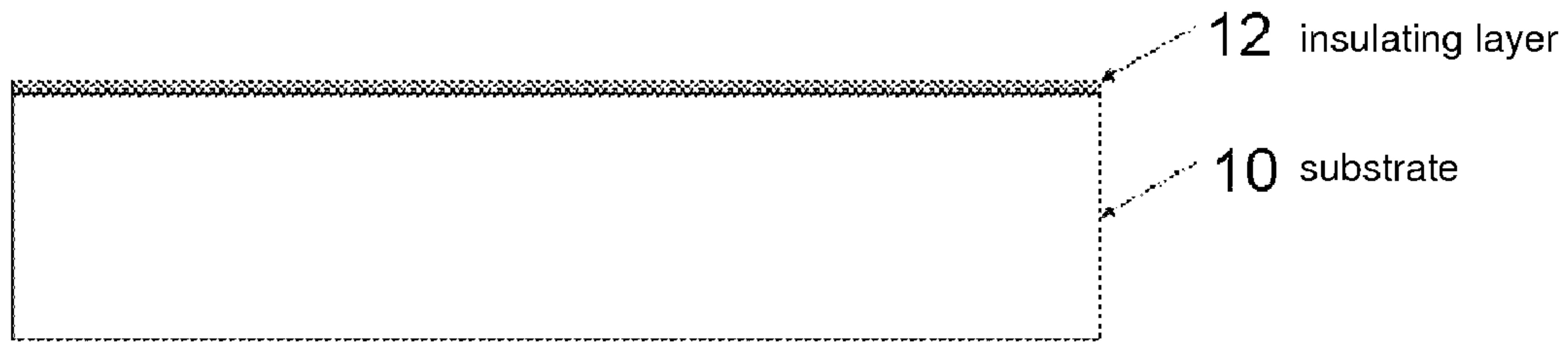


Fig. 3

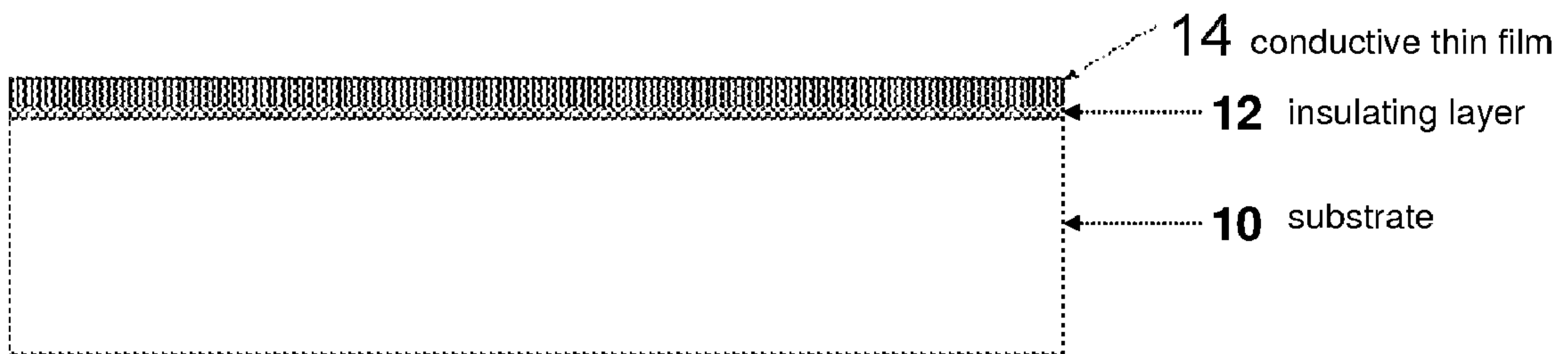


Fig. 4

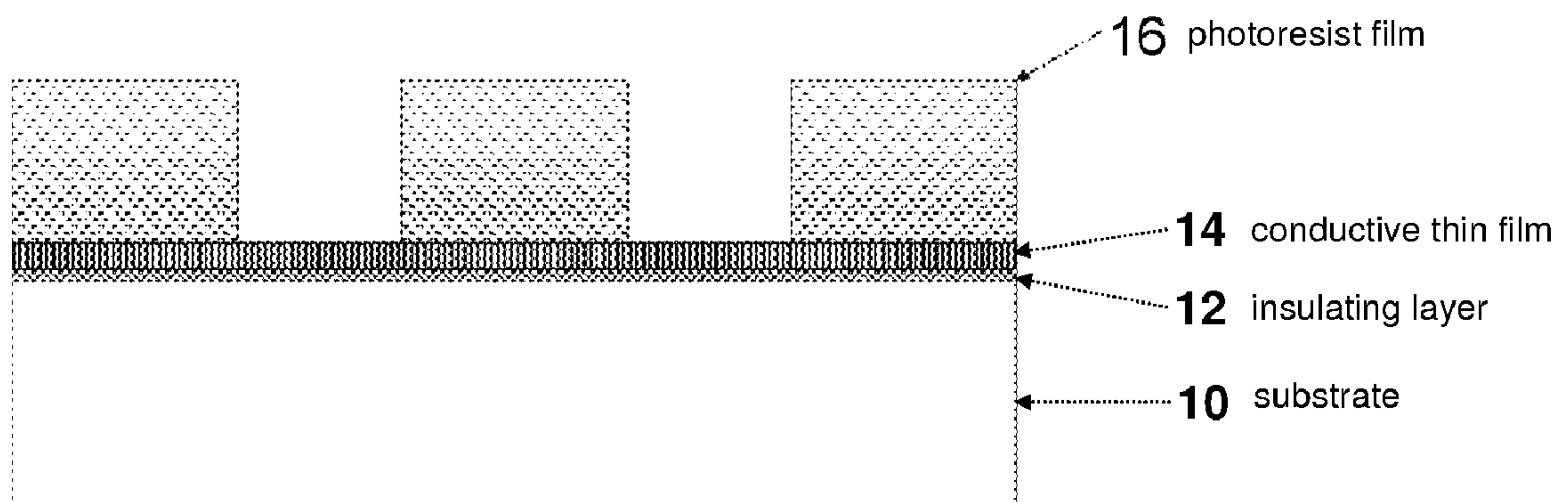


Fig. 5

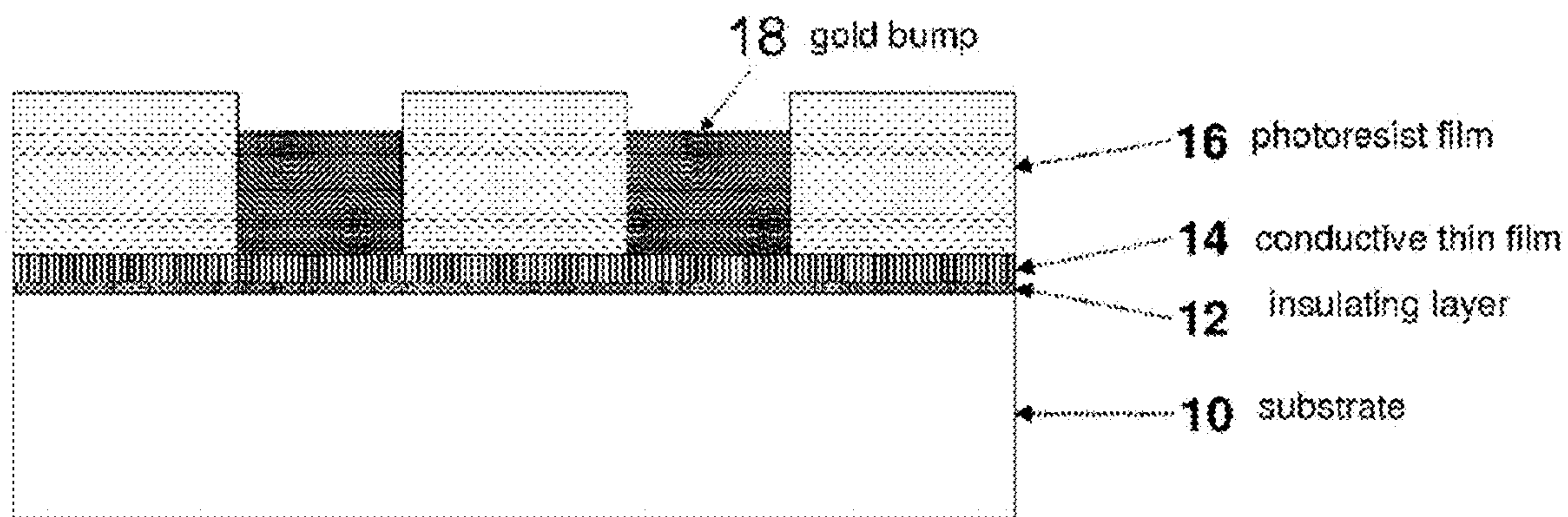


Fig. 6  
(Amended)

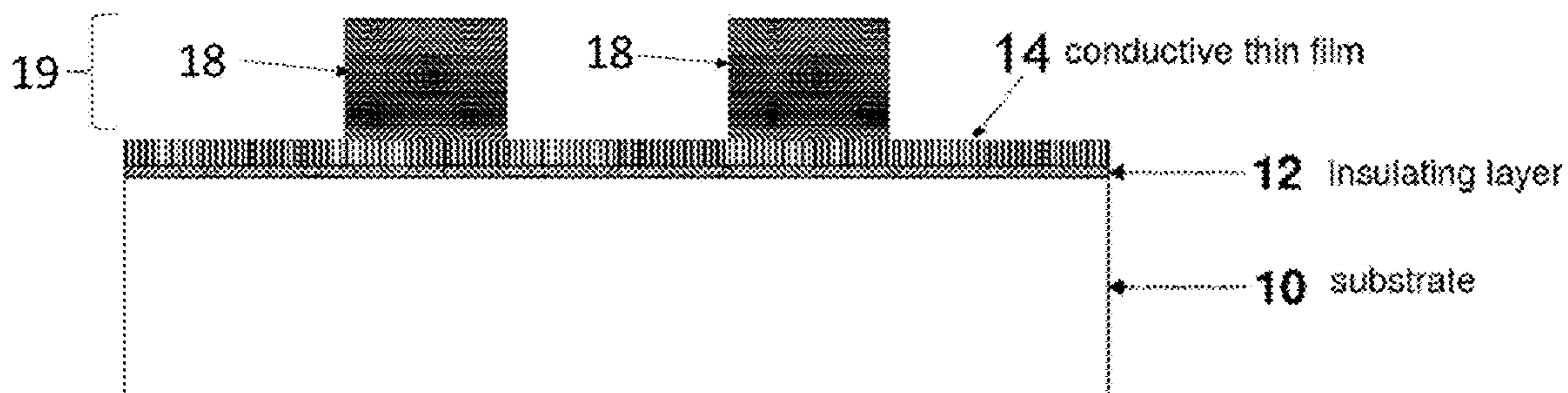


Fig. 7  
(Amended)

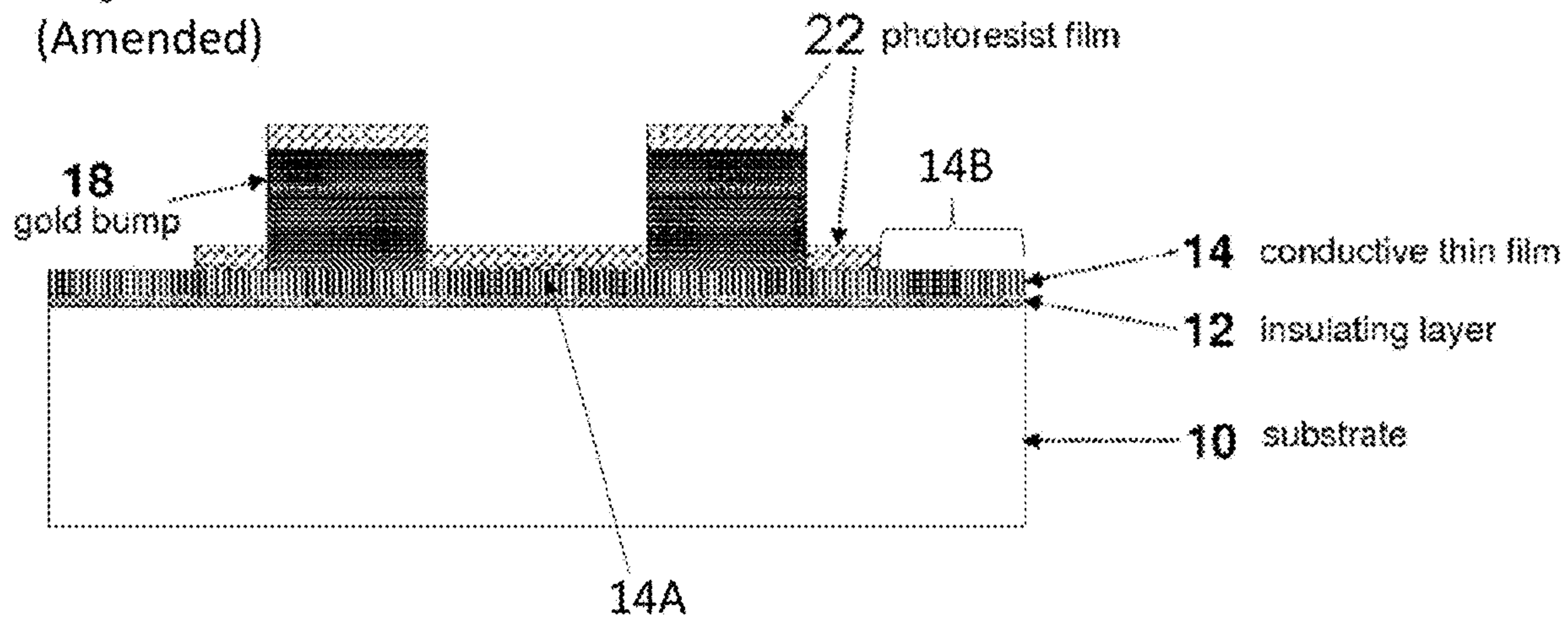


Fig. 8

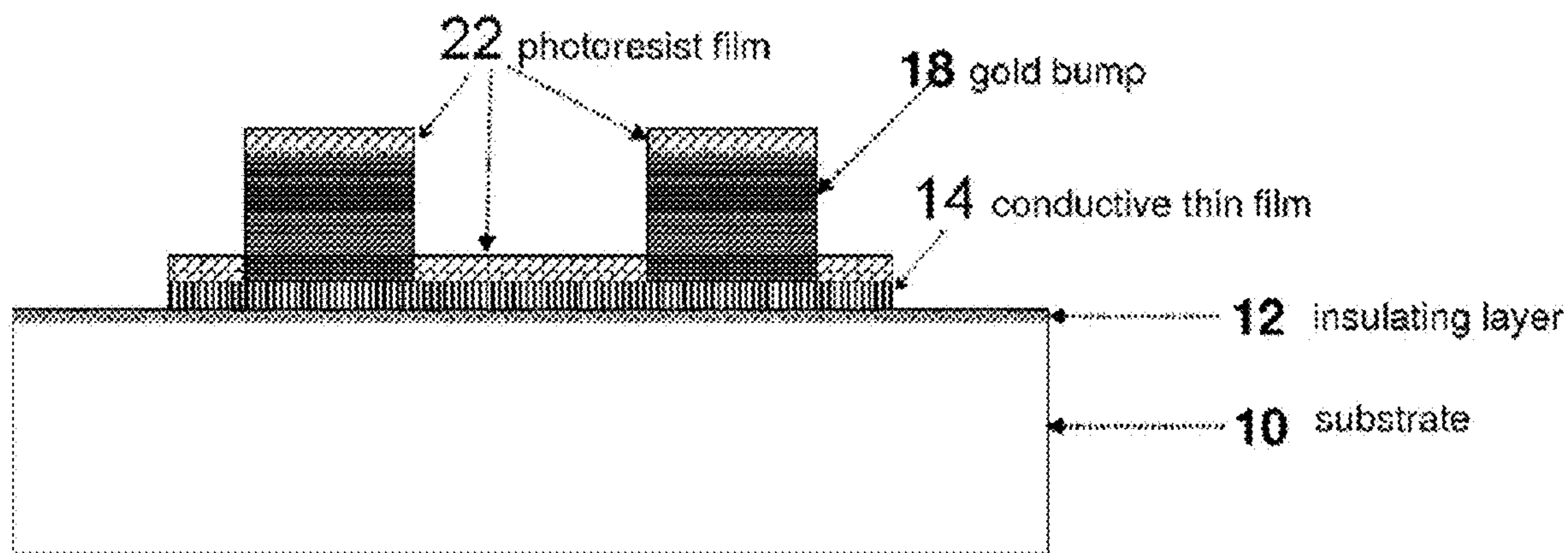


Fig. 9

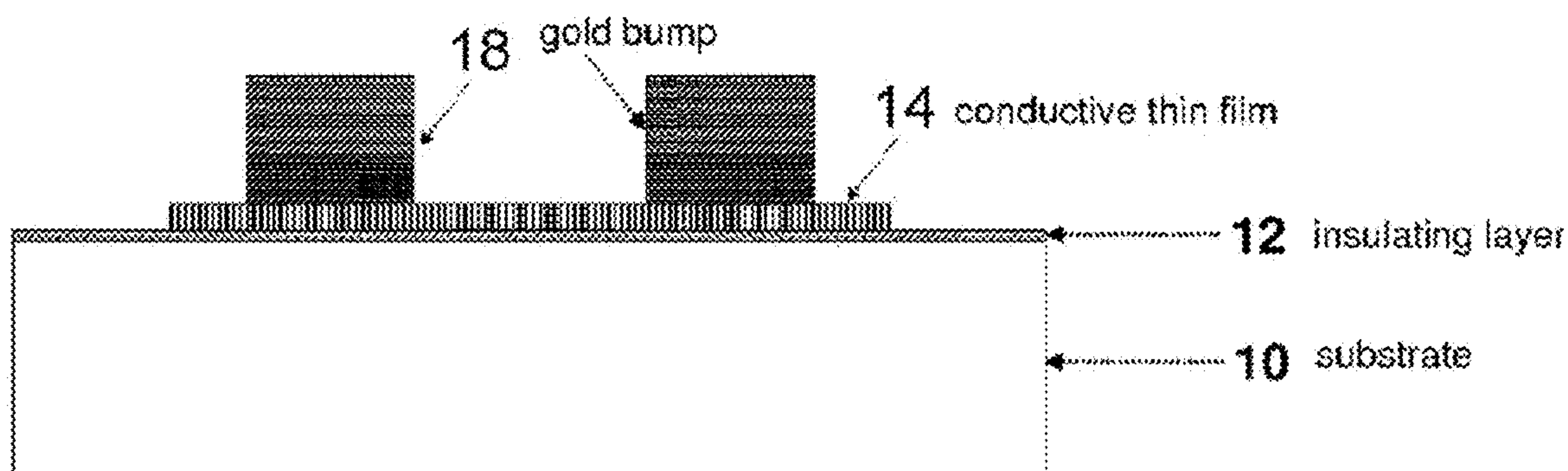


Fig. 10  
(Amended)

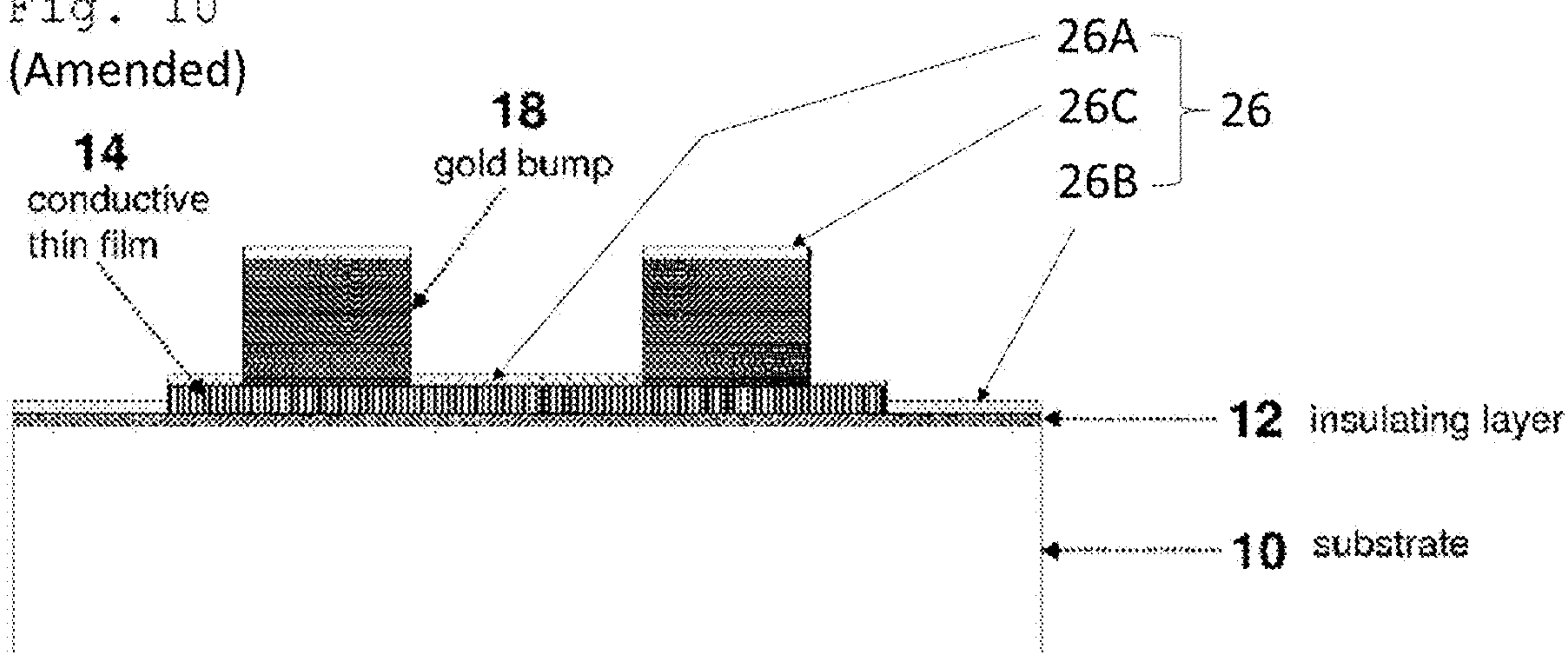




Fig. 11  
(Amended)

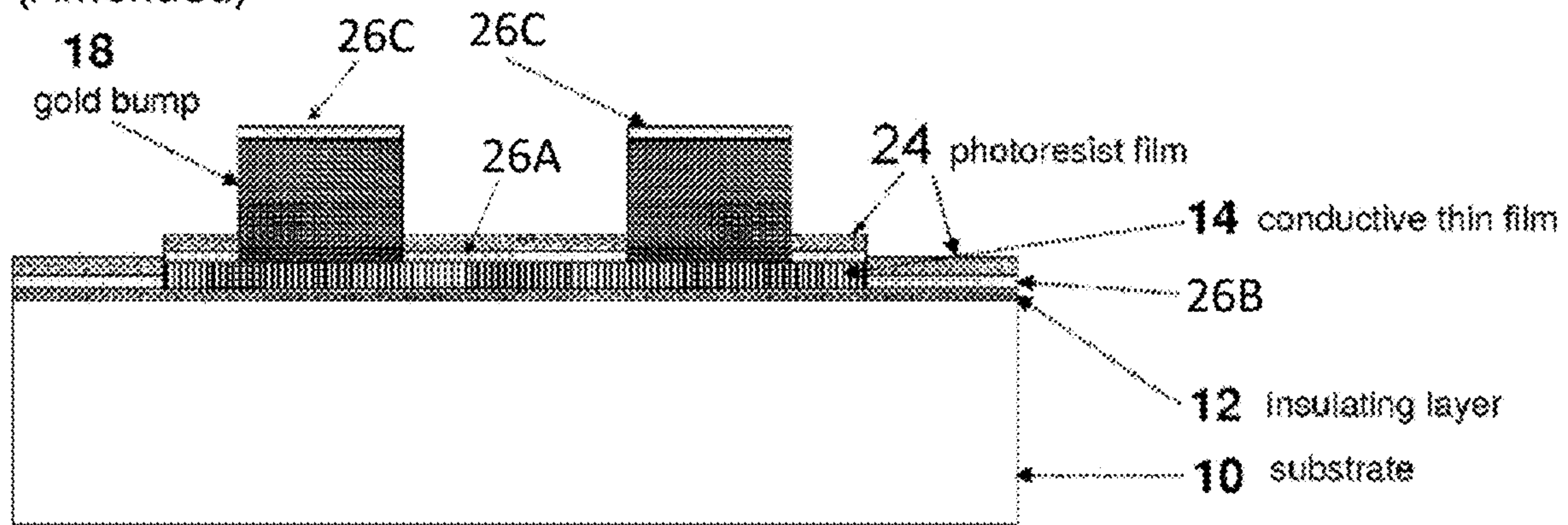


Fig. 12  
(Amended)

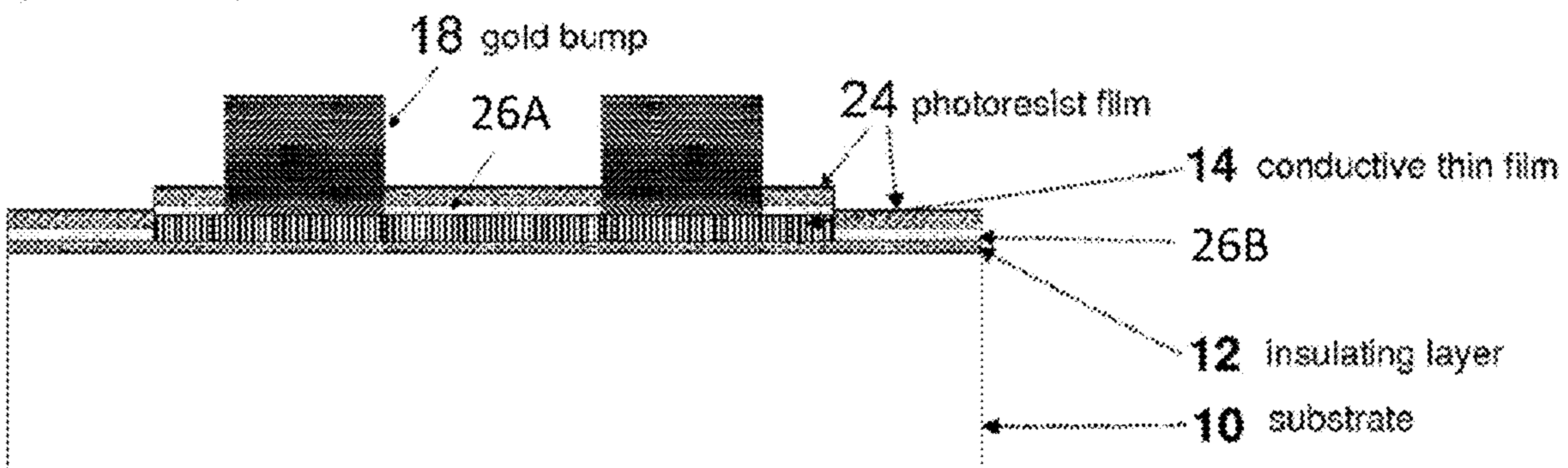


Fig. 13  
(Amended)

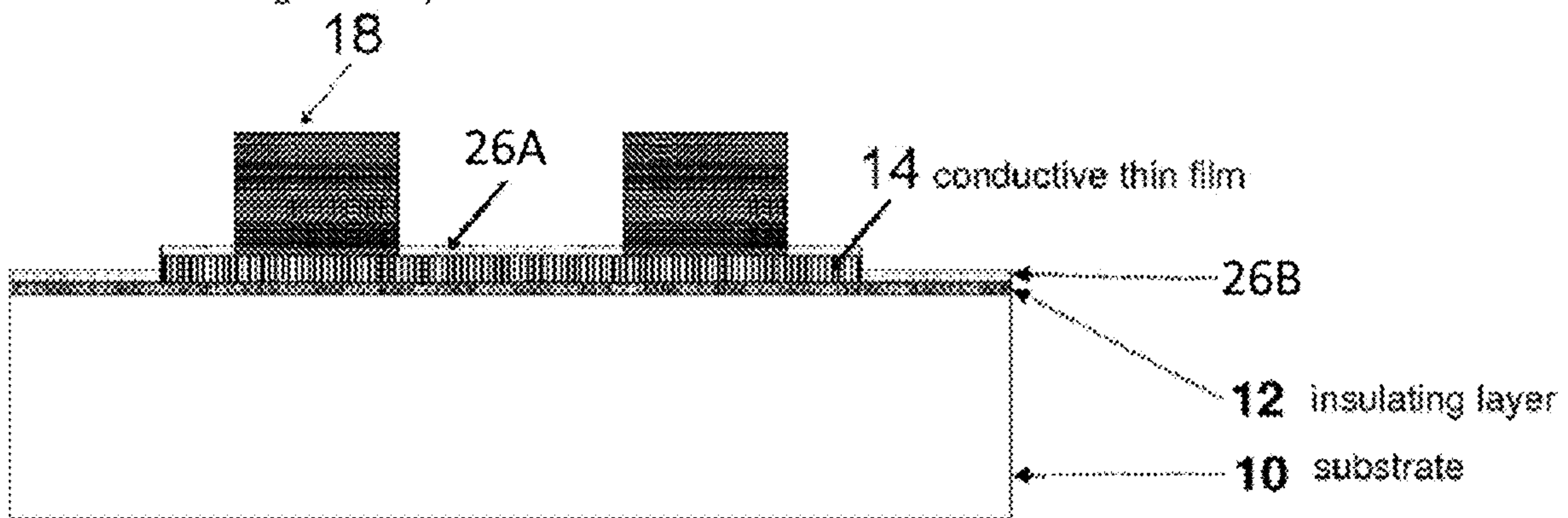
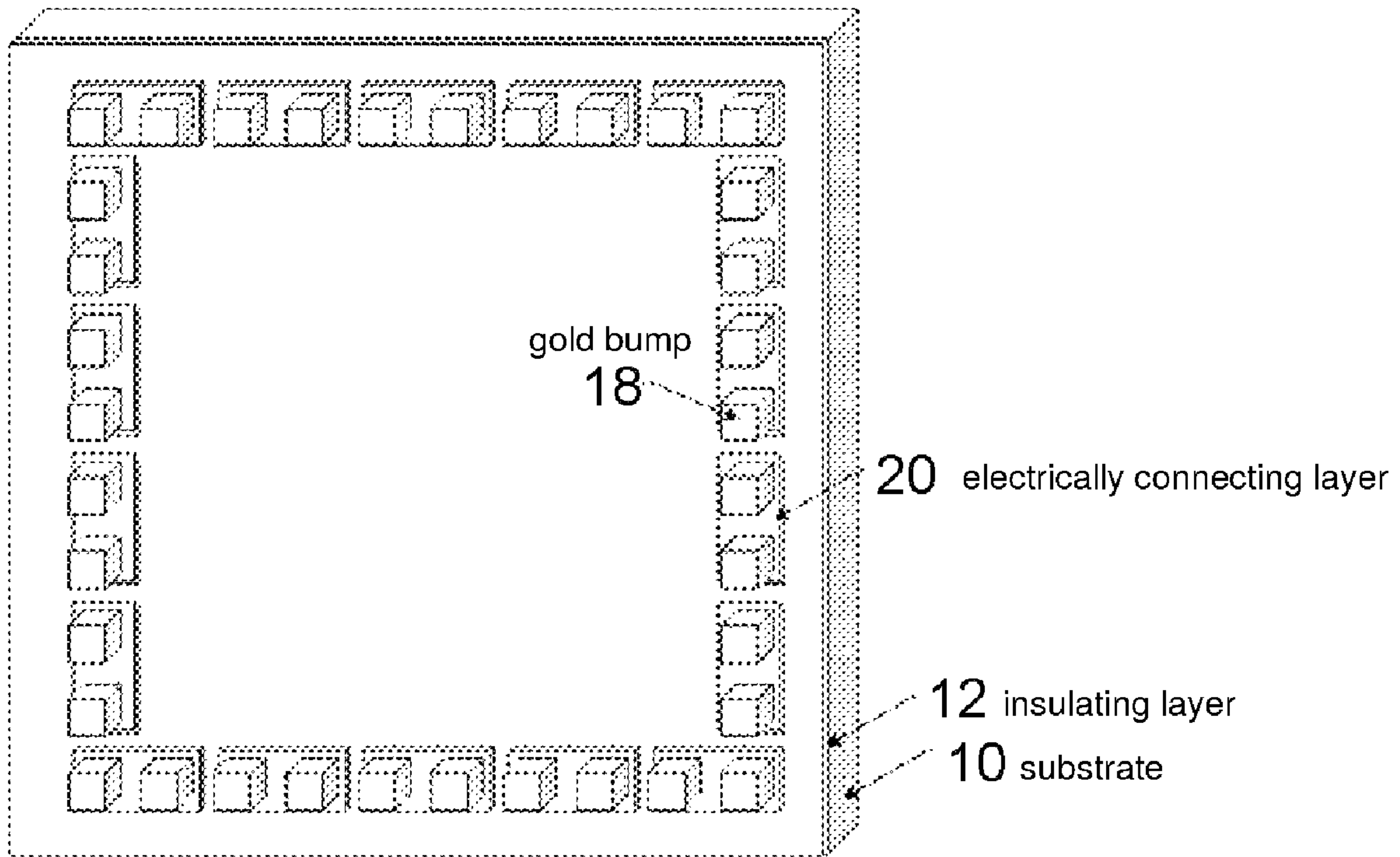


Fig. 14





## FLIP CHIP AND METHOD OF MAKING FLIP CHIP

**Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue; a claim printed with strikethrough indicates that the claim was canceled, disclaimed, or held invalid by a prior post-patent action or proceeding.**

### CROSS-REFERENCE TO RELATED REISSUE APPLICATION

*This application is a reissue application for reissue of U.S. Pat. No. 8,048,793. Reissue application Ser. No. 16/275,199, filed Feb. 13, 2019, is concurrently pending as a continuation reissue application of this application.*

### CROSS-REFERENCE TO RELATED APPLICATION

This application claims under 35 U.S.C. § 119(a) the benefit of Korean Patent Application No. 10-2007-0089905 filed Sep. 5, 2007, the entire contents of which are incorporated herein by reference.

### TECHNICAL FIELD

The present invention relates to a flip chip packaging technique, in which a chip and a substrate are electrically and mechanically connected with each other after the chip is flipped so as to allow a pad of the chip and the substrate to face each other.

### BACKGROUND ART

A flip chip package has a small size and has superior electric characteristic and reliability in comparison with a package formed by a wire bonding technique. The flip chip package is obtained by directly bonding a semiconductor chip and a printed circuit board (PCB) substrate by using a metallic bump. Gold, copper and solder, etc. are applied as the metal bump. Among these, a flip-chip using a gold bump is typically bonded to a substrate by using conductive adhesives. Different from a chip using solder bumps, such a flip chip using the gold bump has recently been popular in a display field because it doesn't include harmful element such as lead to environment and human health and has superior bonding reliability.

A method for forming a gold bump includes an electroplating method, a vacuum depositing method, and a method forming a stud bump by wire bonding. Among these, the electroplating is most advantageous due to a simple manner and the low manufacturing costs.

A research for manufacturing a gold bump of a flip chip by using this electroplating method has been actively proceeded. For example, Korean patent publication NO. 10-2006-0044929 discloses a method for improving non-uniformity of a thickness of the gold bump in such a manner that metal with a low melting point is plated on a bump formed by plating or an alloy having a dome shape is formed thereon. However, after a formation of a gold bump by electroplating, the entire metallic seed layer, except for the gold bump, is etched so that only the gold bump remains on a wafer. Therefore, there is a disadvantage in that it is impossible to evaluate the electrical characteristics of the

gold bump and a flip chip package bonded through electrical connection with the gold bump.

Korean patent registration NO. 10-0574986 discloses a method for forming a bump through an electroplating for a flip chip connection. A seed layer is formed for electroplating, and a shielding layer and a photosensitive mask are formed on the seed layer. Then, the exposed shielding layer, which has undergone a photolithography process and a developing process, is removed through dry etching, and a bump is formed on the exposed seed layer according to a plating method.

However, in the method according to the invention, the gold bump is formed by electroplating after the metal patterning and the shielding layer are formed. Therefore, it is necessary that an electrode wiring for forming the gold bump is formed when the metal pattern is formed, or a metallic seed layer for plating is formed and moved on a top of an insulating layer. Typically, the electrode wire is an unnecessary metal wire in an actual chip so that it has to be removed again after the gold bump is formed. Therefore, an additional process is necessary before and after the gold bump is formed thereby causing inconvenience.

As a similar example, a method for manufacturing a gold bump on an aluminum substrate by an electroplating method is announced [reference: John H. Lau, C. P. Wong, Ning-Cheng Lee, O. W. Ricky Lee, Electronics Manufacturing with Lead-free, Halogen-free, and Conductive-adhesive materials, 4.1-4.9 (2003)]. The process as shown in FIG. 1 is performed in the announced reference. That is, according to the method, an insulating layer is formed on an aluminum pad and the top of the pad, and a metal seed layer for electroplating of a gold bump is formed again on the upper part of the insulating layer. Then, after a formation of the gold bump, the metal seed layer applied for plating is finally removed. Similar to the disclosed invention, this method requires forming and removing process of a metal seed layer to perform electroplating, and, thus, a manufacturing procedure becomes too complicated. Also, conventionally, a mask for photolithography, which is used for plating the gold bump, and a mask for photolithography, which is used in patterning an insulating layer formed on the top of a conductive film, are separately manufactured.

The above information disclosed in this Background Art section is only for enhancement of understanding of the background of the invention and therefore it may contain information that does not form the prior art that is already known in this country to a person of ordinary skill in the art.

### SUMMARY

Therefore, the present invention has been made in view of the above-mentioned problems, and it is an object of the present invention to provide a method for evaluating the electrical connection between gold bumps and a method for improving a flip chip manufacturing process in forming a flip chip.

According to the present invention, a metal seed layer used in electroplating for forming a bump is directly used as metal pattern for forming electrical connection between bumps, so that an electrical function between bumps can be evaluated, and it is possible to omit the processes of forming and removing an electrode wire only for electroplating, which have been essential in the prior art.

According to an aspect of the present invention, there is provided a flip chip comprising: an insulating layer arranged on a substrate; a metal patterned seed layer arranged on the insulating layer; and a plate bump layer formed on the metal



3

seed layer, wherein the metal pattern is formed at a side of the plate bump, and is formed by patterning the metal seed layer.

It is preferable that the substrate is one selected from the group consisting of a silicon wafer, a compound semiconductor, quartz, glass, and ceramic material.

The insulating layer preferably comprises  $\text{SiO}_2$  and  $\text{Si}_3\text{N}_4$ .

The seed layer preferably comprises an adhesive layer and an electrode layer.

The adhesive layer preferably comprises titanium, and the electrode layer comprises copper or gold.

According to another aspect of the present invention, there is provided a flip chip manufacturing method comprising: (a) forming a seed layer on a substrate by using a conductive thin layer; (b) applying and patterning a photoresist or a dry film; (c) forming a gold bump by electroplating; (d) patterning the seed layer; (e) forming an insulating layer on the seed layer and the upper end of the gold bump; and (f) applying and patterning a photoresist or a dry film so as to pattern the insulating layer.

It is preferable that the patterning of steps (b) and (f) are performed by photolithography. Suitably, a photolithography mask used in the patterning processes of step (b) is the same as that of step (f).

It is preferable that the polarity of the photoresist or the dry film of step (b) and that of step (f) are opposite.

Also, it is preferable that the patterning process of step (d) comprises applying and patterning a photoresist or a dry film and etching a portion of the conductive thin film on which portion the photoresist or the dry film is not, so as to form a metal pattern for electrical connection between gold bumps.

In the present invention, it is possible to omit the process of forming and removing an electrode wire by directly utilizing a metal seed layer, which is used for plating, as a metal pattern for electrical connecting between bumps. Therefore, the cost of material and a process cost can be lowered. Also, it is possible to evaluate an electrical function between the bumps by using such a metal pattern so that a flip chip having high reliability can be manufactured.

Also, it is possible to unify a mask for photolithography, which is used for plating a gold bump in such a manner that the polarity of a photoresist or a dry film is opposite, and a mask for photolithography, which is used for patterning an insulating layer formed at an upper part of a conductive film, so that an additional unit manufacturing cost can be reduced. Also, a daisy chain, etc. can be formed by patterning a seed layer for electroplating so that electrical function of a flip chip package can be evaluated.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will become more apparent from the following detailed description when taken in conjunction with the drawings in which:

FIG. 1 is a schematic view illustrating a conventional procedure of manufacturing a gold bump;

FIG. 2 is a schematic view illustrating a structure where an insulating layer is formed on the upper part of a substrate;

FIG. 3 is a view illustrating a structure where a conductive thin film for plating is formed on the upper part of an insulating layer;

FIG. 4 is a view illustrating a structure where a plating wall is formed at an upper part of a conductive thin film so as to plate a gold bump, in which the plating wall is made from photoresist or a dry film;

4

FIG. 5 is a view illustrating a structure where gold is formed by electroplating so as to form a gold bump;

FIG. 6 is a view illustrating a structure where a photoresist or a dry film has been removed;

FIG. 7 is a view illustrating a structure where photolithography is performed after a photoresist or a dry film is applied so as to etch a conductive thin film;

FIG. 8 is a view illustrating a structure where a metal etching process is performed so as to pattern a conductive thin film;

FIG. 9 is a view illustrating a structure where a photoresist or a dry film is removed;

FIG. 10 is a view illustrating a structure where an insulating layer is formed;

FIG. 11 is a view illustrating a structure where photolithography is performed after a photoresist or a dry film is applied so as to etch an insulating layer;

FIG. 12 is a view illustrating a structure where an insulating layer is etched;

FIG. 13 is a view illustrating a structure where a photoresist or a dry film is removed; and

FIG. 14 is a view illustrating a flip chip manufactured through the processes of FIGS. 2 to 13.

#### DETAILED DESCRIPTION

Hereinafter reference will now be made in detail to various embodiments of the present invention, examples of which are illustrated in the accompanying drawings and described below. While the invention will be described in conjunction with exemplary embodiments, it will be understood that present description is not intended to limit the invention to those exemplary embodiments. On the contrary, the invention is intended to cover not only the exemplary embodiments, but also various alternatives, modifications, equivalents and other embodiments, which may be included within the spirit and scope of the invention as defined by the appended claims.

As shown in FIG. 2, an insulating layer 12 is formed so as to prevent electrical connection between a substrate 10 and an upper bump. Examples of the insulating layer 12 include  $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$ , and the like.

As shown in FIG. 3, a conductive thin film 14 is formed so as to be used as a metal seed layer in electroplating. At this time, the conductive thin film 14 is divided into an adhesion layer and an electric wire layer (an electrode layer). Preferably, as the adhesive layer for improving bonding force of the conductive thin film 14, titanium (Ti) may preferably be formed with a height of about 10 nm to 100 nm. As the electrode layer functioning as an electrical passage, copper (Cu) or gold (Au), etc. may suitably be formed with a height of about 100 nm to 1,000 nm.

FIG. 4 is a structure where a photoresist or a dry film 16 is applied so as to form the shape of a gold bump 18 before electroplating of the gold bump 18. Photolithography may be performed by using a mask coated with chrome for patterning. It is preferable that the thickness of the photoresist or the dry film is about 20  $\mu\text{m}$ . Moreover, the size of the gold bump can be made bigger or smaller than the size of the chip pad, when necessary.

As shown in FIG. 5, gold is electroplated so as not to exceed the height of the patterned photoresist or the dry film 16. It is preferable that the height of the gold bump is about 10 nm to 19  $\mu\text{m}$ .

As shown in FIG. 6, the photoresist or dry film 16 is removed when the gold [bump] bumps 18 [is] are com-



5

pletely formed by electroplating. *The gold bumps 18 constitute a plate bump layer 19.*

In order to achieve an electrical connection between bumps, a process of patterning the conductive thin film 14 used as a seed layer in plating is performed. As shown in FIG. 7, for example, a photoresist or dry film 22 is disposed *on the conductive thin film 14* and patterned by photolithography using a new mask *to provide a first portion 14A covered by the patterned photoresist 22 and a second portion 14B not covered by the patterned photoresist 22.*

A metal etching process is then performed so as to remove the *second portion 14B* of the conductive thin film 14, to which the photoresist or the dry film 22 is not disposed. Titanium (Ti) can be etched by hydrofluoric acid (HF) diluted solution, Au can be etched by iodination potassium (KI) solution, and Cu can be etched by ferric chloride (FeCl<sub>3</sub>) aqueous solution. Through this etching process, the shape in which the conductive thin film 14 is patterned can be obtained, as shown in FIG. 8.

FIG. 9 shows a structure where the photoresist or dry film 22 used for etching of the conductive thin film 14 has been removed.

As shown in FIG. 10, an insulating layer 26 is formed so as to protect the thin conductive film 14 and achieve insulation from external environment. *The insulating layer 26 includes insulating layers 26A, 26B and 26C that are formed on different surfaces.* SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>, etc. may suitably be used as the insulating layer 26.

As shown in FIG. 11, a photoresist and dry film 24 is disposed *on the insulating layer 26*, and patterning is performed through the photolithography process, *which provides the patterned photoresist film 24 on the insulating layers 26A and 26B but not on the insulating layer 26C*, so as to achieve patterning of the insulating layer 26. Suitably, the mask used in this photolithography may be the same as the mask used in the process of FIG. 4, except that the polarity of the photoresist or dry film 24 is changed. For example, in a case where the photoresist or dry film 16 used in FIG. 4 is positive, the photoresist or dry film 24 used in FIG. 11 is negative so as to achieve a patterning having an opposite shape. Through such a process, two processes can be performed by using one mask.

As shown in FIG. 12, the insulating layer [26] 26C is etched so as to expose the surface of the gold bump 18 *while the insulating layers 26A and 26B are maintained under the patterned photoresist film 24.*

As shown in FIG. 13, the photoresist or dry film 24 is removed, which was applied to etch the insulating layer 26C.

FIG. 14 is a top view of a flip-chip manufactured through the processes of FIGS. 2 to 13, which includes thereon the insulating layer 12 formed between the substrate 10 and the conductive film 14, the gold bump 18 formed by electroplating, and the electrically connecting layer (*metal patterned seed layer*) 20 formed by patterning the conductive thin film used as the seed layer in electroplating.

The present flip chips and manufacturing methods thereof can be applied to various areas. For example, it is possible to bond a core memory chip and a non-memory chip and stack a horizontal multi chip and a vertical multi chip, in the fields of high-end electronic machines, including, but not limited to, portable multimedia machines, such as cellular phones, and flat panel machines.

The invention has been described in detail with reference to preferred embodiments thereof. However, it will be appreciated by those skilled in the art that changes may be made in these embodiments without departing from the

6

principles and spirit of the invention, the scope of which is defined in the appended claims and their equivalents.

The invention claimed is:

1. A flip chip comprising:

an insulating layer arranged on and directly contacted with a substrate, wherein the insulating layer covers the substrate;

a metal patterned seed layer arranged on the insulating layer and directly contacted with the insulating layer; and

a plate bump layer formed on the metal patterned seed layer, wherein [one] two or more plate bumps are formed;

wherein a metal pattern is formed at a side of the two or more plate [bump,] bumps, and is formed by patterning a precursor of the metal patterned seed layer; wherein the metal pattern is at least a part of the metal patterned seed layer, and forms electrical connection between the plate bumps.

2. The flip chip as claimed in claim 1, wherein the substrate is one selected from the group consisting of a silicon wafer, a compound semiconductor, quartz, glass, and ceramic material.

3. The flip chip as claimed in claim 1, wherein the insulating layer comprises SiO<sub>2</sub> or Si<sub>3</sub>N<sub>4</sub>.

4. The flip chip as claimed in claim 1, wherein the seed layer comprises an adhesive layer and an electrode layer.

5. The flip chip as claimed in claim 4, wherein the adhesive layer comprises titanium, and the electrode layer comprises copper or gold.

[6. A flip chip manufacturing method comprising:

(a) forming a seed layer on a substrate by using a conductive thin layer;

(b) applying and patterning a photoresist or a dry film;

(c) forming gold bumps by electroplating;

(d) patterning the seed layer to form a metal pattern;

(e) forming an insulating layer on the seed layer and the upper end of the gold bumps; and

(f) applying and patterning a photoresist or a dry film so as to pattern the insulating layer;

wherein the metal pattern forms electrical connection between the gold bumps, and the polarity of the photoresist or a dry film in step b) is opposite to the polarity of photoresist or a dry film in step f).]

[7. The flip chip manufacturing method as claimed in claim 6, wherein the patterning of steps (b) and (f) are performed by photolithography.]

[8. The flip chip manufacturing method as claimed in claim 7, wherein a photolithography mask used in the patterning processes of step (b) is the same as that of step (f).]

[9. The flip chip manufacturing method as claimed in claim 6, wherein the patterning process of step (d) comprises applying and patterning a photoresist or a dry film and etching a portion of the conductive thin film on which portion the photoresist or the dry film is not, so as to form a metal pattern for electrical connection between gold bumps.]

10. A flip chip comprising:

a first insulating layer arranged on and directly contacted with a substrate, wherein the first insulating layer covers the substrate,

a metal patterned seed layer arranged on the first insulating layer and comprising a conductive metal directly contacted with the first insulating layer,

a plate bump layer formed on the metal patterned seed layer, wherein two or more plate bumps are formed with



7

a horizontal gap therebetween and constitute the plate bump layer over the first insulating layer, wherein a metal pattern is formed at a side of the two or more plate bumps and is formed by patterning a precursor of the metal patterned seed layer, wherein the metal pattern is at least a part of the metal patterned seed layer and forms electrical connection between the two or more plate bumps, and

a second insulating layer formed over and covering the metal pattern such that the electrical connection electrically connecting between the two or more plate bumps is interposed between the first insulating layer and the second insulating layer, wherein the second insulating layer does not cover top surfaces of the two or more plate bumps.

11. The flip chip of claim 10, wherein the flip chip further comprises a third insulating layer that covers a portion of the first insulating layer on which the conductive metal of the metal pattern is not provided such that the third insulating layer directly contacts the first insulating layer without a conductive layer interposed therebetween.

12. The flip chip of claim 10, wherein the two or more plate bumps are made of at least one material selected from the group consisting of gold, copper and solder.

13. The flip chip of claim 10, wherein each of the first and second insulating layers comprises at least one selected from the group consisting of  $\text{SiO}_2$  and  $\text{Si}_3\text{N}_4$ .

14. The flip chip of claim 10, wherein the metal patterned seed layer comprises an adhesive sublayer and an electrode sublayer that is thicker than the adhesive sublayer.

15. The flip chip of claim 14, wherein the adhesive layer comprises titanium, and the electrode layer comprises copper or gold.

16. A method of making the flip chip of claim 10, the method comprising:

forming the first insulating layer over the substrate;  
forming a conductive metal on the first insulating layer to provide a metal seed layer that is the precursor of the metal patterned seed layer;

forming a photoresist layer over the metal seed layer;  
selectively patterning the photoresist layer to provide two or more openings that expose the metal seed layer through the photoresist layer;

electroplating to grow two or more plate bumps from the metal seed layer exposed through the two or more openings, in which the metal seed layer works as an electroplating electrode for the two or more plate bumps so that an electrode wire does not have to be formed for each of the two or more plate bumps;

subsequent to electroplating, removing the photoresist layer to provide an intermediate structure comprising the substrate, the first insulating layer over the substrate, the metal seed layer over the first insulating layer and the two or more plate bumps that are on the metal seed layer with a horizontal gap therebetween;  
subsequent to removing the photoresist layer, patterning the metal seed layer to form an intermediate device with the metal pattern comprising the electrical connection connecting between the two or more plate bumps, wherein patterning the metal seed layer removes a portion of the conductive metal to expose the portion of the first insulating layer;

forming an insulating material over the intermediate device to provide the second insulating layer over the metal pattern and a third insulating layer over the portion of the first insulating layer, wherein forming the

8

insulating material further forms a fourth insulating layer over the two or more plate bumps; and  
removing the fourth insulating layer to expose a top portion of each of the two or more plate bumps.

17. The flip chip of claim 1, wherein the insulating layer is referred to as a first insulating layer,

wherein the two or more plate bumps constitute the plate bump layer over the first insulating layer,  
wherein the metal pattern is formed at a side of the two or more plate bumps when viewing in a direction from top of the plate bumps toward the substrate,  
wherein the metal pattern is at least a part of the metal patterned seed layer and forms electrical connection between the two or more plate bumps,

wherein the flip chip further comprises a second insulating layer formed over and covering the metal pattern such that the metal pattern comprising the electrical connection between the two or more plate bumps is interposed between the first insulating layer and the second insulating layer.

18. The flip chip of claim 17, wherein the flip chip further comprises a third insulating layer formed over a portion of the first insulating layer on which the metal pattern is not provided such that no conductive layer is interposed between the first insulating layer and the third insulating layer, wherein the second insulating layer and the third insulating layer are formed together but at different levels from the substrate.

19. The flip chip of claim 17, wherein the two or more plate bumps are made of at least one material selected from the group consisting of gold, copper and solder.

20. The flip chip of claim 17, wherein each of the first and second insulating layers comprises at least one selected from the group consisting of  $\text{SiO}_2$  and  $\text{Si}_3\text{N}_4$ .

21. The flip chip of claim 17, wherein the metal patterned seed layer comprises an adhesive layer and an electrode layer.

22. The flip chip of claim 21, wherein the adhesive layer comprises titanium, and the electrode layer comprises copper or gold.

23. A method of making the flip chip of claim 17, the method comprising:

forming the first insulating layer over the substrate;  
forming a conductive metal on the first insulating layer to provide a metal seed layer that is the precursor of the metal patterned seed layer;

forming a photoresist layer over the metal seed layer;  
selectively patterning the photoresist layer to provide two or more openings that expose the metal seed layer through the photoresist layer;

electroplating to form two or more plate bumps from the metal seed layer exposed through the two or more openings, in which the metal seed layer works as an electroplating electrode for the two or more plate bumps so that an electrode wire does not have to be formed for each of the two or more plate bumps that would need to be removed after electroplating;

subsequent to electroplating, removing the photoresist layer to provide an intermediate structure comprising the substrate, the first insulating layer over the substrate, the metal seed layer over the first insulating layer and the two or more plate bumps that are on the metal seed layer with a horizontal gap therebetween;  
subsequent to removing the photoresist layer, patterning the metal seed layer to form an intermediate device with the metal pattern comprising the electrical connection between the two or more plate bumps, wherein

*patterning the metal seed layer removes a portion of the  
conductive metal to expose the portion of the first  
insulating layer;*  
*forming an insulating material over the intermediate  
device to provide the second insulating layer over the 5  
metal pattern and a third insulating layer over the  
portion of the first insulating layer, wherein forming the  
insulating material further forms a fourth insulating  
layer over the two or more plate bumps; and*  
*removing the fourth insulating layer to expose a top 10  
portion of each of the two or more plate bumps.*

\* \* \* \* \*