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Camacho et al.

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(54) SEMICONDUCTOR DEVICE AND METHOD OF FORMING PIP WITH INNER KNOWN GOOD DIE INTERCONNECTED WITH CONDUCTIVE BUMPS

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(21) Appl. No.: **15/058,005**

(22) Filed: **Mar. 1, 2016**

Related U.S. Patent Documents

Reissue of:

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	Issued:	**Nov. 11, 2014**
	Appl. No.:	**13/606,451**
	Filed:	**Sep. 7, 2012**

U.S. Applications:

(60) Division of application No. 12/635,631, filed on Dec. 10, 2009, now Pat. No. 8,283,209, which is a

(Continued)

(51) **Int. Cl.**

H01L 23/24	(2006.01)
H01L 23/28	(2006.01)

(Continued)

(52) **U.S. Cl.**

CPC ***H01L 23/49548*** (2013.01); ***H01L 21/4832*** (2013.01); ***H01L 21/568*** (2013.01);

(Continued)

(58) **Field of Classification Search**

CPC H01L 23/28; H01L 23/48; H01L 25/11; H01L 23/24

See application file for complete search history.

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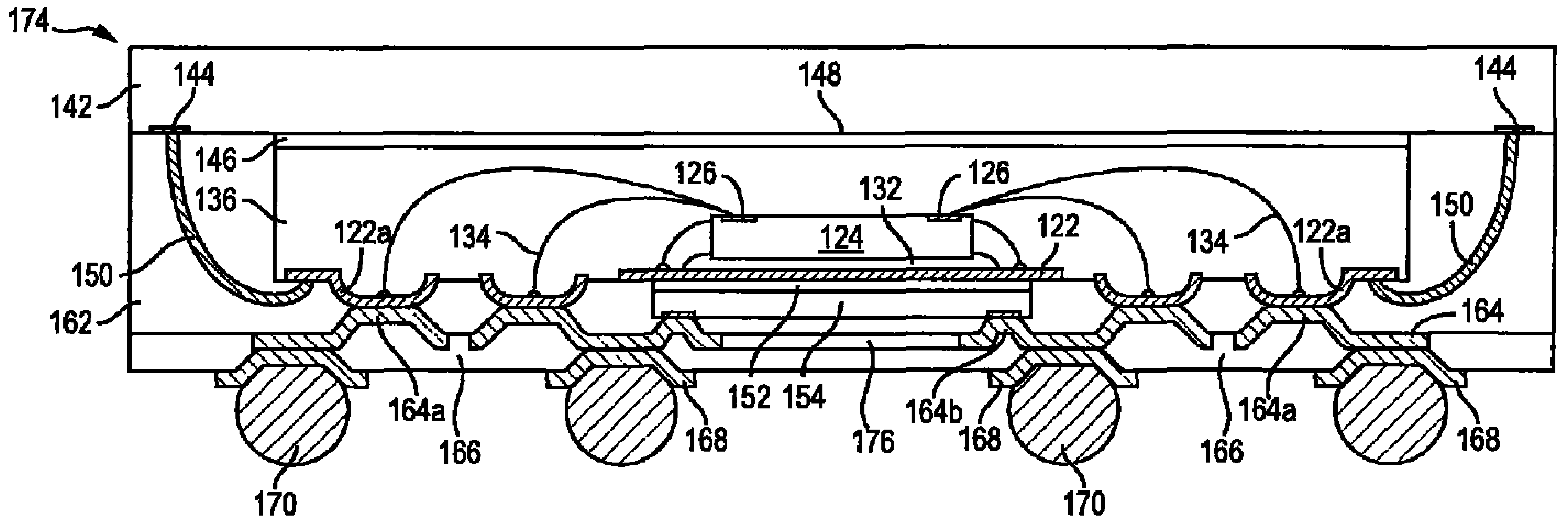
Primary Examiner — Leonardo Andujar

(74) *Attorney, Agent, or Firm* — Robert D. Atkins; Patent Law Group: Atkins and Associates, P.C.

(57) ABSTRACT

A PiP semiconductor device has an inner known good semiconductor package. In the semiconductor package, a first via is formed in a temporary carrier. A first conductive layer is formed over the carrier and into the first via. The first conductive layer in the first via forms a conductive bump. A first semiconductor die is mounted to the first conductive layer. A first encapsulant is deposited over the first die and carrier. The semiconductor package is mounted to a substrate. A second semiconductor die is mounted to the first conductive layer opposite the first die. A second encapsulant is deposited over the second die and semiconductor package. A second via is formed in the second encapsulant to expose the conductive bump. A second conductive layer is formed over the second encapsulant and into the second via. The second conductive layer is electrically connected to the second die.

13 Claims, 13 Drawing Sheets



Related U.S. Application Data

continuation-in-part of application No. 12/136,768, filed on Jun. 10, 2008, now Pat. No. 7,977,779.

(51) **Int. Cl.**

H01L 23/495	(2006.01)
H01L 21/48	(2006.01)
H01L 21/56	(2006.01)
H01L 21/683	(2006.01)
H01L 23/31	(2006.01)
H01L 23/498	(2006.01)
H01L 23/538	(2006.01)
H01L 23/00	(2006.01)
H01L 25/065	(2006.01)
H01L 25/00	(2006.01)
H01L 25/03	(2006.01)
H01L 25/10	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 21/6835*** (2013.01); ***H01L 23/3135*** (2013.01); ***H01L 23/49816*** (2013.01); ***H01L 23/5389*** (2013.01); ***H01L 24/24*** (2013.01); ***H01L 24/29*** (2013.01); ***H01L 25/03*** (2013.01); ***H01L 25/0657*** (2013.01); ***H01L 25/105*** (2013.01); ***H01L 25/50*** (2013.01); *H01L 23/3128* (2013.01); *H01L 23/49541* (2013.01); *H01L 24/48* (2013.01); *H01L 24/73* (2013.01); *H01L 2224/04105* (2013.01); *H01L 2224/12105* (2013.01); *H01L 2224/16* (2013.01); *H01L 2224/16225* (2013.01); *H01L 2224/24226* (2013.01); *H01L 2224/2919* (2013.01); *H01L 2224/2929* (2013.01); *H01L 2224/29111* (2013.01); *H01L 2224/29299* (2013.01); *H01L 2224/32225* (2013.01); *H01L 2224/32245* (2013.01); *H01L 2224/48091* (2013.01); *H01L 2224/48227* (2013.01); *H01L 2224/48247* (2013.01); *H01L 2224/73204* (2013.01); *H01L 2224/73265* (2013.01); *H01L 2224/73267* (2013.01); *H01L 2224/83411* (2013.01); *H01L 2224/83424* (2013.01); *H01L 2224/83439* (2013.01); *H01L 2224/83444* (2013.01); *H01L 2224/83447* (2013.01); *H01L 2224/83455* (2013.01); *H01L 2224/85001* (2013.01); *H01L 2225/0651* (2013.01); *H01L 2225/06524* (2013.01); *H01L 2225/1023* (2013.01); *H01L 2225/1058* (2013.01); *H01L 2924/00013* (2013.01); *H01L 2924/00014* (2013.01); *H01L 2924/0103* (2013.01); *H01L 2924/01004* (2013.01); *H01L 2924/014* (2013.01); *H01L 2924/01005* (2013.01); *H01L 2924/01006* (2013.01); *H01L 2924/01013* (2013.01); *H01L 2924/01023* (2013.01); *H01L 2924/01024* (2013.01); *H01L 2924/01029* (2013.01); *H01L 2924/0132* (2013.01); *H01L 2924/01046* (2013.01); *H01L 2924/01047* (2013.01); *H01L 2924/01049* (2013.01); *H01L 2924/01073* (2013.01); *H01L 2924/01074* (2013.01); *H01L 2924/01078* (2013.01); *H01L 2924/01079* (2013.01); *H01L 2924/01082* (2013.01); *H01L 2924/01322* (2013.01); *H01L 2924/04941* (2013.01); *H01L 2924/09701* (2013.01); *H01L 2924/12041* (2013.01); *H01L 2924/12042* (2013.01); *H01L 2924/1306* (2013.01); *H01L 2924/13091* (2013.01); *H01L 2924/14* (2013.01); *H01L 2924/1433* (2013.01); *H01L 2924/15311* (2013.01); *H01L 2924/15747* (2013.01); *H01L 2924/16195* (2013.01); *H01L 2924/181* (2013.01); *H01L 2924/19041* (2013.01); *H01L 2924/19105* (2013.01); *H01L 2924/19107* (2013.01); *H01L 2924/3025* (2013.01); *H01L 2924/30105* (2013.01)

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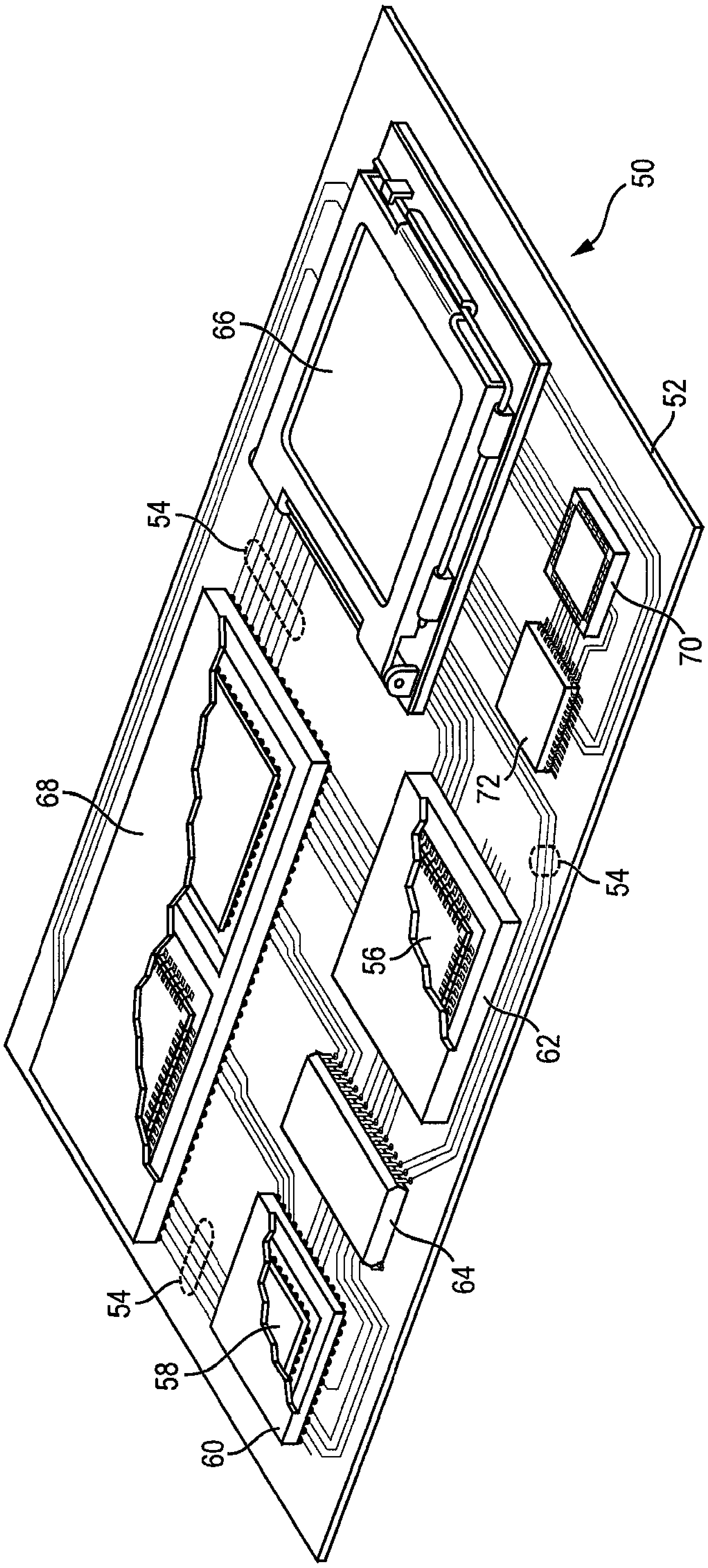

FIG. 1

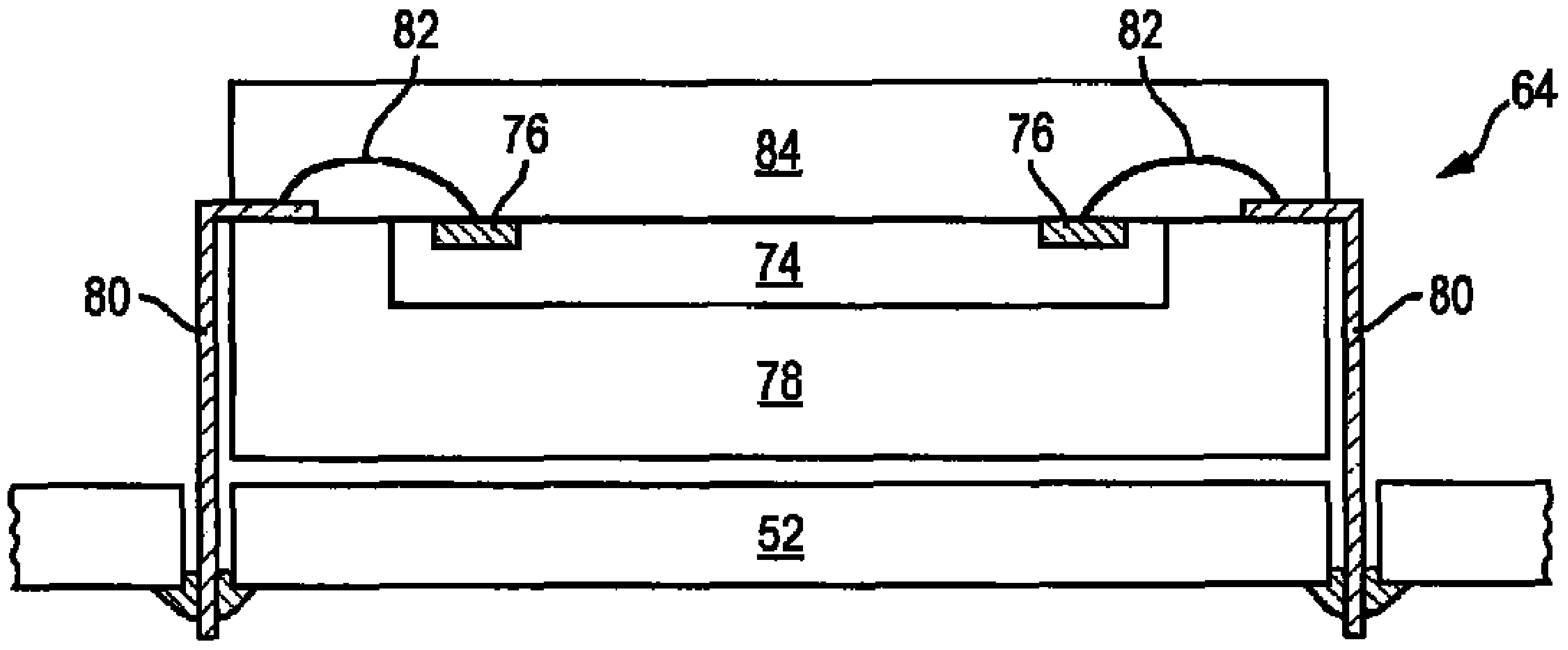

FIG. 2a

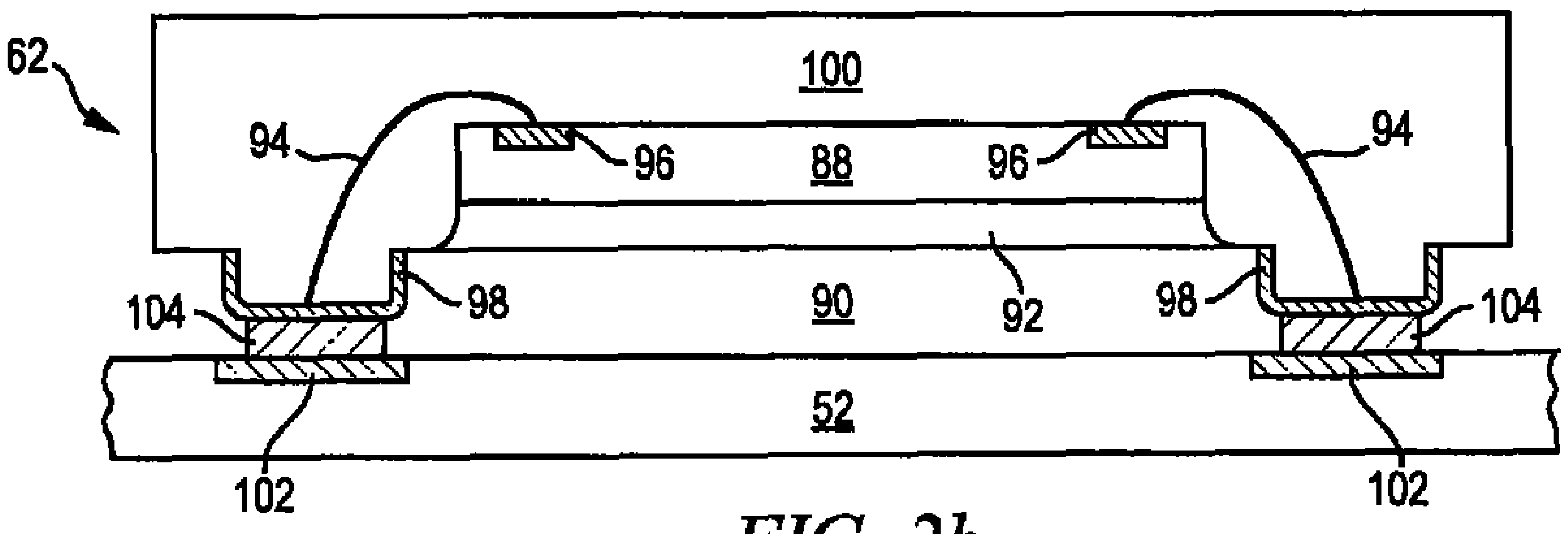

FIG. 2b

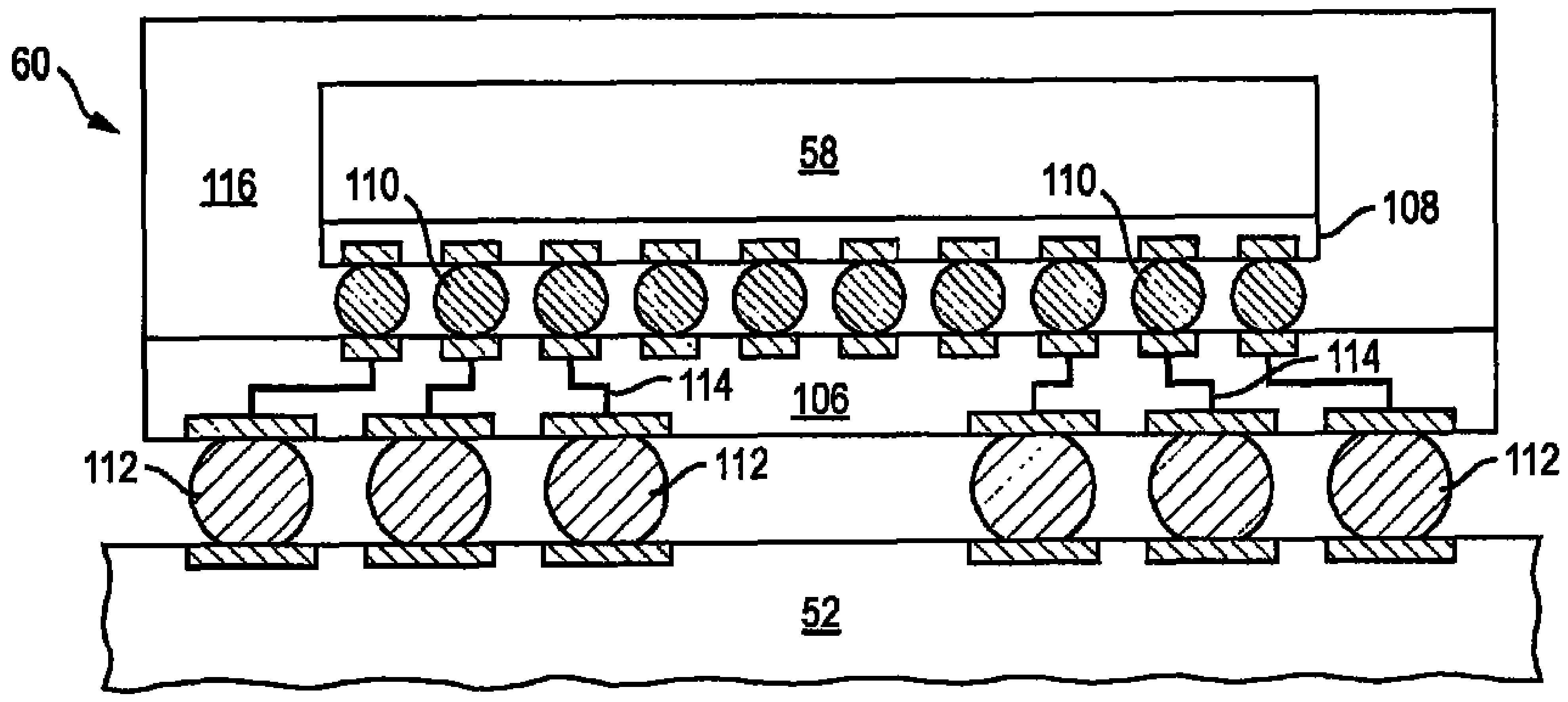

FIG. 2c

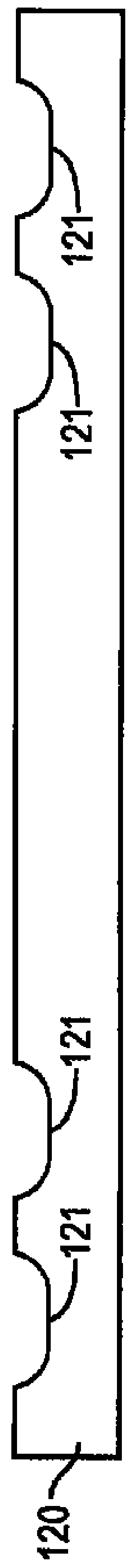

FIG. 3a

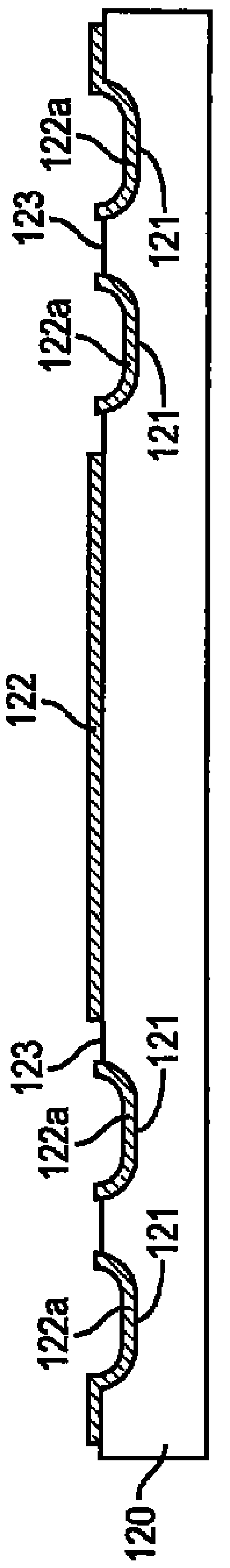

FIG. 3b

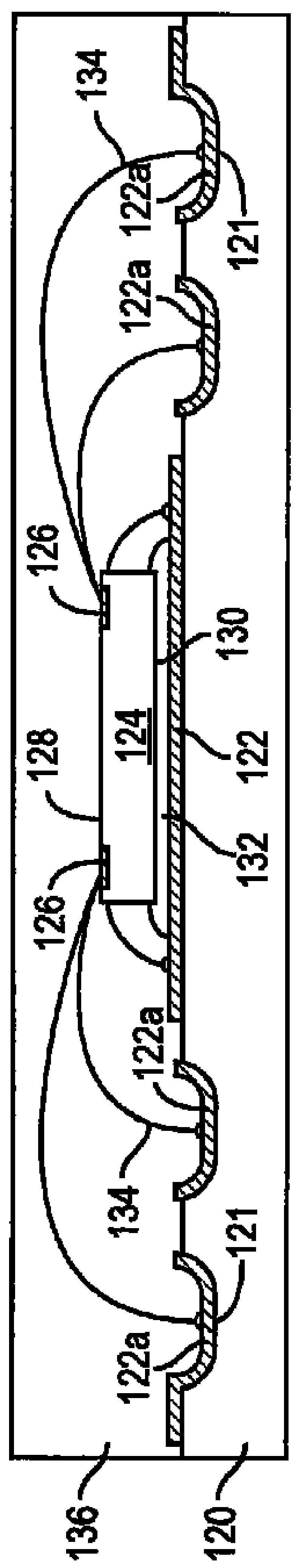

FIG. 3c

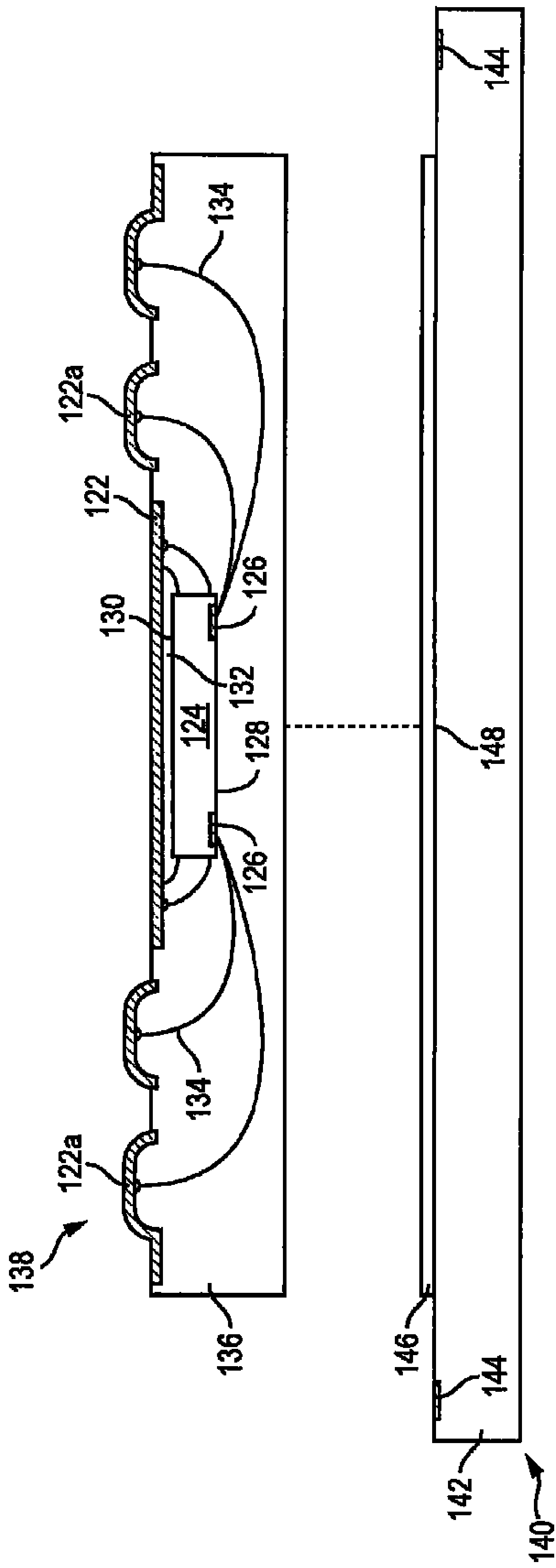
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FIG. 3d

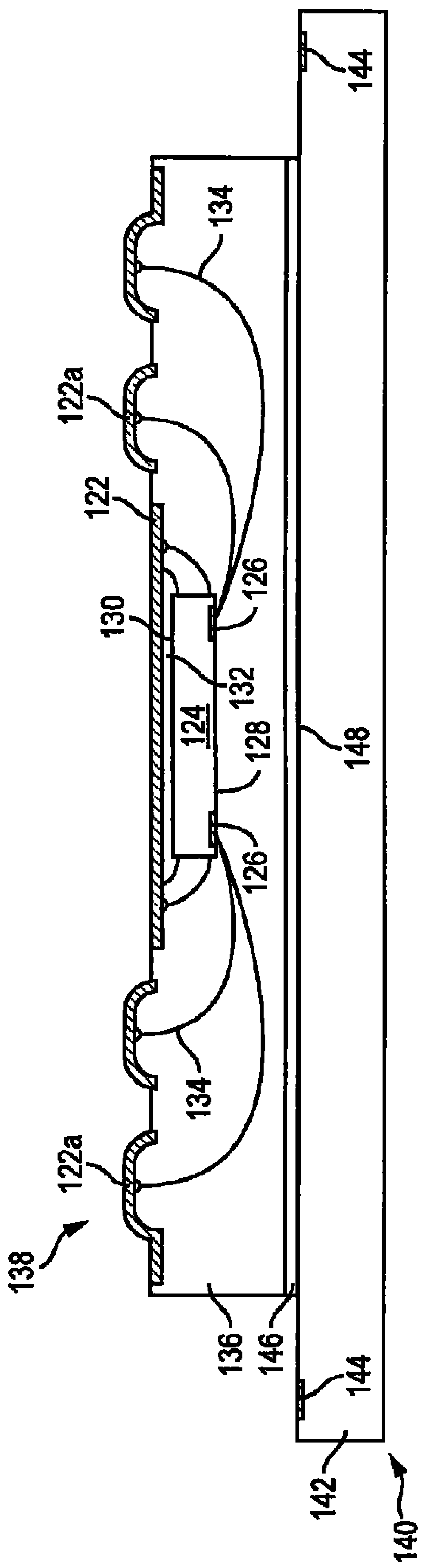
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FIG. 3e

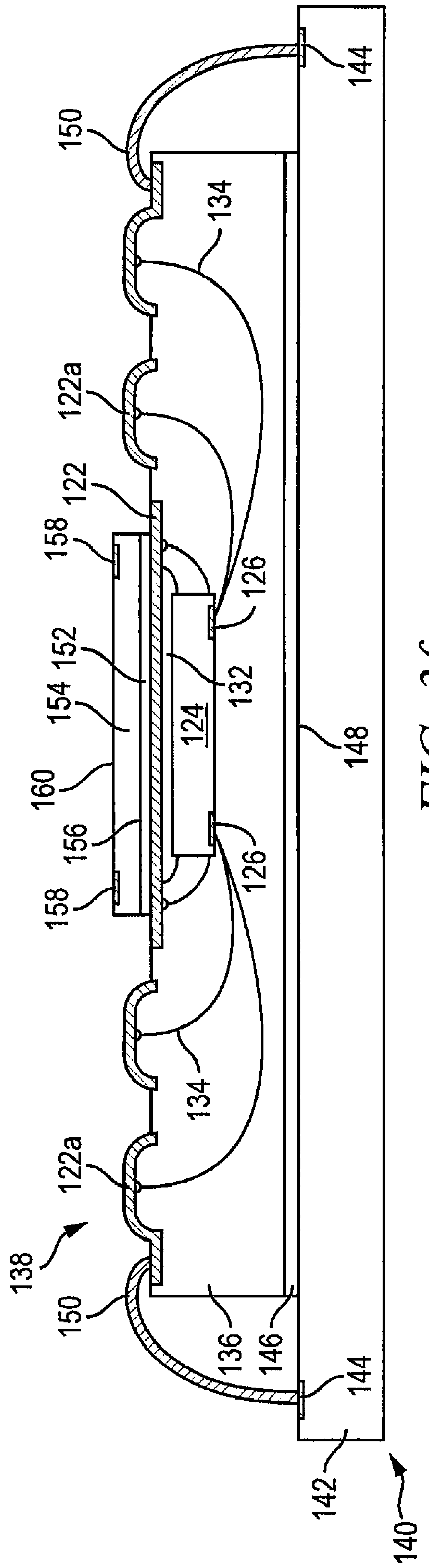
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FIG. 3f

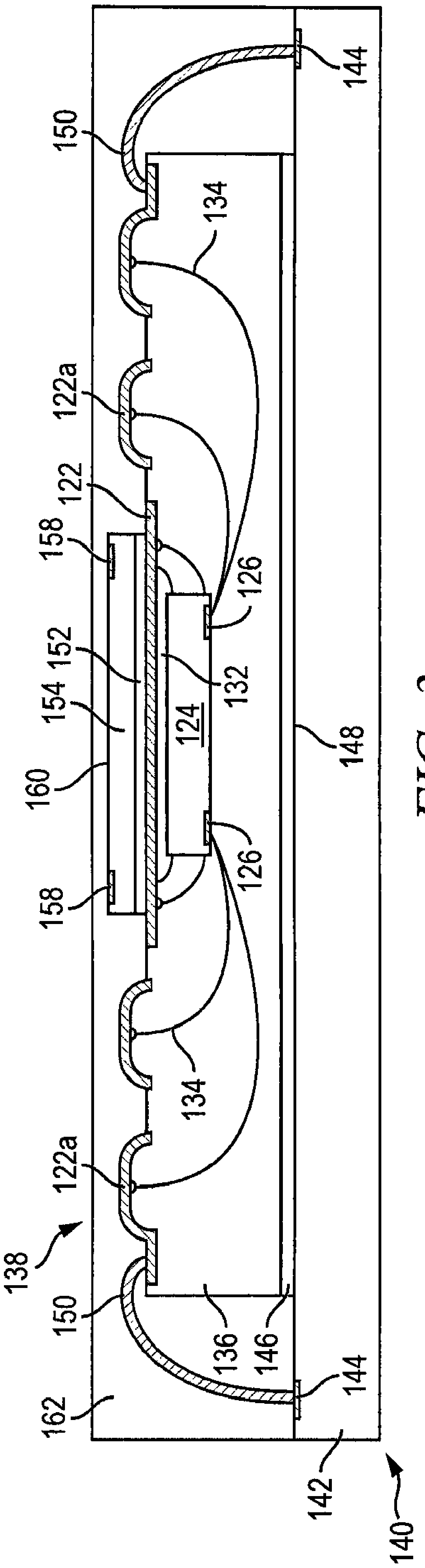
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FIG. 3g

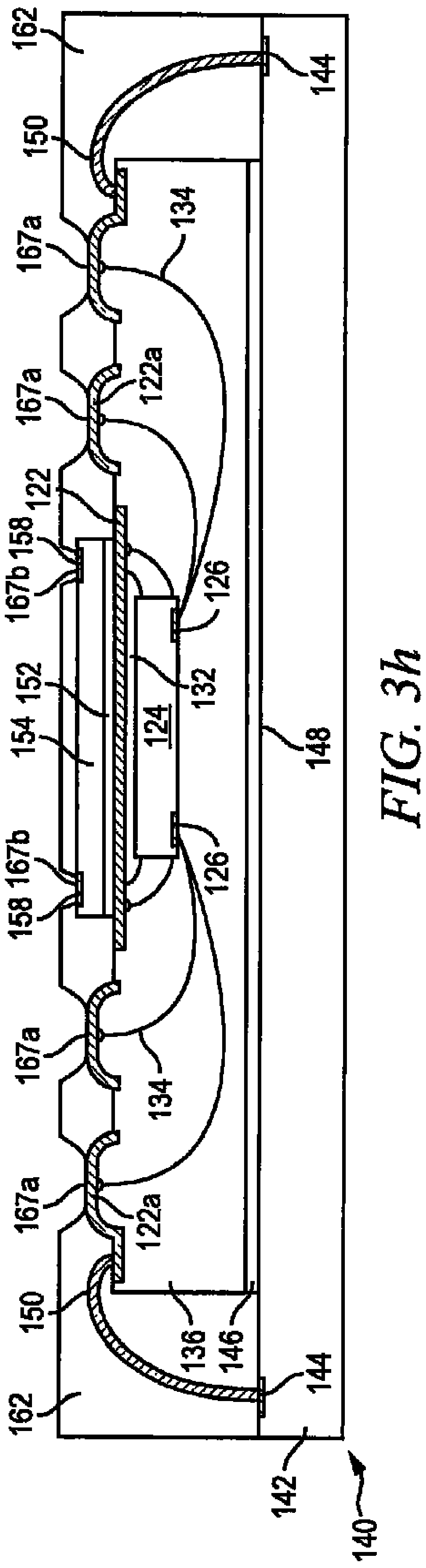
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FIG. 3h

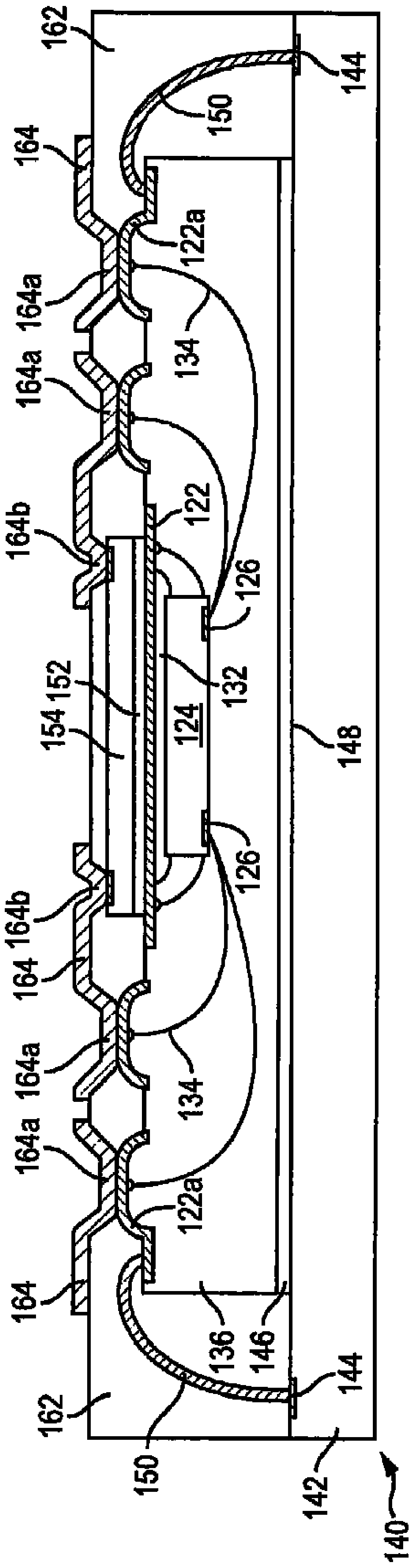
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FIG. 3i

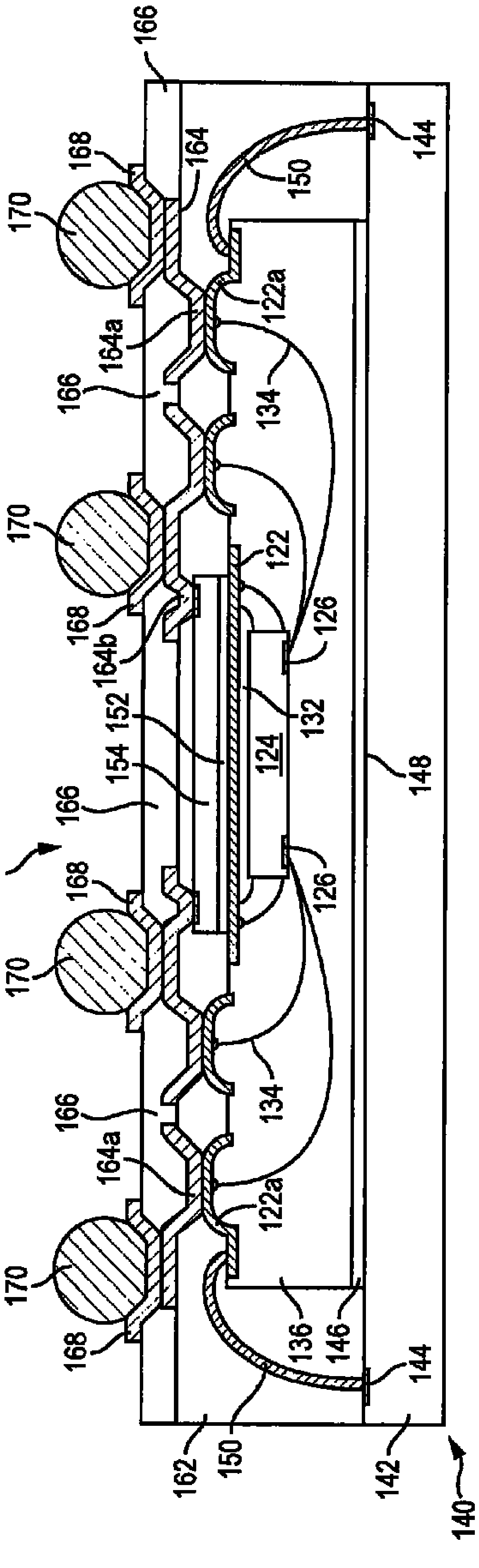
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FIG. 3j

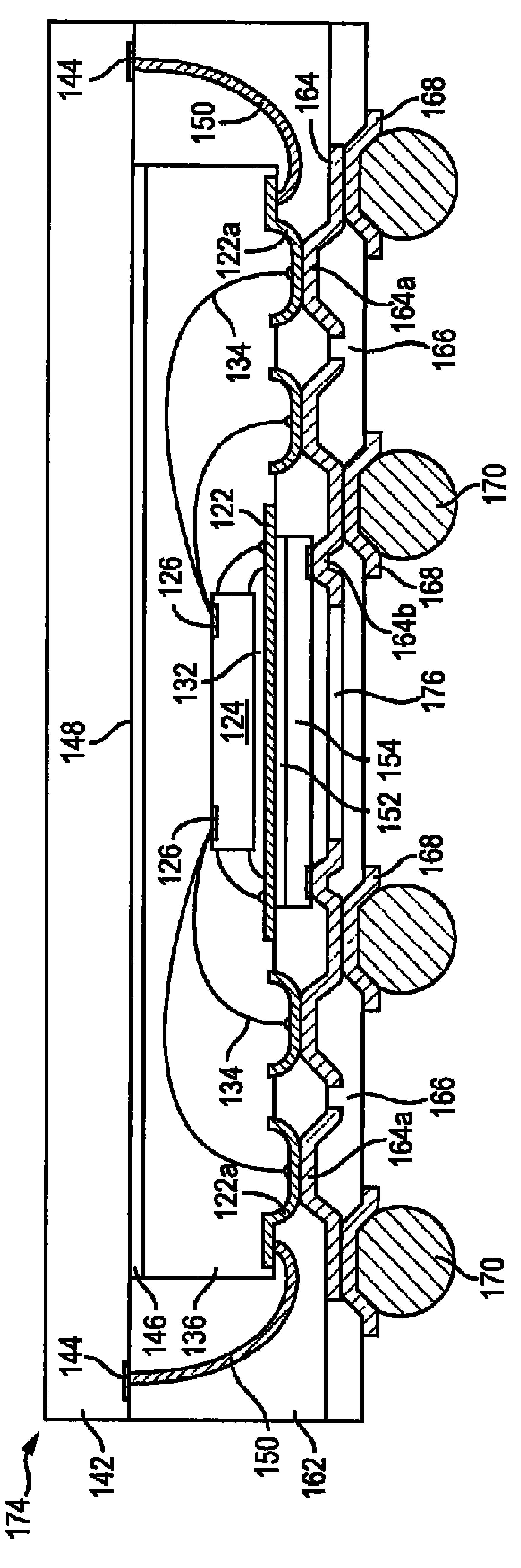
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FIG. 4

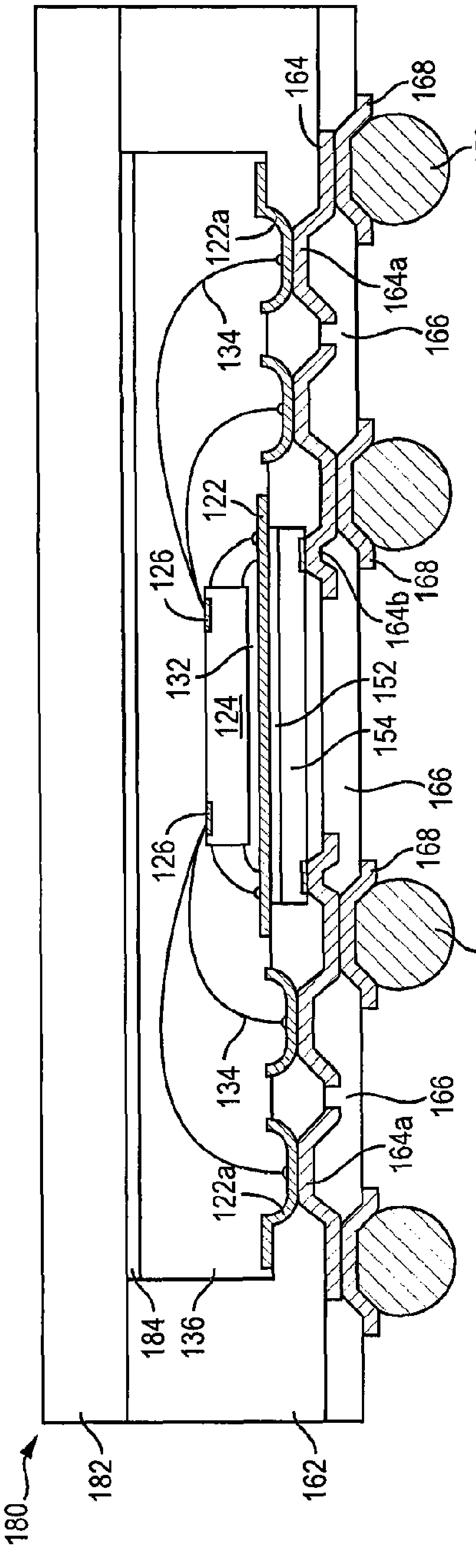
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FIG. 5

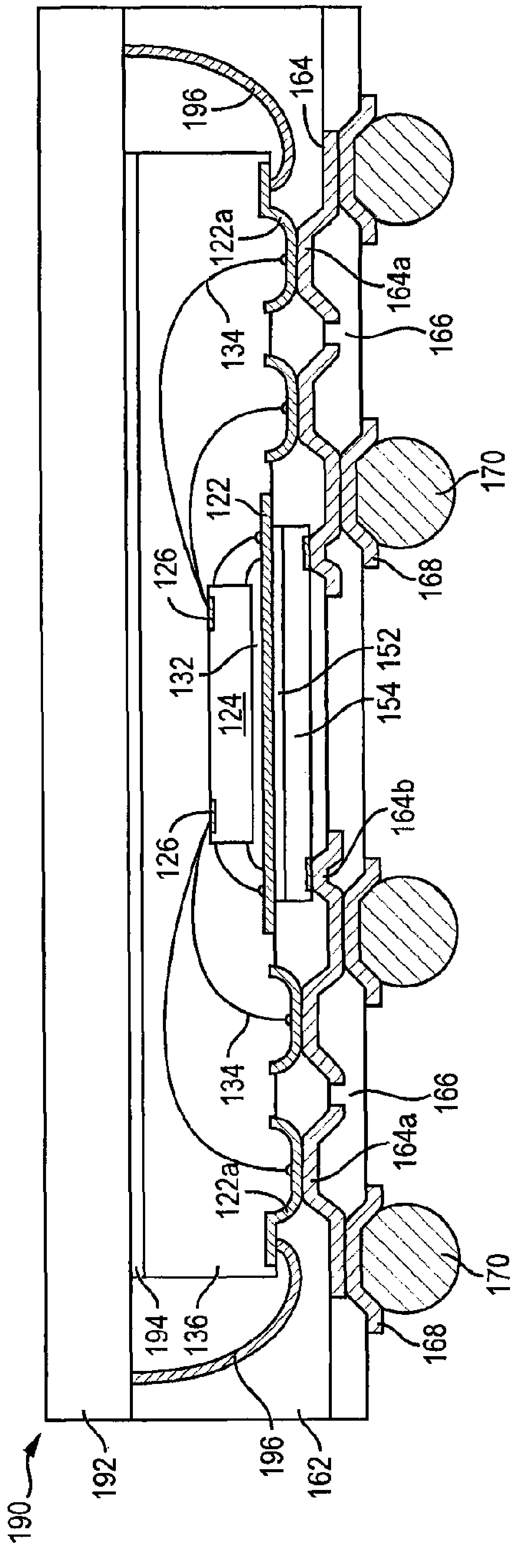
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FIG. 6

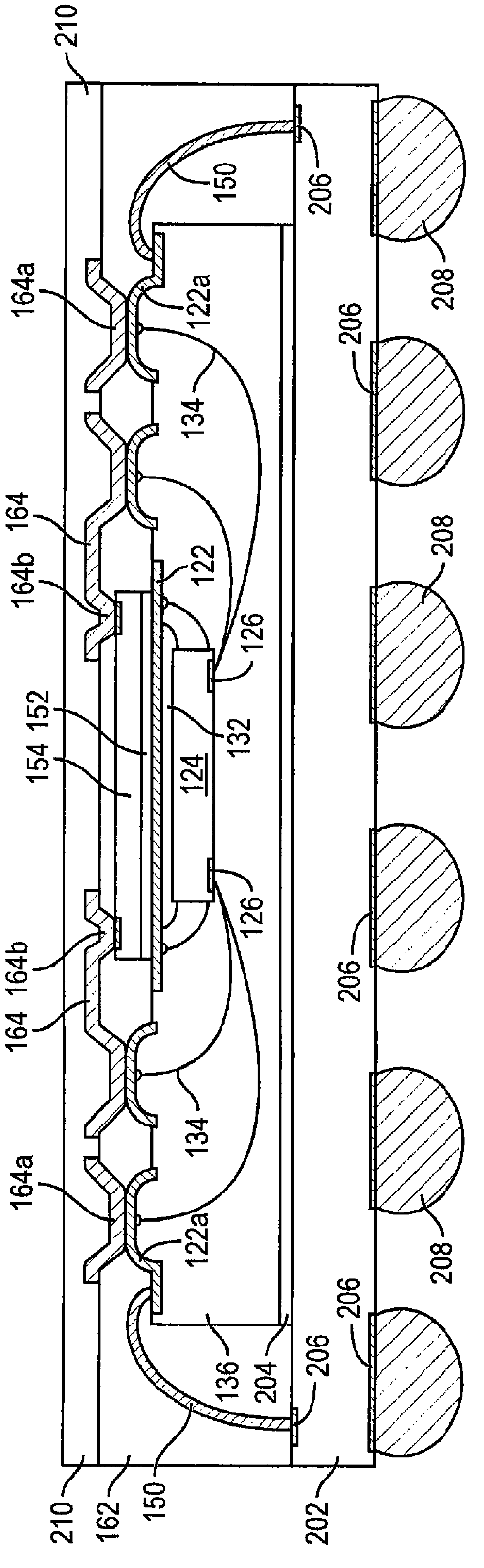
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FIG. 7a

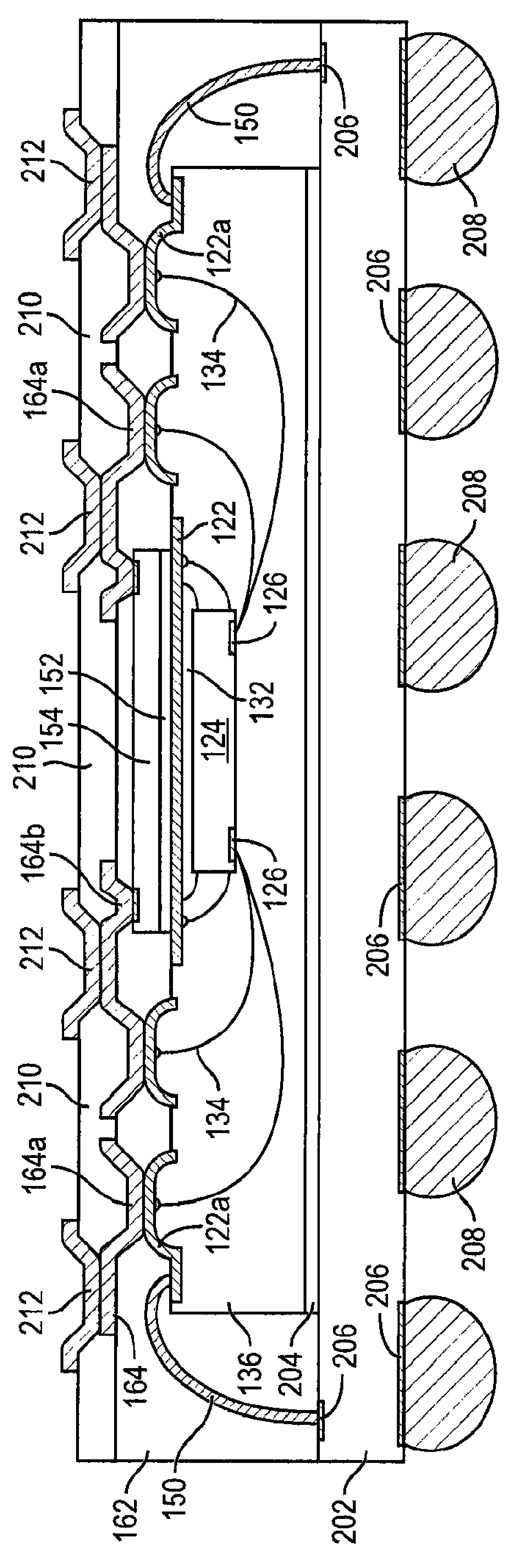
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FIG. 7b

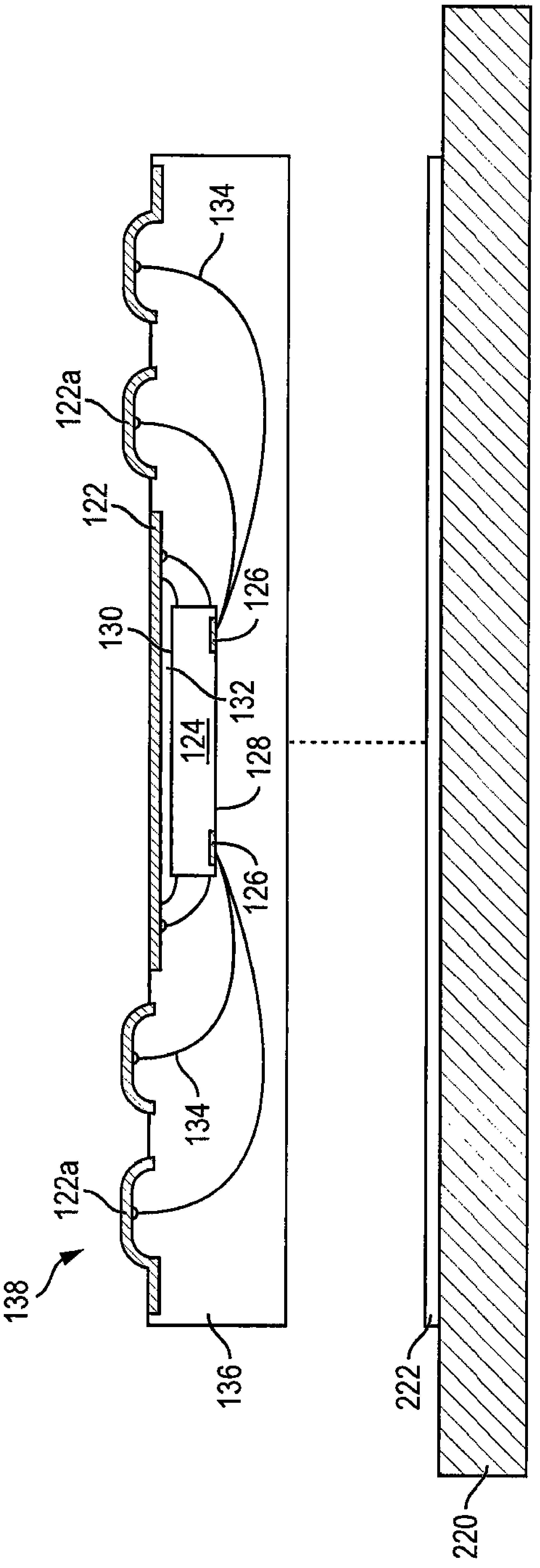
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FIG. 8a

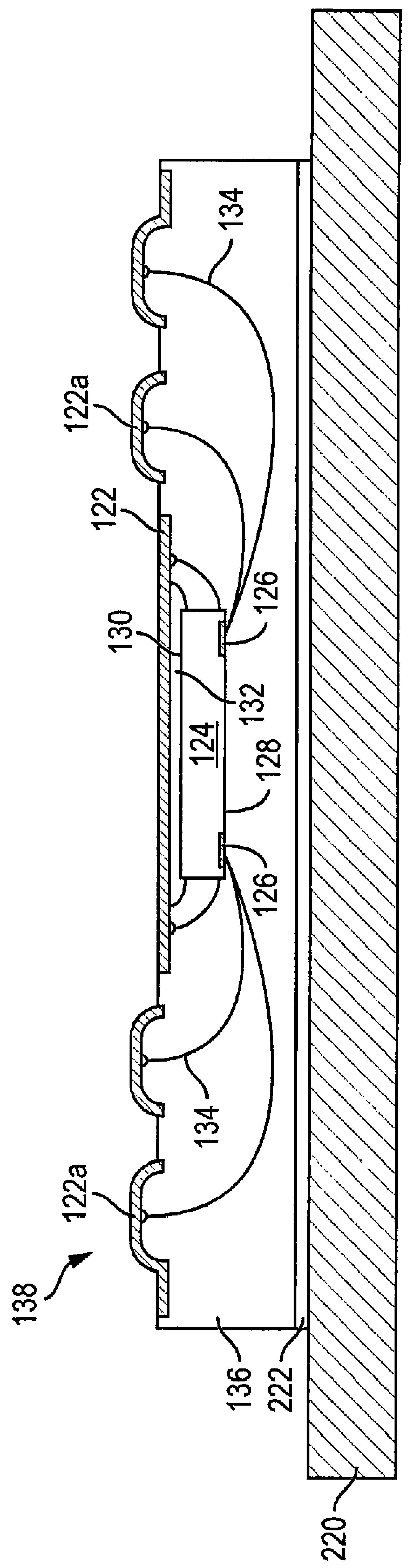
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FIG. 8b

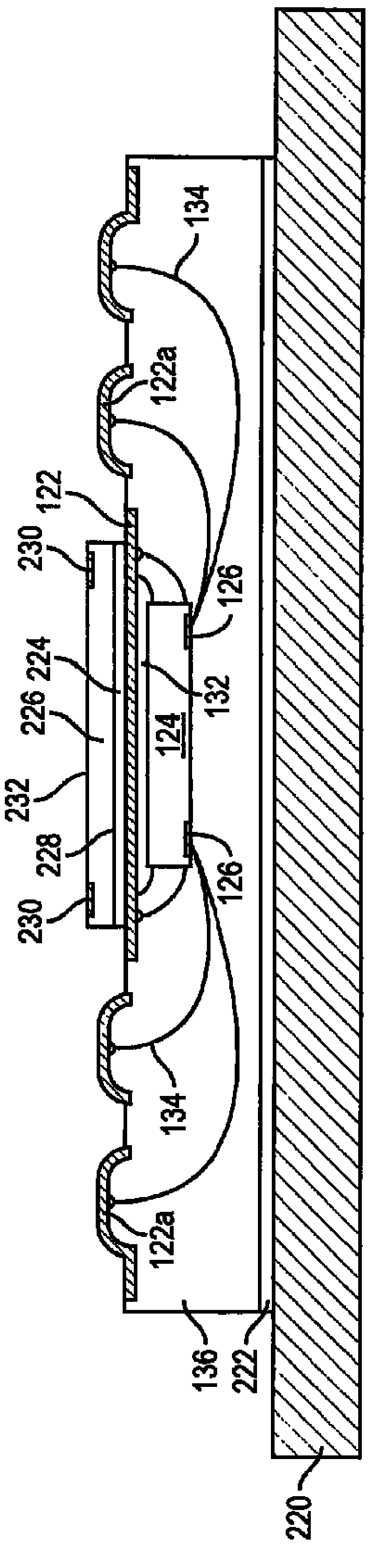
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FIG. 8c

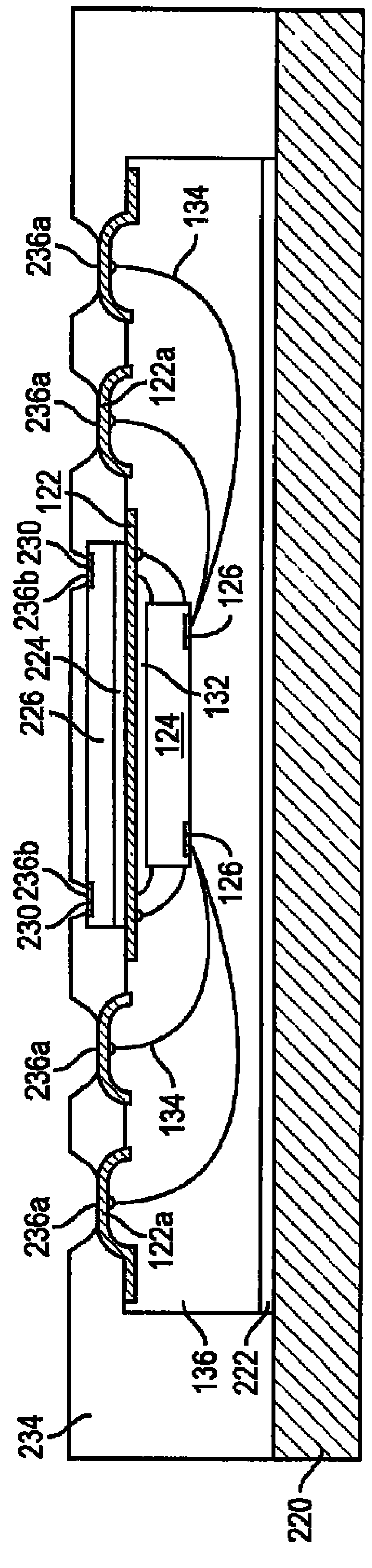
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FIG. 8d

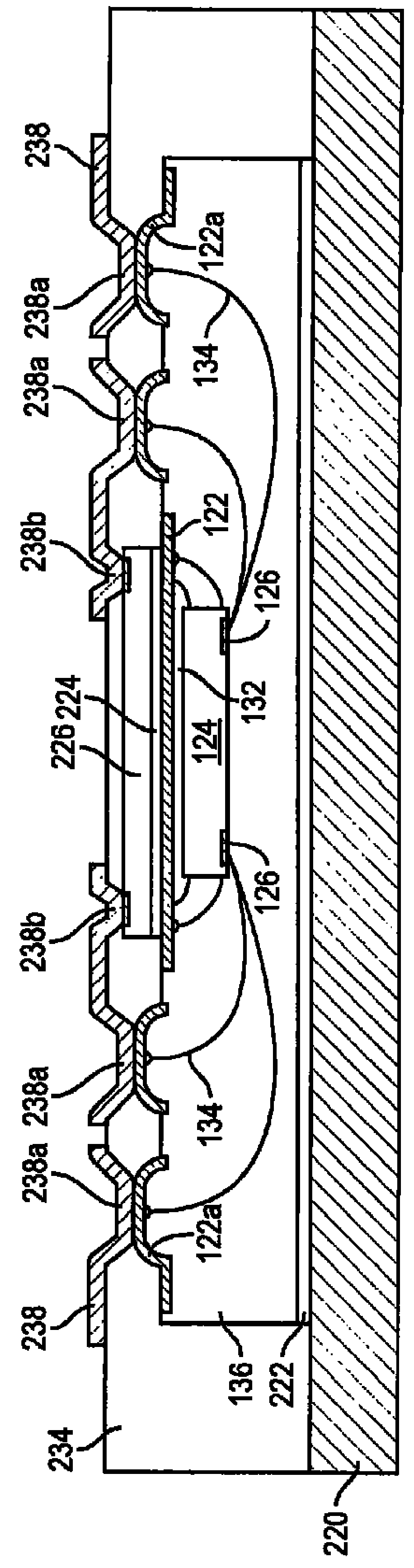
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FIG. 8e

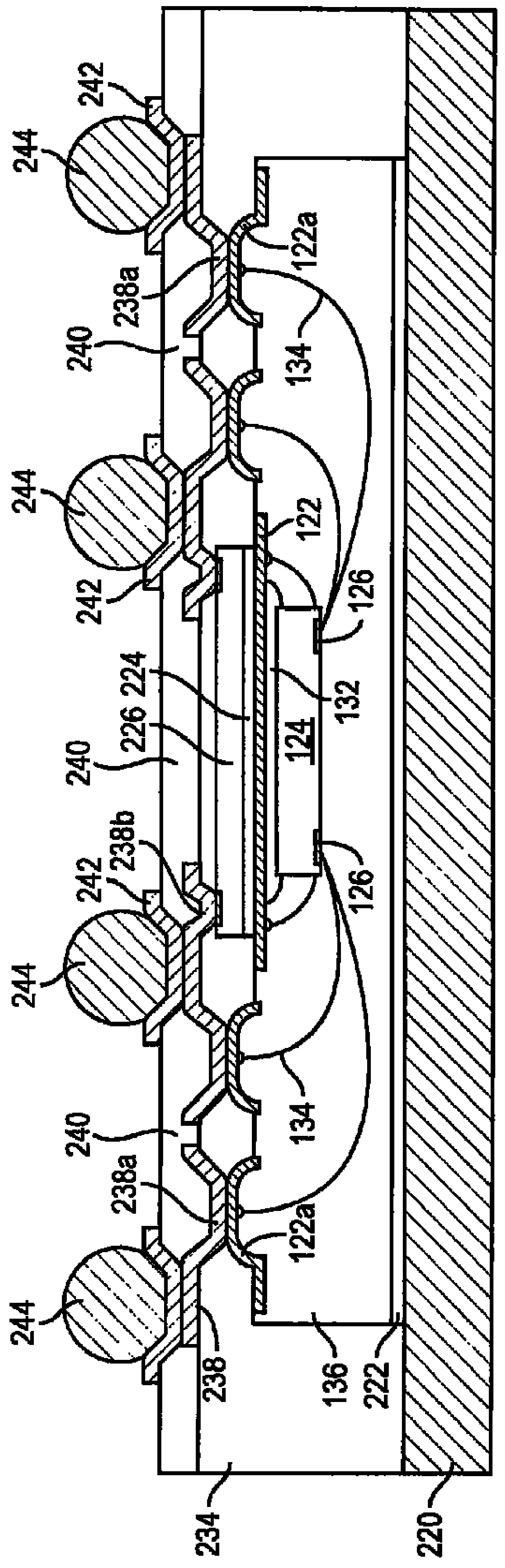
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FIG. 8f

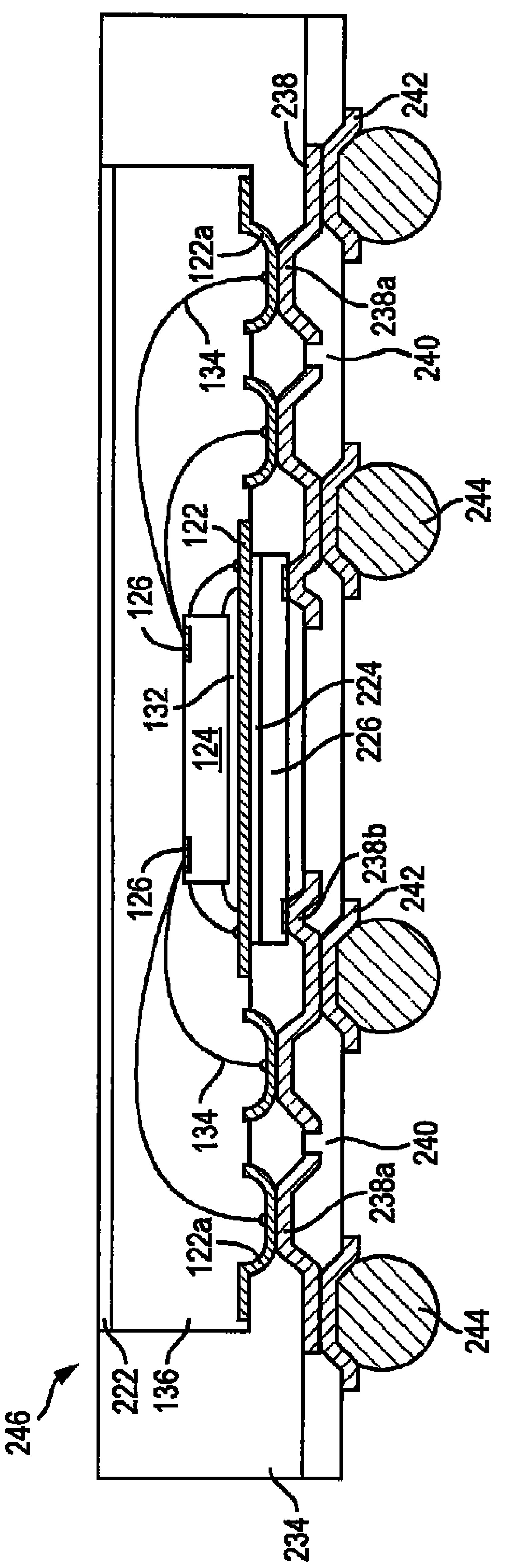
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FIG. 8g

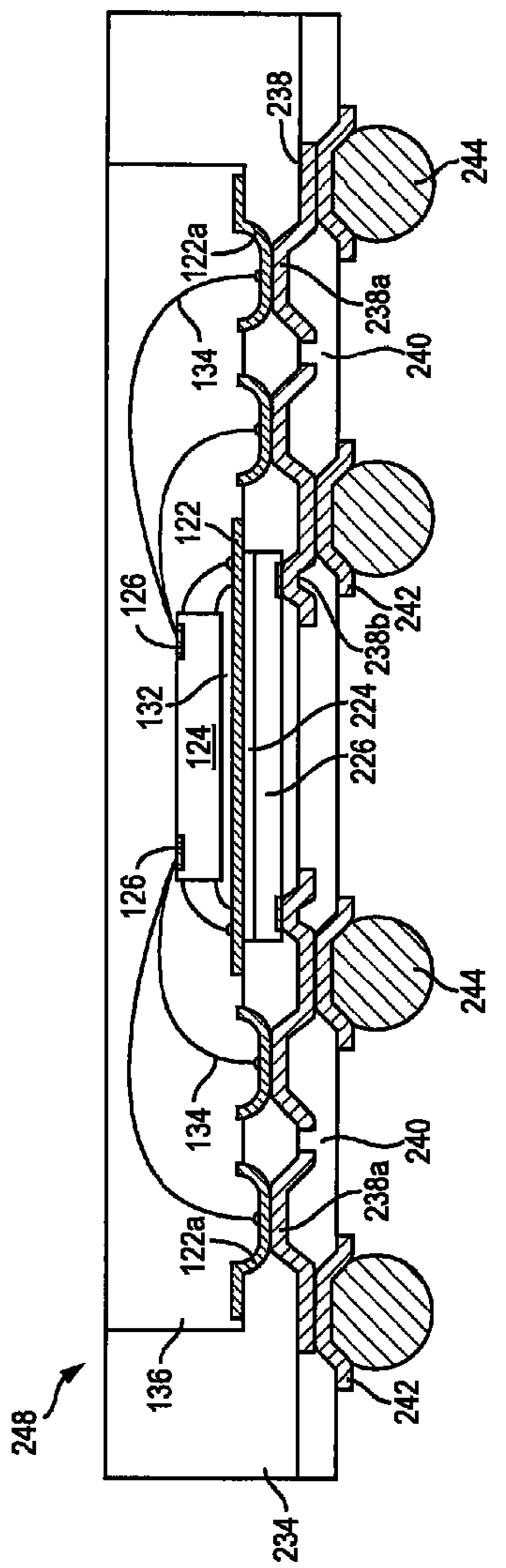
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FIG. 8h

SEMICONDUCTOR DEVICE AND METHOD OF FORMING PIP WITH INNER KNOWN GOOD DIE INTERCONNECTED WITH CONDUCTIVE BUMPS

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue; a claim printed with strikethrough indicates that the claim was canceled, disclaimed, or held invalid by a prior post-patent action or proceeding.

CLAIM TO DOMESTIC PRIORITY

The present application is *a reissue of U.S. patent application Ser. No. 13/606,451, now U.S. Pat. No. 8,884,418, filed Sep. 7, 2012, which is* a division of U.S. patent application Ser. No. 12/635,631, now U.S. Pat. No. 8,283,209, filed Dec. 10, 2009, which application is incorporated herein by reference and which is a continuation-in-part of U.S. patent application Ser. No. 12/136,768, now U.S. Pat. No. 7,977,779, filed Jun. 10, 2008.

FIELD OF THE INVENTION

The present invention relates in general to semiconductor devices and, more particularly, to a semiconductor device and method of forming a package-in-package configuration with an inner known good die interconnected with conductive bumps formed in shallow vias.

BACKGROUND OF THE INVENTION

Semiconductor devices are commonly found in modern electronic products. Semiconductor devices vary in the number and density of electrical components. Discrete semiconductor devices generally contain one type of electrical component, e.g., light emitting diode (LED), small signal transistor, resistor, capacitor, inductor, and power metal oxide semiconductor field effect transistor (MOSFET). Integrated semiconductor devices typically contain hundreds to millions of electrical components. Examples of integrated semiconductor devices include microcontrollers, microprocessors, charged-coupled devices (CCDs), solar cells, and digital micro-mirror devices (DMDs).

Semiconductor devices perform a wide range of functions such as high-speed calculations, transmitting and receiving electromagnetic signals, controlling electronic devices, transforming sunlight to electricity, and creating visual projections for television displays. Semiconductor devices are found in the fields of entertainment, communications, power conversion, networks, computers, and consumer products. Semiconductor devices are also found in military applications, aviation, automotive, industrial controllers, and office equipment.

Semiconductor devices exploit the electrical properties of semiconductor materials. The atomic structure of semiconductor material allows its electrical conductivity to be manipulated by the application of an electric field or base current or through the process of doping. Doping introduces impurities into the semiconductor material to manipulate and control the conductivity of the semiconductor device.

A semiconductor device contains active and passive electrical structures. Active structures, including bipolar and field effect transistors, control the flow of electrical current. By varying levels of doping and application of an electric field or base current, the transistor either promotes or restricts the flow of electrical current. Passive structures, including resistors, capacitors, and inductors, create a relationship between voltage and current necessary to perform a variety of electrical functions. The passive and active structures are electrically connected to form circuits, which enable the semiconductor device to perform high-speed calculations and other useful functions.

Semiconductor devices are generally manufactured using two complex manufacturing processes, i.e., front-end manufacturing, and back-end manufacturing, each involving potentially hundreds of steps. Front-end manufacturing involves the formation of a plurality of die on the surface of a semiconductor wafer. Each die is typically identical and contains circuits formed by electrically connecting active and passive components. Back-end manufacturing involves singulating individual die from the finished wafer and packaging the die to provide structural support and environmental isolation.

One goal of semiconductor manufacturing is to produce smaller semiconductor devices. Smaller devices typically consume less power, have higher performance, and can be produced more efficiently. In addition, smaller semiconductor devices have a smaller footprint, which is desirable for smaller end products. A smaller die size may be achieved by improvements in the front-end process resulting in die with smaller, higher density active and passive components. Back-end processes may result in semiconductor device packages with a smaller footprint by improvements in electrical interconnection and packaging materials.

Some semiconductor devices are configured as a package-in-package (PiP). The semiconductor die are interconnected by bond wires or deep conductive through silicon vias (TSV) or deep conductive through hole vias (THV). The interconnect structure increases the PiP thickness and manufacturing costs.

SUMMARY OF THE INVENTION

A need exists to electrically interconnect PiP without deep TSV or THV. Accordingly, in one embodiment, the present invention is a semiconductor device comprising a support layer and semiconductor package disposed over the support layer. The semiconductor package includes a first semiconductor die or component, first encapsulant deposited over the first semiconductor die or component with an encapsulant bump extending from a body of the first encapsulant, and first conductive layer disposed over the first encapsulant including the encapsulant bump to form a conductive bump. A second encapsulant is deposited over the semiconductor package and support layer.

In another embodiment, the present invention is a semiconductor device comprising a first semiconductor die or component. A first encapsulant is deposited over the first semiconductor die or component with an encapsulant bump extending from a body of the first encapsulant. A first conductive layer is disposed over a first surface of the first encapsulant including the encapsulant bump to form a conductive bump.

In another embodiment, the present invention is a semiconductor device comprising a support layer and semiconductor package disposed over the support layer. The semiconductor package includes a first semiconductor die or component, first encapsulant deposited over the first semiconductor die or component with an encapsulant bump extending from a body of the first encapsulant, and first conductive layer disposed over a first surface of the first encapsulant including the encapsulant bump to form a conductive bump.

In another embodiment, the present invention is a semiconductor device comprising a support layer and semiconductor package disposed over the support layer. The semiconductor package includes a bump comprising an inner insulating material and outer conductive material.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a PCB with different types of packages mounted to its surface;

FIGS. **2**a-**2**c illustrate further detail of the representative semiconductor packages mounted to the PCB;

FIGS. **3**a-**3**j illustrate a process of forming wafer level PiP mounted to a substrate with inner known good die interconnected with conductive bumps formed in shallow vias;

FIG. **4** illustrates the PiP with an IPD;

FIG. **5** illustrates the inner package mounted to a support layer;

FIG. **6** illustrates the inner package mounted to an EMI and RFI shielding layer;

FIGS. **7**a-**7**b illustrates the inner package mounted to a PCB; and

FIGS. **8**a-**8**h illustrate a process of forming PiP mounted to a carrier with inner known good die interconnected with conductive bumps formed in shallow vias.

DETAILED DESCRIPTION OF THE DRAWINGS

The present invention is described in one or more embodiments in the following description with reference to the figures, in which like numerals represent the same or similar elements. While the invention is described in terms of the best mode for achieving the invention's objectives, it will be appreciated by those skilled in the art that it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims and their equivalents as supported by the following disclosure and drawings.

Semiconductor devices are generally manufactured using two complex manufacturing processes: front-end manufacturing and back-end manufacturing. Front-end manufacturing involves the formation of a plurality of die on the surface of a semiconductor wafer. Each die on the wafer contains active and passive electrical components, which are electrically connected to form functional electrical circuits. Active electrical components, such as transistors and diodes, have the ability to control the flow of electrical current. Passive electrical components, such as capacitors, inductors, resistors, and transformers, create a relationship between voltage and current necessary to perform electrical circuit functions.

Passive and active components are formed over the surface of the semiconductor wafer by a series of process steps including doping, deposition, photolithography, etching, and planarization. Doping introduces impurities into the semiconductor material by techniques such as ion implantation or thermal diffusion. The doping process modifies the electrical conductivity of semiconductor material in active devices, transforming the semiconductor material into an insulator, conductor, or dynamically changing the semiconductor material conductivity in response to an electric field or base current. Transistors contain regions of varying types and degrees of doping arranged as necessary to enable the transistor to promote or restrict the flow of electrical current upon the application of the electric field or base current.

Active and passive components are formed by layers of materials with different electrical properties. The layers can be formed by a variety of deposition techniques determined in part by the type of material being deposited. For example, thin film deposition may involve chemical vapor deposition (CVD), physical vapor deposition (PVD), electrolytic plating, and electroless plating processes. Each layer is generally patterned to form portions of active components, passive components, or electrical connections between components.

The layers can be patterned using photolithography, which involves the deposition of light sensitive material, e.g., photoresist, over the layer to be patterned. A pattern is transferred from a photomask to the photoresist using light. The portion of the photoresist pattern subjected to light is removed using a solvent, exposing portions of the underlying layer to be patterned. The remainder of the photoresist is removed, leaving behind a patterned layer. Alternatively, some types of materials are patterned by directly depositing the material into the areas or voids formed by a previous deposition/etch process using techniques such as electroless and electrolytic plating.

Depositing a thin film of material over an existing pattern can exaggerate the underlying pattern and create a non-uniformly flat surface. A uniformly flat surface is required to produce smaller and more densely packed active and passive components. Planarization can be used to remove material from the surface of the wafer and produce a uniformly flat surface. Planarization involves polishing the surface of the wafer with a polishing pad. An abrasive material and corrosive chemical are added to the surface of the wafer during polishing. The combined mechanical action of the abrasive and corrosive action of the chemical removes any irregular topography, resulting in a uniformly flat surface.

Back-end manufacturing refers to cutting or singulating the finished wafer into the individual die and then packaging the die for structural support and environmental isolation. To singulate the die, the wafer is scored and broken along non-functional regions of the wafer called saw streets or scribes. The wafer is singulated using a laser cutting tool or saw blade. After singulation, the individual die are mounted to a package substrate that includes pins or contact pads for interconnection with other system components. Contact pads formed over the semiconductor die are then connected to contact pads within the package. The electrical connections can be made with solder bumps, stud bumps, conductive paste, or wirebonds. An encapsulant or other molding material is deposited over the package to provide physical support and electrical isolation. The finished package is then inserted into an electrical system and the functionality of the semiconductor device is made available to the other system components.

FIG. **1** illustrates electronic device **50** having a chip carrier substrate or printed circuit board (PCB) **52** with a plurality of semiconductor packages mounted on its surface. Electronic device **50** may have one type of semiconductor package, or multiple types of semiconductor packages, depending on the application. The different types of semiconductor packages are shown in FIG. **1** for purposes of illustration.

Electronic device **50** may be a stand-alone system that uses the semiconductor packages to perform one or more electrical functions. Alternatively, electronic device **50** may be a sub-component of a larger system. For example, electronic device **50** may be a graphics card, network interface card, or other signal processing card that can be inserted into a computer. The semiconductor package can include microprocessors, memories, application specific integrated circuits (ASIC), logic circuits, analog circuits, RF circuits, discrete devices, or other semiconductor die or electrical components.

In FIG. **1**, PCB **52** provides a general substrate for structural support and electrical interconnect of the semiconductor packages mounted on the PCB. Conductive signal traces **54** are formed over a surface or within layers of PCB **52** using evaporation, electrolytic plating, electroless plating, screen printing, or other suitable metal deposition process. Signal traces **54** provide for electrical communication between each of the semiconductor packages, mounted components, and other external system components. Traces **54** also provide power and ground connections to each of the semiconductor packages.

In some embodiments, a semiconductor device has two packaging levels. First level packaging is a technique for mechanically and electrically attaching the semiconductor die to an intermediate carrier. Second level packaging involves mechanically and electrically attaching the intermediate carrier to the PCB. In other embodiments, a semiconductor device may only have the first level packaging where the die is mechanically and electrically mounted directly to the PCB.

For the purpose of illustration, several types of first level packaging, including wire bond package **56** and flip chip **58**, are shown on PCB **52**. Additionally, several types of second level packaging, including ball grid array (BGA) **60**, bump chip carrier (BCC) **62**, dual in-line package (DIP) **64**, land grid array (LGA) **66**, multi-chip module (MCM) **68**, quad flat non-leaded package (QFN) **70**, and quad flat package **72**, are shown mounted on PCB **52**. Depending upon the system requirements, any combination of semiconductor packages, configured with any combination of first and second level packaging styles, as well as other electronic components, can be connected to PCB **52**. In some embodiments, electronic device **50** includes a single attached semiconductor package, while other embodiments call for multiple interconnected packages. By combining one or more semiconductor packages over a single substrate, manufacturers can incorporate pre-made components into electronic devices and systems. Because the semiconductor packages include sophisticated functionality, electronic devices can be manufactured using cheaper components and a streamlined manufacturing process. The resulting devices are less likely to fail and less expensive to manufacture resulting in a lower cost for consumers.

FIGS. **2**a-**2**c show exemplary semiconductor packages. FIG. **2**a illustrates further detail of DIP **64** mounted on PCB **52**. Semiconductor die **74** includes an active region containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and are electrically interconnected according to the electrical design of the die. For example, the circuit may include one or more transistors, diodes, inductors, capacitors, resistors, and other circuit elements formed within the active region of semiconductor die **74**. Contact pads **76** are one or more layers of conductive material, such as aluminum (Al), copper (Cu), tin (Sn), nickel (Ni), gold (Au), or silver (Ag), and are electrically connected to the circuit elements formed within semiconductor die **74**. During assembly of DIP **64**, semiconductor die **74** is mounted to an intermediate carrier **78** using a gold-silicon eutectic layer or adhesive material such as thermal epoxy or epoxy resin. The package body includes an insulative packaging material such as polymer or ceramic. Conductor leads **80** and wire bonds **82** provide electrical interconnect between semiconductor die **74** and PCB **52**. Encapsulant **84** is deposited over the package for environmental protection by preventing moisture and particles from entering the package and contaminating die **74** or wire bonds **82**.

FIG. **2**b illustrates further detail of BCC **62** mounted on PCB **52**. Semiconductor die **88** is mounted over carrier **90** using an underfill or epoxy-resin adhesive material **92**. Wire bonds **94** provide first level packing interconnect between contact pads **96** and **98**. Molding compound or encapsulant **100** is deposited over semiconductor die **88** and wire bonds **94** to provide physical support and electrical isolation for the device. Contact pads **102** are formed over a surface of PCB **52** using a suitable metal deposition process such as electrolytic plating or electroless plating to prevent oxidation. Contact pads **102** are electrically connected to one or more conductive signal traces **54** in PCB **52**. Bumps **104** are formed between contact pads **98** of BCC **62** and contact pads **102** of PCB **52**.

In FIG. **2**c, semiconductor die **58** is mounted face down to intermediate carrier **106** with a flip chip style first level packaging. Active region **108** of semiconductor die **58** contains analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed according to the electrical design of the die. For example, the circuit may include one or more transistors, diodes, inductors, capacitors, resistors, and other circuit elements within active region **108**. Semiconductor die **58** is electrically and mechanically connected to carrier **106** through bumps **110**.

BGA **60** is electrically and mechanically connected to PCB **52** with a BGA style second level packaging using bumps **112**. Semiconductor die **58** is electrically connected to conductive signal traces **54** in PCB **52** through bumps **110**, signal lines **114**, and bumps **112**. A molding compound or encapsulant **116** is deposited over semiconductor die **58** and carrier **106** to provide physical support and electrical isolation for the device. The flip chip semiconductor device provides a short electrical conduction path from the active devices on semiconductor die **58** to conduction tracks on PCB **52** in order to reduce signal propagation distance, lower capacitance, and improve overall circuit performance. In another embodiment, the semiconductor die **58** can be mechanically and electrically connected directly to PCB **52** using flip chip style first level packaging without intermediate carrier **106**.

FIGS. **3**a-**3**j illustrate, in relation to FIGS. **1** and **2**a-**2**c, a process of forming wafer level PiP mounted to a substrate with inner known good die interconnected with conductive bumps formed in shallow vias. In FIG. **3**a, a substrate or carrier **120** contains temporary or sacrificial base material such as silicon, polymer, polymer composite, metal, ceramic, glass, glass epoxy, beryllium oxide, or other suitable low-cost, rigid material or bulk semiconductor material for structural support. A plurality of shallow vias **121** is formed in the surface of carrier **120**.

In FIG. **3**b, an electrically conductive layer **122** is formed over surface **123** of carrier **120**, including following the contour of vias **121**, using a patterning and metal deposition process such as PVD, CVD, sputtering, electrolytic plating, and electroless plating. A portion of conductive layer **122**, denoted as conductive bumps **122**a, resides in vias **121**. Conductive layer **122** can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Portions of conductive layer **122** can be electrically common or electrically isolated depending on the design and function of the semiconductor device.

In FIG. **3**c, semiconductor die or component **124** is mounted to conductive layer **122** with contact pads **126** on active surface **128** oriented upward away from carrier **120**. Active surface **128** contains analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical design and function of the die. For example, the circuit may include one or more transistors, diodes, and other circuit elements formed within active surface **128** to implement analog circuits or digital circuits, such as digital signal processor (DSP), ASIC, memory, or other signal processing circuit. Semiconductor die **124** may also contain IPDs, such as inductors, capacitors, and resistors, for RF signal processing. Back surface **130** is secured to conductive layer **122** with an adhesive material **132**, such as thermal epoxy or epoxy resin. Bond wires **134** are formed between contact pads **126** to conductive layer **122** for electrical interconnect.

An encapsulant or molding compound **136** is deposited over semiconductor die **124**, conductive layer **122**, and bond wires **134** using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant **136** can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant **136** is non-conductive and environmentally protects the semiconductor device from external elements and contaminants.

FIG. **3**d shows a semiconductor wafer **140** containing a base substrate material **142** such as silicon, germanium, gallium arsenide, indium phosphide, or silicon carbide, for structural support. An electrically conductive layer **144** is formed over substrate **142** using a patterning and metal deposition process such as PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer **144** can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer **144** provides electrical interconnect. Portions of conductive layer **144** can be electrically common or electrically isolated depending on the design and function of the semiconductor device. An adhesive layer **146**, such as thermal epoxy or epoxy resin, is formed over a surface of substrate **142**.

In another embodiment, semiconductor wafer **140** may also contain a plurality of semiconductor die each having an active region **148** containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical design and function of the die. For example, the circuit may include one or more transistors, diodes, and other circuit elements formed within active surface **148** to implement baseband analog circuits or digital circuits, such as DSP, memory, or other signal processing circuit. Semiconductor wafer **140** may also contain IPDs, such as inductors, capacitors, and resistors, for RF signal processing. Conductive layer **144** is electrically connected to the active and passive circuits in active region **148**.

The temporary carrier **120** is removed by chemical etching, mechanical peel-off, CMP, mechanical grinding, thermal bake, laser scanning, or wet stripping to expose conductive bumps **122**a. The semiconductor package **138** is inverted and mounted to substrate **142** with encapsulant **136** contacting adhesive layer **146**, as shown in FIGS. **3**d-**3**e.

In FIG. **3**f, bond wires **150** are formed between conductive layer **122** and conductive layer **144**. The active and passive circuits of semiconductor die **124** are electrically

connected through contact pads **126**, bond wires **134**, conductive layer **122**, and bond wires **150** to conductive layer **144** of substrate **142**.

An adhesive layer **152**, such as thermal epoxy or epoxy resin, is formed over a portion of conductive layer **122** opposite semiconductor die **124**. A semiconductor die or component **154** is mounted with back surface **156** to conductive layer **122** and contact pads **158** on active surface **160** oriented upward away from conductive layer **122**. Active surface **160** contains analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical design and function of the die. For example, the circuit may include one or more transistors, diodes, and other circuit elements formed within active surface **160** to implement analog circuits or digital circuits, such as DSP, ASIC, memory, or other signal processing circuit. Semiconductor die **154** may also contain IPDs, such as inductors, capacitors, and resistors, for RF signal processing.

In FIG. **3**g, an encapsulant or molding compound **162** is deposited over semiconductor package **138**, bond wires **150**, and substrate **142** using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant **162** can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant **162** is non-conductive and environmentally protects the semiconductor device from external elements and contaminants.

In FIG. **3**h, a plurality of shallow vias **167**a and **167**b is formed in the surface of encapsulant **162** by an etching process to expose conductive bumps **122**a and contact pads **158**.

In FIG. **3**i, an electrically conductive layer **164** is formed over encapsulant **162**, conductive bumps **122**a, and contact pads **158** using a patterning and metal deposition process such as PVD, CVD, sputtering, electrolytic plating, and electroless plating. A portion of conductive layer **164**, denoted as conductive bumps **164**a and **164**b, resides in vias **167**a and **167**b. Conductive layer **164** can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer **164** operates as a redistribution layer (RDL) and provides electrical interconnect between the active and passive circuits of semiconductor die **154** and conductive layer **122**. Conductive bumps **164**a are electrically connected to conductive bumps **122**a, and conductive bumps **164**b are electrically connected to contact pads **158**. Other portions of conductive layer **164** can be electrically common or electrically isolated depending on the design and function of the semiconductor device.

In FIG. **3**j, an insulating or passivation layer **166** is formed over encapsulant **162** and conductive layer **164** using PVD, CVD, printing, spin coating, spray coating, sintering or thermal oxidation. The insulating layer **166** can be one or more layers of silicon dioxide (SiO2), silicon nitride (Si3N4), silicon oxynitride (SiON), tantalum pentoxide (Ta2O5), aluminum oxide (Al2O3), or other material having similar insulating and structural properties. A portion of insulating layer **166** is removed by an etching process to expose conductive layer **164**.

An electrically conductive layer **168** is formed over conductive layer **164** and insulating layer **166** using a patterning and deposition process such as PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer **168** forms a multi-layer under bump metallization (UBM) including a barrier layer and adhesion layer.

In one embodiment, the barrier layer contains Ni, titanium tungsten (TiW), chromium copper (CrCu), nickel vanadium (NiV), platinum (Pt), or palladium (Pd). The adhesion layer contains Al, titanium (Ti), chromium (Cr), or titanium nitride (TiN). UBM **168** provides a low resistive interconnect, as well as a barrier to Cu or solder diffusion.

An electrically conductive bump material is deposited over UBM **168** using an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process. The bump material can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof, with an optional flux solution. For example, the bump material can be eutectic Sn/Pb, high-lead solder, or lead-free solder. The bump material is bonded to UBM **168** using a suitable attachment or bonding process. In one embodiment, the bump material is reflowed by heating the material above its melting point to form spherical balls or bumps **170**. In some applications, bumps **170** are reflowed a second time to improve electrical contact to UBM **168**. The bumps can also be compression bonded to UBM **168**. Bumps **170** represent one type of interconnect structure that can be formed over UBM **168**. The interconnect structure can also use stud bumps, micro bumps, conductive pillars, or other electrical interconnect.

Semiconductor die **124** is a known good die (KGD) having been tested and passed functionality, reliability, and interconnect specifications. Semiconductor die **124** is packaged within encapsulant **136** and serves as an inner KGD of wafer-level PiP **172**. The active and passive circuits of KGD **124** are electrically connected through contact pads **126**, bond wires **134**, conductive layer **122**, conductive layer **144**, conductive bumps **122**a and **164**a, and contact pads **158** to the active and passive circuits of semiconductor die **154**. The active and passive circuits of KGD **124** and semiconductor die **154** are also electrically connected through bond wires **150** to conductive layer **144** of substrate **142**, and through conductive layer **168** and bumps **170** to external devices. The shallow via **121** and **167** with associated conductive bumps **122**a and **164**a have reduced the headroom needed for semiconductor die **154** and to electrically interconnect semiconductor die **124** and **154** in PiP **172**.

FIG. **4** shows an embodiment of wafer level PiP **174**, similar to the structure described in FIGS. **3**a-**3**j, with IPD **176** formed over encapsulant **162** adjacent to semiconductor die **154**. IPD **176** constitutes one or more inductors, capacitors, and resistors for RF signal processing. IPD **176** is electrically connected to conductive layer **164**.

FIG. **5** shows an embodiment of PiP **180**, similar to the structure described in FIGS. **3**a-**3**j, with semiconductor package **138** mounted to support layer **182** (instead of substrate **142**) by adhesive layer **184**. Support layer **182** can be a carrier, stiffener, or heat sink. In the case of a heat sink, support layer **182** can be Al, Cu, or another material with high thermal conductivity to provide heat dissipation for semiconductor die **122**. An optional thermal interface material, such as aluminum oxide, zinc oxide, boron nitride, or pulverized silver, between heat sink **182** and semiconductor package **138** aids in the distribution and dissipation of heat generated by semiconductor die **124** and **154**.

FIG. **6** shows an embodiment of PiP **190**, similar to the structure described in FIGS. **3**a-**3**j, with semiconductor package **138** mounted to electromagnetic interference (EMI) and radio frequency interference (RFI) shielding layer **192** (instead of substrate **142**) by adhesive layer **194**. Shielding layer **192** can be Cu, Al, ferrite or carbonyl iron, stainless steel, nickel silver, low-carbon steel, silicon-iron steel, foil, epoxy, conductive resin, and other metals and composites capable of blocking or absorbing EMI, RFI, and other inter-device interference. Shielding layer **192** can also be a non-metal material such as carbon-black or aluminum flake to reduce the effects of EMI and RFI. Shielding layer **192** is grounded through bond wires **196** to conductive layer **122** and **164** to bumps **170**.

FIG. **7**a shows an embodiment of PiP **200**, similar to the structure described in FIGS. **3**a-**3**i, with semiconductor package **138** mounted to PCB **202** (instead of substrate **142**) by adhesive layer **204**. PCB **202** includes conductive layer **206** for electrical interconnect. Bond wires **150** are electrically connected to conductive layer **206**. Bumps **208** are formed on conductive layer **206**. An insulating or passivation layer **210** is formed over encapsulant **162** and conductive layer **164**a using PVD, CVD, printing, spin coating, spray coating, sintering or thermal oxidation. The insulating layer **210** can be one or more layers of SiO2, Si3N4, SiON, Ta2O5, Al2O3, or other material having similar insulating and structural properties.

In FIG. **7**b, a portion of insulating layer **210** is removed by an etching process to expose conductive layer **164**. An electrically conductive layer **212** is formed over conductive layer **164** using a patterning and metal deposition process such as PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer **212** forms a multi-layer UBM including a barrier layer and adhesion layer. In one embodiment, the barrier layer contains Ni, NiV, TiW, CrCu, Pt, or Pd. The adhesion layer contains Al, Ti, Cr, or TiN. UBM **168** provides a low resistive interconnect, as well as a barrier to Cu or solder diffusion.

FIGS. **8**a-**8**h illustrate, in relation to FIGS. **1** and **2**a-**2**c, a process of forming PiP mounted to a carrier with inner known good die interconnected with conductive bumps formed in shallow vias. In FIG. **8**a, a substrate or carrier **220** contains temporary or sacrificial base material such as silicon, polymer, polymer composite, metal, ceramic, glass, glass epoxy, beryllium oxide, or other suitable low-cost, rigid material or bulk semiconductor material for structural support. In one embodiment, carrier **120** is Cu. An adhesive layer **222**, such as thermal epoxy or epoxy resin, is formed over a surface of carrier **220**. The semiconductor package **138** from FIG. **3**d is mounted to carrier **220** with encapsulant **136** contacting adhesive layer **222**, as shown in FIGS. **8**a-**8**b.

In FIG. **8**c, an adhesive layer **224**, such as thermal epoxy or epoxy resin, is formed over a portion of conductive layer **122** opposite semiconductor die **124**. A semiconductor die or component **226** is mounted with back surface **228** to conductive layer **122** and contact pads **230** on active surface **232** oriented upward away from conductive layer **122**. Active surface **232** contains analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical design and function of the die. For example, the circuit may include one or more transistors, diodes, and other circuit elements formed within active surface **232** to implement analog circuits or digital circuits, such as DSP, ASIC, memory, or other signal processing circuit. Semiconductor die **226** may also contain IPDs, such as inductors, capacitors, and resistors, for RF signal processing.

In FIG. **8**d, an encapsulant or molding compound **234** is deposited over semiconductor package **138** and carrier **220** using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant **234** can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant **234** is non-conductive and environmentally protects the semiconductor device from external elements and contaminants. A plurality of shallow vias **236**a and **236**b is formed in the surface of encapsulant **234** by an etching process to expose conductive bumps **122**a and contact pads **230**.

In FIG. **8**e, an electrically conductive layer **238** is formed over encapsulant **234**, conductive bumps **122**a, and contact pads **230** using a patterning and metal deposition process such as PVD, CVD, sputtering, electrolytic plating, and electroless plating. A portion of conductive layer **238**, denoted as conductive bumps **238**a and **238**b, resides in vias **236**a and **236**b. Conductive layer **238** can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer **238** operates as an RDL and provides electrical interconnect between the active and passive circuits of semiconductor die **226** and conductive layer **122**. Conductive bumps **238**a are electrically connected to conductive bumps **122**a and contact pads **230**. Other portions of conductive layer **238** can be electrically common or electrically isolated depending on the design and function of the semiconductor device.

In FIG. **8**f, an insulating or passivation layer **240** is formed over encapsulant **234** and conductive layer **238** using PVD, CVD, printing, spin coating, spray coating, sintering or thermal oxidation. The insulating layer **240** can be one or more layers of SiO2, Si3N4, SiON, Ta2O5, Al2O3, or other material having similar insulating and structural properties. A portion of insulating layer **240** is removed by an etching process to expose conductive layer **238**.

An electrically conductive layer **242** is formed over conductive layer **238** using a patterning and deposition process such as PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer **242** forms a multilayer UBM including a barrier layer and adhesion layer. In one embodiment, the barrier layer contains Ni, NiV, TiW, CrCu, Pt, or Pd. The adhesion layer contains Al, Ti, Cr, or TiN. UBM **242** provides a low resistive interconnect, as well as a barrier to Cu or solder diffusion.

An electrically conductive bump material is deposited over UBM **242** using an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process. The bump material can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof, with an optional flux solution. For example, the bump material can be eutectic Sn/Pb, high-lead solder, or lead-free solder. The bump material is bonded to UBM **242** using a suitable attachment or bonding process. In one embodiment, the bump material is reflowed by heating the material above its melting point to form spherical balls or bumps **244**. In some applications, bumps **244** are reflowed a second time to improve electrical contact to UBM **242**. The bumps can also be compression bonded to UBM **242**. Bumps **244** represent one type of interconnect structure that can be formed over UBM **242**. The interconnect structure can also use stud bumps, micro bumps, conductive pillars, or other electrical interconnect.

In FIG. **8**g, temporary carrier **220** is removed by chemical etching, mechanical peel-off, CMP, mechanical grinding, thermal bake, laser scanning, or wet stripping. Adhesive layer **222** remains exposed in PiP **246**. FIG. **8**h shows PiP **248** with both carrier **220** and adhesive layer **222** removed.

Semiconductor die **124** is a known good die (KGD) having been tested and passed functionality, reliability, and interconnect specifications. Semiconductor die **124** is packaged within encapsulant **136** and serves as an inner KGD of PiP **246**. The active and passive circuits of KGD **124** are electrically connected through contact pads **126**, bond wires **134**, conductive layer **122**, conductive layer **144**, conductive bumps **122**a and **238**a, and contact pads **230** to the active and passive circuits of semiconductor die **226**. The active and passive circuits of KGD **124** and semiconductor die **226** are also electrically connected through conductive layer **242** and bumps **244** to external devices. The shallow vias **121**, **167**, and **236** with associated conductive bumps **122**a, **164**a, and **238**a have reduced the headroom needed for semiconductor die **226** and to electrically interconnect semiconductor die **124** and **226** in PiP **246**.

While one or more embodiments of the present invention have been illustrated in detail, the skilled artisan will appreciate that modifications and adaptations to those embodiments may be made without departing from the scope of the present invention as set forth in the following claims.

What is claimed:

1. A semiconductor device, comprising:

a support layer;

a semiconductor package disposed over the support layer, the semiconductor package including,

(a) a first semiconductor die or component,

(b) a first encapsulant deposited over the first semiconductor die or component with an encapsulant bump extending from a body of the first encapsulant, and

(c) a first conductive layer disposed over the first encapsulant including the encapsulant bump to form a conductive bump;

a second encapsulant deposited over a surface of the semiconductor package opposite the support layer, the second encapsulant including an opening over the conductive bump; and

a second conductive layer formed in the opening over the conductive bump.

2. The semiconductor device of claim **1**, further including an interconnect structure formed over the second encapsulant, the interconnect structure being electrically connected to the conductive bump.

3. The semiconductor device of claim **1**, further including a second semiconductor die or component disposed over the semiconductor package.

4. The semiconductor device of claim **1**, wherein the semiconductor package further includes a bond wire formed between the conductive bump and first semiconductor die or component.

5. The semiconductor device of claim **1**, wherein the first semiconductor die or component includes a known good die or component.

6. The semiconductor device of claim **1**, wherein the support layer operates as a substrate, stiffener, heat sink, shielding layer, printed circuit board, or carrier.

7. A semiconductor device, comprising:

a first semiconductor die or component;

a first encapsulant deposited over the first semiconductor die or component with an encapsulant bump extending from a body of the first encapsulant;

a first conductive layer disposed over a first surface of the first encapsulant including the encapsulant bump to form a conductive bump; and

a second encapsulant deposited over and around the first encapsulant, the second encapsulant including a via formed through a surface of the second encapsulant *and extending to conductive bump*.

8. The semiconductor device of claim **7**, further including a bond wire formed between the conductive bump and first semiconductor die or component.

9. The semiconductor device of claim **7**, further including:

a support layer disposed over a second surface of the first encapsulant opposite the first surface of the first encapsulant;

the second encapsulant deposited over the support layer; and

an interconnect structure formed over the second encapsulant and within the via.

10. The semiconductor device of claim **9**, further including a second semiconductor die or component disposed over the first surface of the first encapsulant.

11. The semiconductor device of claim **9**, wherein the interconnect structure includes:

a second conductive layer formed over the second encapsulant;

an insulating layer formed over the second conductive layer; and

a third conductive layer formed over the second conductive layer.

12. The semiconductor device of claim **9**, wherein the support layer operates as a substrate, stiffener, heat sink, shielding layer, printed circuit board, or carrier.

13. The semiconductor device of claim **7**, wherein the first semiconductor die or component includes a known good die or component.

[14. A semiconductor device, comprising:

a support layer; and

a semiconductor package disposed over the support layer, the semiconductor package including,

(a) a first semiconductor die or component,

(b) a first non-conductive encapsulant deposited over the first semiconductor die or component with an encapsulant bump extending from a body of the first nonconductive encapsulant, and

(c) a first conductive layer disposed over a first surface of the first non-conductive encapsulant including the encapsulant bump to form a conductive bump.**]**

[15. The semiconductor device of claim **14**, wherein the semiconductor package further includes a bond wire formed between the conductive bump and first semiconductor die or component.**]**

[16. The semiconductor device of claim **14**, further including:

a second encapsulant deposited over the support layer and semiconductor package; and

an interconnect structure formed over the second encapsulant.**]**

[17. The semiconductor device of claim **16**, wherein the interconnect structure includes:

a second conductive layer formed over the second encapsulant;

an insulating layer formed over the second conductive layer; and

a third conductive layer formed over the second conductive layer.**]**

[18. The semiconductor device of claim **14**, further including a second semiconductor die or component disposed over the semiconductor package.**]**

[19. The semiconductor device of claim **14**, wherein the support layer operates as a substrate, stiffener, heat sink, shielding layer, printed circuit board, or carrier.**]**

[20. The semiconductor device of claim **14**, wherein the first semiconductor die or component includes a known good die or component.**]**

[21. A semiconductor device, comprising:

a support layer; and

a semiconductor package disposed over the support layer, the semiconductor package including a bump comprising an inner insulating material and outer conductive material.**]**

[22. The semiconductor device of claim **21**, wherein the semiconductor package includes:

a first semiconductor die or component;

an encapsulant deposited over the first semiconductor die or component, wherein a portion of the encapsulant constitutes the inner insulating material of the bump; and

a conductive layer formed over the encapsulant, wherein a portion of the conductive layer constitutes the outer conductive material of the bump.**]**

[23. The semiconductor device of claim **21**, further including:

an encapsulant deposited over the support layer and semiconductor package; and

an interconnect structure formed over the encapsulant.**]**

[24. The semiconductor device of claim **21**, further including a second semiconductor die or component disposed over the semiconductor package.**]**

[25. The semiconductor device of claim **21**, wherein the support layer operates as a substrate, stiffener, heat sink, shielding layer, printed circuit board, or carrier.**]**

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