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(54) **POWER SEMICONDUCTOR HAVING A LIGHTLY DOPED DRIFT AND BUFFER LAYER**

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H01L 29/06	(2006.01)
H01L 29/08	(2006.01)

(52) **U.S. Cl.**
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(58) **Field of Classification Search**
CPC . H01L 29/78; H01L 29/0634; H01L 29/1095; H01L 29/0878
See application file for complete search history.

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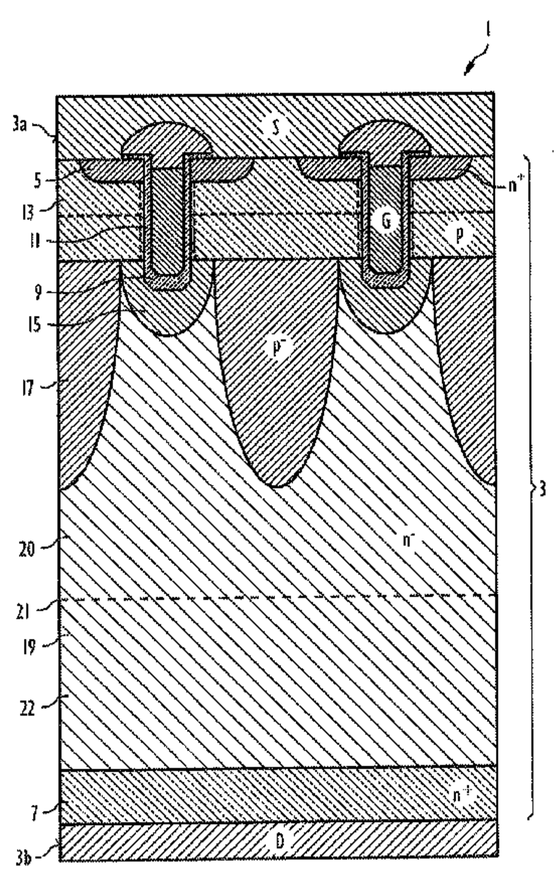
(57) **ABSTRACT**

A power semiconductor element having a lightly doped drift and buffer layer is disclosed. One embodiment has, underneath and between deep well regions of a first conductivity type, a lightly doped drift and buffer layer of a second conductivity type. The drift and buffer layer has a minimum vertical extension between a drain contact layer on the adjacent surface of a semiconductor substrate and the bottom of the deepest well region which is at least equal to a minimum lateral distance between the deep well regions. The vertical extension can also be determined such that a total amount of dopant per unit area in the drift and buffer layer is larger than a breakdown charge amount at breakdown voltage.

31 Claims, 1 Drawing Sheet



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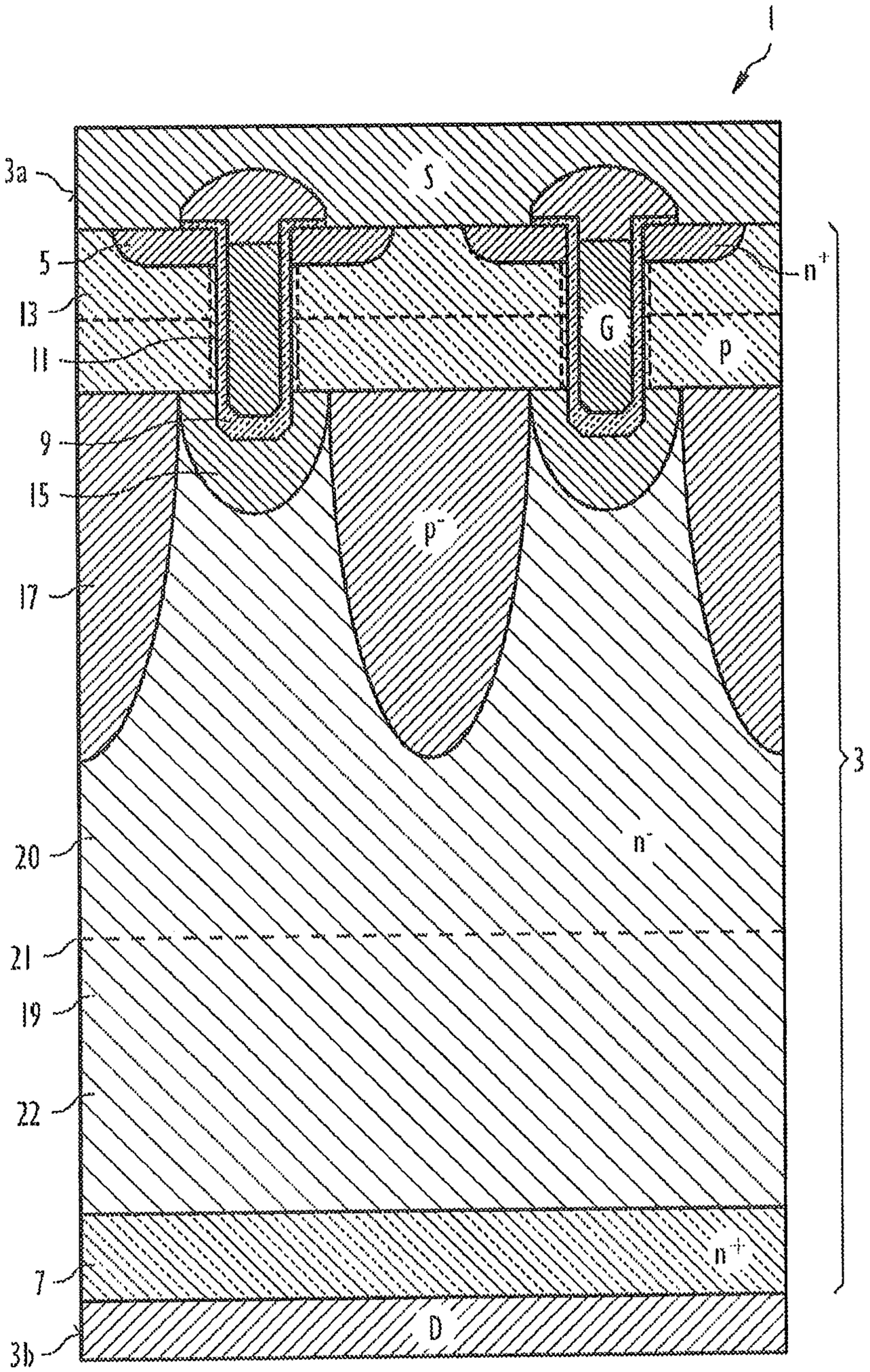
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POWER SEMICONDUCTOR HAVING A LIGHTLY DOPED DRIFT AND BUFFER LAYER

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue; a claim printed with strikethrough indicates that the claim was canceled, disclaimed, or held invalid by a prior post-patent action or proceeding.

CROSS-REFERENCE TO RELATED APPLICATIONS

This [Utility] patent application is a *broadening reissue continuation of U.S. application Ser. No. 13/873,295, which is an application for broadening reissue of U.S. Pat. No. 7,936,010, U.S. Pat. No. 7,936,010 is a* Continuation-in-Part of U.S. application Ser. No. 11/965,387, filed Dec. 27, 2007, *both of* which [is] *are* herewith incorporated in [its] *their* entirety by reference.

BACKGROUND

The invention relates to a power semiconductor element, in particular to a power MOS transistor of the planar type or a power transistor of the trench type.

In the course of the development of new generations of DMOS power transistors, the reduction of the specific On-resistance R_{on}. A is an important objective. Reducing the value of this parameter results in minimizing of the static power loss, whereas higher current densities may be achieved. Both effects make it possible to use smaller and cheaper semiconductor elements or chips, respectively, for controlling a total current of a predetermined level. Another parameter of such semiconductor element is a high resistivity against avalanche breakdown in the blocking or reverse operation mode of the element.

Prior developments in this field had frequently the unsatisfactory result that some progress in optimizing the one of the important parameters could be achieved, whereas at the same time the other important parameter could not be maintained at a favourable level.

For these and other reasons, there is a need for the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of embodiments and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments and together with the description serve to explain principles of embodiments. Other embodiments and many of the intended advantages of embodiments will be readily appreciated as they become better understood by reference to the following detailed description. The elements of the drawings are not necessarily to scale relative to each other. Like reference numerals designate corresponding similar parts.

FIG. **1** illustrates a schematic representation of an exemplary embodiment, as a cross-sectional representation of a first power semiconductor element structure.

DETAILED DESCRIPTION

In the following Detailed Description, reference is made to the accompanying drawings, which form a part hereof,

and in which is shown by way of illustration specific embodiments in which the invention may be practiced. In this regard, directional terminology, such as "top," "bottom," "front," "back," "leading," "trailing," etc., is used with reference to the orientation of the FIGURE(S) being described. Because components of embodiments can be positioned in a number of different orientations, the directional terminology is used for purposes of illustration and is in no way limiting. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present invention. The following detailed description, therefore, is not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

It is to be understood that the features of the various exemplary embodiments described herein may be combined with each other, unless specifically noted otherwise.

One embodiment provides a power semiconductor element which is made in a semiconductor substrate and includes a semiconductor body having a first and a second surface, being of a first conductivity type and having a first dopant concentration, formed in the first surface. A contact arrangement is provided in or on the first surface, and at least two deep, lightly doped well regions of the first conductivity type having a second, lower dopant concentration are provided near the first surface and have a minimum lateral distance therebetween. A highly doped drain contact layer of a second conductivity type and a first dopant concentration is provided in or on the second surface and an electrode is provided on the free surface of the drain contact layer.

In this semiconductor element, underneath and between the deep well regions of the first conductivity type a lightly doped drift and buffer layer of the second conductivity type and of a second dopant concentration is provided, wherein the drift and buffer layer has a minimum vertical extension (dimension) between the drain contact layer and the bottom of the deepest well region which is at least equal to a minimum lateral distance between the deep well region.

In one or more embodiments, the idea of providing a trench cell structure as a means to arrive at a significant reduction of the channel resistance, as a result of a significant increase of the channel width per unit area, is used. On the other hand, the inventors have dealt with the possible problem of a decrease of the blocking or reverse voltage already at moderate current densities, with the danger of a destruction of the semiconductor element, by providing an additional voltage buffer zone for the high current avalanche mode.

In other words a safety zone underneath the trenches is proposed, this safety zone serving as an extension zone for the dynamic extension of a space-charge region in a high current density avalanche case. In such case, in a drift zone a high density of holes will be established and this presence of a large amount of positive charges increases an already existing positive epi background charge within the drift zone. As a result thereof, the distribution of the electrical field through the drift zone is dynamically changed, insofar as in this situation the maximum of the field strength is approximately in the region of a trench bottom, whereas the original field's strength maximum is decreased. As a result thereof, the achievable blocking voltage decreases, and a negative differential breakdown voltage characteristic will be established. Then, in that cell of a semiconductor cell or array where this effect first occurs, most of the resulting avalanche current is concentrated and this portion of the array may be thermicaly destroyed due to an unduly large current density. The invention, however, aims at adequate

means for depleting addition charges, and, therefore, providing an additional region of maximum electrical field strength, contributing to a higher achievable total blocking or reverse voltage.

Whereas the above explained negative effects of the prior art in semiconductor elements of low reverse voltage (below typically 40 V) do rarely occur, embodiments herein are, for example, in power semiconductor elements of higher reverse voltage classes, in particular in the range of 40 V to 1200 V.

In one embodiment, the above mentioned vertical extension of the drift and buffer layer amounts to at least twice the minimum lateral distance between the deep well regions. The exact extension is dependent on the specific element structure, wherein it may be a helpful design rule to consider that the "safety zone" should have a thickness which is not completely depleted by the space-charge region at low current densities.

In a further embodiment, the second dopant concentration is constant through the drift and buffer layer. In one or more embodiments, under certain circumstances it may be useful if the second dopant concentration in the drift and buffer layer increases towards the drain contact layer. Even in this regard, specific design rules, in accordance with the above explained physical effects, are dependent on the predetermined device parameters and design features.

In a further embodiment, underneath and between the deep well regions of the first conductivity type a lightly doped drift and buffer layer of the second conductivity type and a second dopant concentration is provided, the minimum vertical extension of the drift and buffer layer between the drain contact layer and the bottom of the deepest well region being determined such that a total amount of its dopants per unit area is larger than a breakdown charge amount at breakdown voltage.

Herein, the term "breakdown charge amount" means the charge amount which may be depleted by a pn junction before the avalanche factor 1 is reached. This charge is dependent on the dopant concentration, typical values are about $2\text{-}3\cdot10^{12}$ cm^{-2}.

In a design option of this embodiment, the vertical extension of the drift and buffer layer is determined such that the total amount of the dopants per unit area is within the range of the 1.5-2.5 fold charge at breakdown voltage.

In a further embodiment, the second dopant concentration is constant through the drift and buffer layer. Once again, in one embodiment the second dopant concentration in the drift and buffer layer may increase towards the drain contact layer, i.e. towards the second main surface of the substrate.

In both above explained basic embodiments, a technology is useful wherein the semiconductor body and the drift and buffer layer include a semiconductor substrate and the drain contact layer includes an ion implantation layer within the semiconductor substrate.

To enhance the advantages of the physical effects explained above, a further embodiment may be useful wherein an interface between the drift and buffer layer and the drain contact layer includes valleys under the (in a cross-section more or less U or V shaped) deep well regions. In this regard, the interface between the "safety zone" and the drain contact layer may be undulated.

In a further embodiment of the invention, the dopant concentration of the drift zone beneath the deep wells may either be significantly decreased (down to a factor of 0.01) or, increased (e.g., up to a factor 3), as compared to the dopant concentration between the deep well regions.

As an important embodiment, a power MOS transistor of the planar type is provided including a semiconductor body having a first and a second surface and body regions of a first conductivity type and having a first dopant concentration, formed in the first surface. At its first surface, this planar transistor has a highly doped source region of the second conductivity type having a first dopant concentration; as well as a contact arrangement including a gate electrode over an insulating layer on the first surface and source electrode, directly over the first surface and in contact with the source region.

Similar to the semiconductor element explained above, this transistor has at least two deep, lightly doped well regions of the first conductivity type having a second dopant concentration, and having a minimum lateral distance therebetween, a highly doped drain contact layer of the second conductivity type and a second dopant concentration provided in or on the second surface of the semiconductor base layer, and an electrode provided on the free surface of the drain contact layer.

As in the element explained above, underneath and between the deep well regions of the first conductivity type a lightly doped drift and buffer layer of the second conductivity type and a third dopant concentration is provided, wherein the drift and buffer layer has a minimum vertical extension between the drain contact layer and the bottom of the deepest well region which is at least equal to the minimum lateral distance between the deep well region.

In a further embodiment, the vertical dimension of the drift and buffer layer between the drain contact layer and the bottom of the deepest well region is determined such that a total amount of its dopants per unit area is larger than a breakdown charge amount at breakdown voltage. Incidentally, the latter design rule may be combined with the former rule, making the vertical extension of the "safety zone" dependent on the minimum lateral distance between the deep well regions above it.

According to a further embodiment, a power transistor of the trench type is provided. Whereas most of the structural components or portions, respectively, of this transistor are similar to those of the planar type, as described further above, this transistor includes a gate electrode provided within a trench extending vertically into the first surface of the semiconductor body and being separated from the walls of the trench by an insulating layer. Even its this transistor, in accordance with an embodiment of the invention, a lightly doped drift and buffer layer or safety zone, respectively, is provided underneath and between the deep well regions of the opposite conductivity type, and this combined layer or zone has a minimum vertical extension which is at least equal to the minimum lateral distance between the deep well regions.

According to a further embodiment, the vertical extension of this layer or zone is determined such that a total amount of its dopants per unit area is larger than a break down charge amount at break down voltage. Similar as in the above explained semiconductor elements, both design rules to determine a useful extension of the "safety zone" may be combined.

Even in the trench type embodiment of the invention, the dopant concentration of the drift and buffer layer may be constant through the entire thickness of this combined layer, or it may increase towards the adjacent drain contact layer.

According to any of the above embodiments, the deep lightly doped well regions need not necessarily be continuous regions. In a further embodiment of the invention, each

of them may be constituted by a basically vertical stack of separated, bubble-shaped well regions.

In the various embodiments, the "first conductivity type" may, in particular, be the p type, whereas in such case the "second conductivity type" is the n type, both types in general covering all technically reasonable dopant concentrations, i.e. p^- to p^+ ranges or n^- to n^+ ranges, respectively. In one embodiment, in semiconductor elements of the respective reverse type the first conductivity type may be the n type, whereas the second conductivity type is the p type.

The FIGURE schematically illustrates a cross-sectional structure of a power MOS transistor **1** of the trench type including a semiconductor substrate **3** with first and second main surfaces **3**a, **3**b. On the first main surface **3**a, a source contact layer S is provided to connect source regions **5**, whereas at the second main surface **3**b a planar drain contact layer D is provided on a likewise planar drain layer **7**. Gate electrodes G are provided in trenches **9**, each of the gate electrodes being isolated with respect to the semiconductor material by using insulating side wall layers **11** within the respective trench **9**. The general structure of the element is known and will, therefore, not be described in more detail. In particular, the layer structure including several differently doped semiconductor layers is schematically illustrated, the respective conductivity type being designated with the typical numerals "p" or "p^-" or "n^-" or "n^+", respectively.

With regard to the present invention, it should be mentioned that underneath a p body layer **13**, adjacent to the source contact layer S, an arrangement of alternating shallow and deep n-type well regions **15** and p-type well regions **17** is provided within the substrate.

The lightly doped (n^-) region between the deeper wells and underneath all of the wells provides for a buffer or safety zone **19** having the above explained effects on the space-charge behaviour in the high current avalanche situation. Thereby, the zone **20** shown in FIG. **1** refers to a space-charge region, which forms at low current densities in an upper portion of the buffer or safety zone **19**. The zone **20** is also referred to as a drift layer whereas the zone below the border **21** of the space-charge region is referred to as a buffer layer **22**. For this zone or region **19**, the above mentioned rules to determine the vertical extension or dimension are valid.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that a variety of alternate and/or equivalent implementations may be substituted for the specific embodiments shown and described without departing from the scope of the present invention. This application is intended to cover any adaptations or variations of the specific embodiments discussed herein. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

[1. A power MOS transistor of the planar type, comprising:

a semiconductor body having a first and a second surface,

body regions of a first conductivity type and a first dopant concentration formed in the first surface;

a highly doped source region of a second conductivity type having a first dopant concentration, provided at the first surface;

a contact arrangement provided at the first surface, the contact arrangement comprising a gate electrode over an insulating layer on the first surface and source electrode, directly over the first surface and in contact with the source region;

at least two deep, lightly doped well regions of the first conductivity type having a second dopant concentration, and having a minimum lateral distance therebetween;

a highly doped drain contact layer of the second conductivity type and a second dopant concentration provided in or on the second surface of the semiconductor body; and

an electrode provided on the free surface of the drain contact layer;

wherein underneath and between the deep well regions of the first conductivity type a lightly doped drift and buffer layer of the second conductivity type and a third dopant concentration is provided, wherein the drift and buffer layer has a minimum vertical extension between the drain contact layer and the bottom of the deepest well region which is at least equal to the minimum lateral distance between the deep well regions

wherein the vertical extension of the drift and buffer layer amounts to at least twice the minimum lateral distance between the deep well regions; and

wherein the vertical extension of the drift and buffer layer between the drain contact layer and the bottom of the deepest well region is determined such that a total amount of its dopants per unit area is larger than a breakdown charge amount.**]**

[2. The power transistor of claim **1**, wherein the second dopant concentration in the drift and buffer layer increases towards the drain contact layer.**]**

[3. The power transistor of claim **1**, of the superjunction type, wherein the deep, lightly doped well regions are constituted by a basically vertical stack of separated, bubble-shaped well regions.**]**

[4. The power transistor of claim **1**, wherein the semiconductor body and the drift and buffer layer comprise a semiconductor substrate and the drain contact layer comprises an ion implantation layer within the semiconductor substrate.**]**

[5. The power transistor of claim **1**, wherein the second dopant concentration is constant through the drift and buffer layer.**]**

[6. The power transistor of claim **1**, wherein an interface between the drift and buffer layer and the drain contact layer comprises valleys under the deep well regions.**]**

7. A super junction power transistor of a trench type, comprising:

a semiconductor body having a first surface and a second surface;

a body region of a first conductivity type and a first dopant concentration formed in the first surface;

a source region of a second conductivity type provided at the first surface;

a contact arrangement which comprises a source electrode over a first insulating layer on the first surface and in contact with the source region and a gate electrode provided within a trench extending vertically into the first surface of the semiconductor body and being separated from walls of the trench by a second insulating layer;

at least two deep well regions of the first conductivity type having a second dopant concentration, the deep well regions having a minimum lateral distance therebetween and having a shallow well region disposed therebetween, and wherein the deep well regions are constituted by a vertical stack of bubble-shaped well regions;

a drain contact layer of the second conductivity type provided at the second surface;

an electrode provided on a surface of the drain contact layer; and

a drift and buffer layer of the second conductivity type and including a third dopant concentration, wherein the drift and buffer layer is provided underneath the deep well regions of the first conductivity type,

wherein the drift and buffer layer has a minimum vertical extension between the drain contact layer and a bottom of a deepest well region of the deep well regions and which is at least equal to the minimum lateral distance between the deep well regions.

8. The super junction power transistor of claim 7, wherein the minimum vertical extension of the drift and buffer layer amounts to at least twice the minimum lateral distance between the deep well regions.

9. The super junction power transistor of claim 7, wherein the minimum vertical extension of the drift and buffer layer between the drain contact layer and the bottom of the deepest well region is determined such that a total amount of its dopants per unit area is larger than a breakdown charge amount.

10. The super junction power transistor of claim 7, wherein the third dopant concentration in the drift and buffer layer increases towards the drain contact layer.

11. The super junction power transistor of claim 7, wherein the third dopant concentration is constant through the drift and buffer layer.

12. The super junction power transistor of claim 7, wherein the semiconductor body and the drift and buffer layer comprise a semiconductor substrate and the drain contact layer comprises an ion implantation layer within the semiconductor substrate.

13. The super junction power transistor of claim 7, wherein the power semiconductor is capable of blocking at least one reverse voltage within a range of 40 V to 1200V.

14. The super junction power transistor of claim 7, wherein the minimum vertical extension of the drift and buffer layer is determined such that the total amount of the dopants per unit area is within a range of a factor of 1.5-2.5 of a charge at breakdown voltage.

15. The super junction power transistor of claim 7, further comprising a drift layer of the second conductivity type, located between the deep well regions and having a fourth dopant concentration,

wherein the third dopant concentration is located underneath the deep well regions and is within a range of a factor of 0.01 to 3 of the fourth dopant concentration.

16. A super junction power transistor of a trench type, comprising:

a semiconductor body having a first surface and a second surface;

a body region of a first conductivity type and a first dopant concentration formed in the first surface;

a source region of a second conductivity type provided at the first surface;

a contact arrangement with a trench which extends into the first surface;

at least two well regions of the first conductivity type having a second dopant concentration, and having a minimum lateral distance therebetween;

a drain contact layer of the second conductivity type provided at the second surface;

an electrode provided on a surface of the drain contact layer; and

a drift and buffer layer of the second conductivity type and including a third dopant concentration is provided underneath the well regions of the first conductivity type,

wherein the drift and buffer layer has a minimum vertical extension between the drain contact layer and a bottom of a deepest well region of the well regions and which is at least equal to the minimum lateral distance between the well regions.

17. The super junction power transistor of claim 16, wherein the contact arrangement comprises a gate electrode provided within the trench extending vertically into the first surface of the semiconductor body and being separated from walls of the trench by a second insulating layer.

18. The super junction power transistor of claim 16, wherein the well regions are constituted by a vertical stack of bubble-shaped well regions.

19. The super junction power transistor of claim 16, wherein the minimum vertical extension of the drift and buffer layer amounts to at least twice the minimum lateral distance between the well regions.

20. The super junction power transistor of claim 16, wherein the minimum vertical extension of the drift and buffer layer between the drain contact layer and the bottom of the deepest well region is determined such that a total amount of its dopants per unit area is larger than a breakdown charge amount.

21. The super junction power transistor of claim 16, wherein the third dopant concentration in the drift and buffer layer increases towards the drain contact layer.

22. The super junction power transistor of claim 16, wherein the third dopant concentration is constant through the drift and buffer layer.

23. The super junction power transistor of claim 16, wherein the semiconductor body and the drift and buffer layer comprise a semiconductor substrate and the drain contact layer comprises an ion implantation layer within the semiconductor substrate.

24. The super junction power transistor of claim 16, wherein the power semiconductor is capable of blocking at least one reverse voltage within a range of 40 V to 1200V.

25. The super junction power transistor of claim 16, wherein the minimum vertical extension of the drift and buffer layer is determined such that the total amount of the dopants per unit area is within a range of a factor of 1.5-2.5 of a charge at breakdown voltage.

26. The super junction power transistor of claim 16, further comprising a drift layer of the second conductivity type, located between the well regions, and having a fourth dopant concentration,

wherein the third dopant concentration is located underneath the well regions and is within a range of a factor of 0.01 to 3 of the fourth dopant concentration.

27. A power semiconductor, comprising:

a semiconductor body having a first surface and a second surface;

a body region of a first conductivity type and a first dopant concentration formed in the first surface;

a source region of a second conductivity type provided at the first surface;

a contact arrangement provided at the first surface;

at least two well regions of the first conductivity type having a second dopant concentration, and having a minimum lateral distance therebetween;

a drain contact layer of the second conductivity type provided in or on the second surface of the semiconductor body;

an electrode provided on a surface of the drain contact layer;

a drift layer of the second conductivity type, wherein the drift layer is provided underneath and between the well regions of the first conductivity type; and

a buffer layer of the second conductivity type provided underneath the drift layer,

wherein a portion of the drift layer that is provided underneath the well regions combined with the buffer layer have a minimum vertical extension between the drain contact layer and a bottom of a deepest well region of the well regions and which is at least equal to the minimum lateral distance between the well regions,

wherein the power semiconductor is a super junction power transistor of a trench type.

28. The power semiconductor of claim 27, wherein the contact arrangement comprises a gate electrode provided within a trench extending vertically into the first surface of the semiconductor body and being separated from walls of the trench by a second insulating.

29. The power semiconductor of claim 27, wherein the deep, lightly doped well regions are constituted by a vertical stack of bubble-shaped well regions.

30. The power semiconductor of claim 27, wherein the minimum vertical extension amounts to at least twice the minimum lateral distance between the well regions.

31. The power semiconductor of claim 27, wherein the minimum vertical extension is determined such that a total amount of its dopants per unit area is larger than a break-down charge amount.

32. The power semiconductor of claim 27, wherein the semiconductor body, the drift layer and the buffer layer comprise a semiconductor substrate and the drain contact layer comprises an ion implantation layer within the semi-conductor substrate.

33. The power semiconductor of claim 27, wherein the power semiconductor is capable of blocking at least one reverse voltage within a range of 40 V to 1200V.

34. The power semiconductor of claim 27, wherein the minimum vertical extension is determined such that the total amount of the dopants per unit area is within a range of a factor of 1.5-2.5 of a charge at breakdown voltage.

35. The power semiconductor of claim 27, wherein the portion of the drift layer provided underneath the well regions and the buffer layer together include a third dopant concentration, and

the drift layer, located between the well regions, has a fourth dopant concentration, wherein the third dopant concentration is within a range of a factor of 0.01 to 3 of the fourth dopant concentration.

36. The power semiconductor of claim 35, wherein the third dopant concentration increases towards the drain contact layer.

37. The power semiconductor of claim 35, wherein the third dopant concentration is constant through the portion of the drift layer that is provided underneath the well regions and the buffer layer.

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