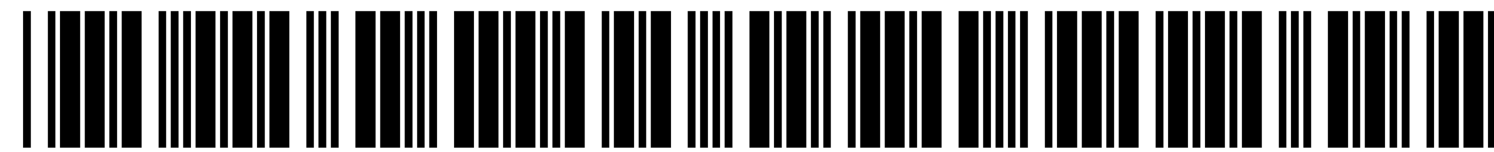

(19) **United States**
(12) **Reissued Patent**
Nii

(10) **Patent Number: US RE47,679 E**
(45) **Date of Reissued Patent: Oct. 29, 2019**

(54) **SEMICONDUCTOR MEMORY**

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(73) Assignee: **RENESAS ELECTRONICS CORPORATION**, Tokyo (JP)

(21) Appl. No.: **15/377,664**

(22) Filed: **Dec. 13, 2016**

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Issued: **Nov. 4, 2003**
Appl. No.: **10/350,221**
Filed: **Jan. 24, 2003**

U.S. Applications:
(63) Continuation of application No. 13/863,011, filed on Apr. 15, 2013, now Pat. No. Re. 46,272, which is a continuation of application No. 12/846,450, filed on Jul. 29, 2010, now Pat. No. Re. 44,242, which is a continuation of application No. 11/265,744, filed on Nov. 3, 2005, now Pat. No. Re. 41,638, which is an
(Continued)

(30) **Foreign Application Priority Data**

Dec. 6, 2000 (JP) 2000-371153

(51) **Int. Cl.**
G11C 11/00 (2006.01)
G11C 11/412 (2006.01)
G11C 5/00 (2006.01)

(52) **U.S. Cl.**
CPC *G11C 11/4125* (2013.01); *G11C 5/005* (2013.01)

(58) **Field of Classification Search**
CPC G11C 11/4125; G11C 5/005
USPC 365/154, 226, 230.05, 181
See application file for complete search history.

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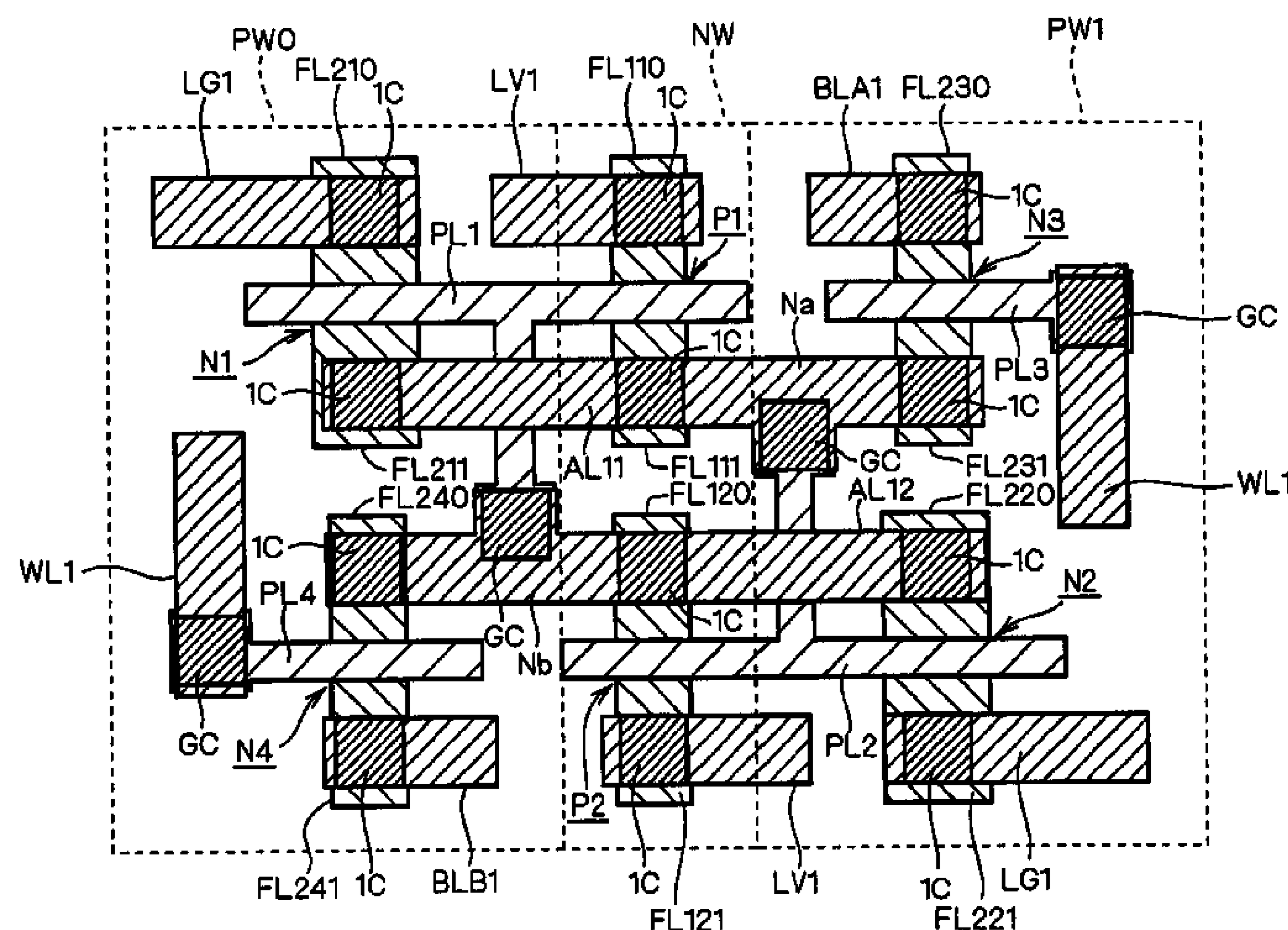
Primary Examiner — Angela M Lie
(74) *Attorney, Agent, or Firm* — McDermott Will & Emery LLP

(57) **ABSTRACT**

A semiconductor memory having a memory cell structure capable of reducing soft error without complicating a circuit configuration. Specifically, an inverter (I**1**) consists of a NMOS transistor (N**1**) and a PMOS transistor (P**1**), and an inverter (I**2**) consists of a NMOS transistor (N**2**) and a PMOS transistor (P**2**). The inverters (I**1**, I**2**) are subjected to cross section. The NMOS transistor (N**1**) is formed within a P well region (PW**0**), and the NMOS transistor (N**2**) is formed within a P well region (PW**1**). The P well regions (PW**0**, PW**1**) are oppositely disposed with an N well region (NW) interposed therebetween.

8 Claims, 37 Drawing Sheets



Related U.S. Application Data

application for the reissue of Pat. No. 6,643,167, which is a continuation of application No. 09/900,917, filed on Jul. 10, 2001, now Pat. No. 6,529,401.

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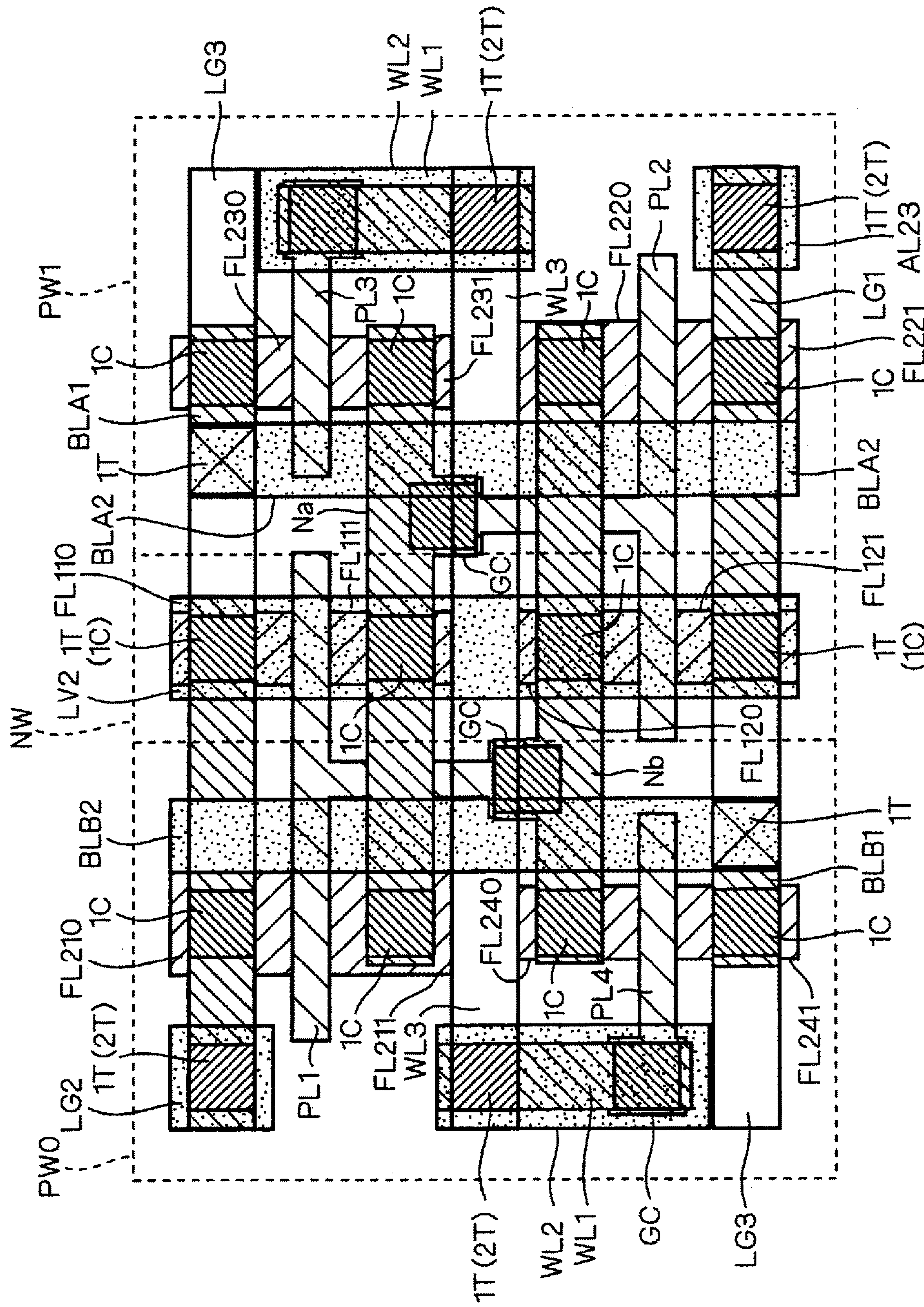

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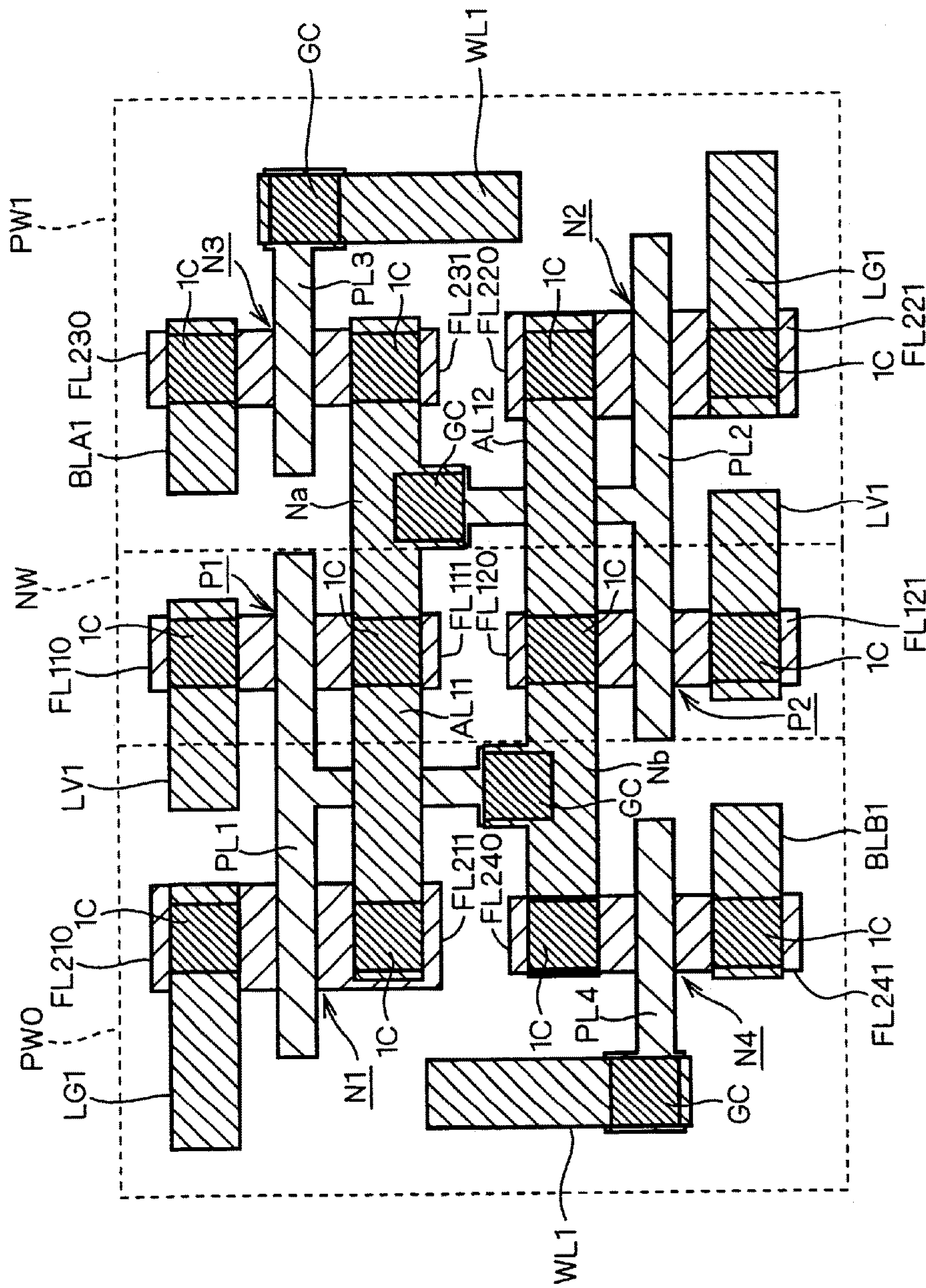

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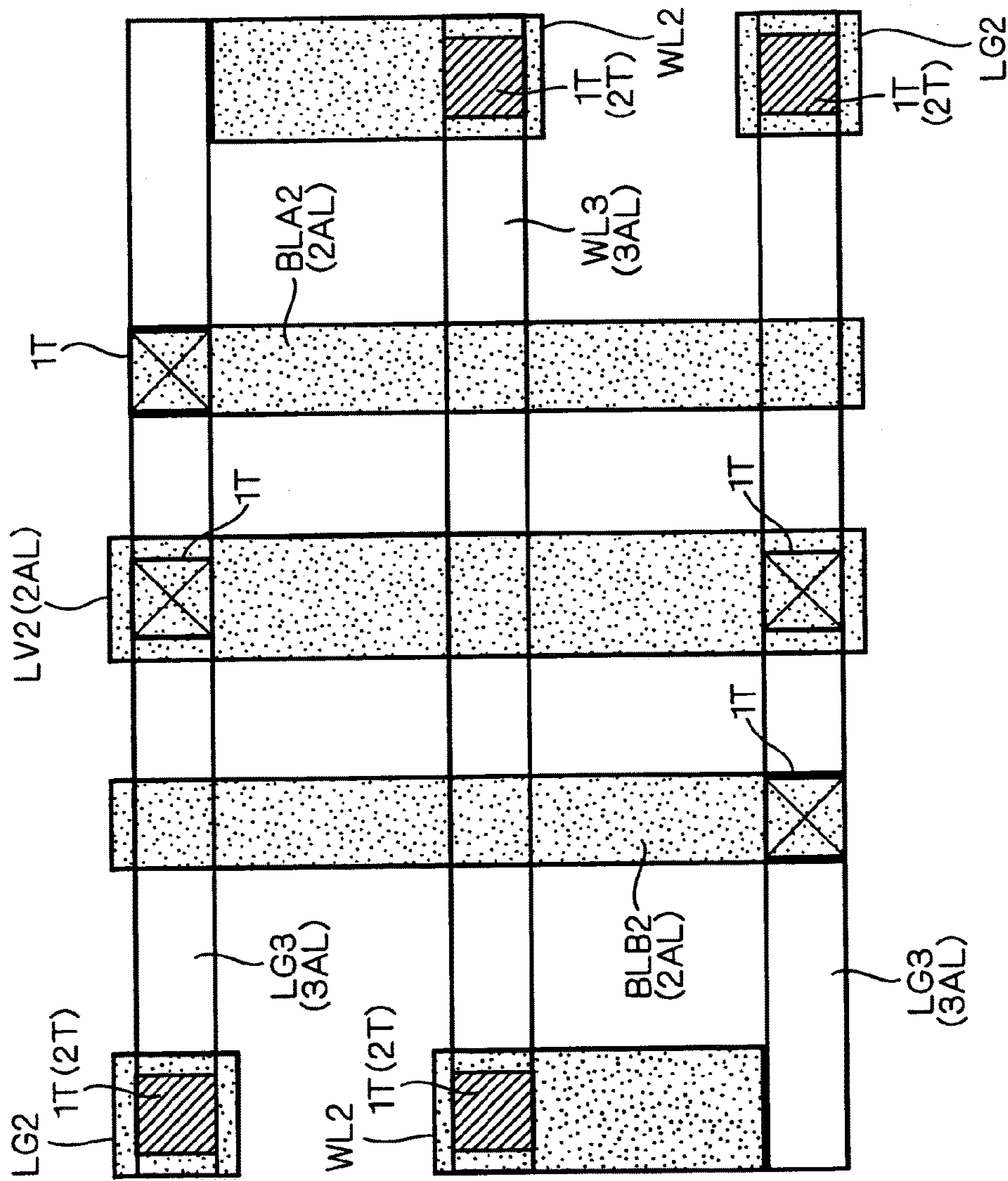
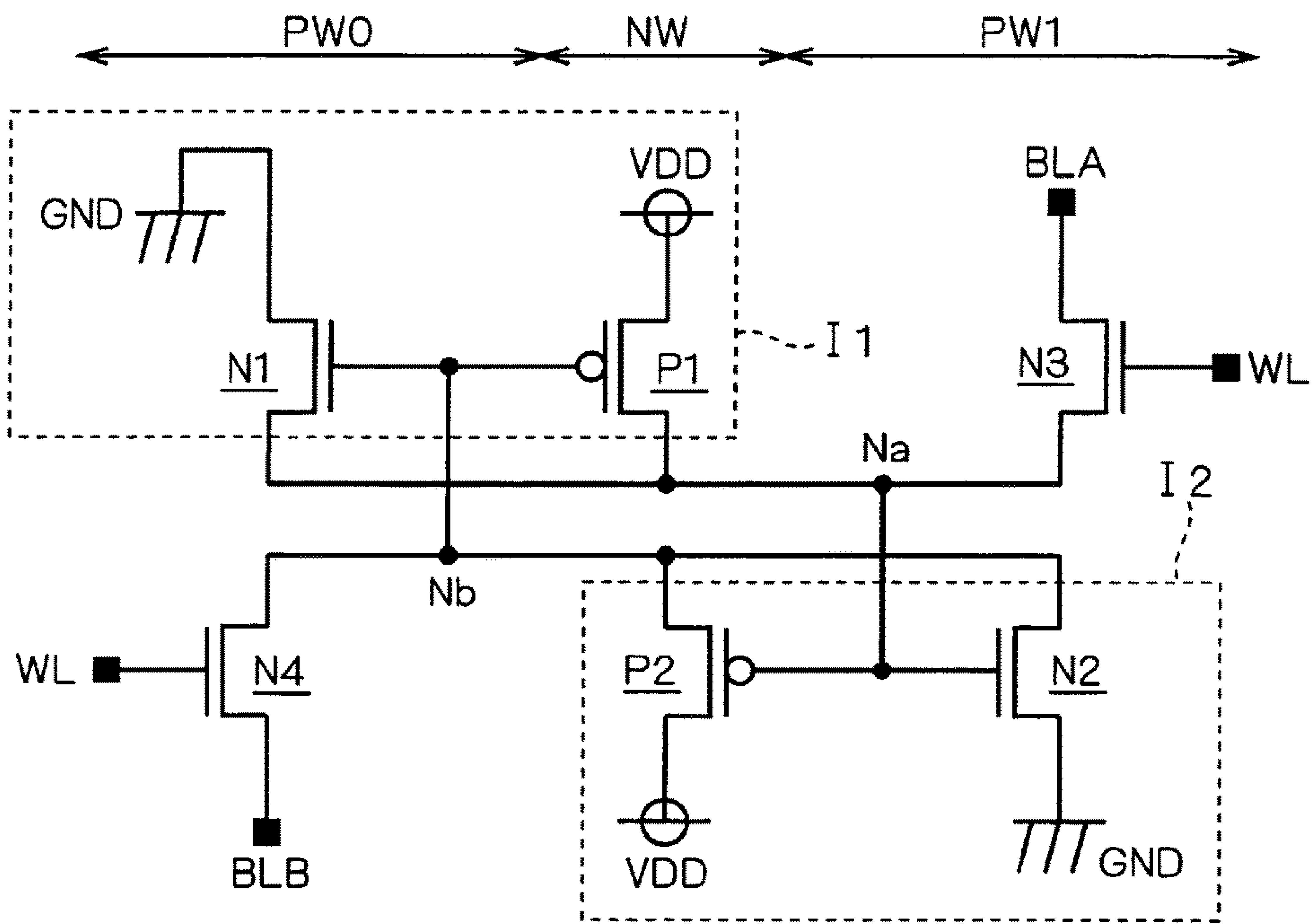


FIG. 3

F I G . 4



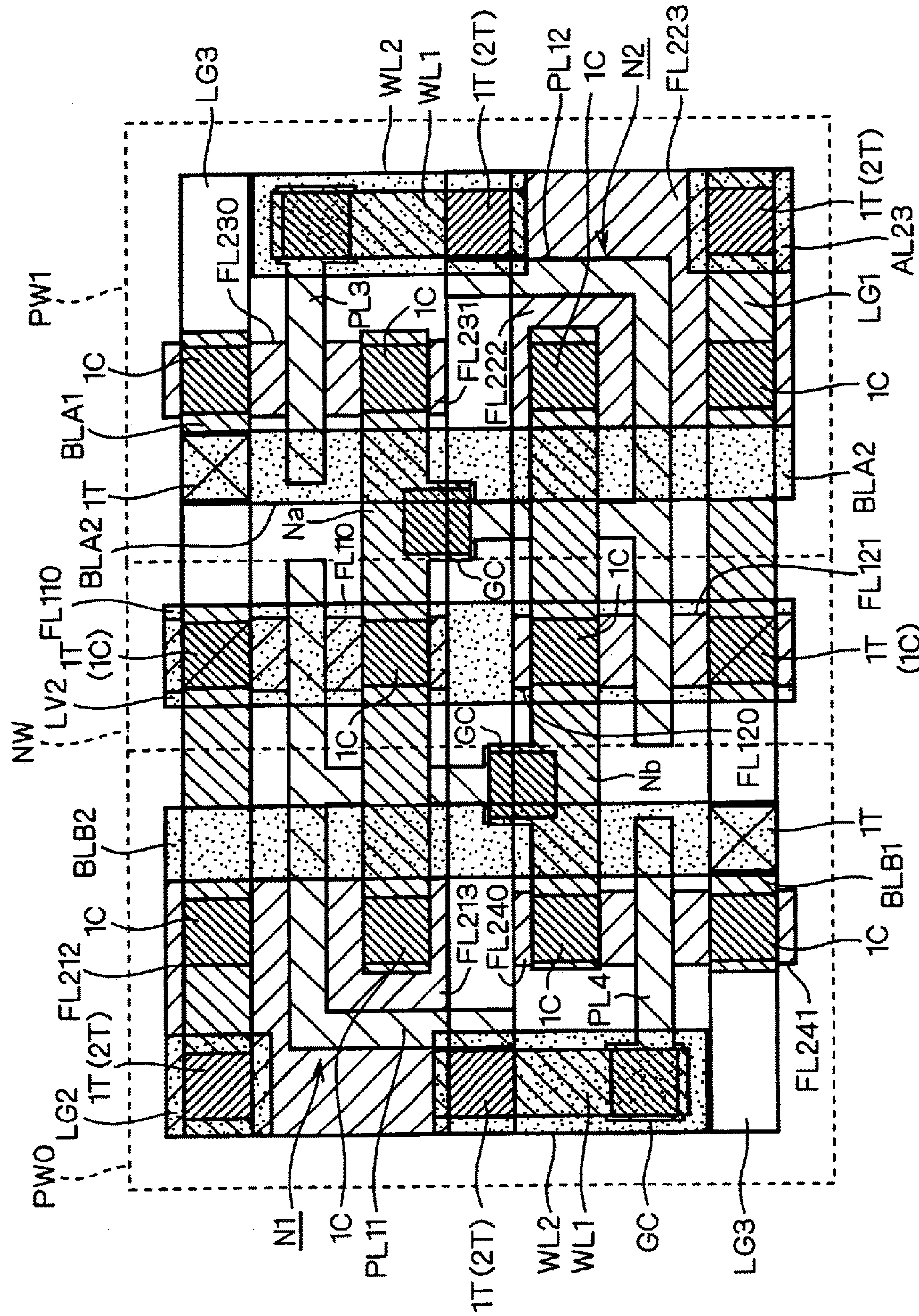
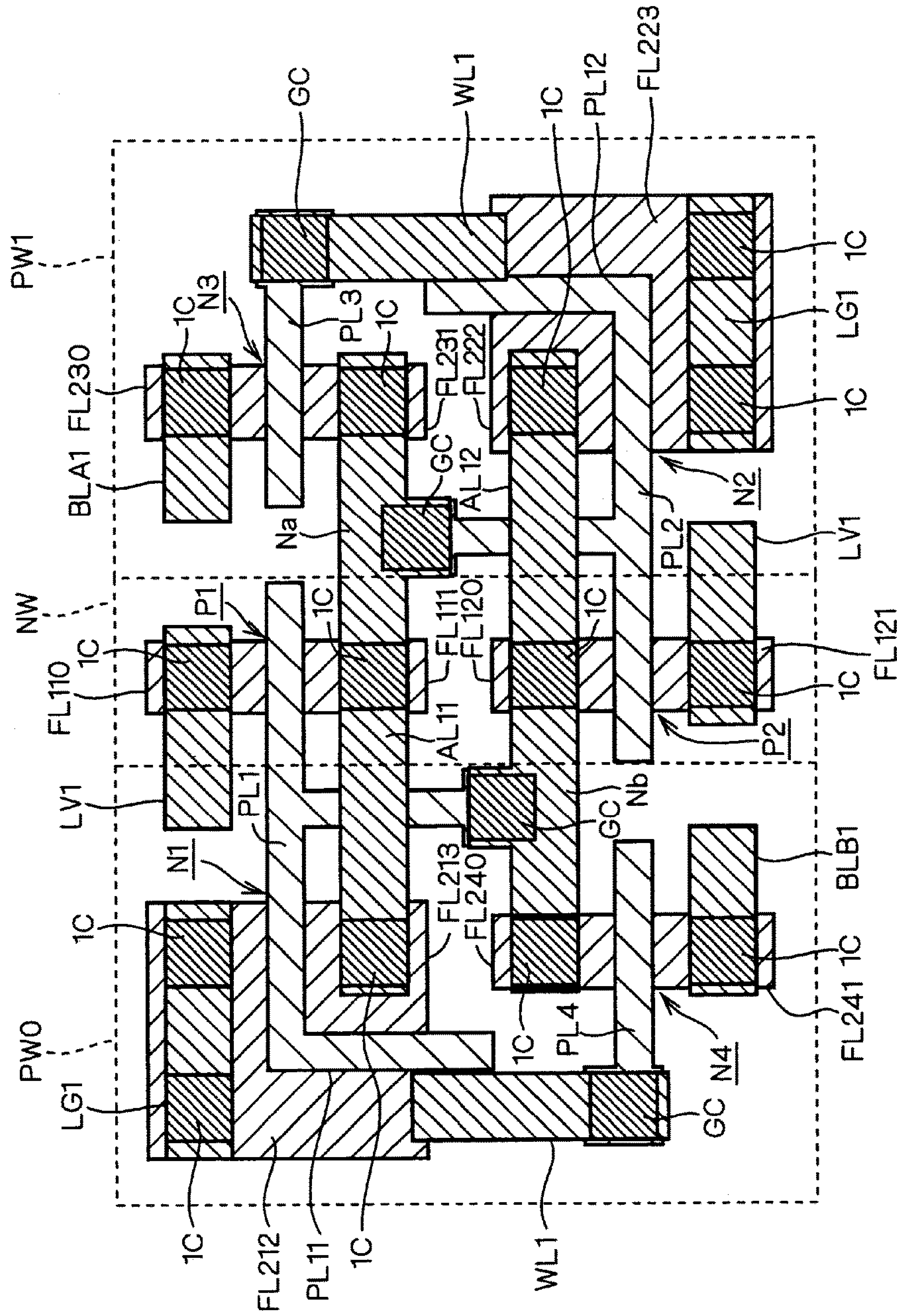


FIG. 5



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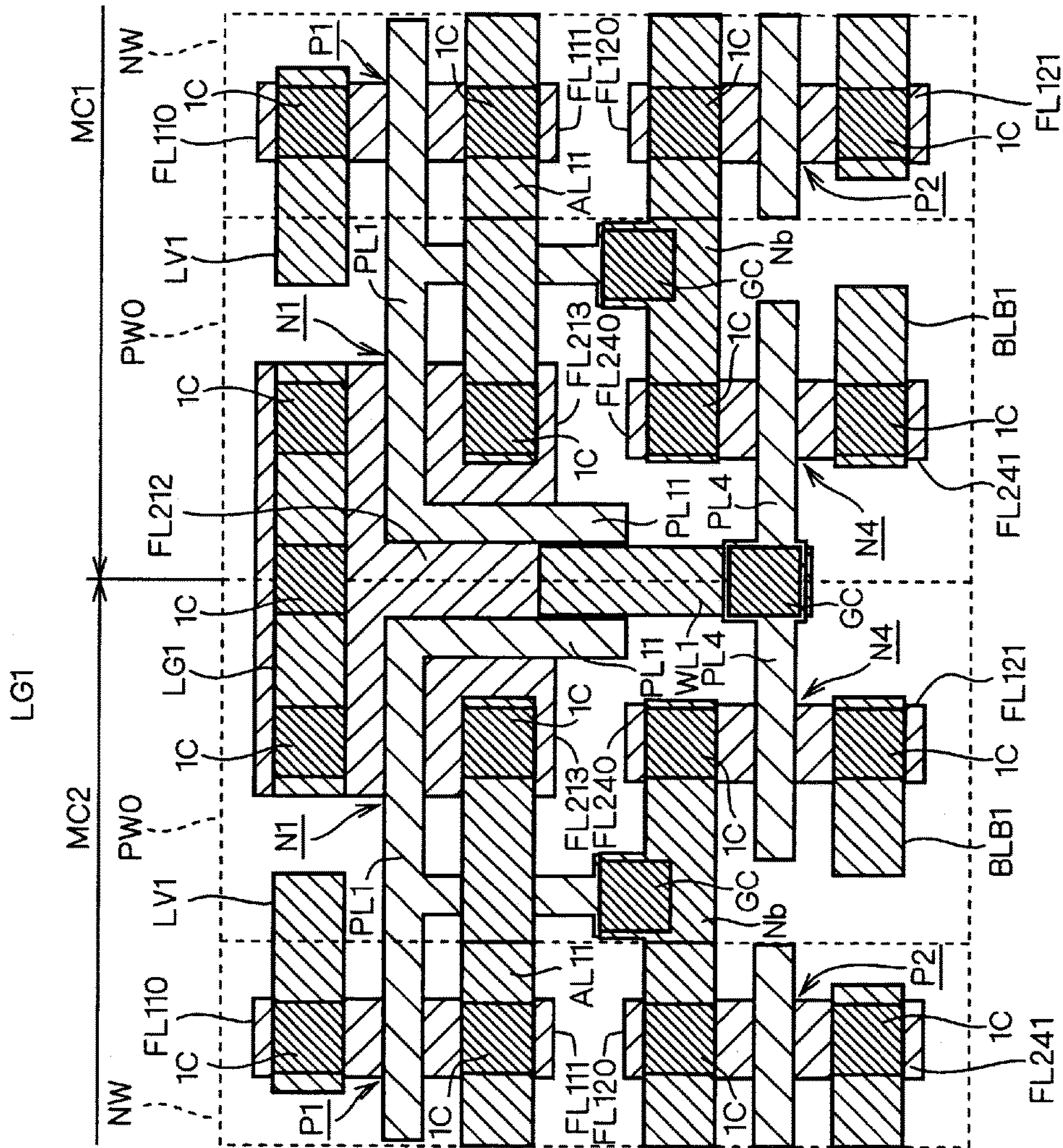

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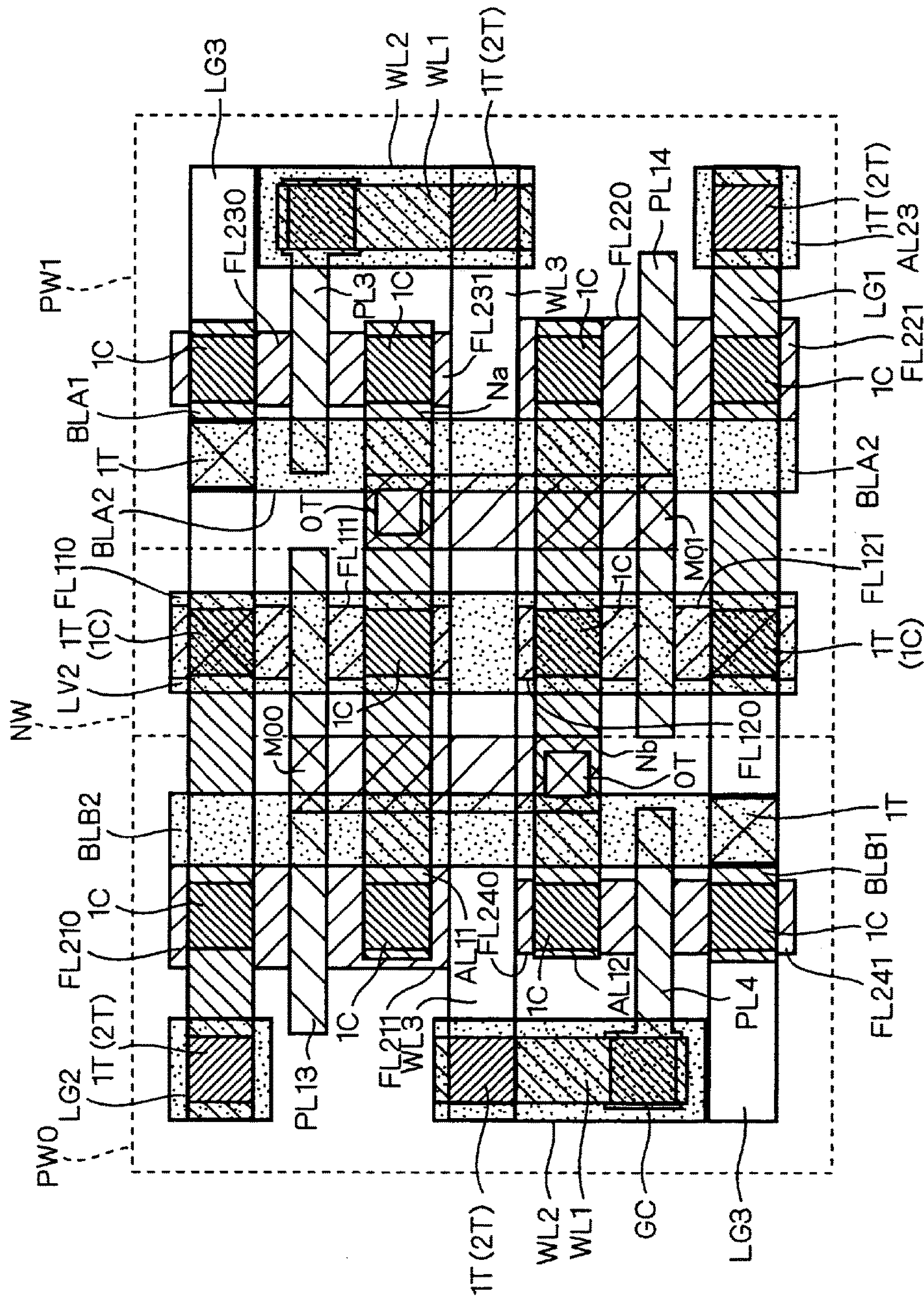

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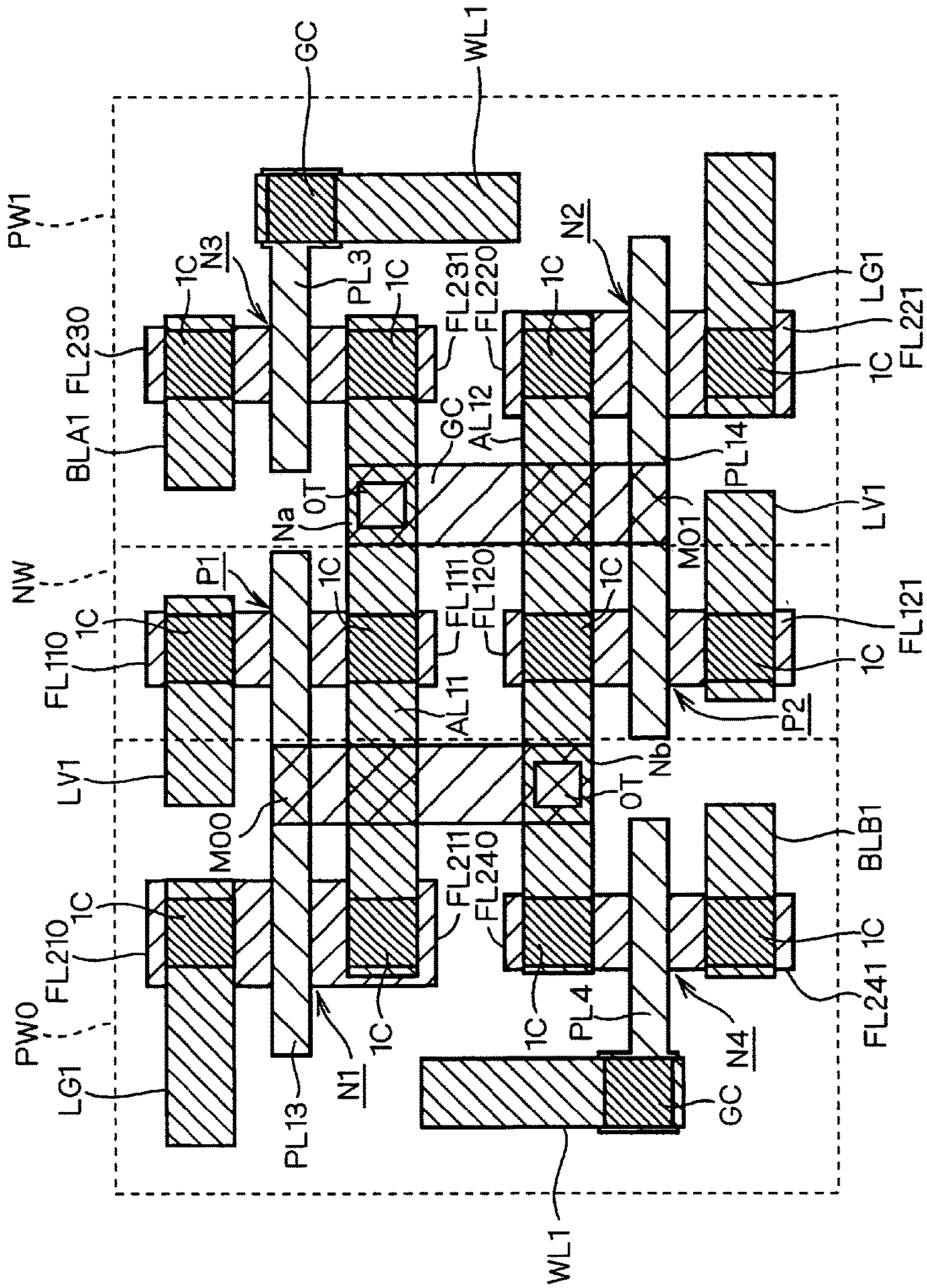
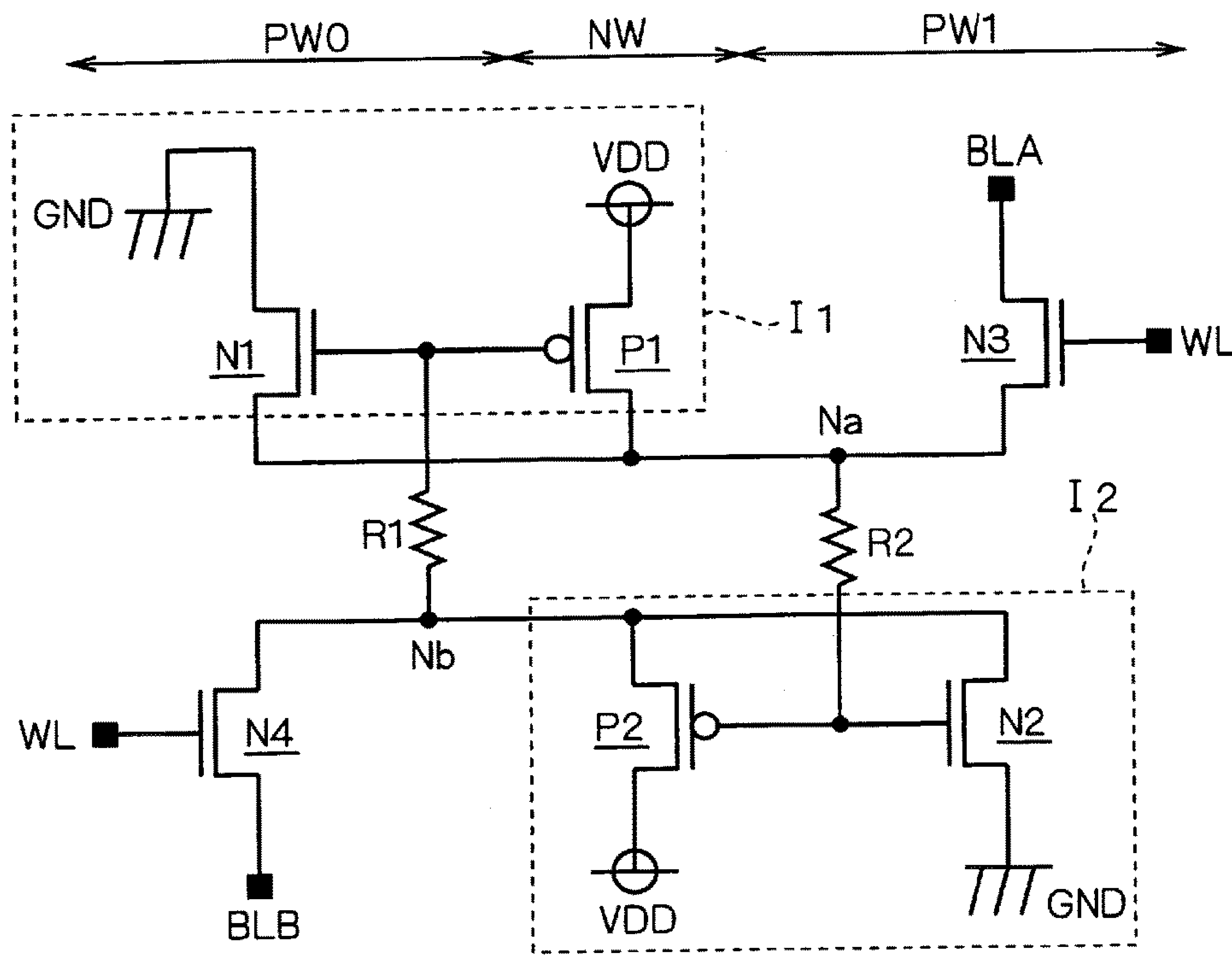
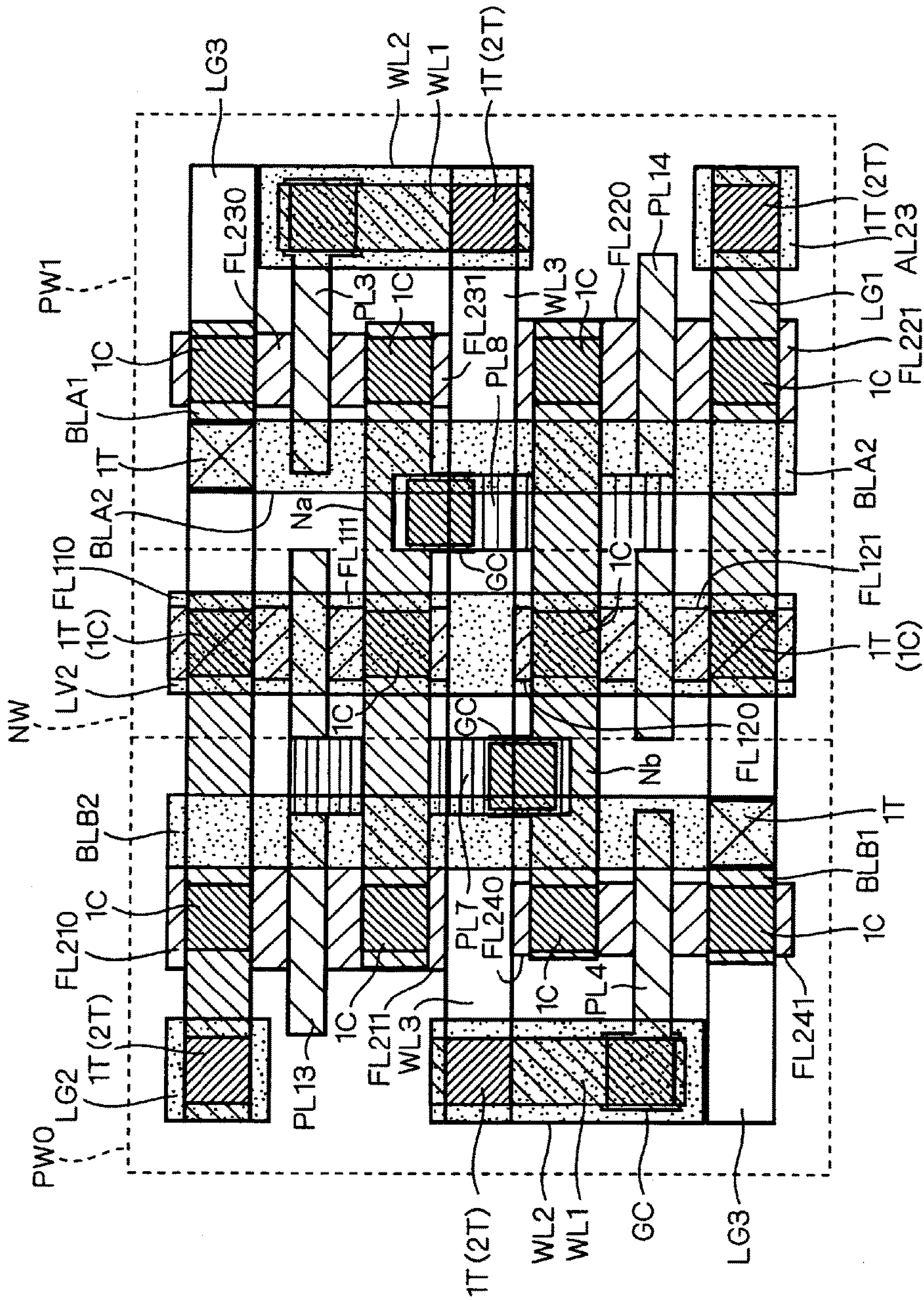


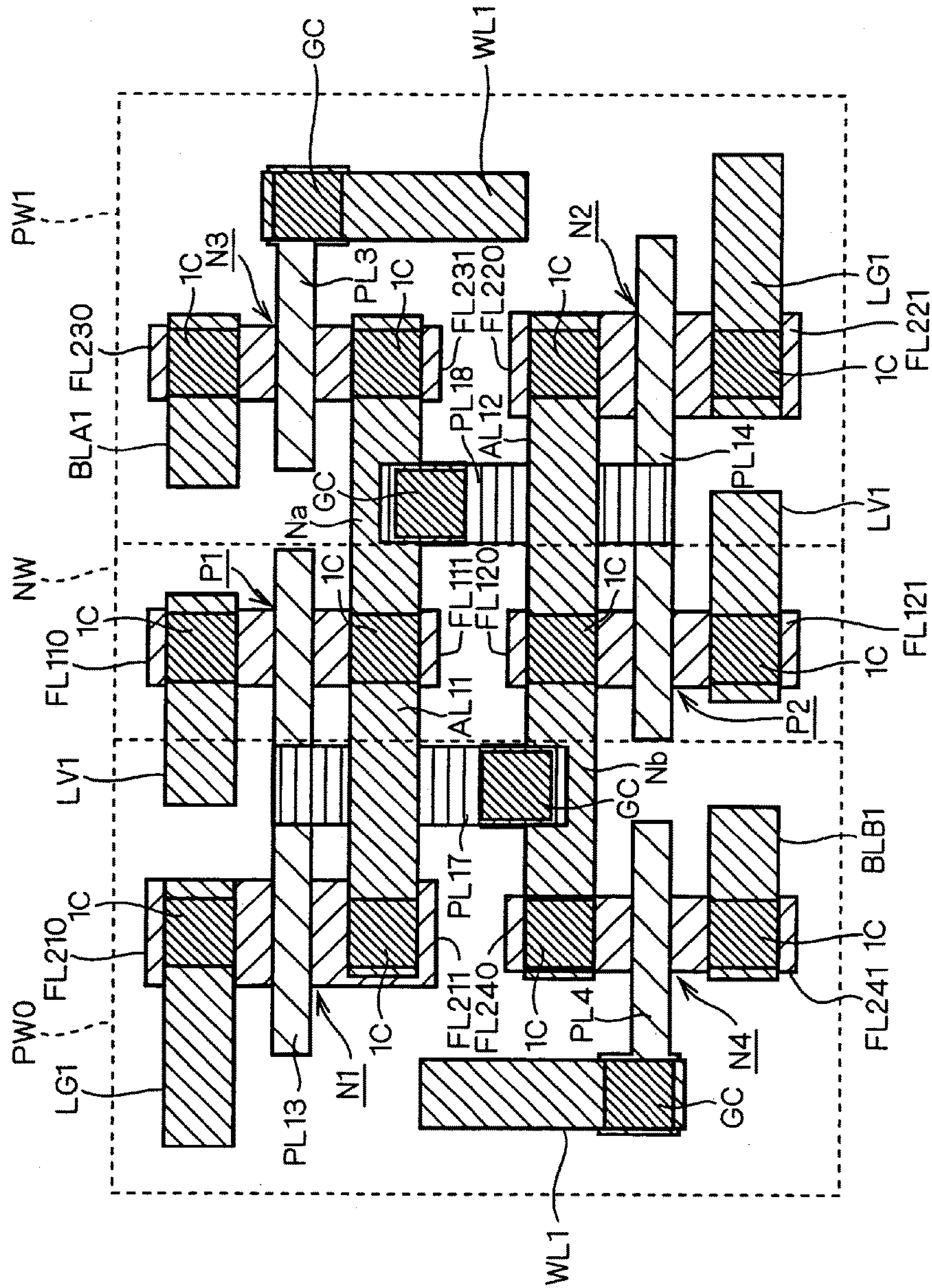
F I G . 9

F I G . 1 0





F I G . 1 1



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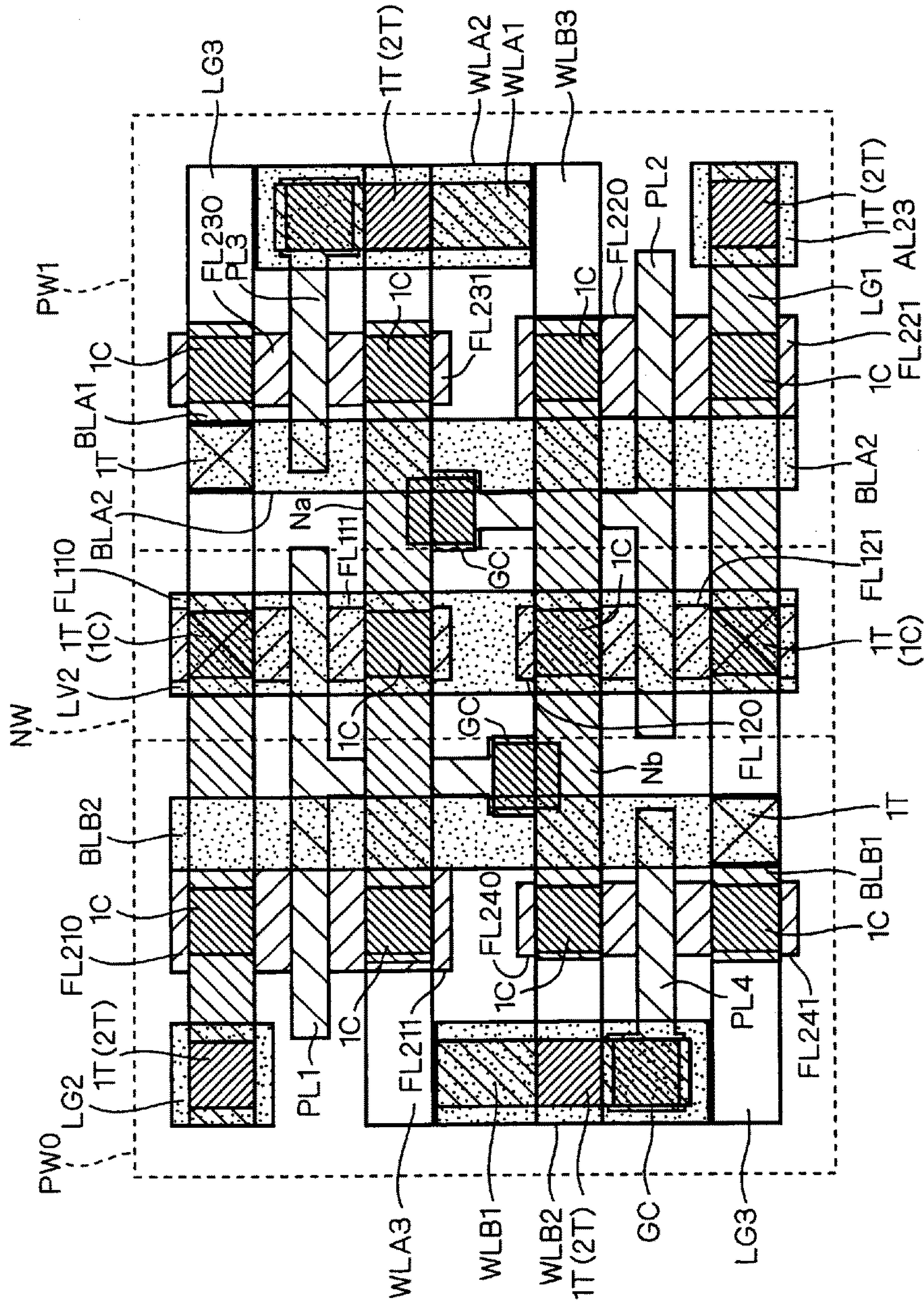

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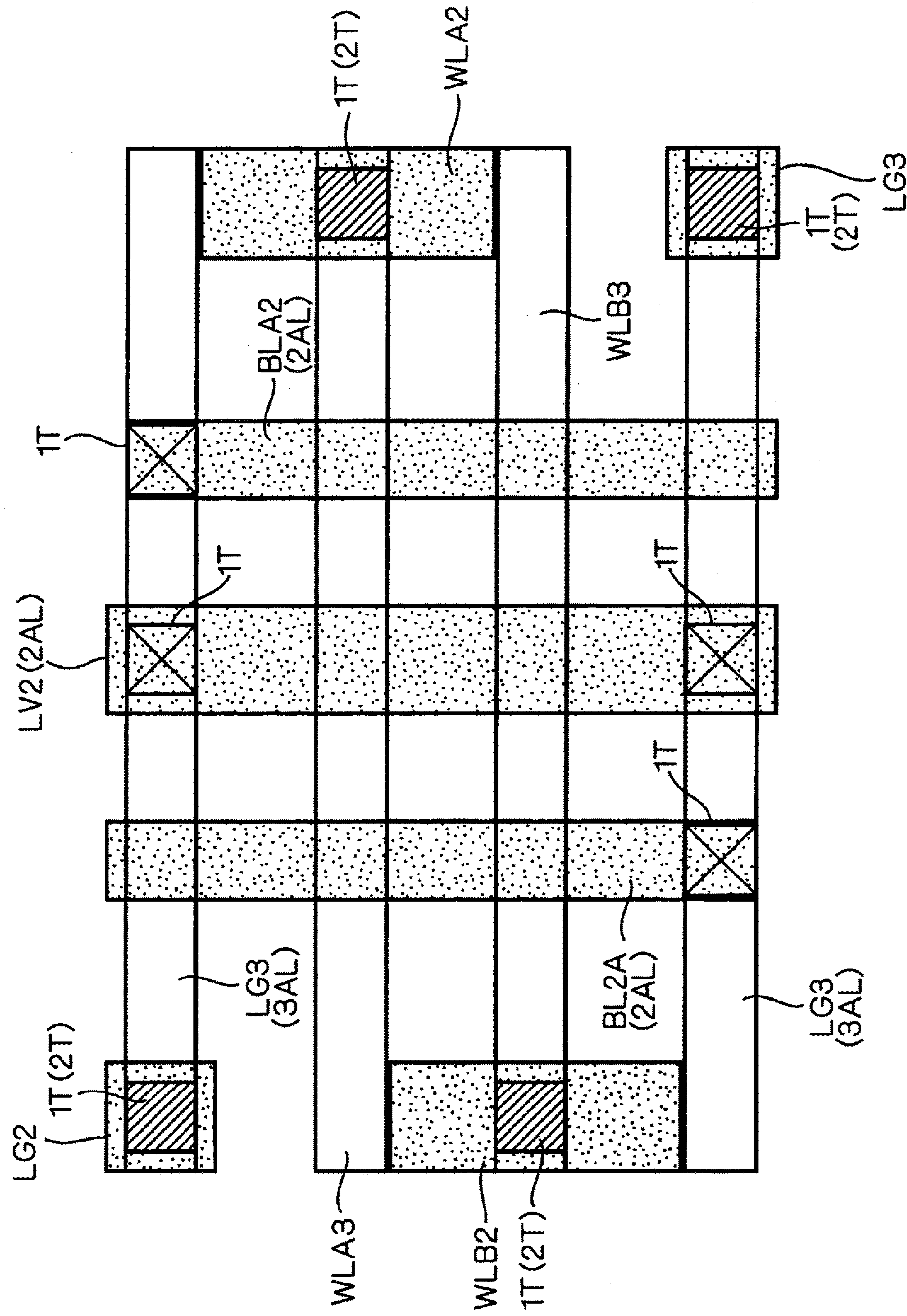
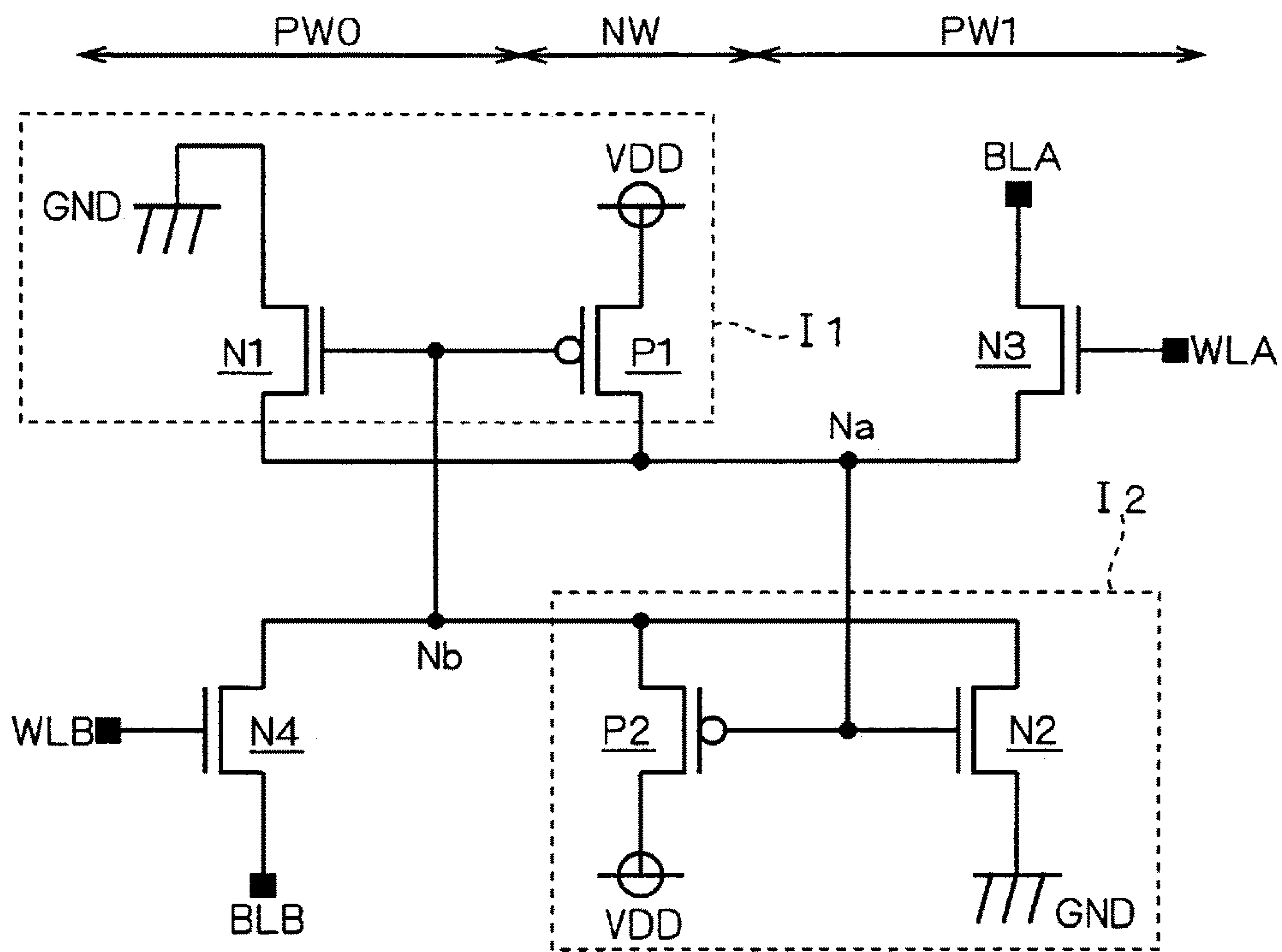


FIG. 14

F I G . 1 5



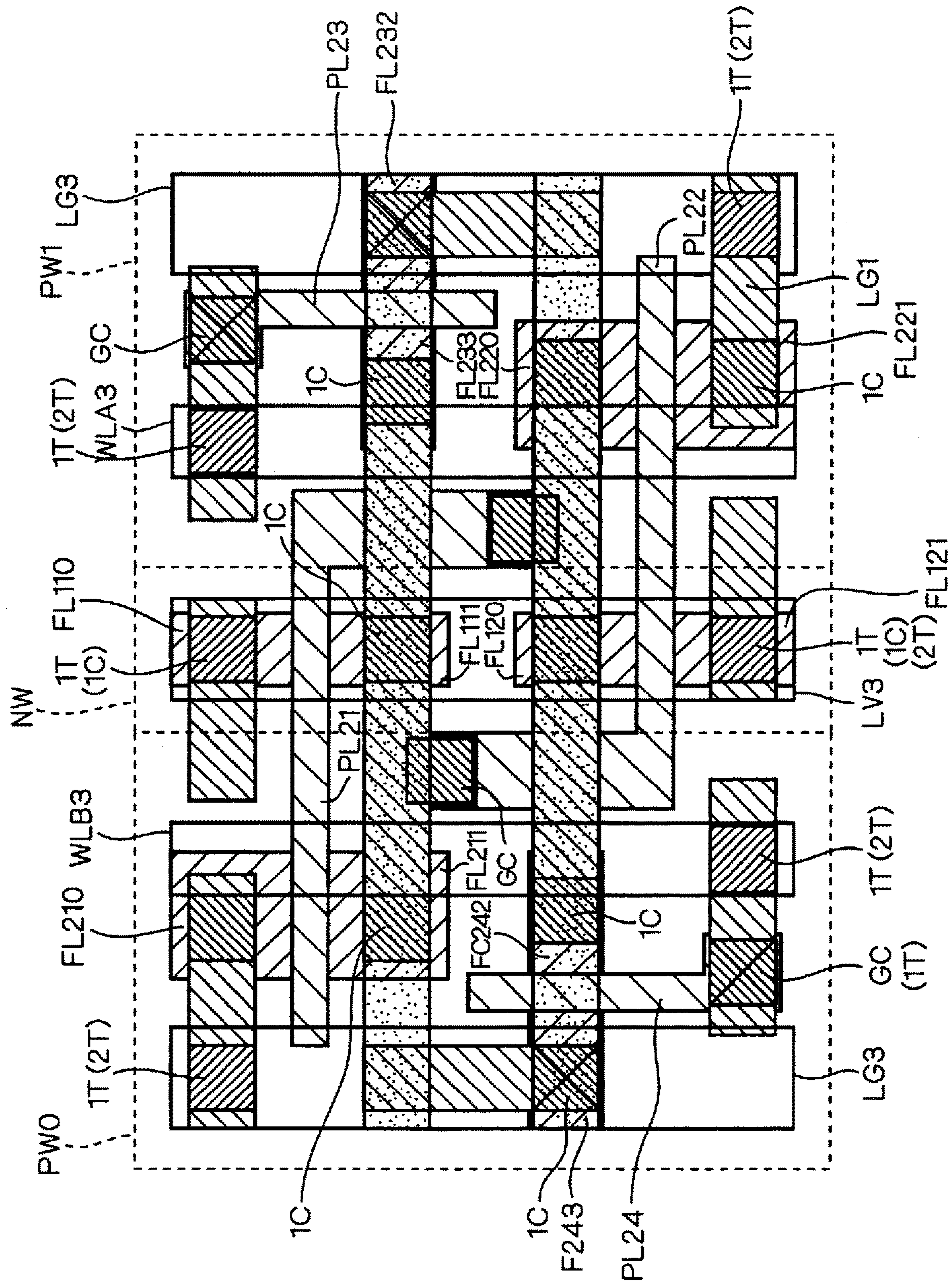
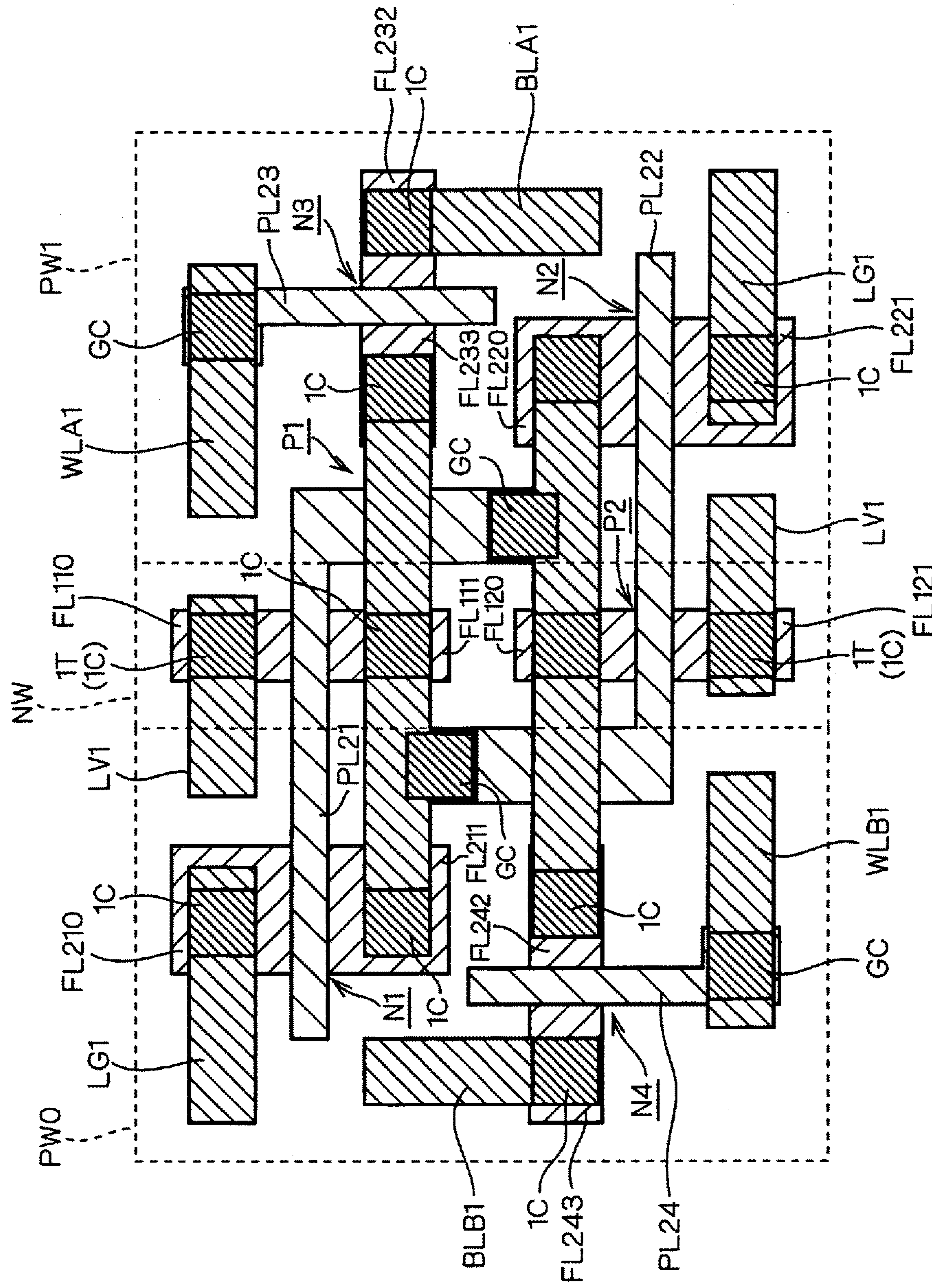


FIG. 16



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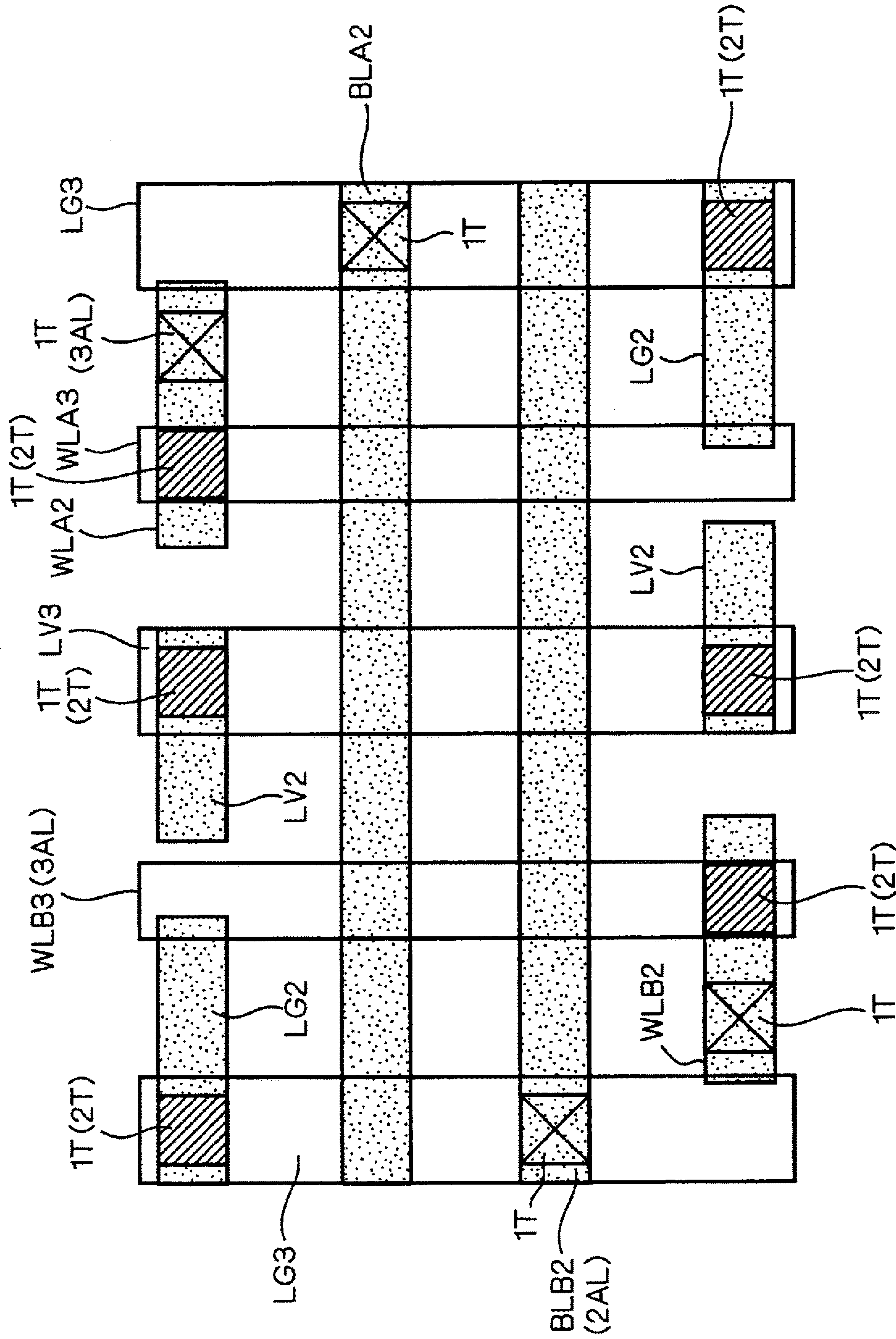


FIG. 18

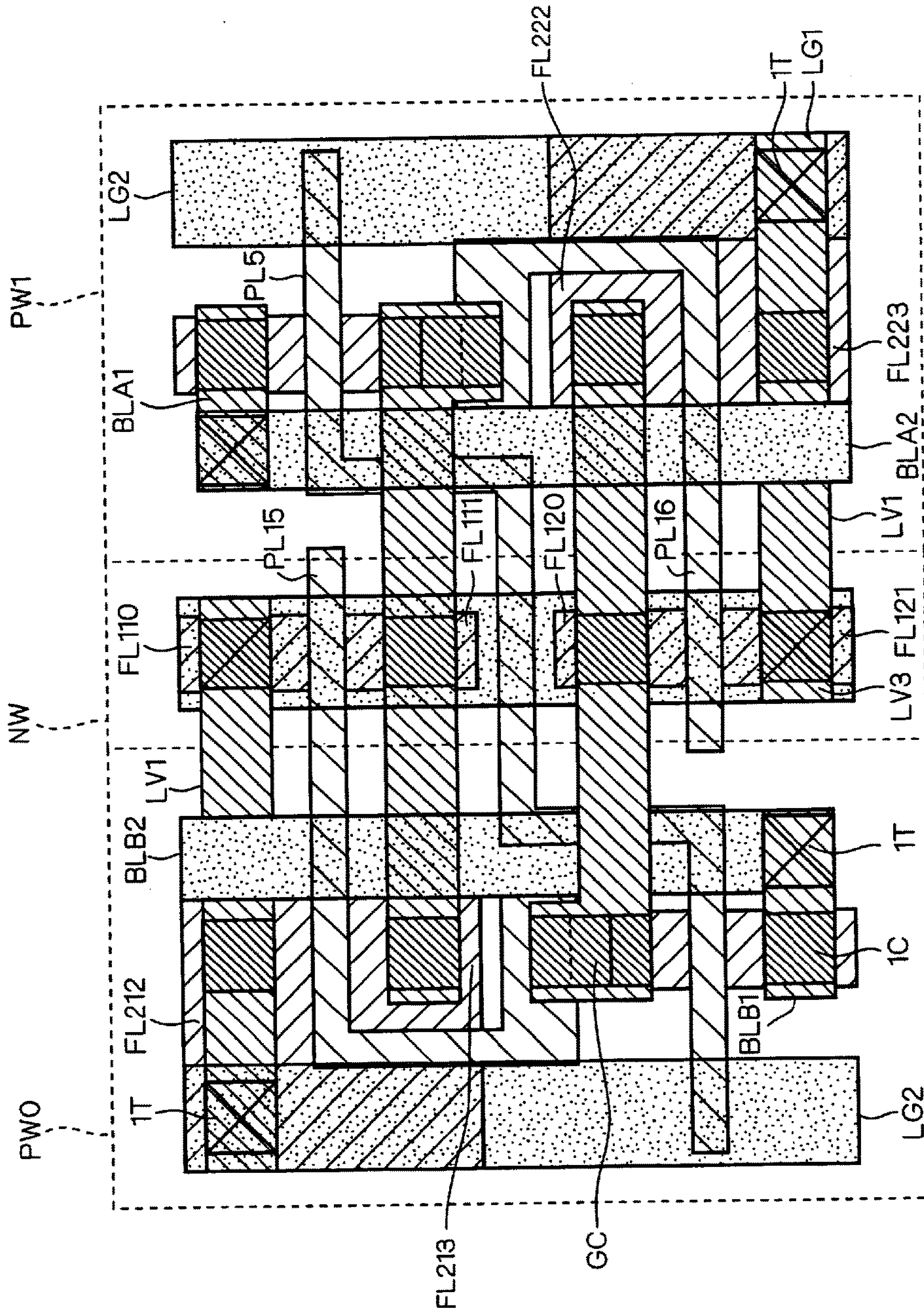


FIG. 19

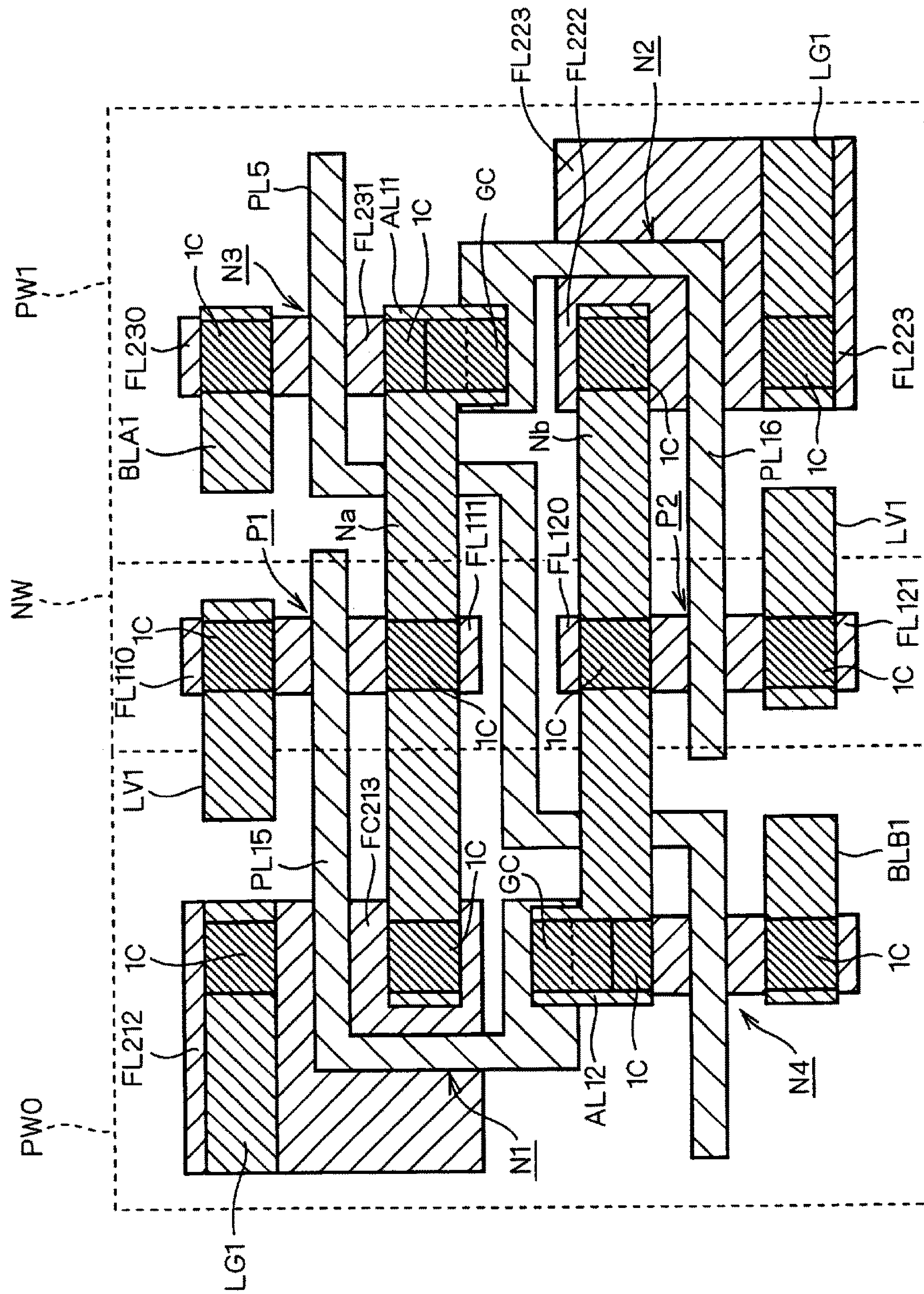


FIG. 20

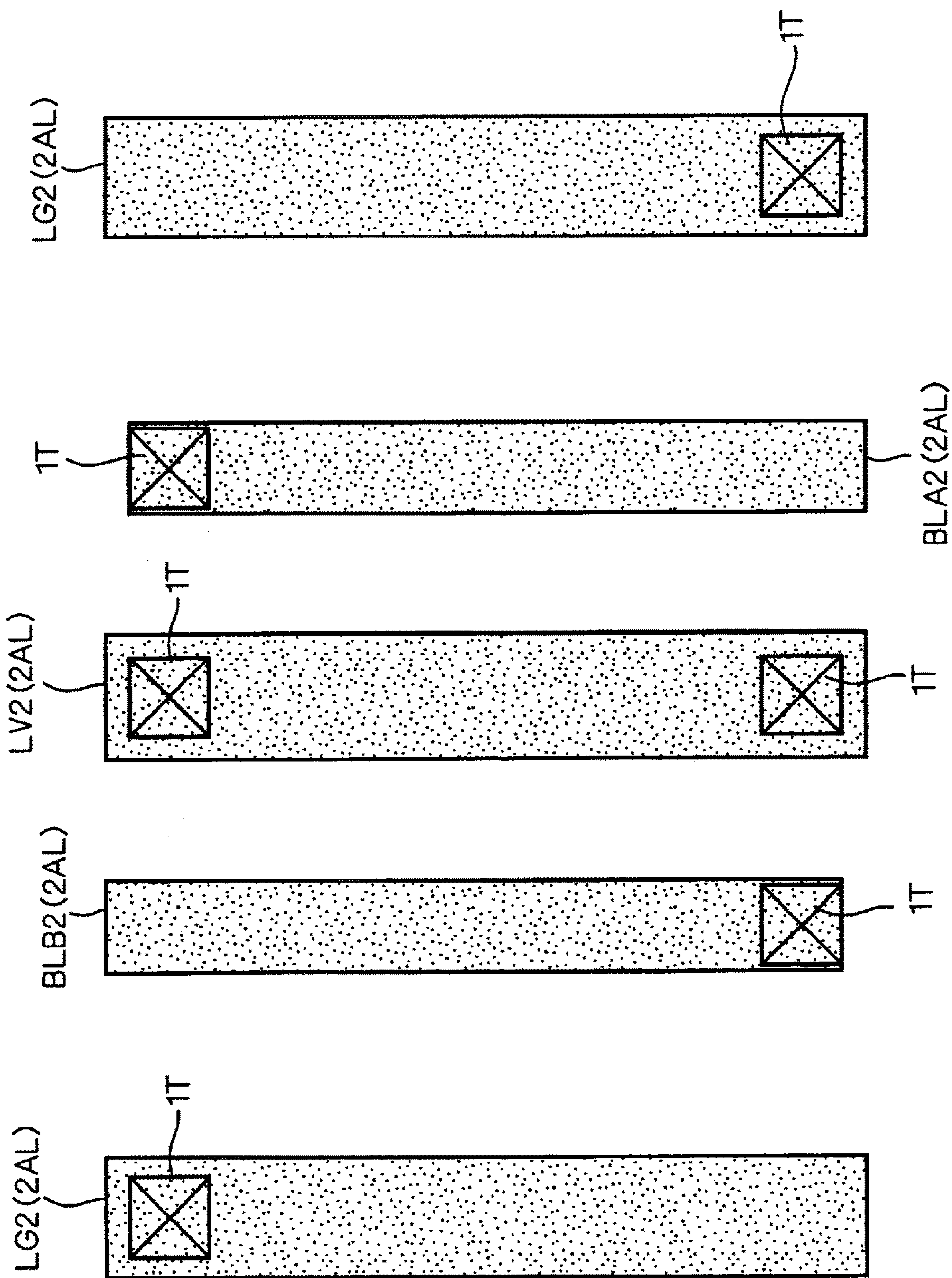
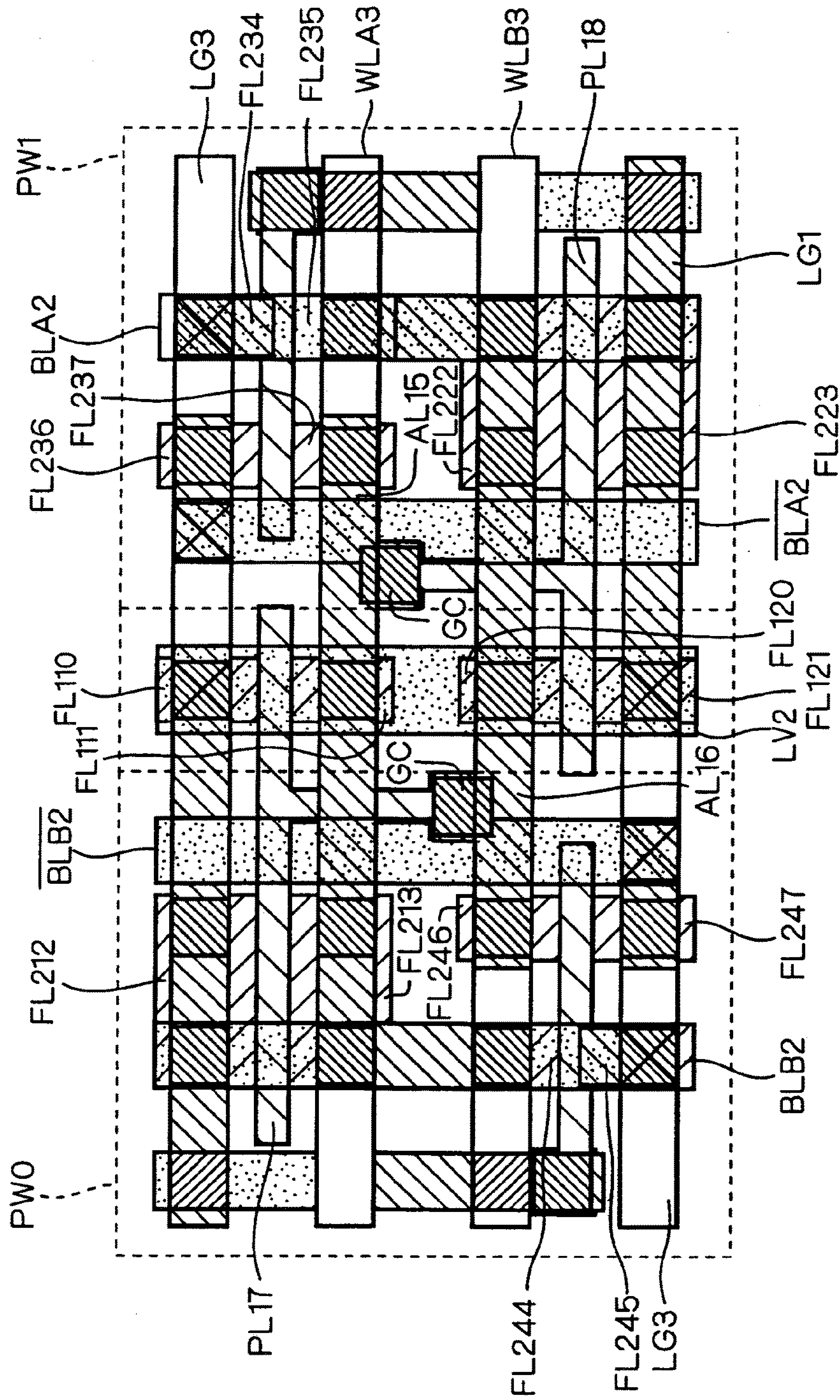


FIG. 21



F I G . 2 2

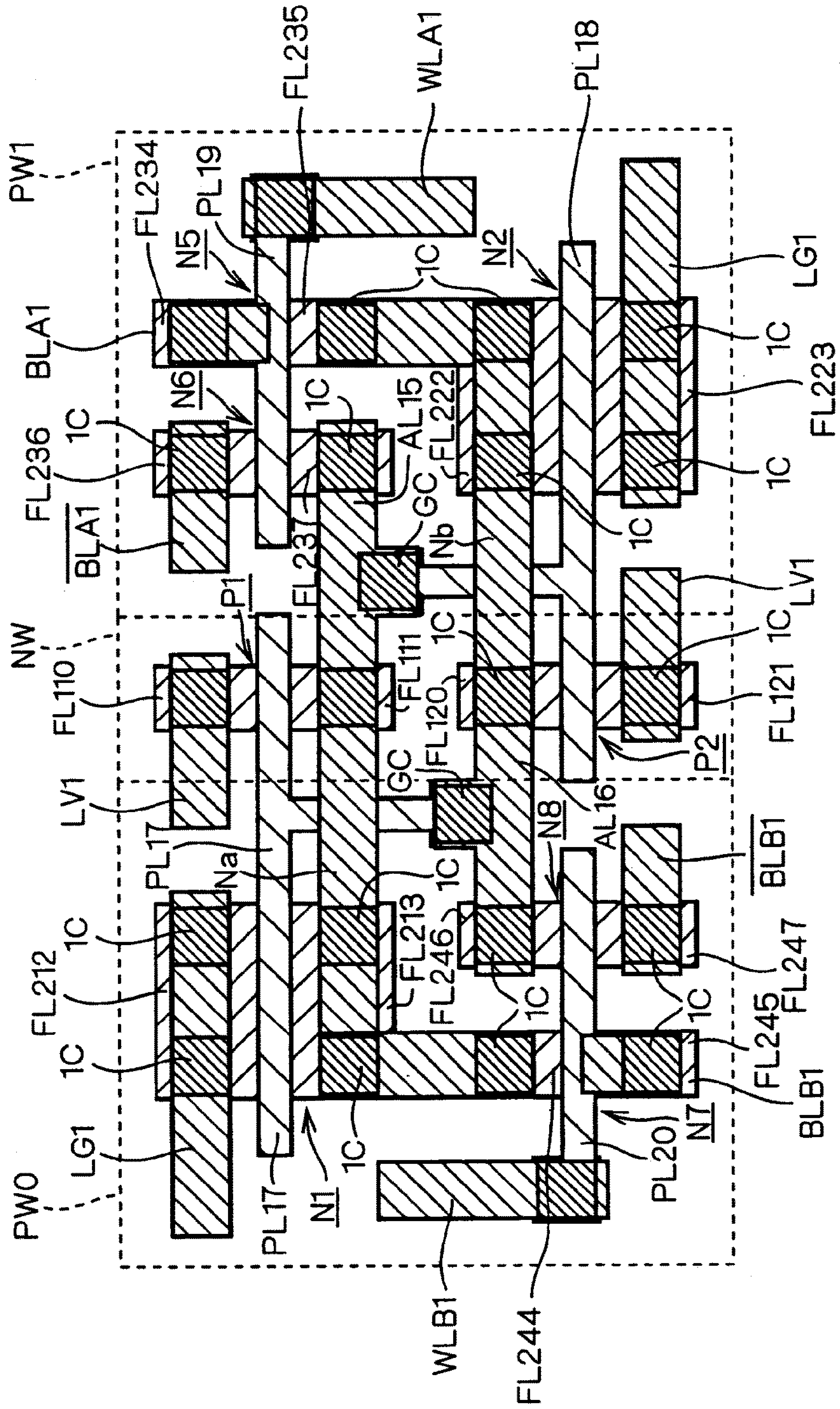
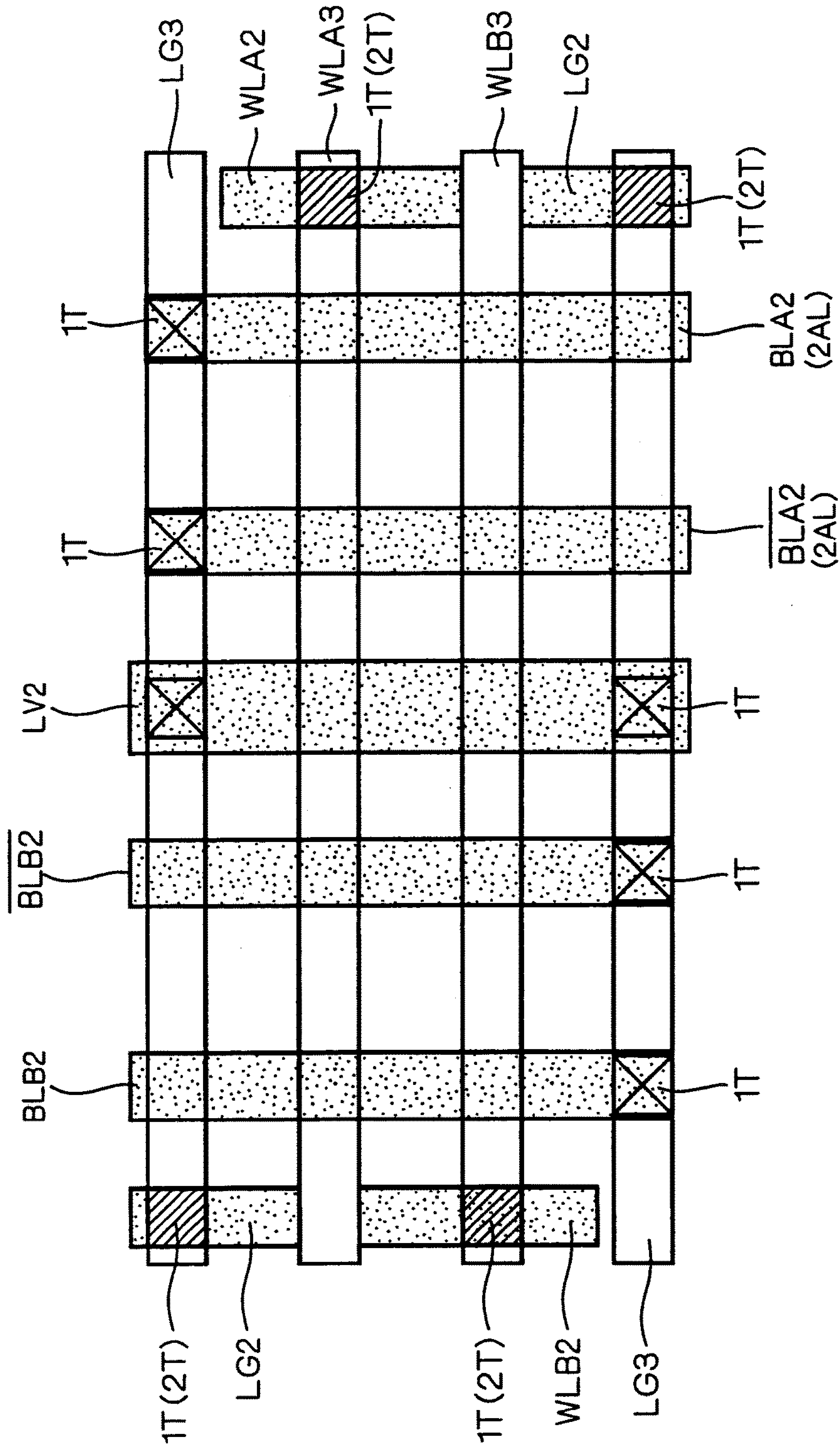


FIG. 23



F I G . 2 4

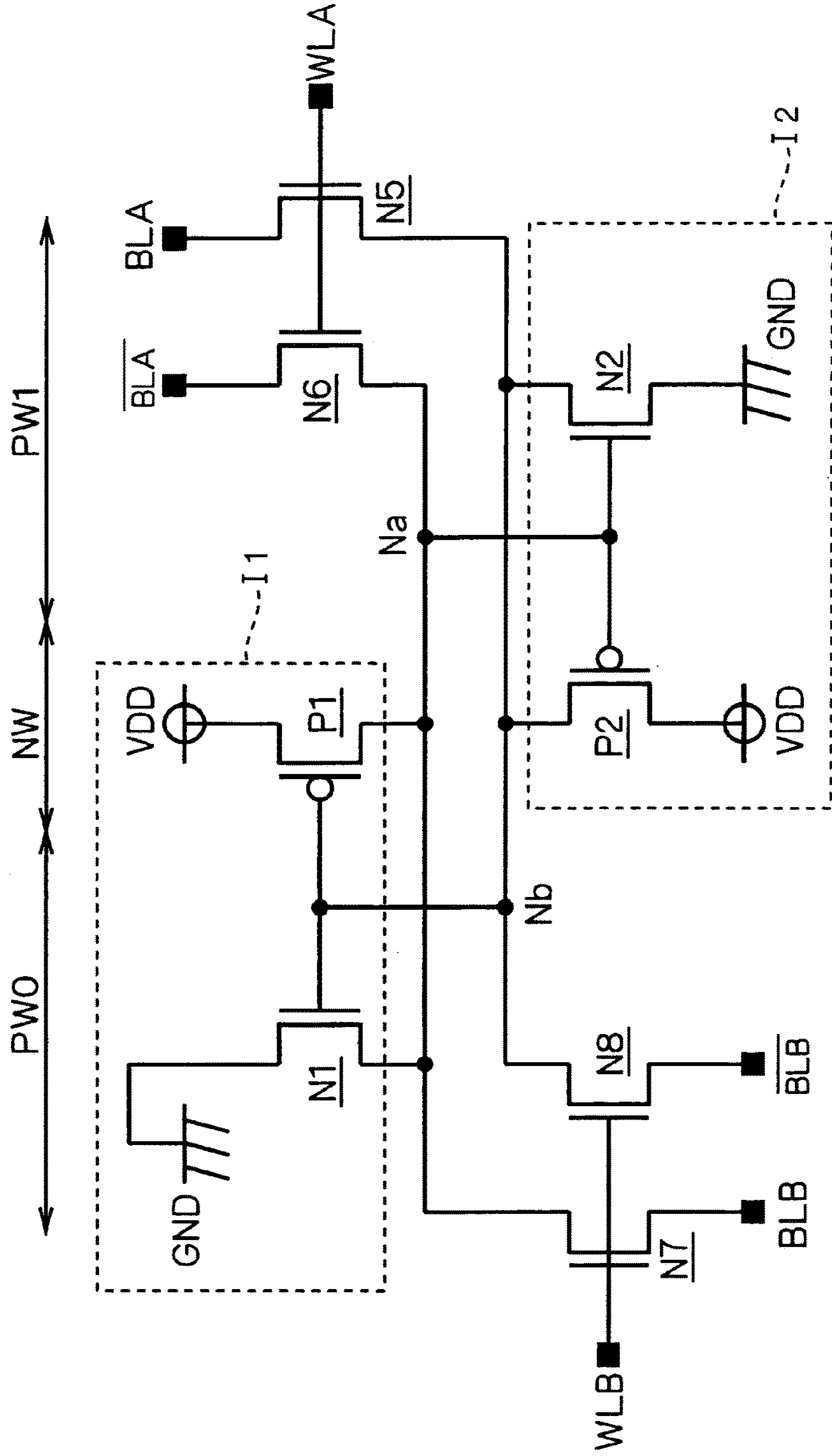
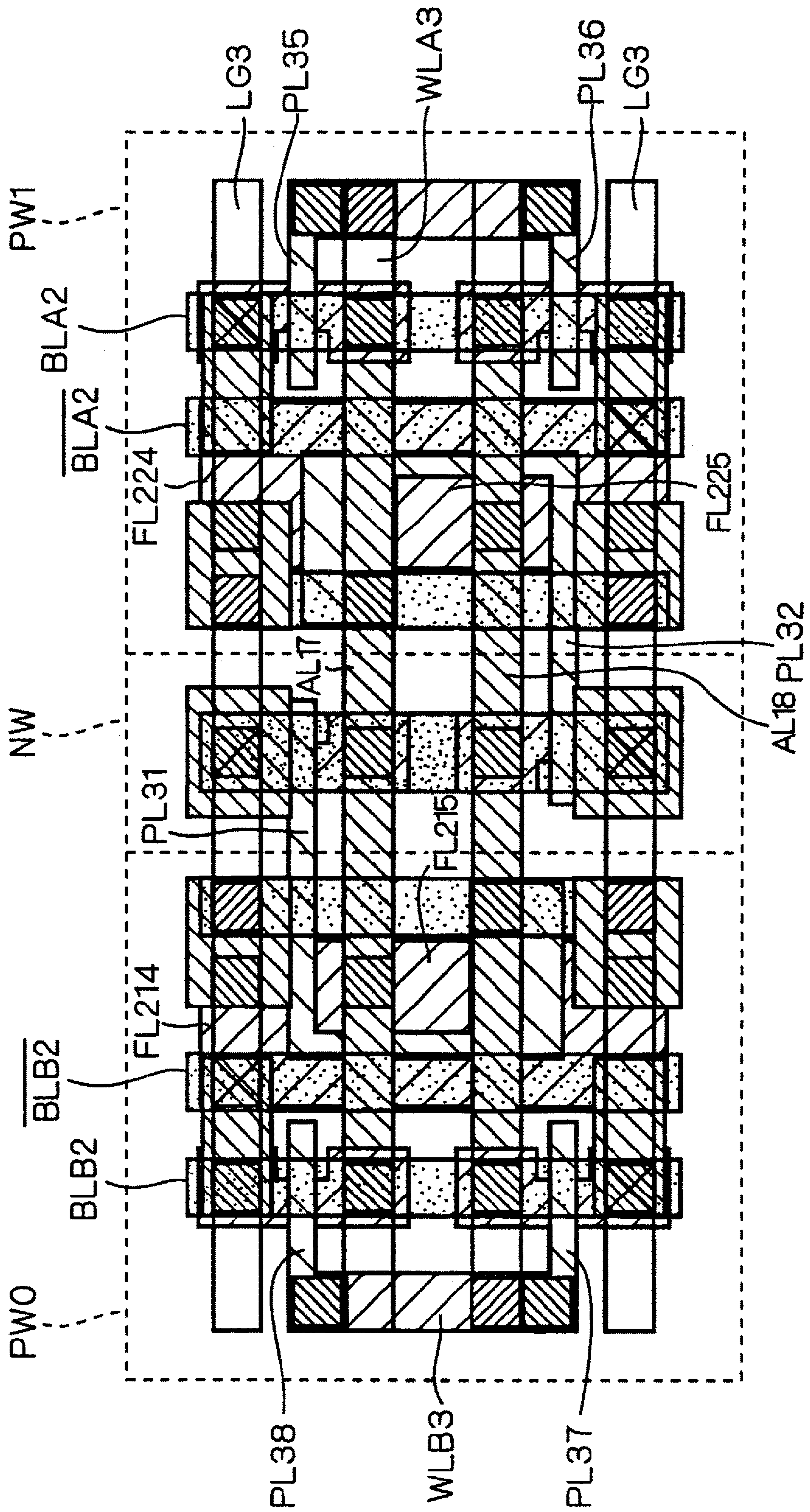
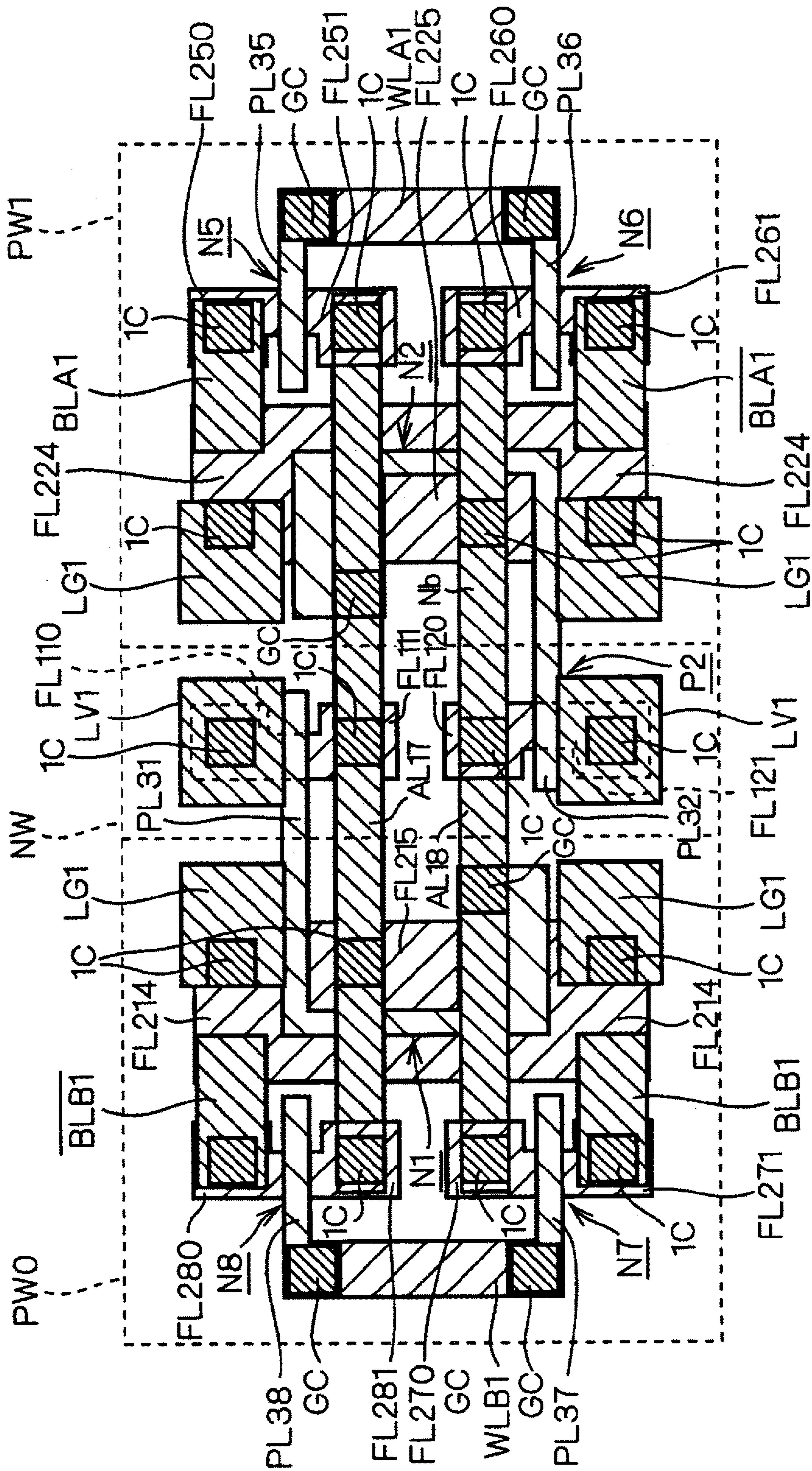


FIG. 25



F I G . 2 6



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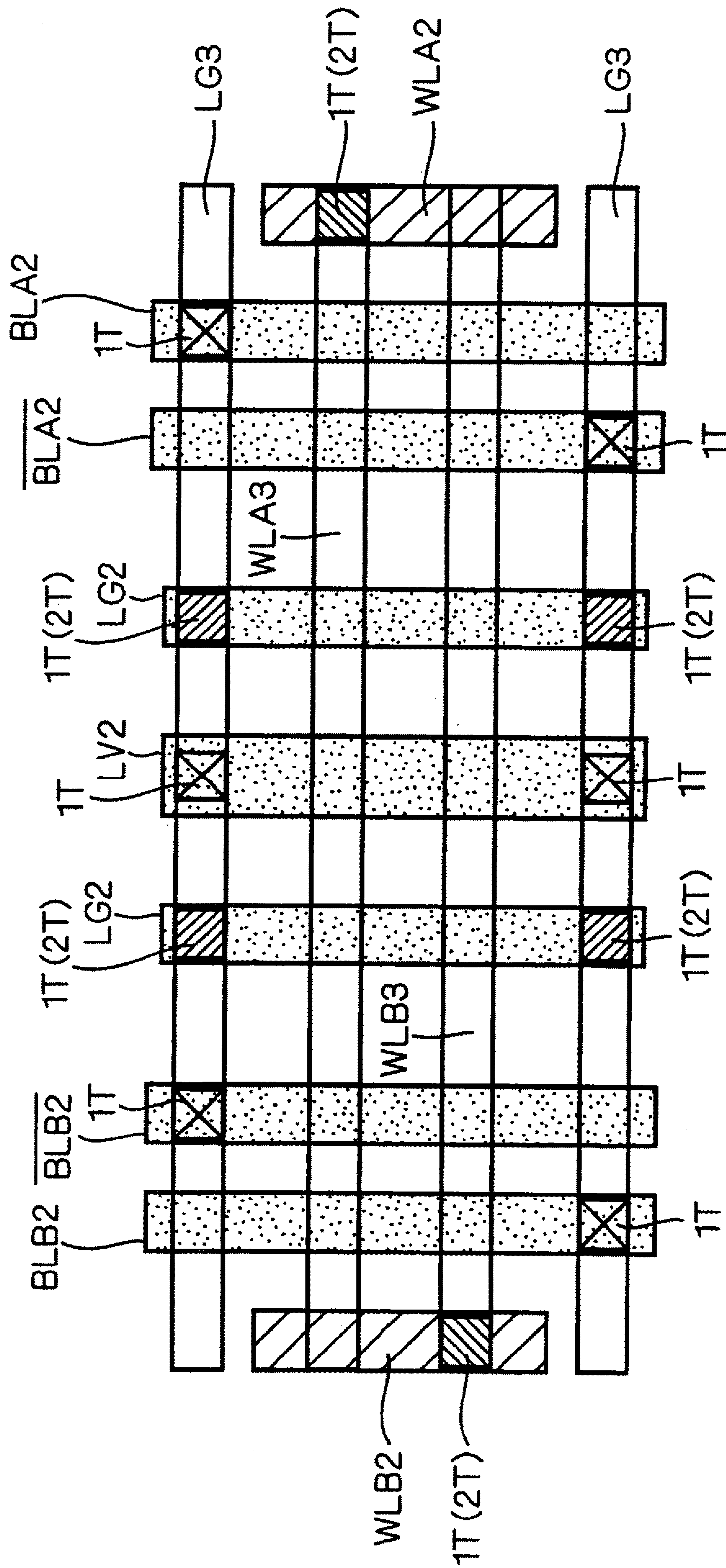
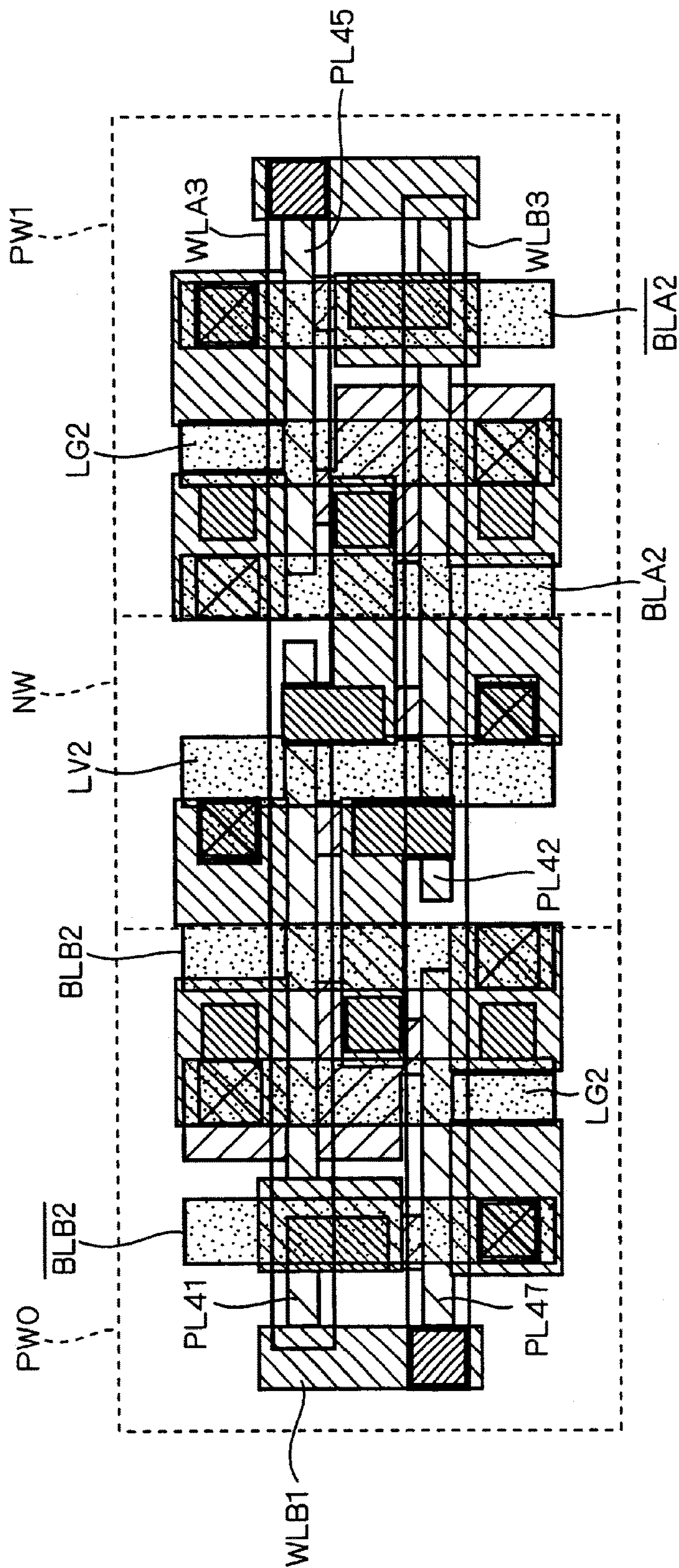
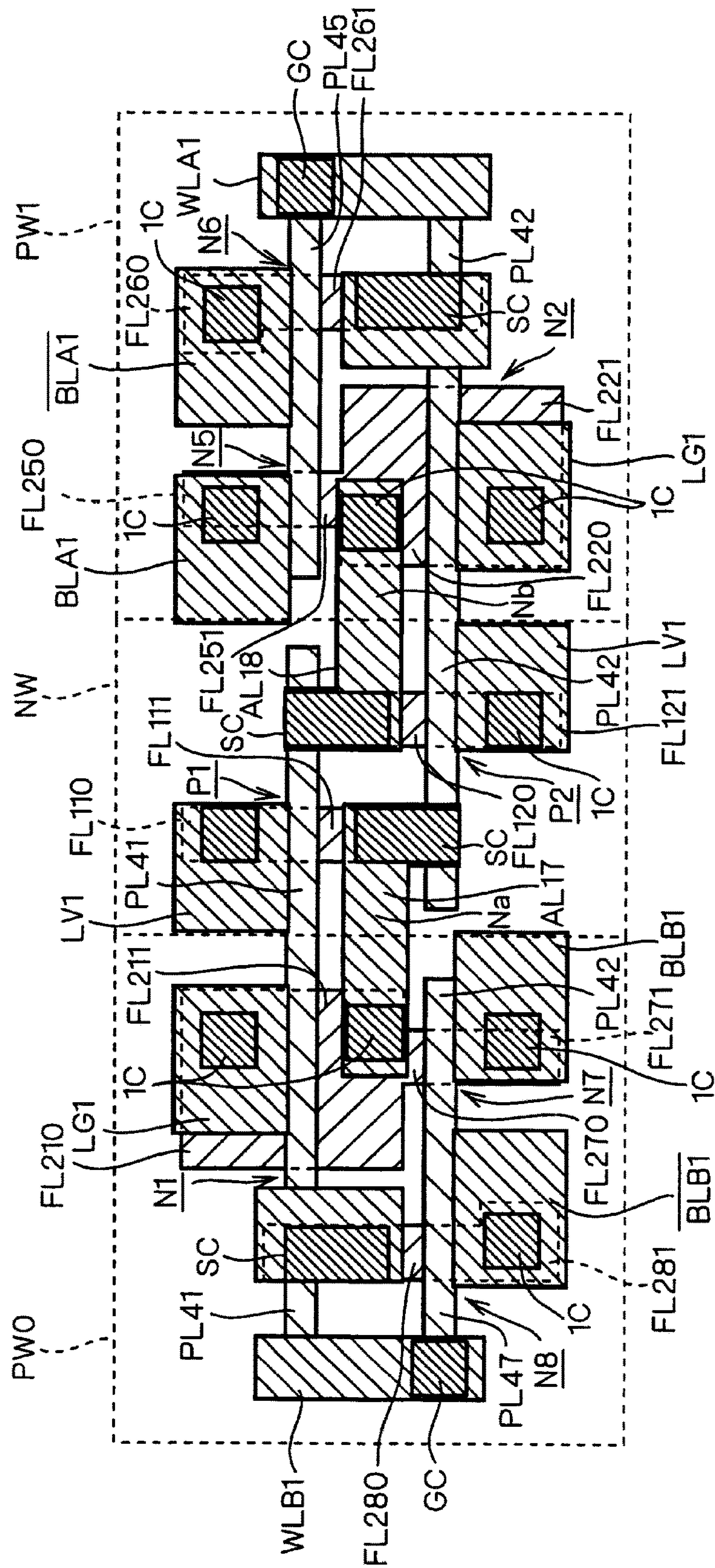


FIG. 28



F I G . 2 9



F I G . 3 0

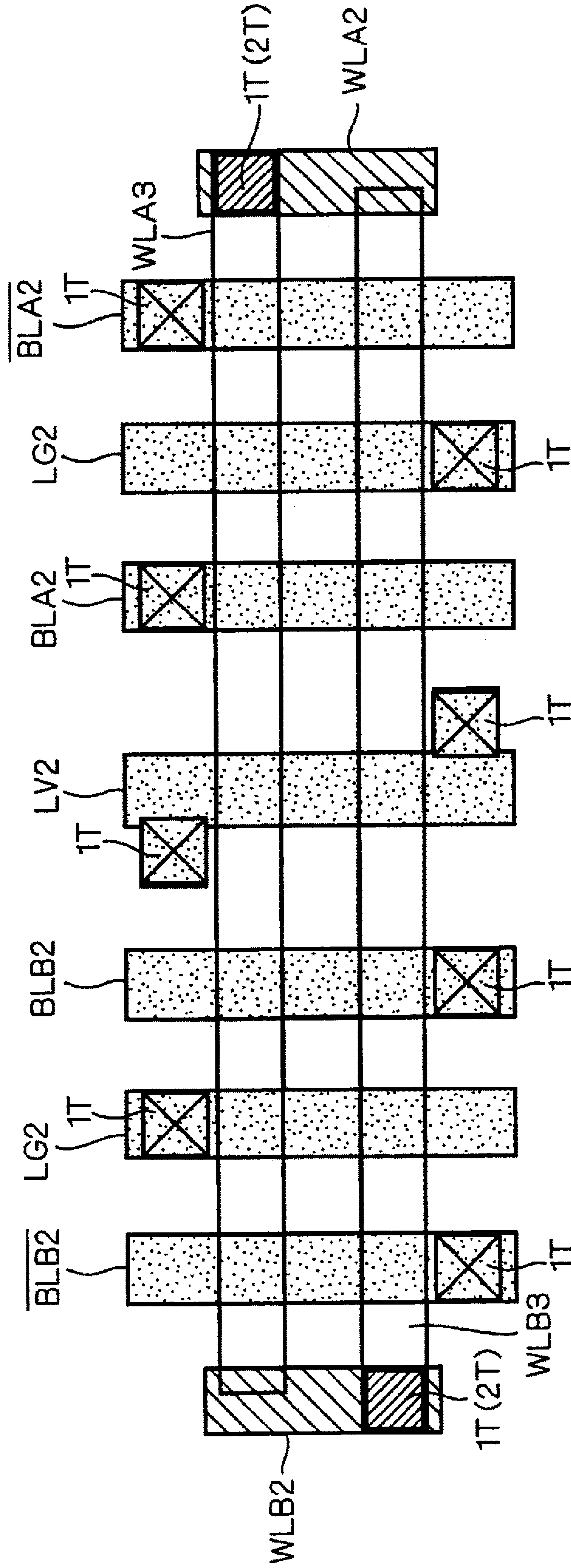


FIG. 31

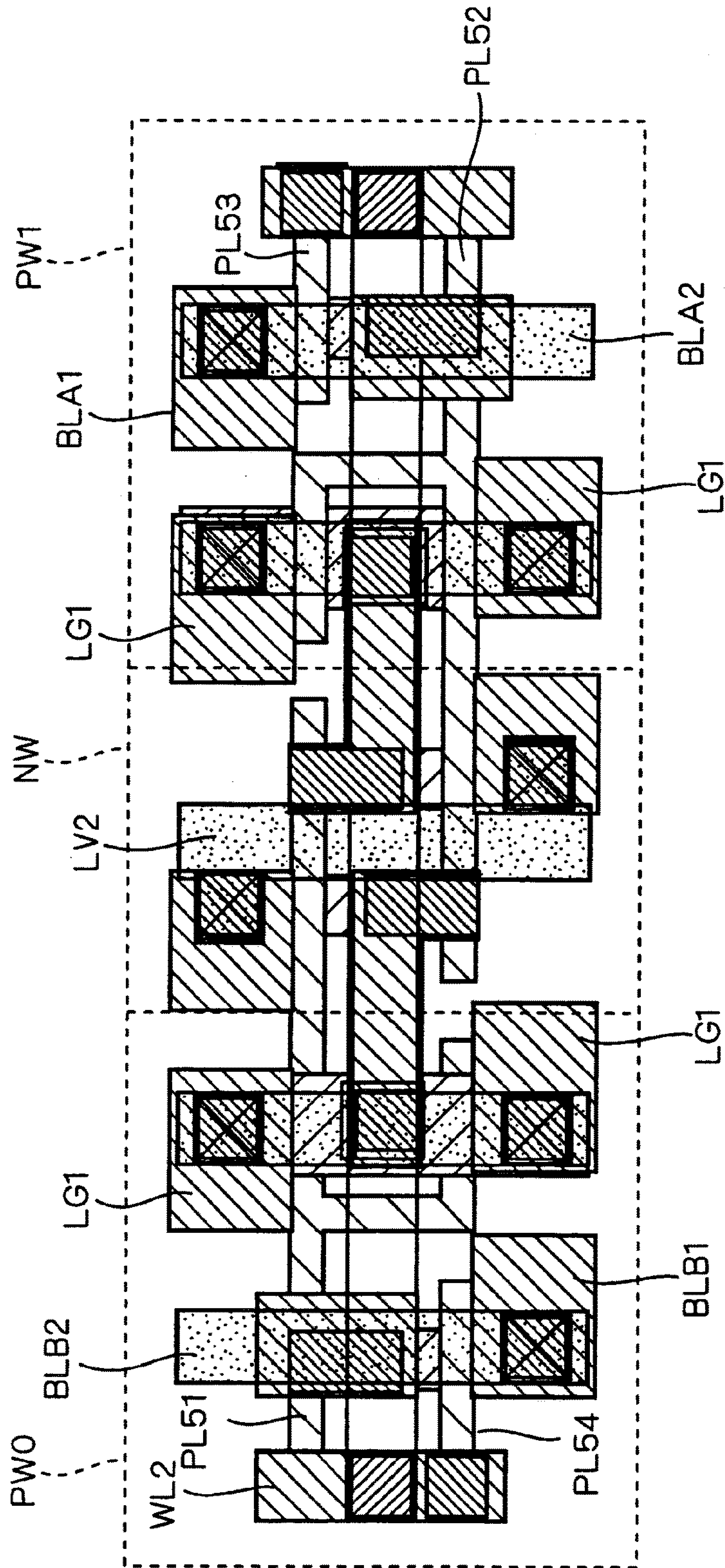


FIG. 32

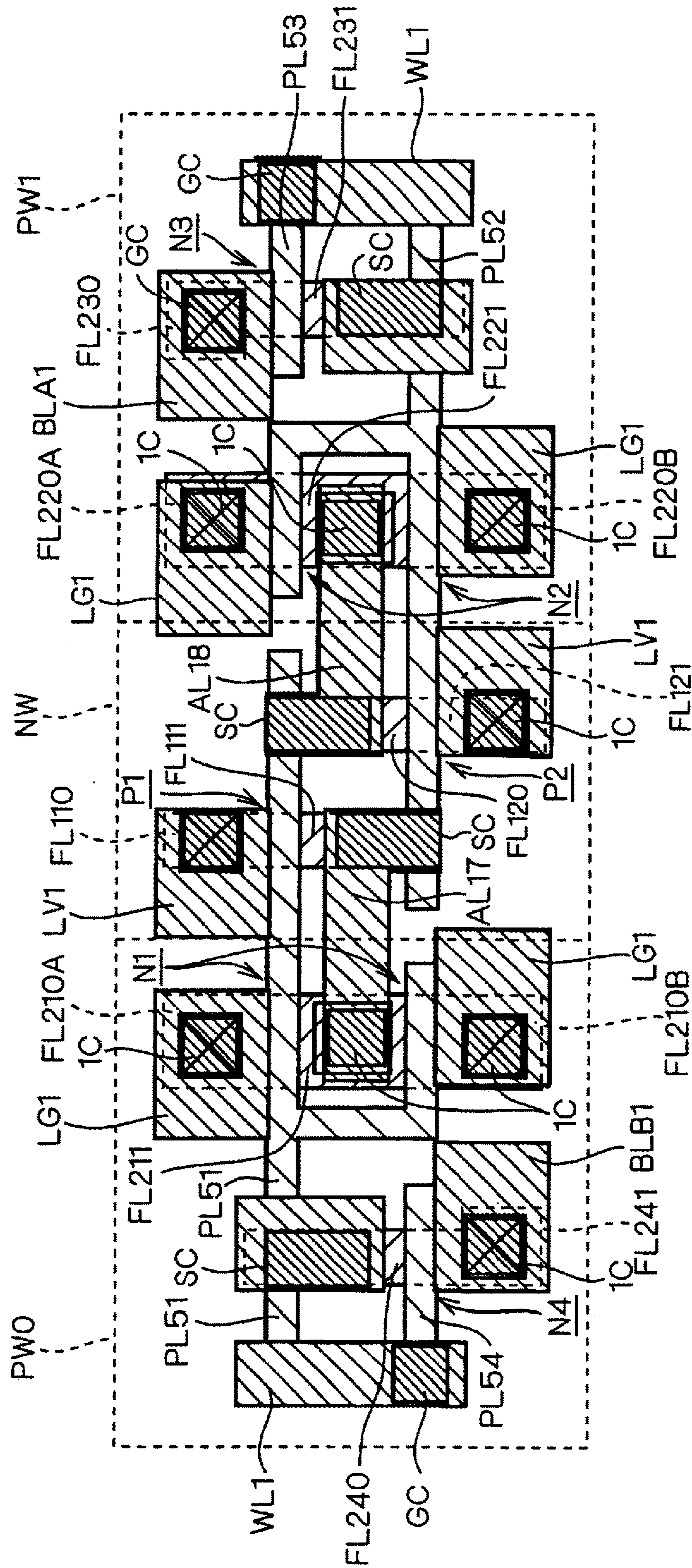


FIG. 33

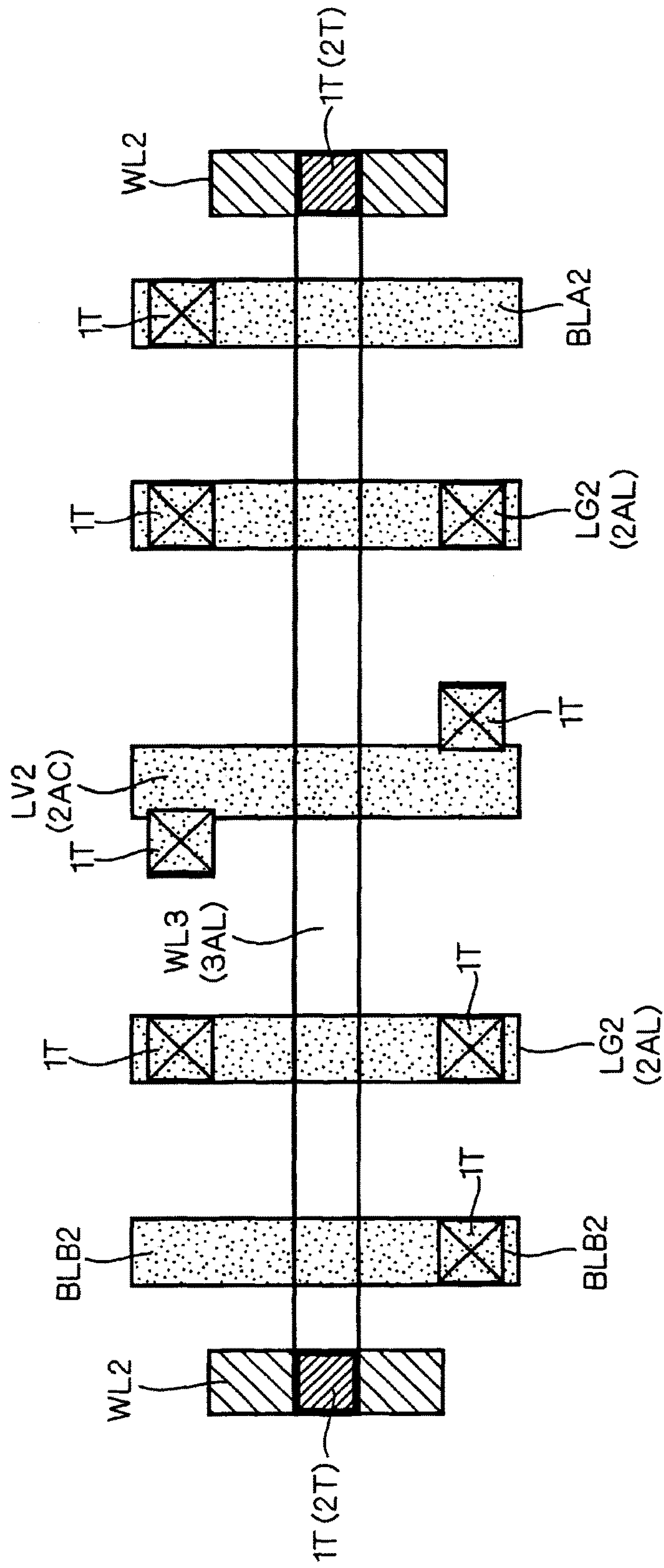


FIG. 34

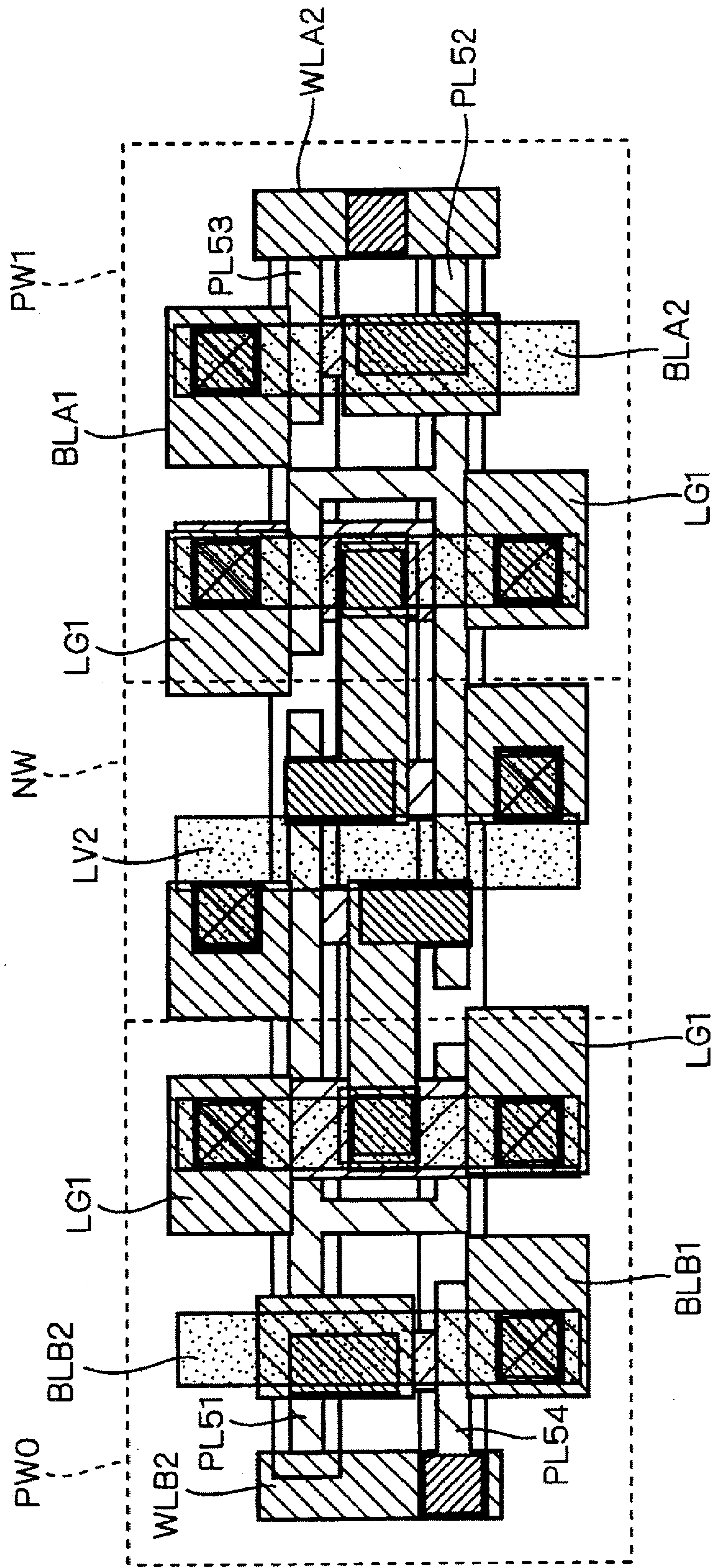
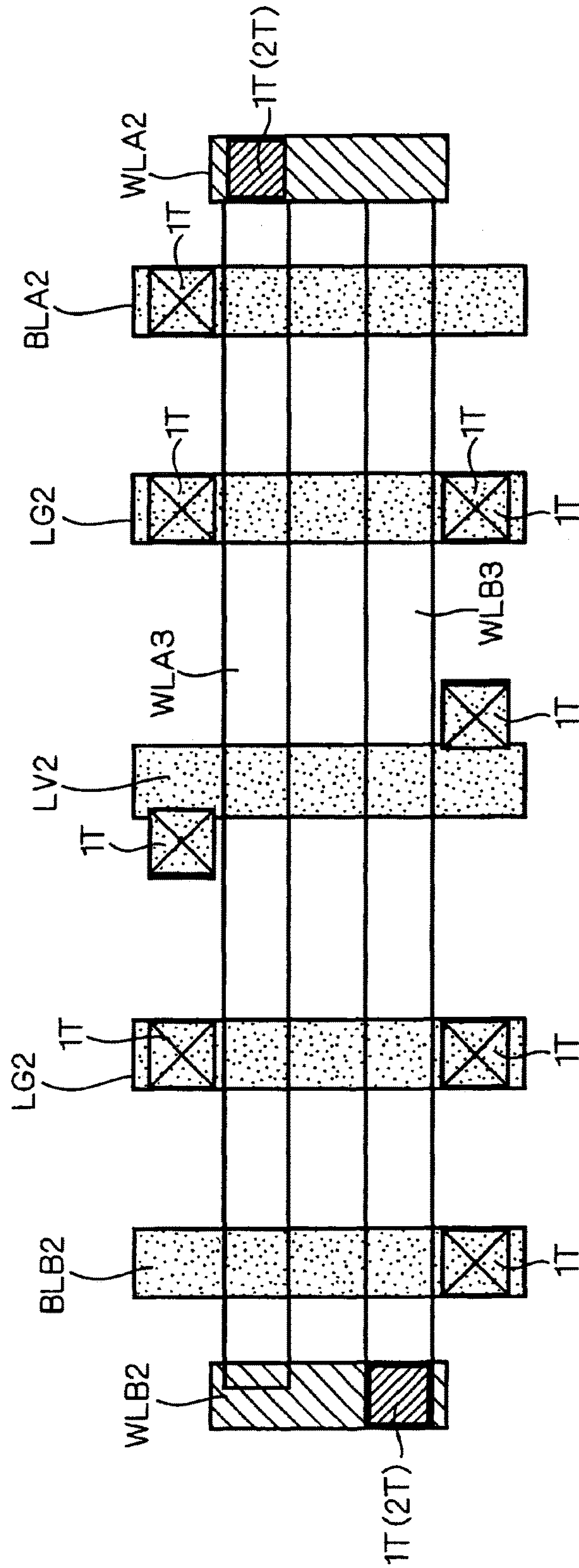
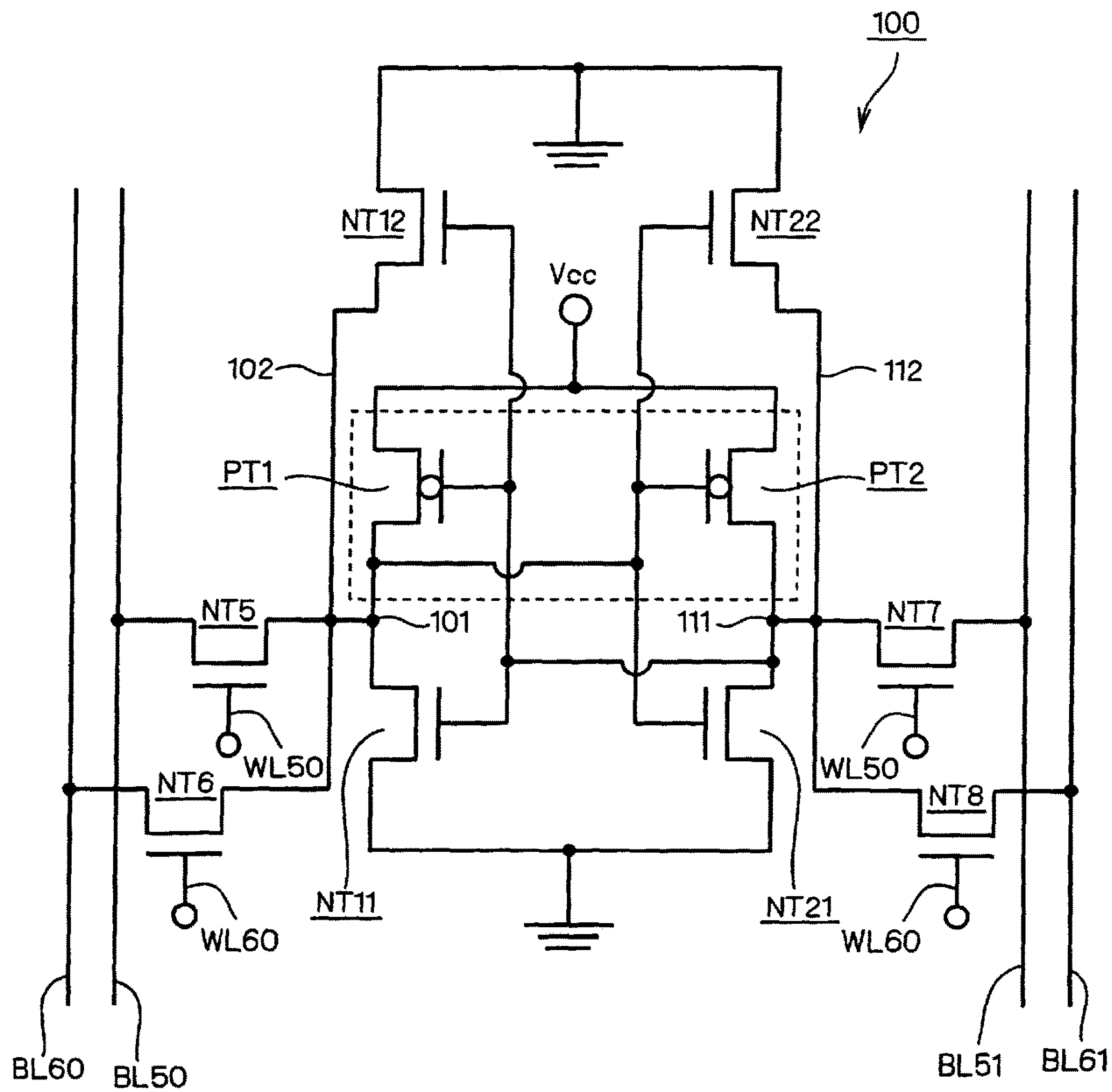


FIG. 35



F I G . 3 6

F I G . 3 7 **PRIOR ART**



SEMICONDUCTOR MEMORY

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue; a claim printed with strikethrough indicates that the claim was canceled, disclaimed, or held invalid by a prior post-patent action or proceeding.

Notice: More than one reissue application has been filed for the reissue of U.S. Pat. No. 6,643,167. The reissue applications that have been filed include parent reissue application Ser. No. 11/265,744 filed on Nov. 3, 2005, and reissue application Ser. No. 12/846,450 filed Jul. 29, 2010, and reissue application Ser. No. 13/863,011 filed Apr. 15, 2013, and the present reissue application which is a continuation reissue of the '011 reissue application.

This application is a Continuation of U.S. application Ser. No. 13/863,011, filed on Apr. 15, 2013, now U.S. Pat. No. RE46,272, issued on Jan. 10, 2017, which is a Continuation of U.S. application Ser. No. 12/846,450, filed on Jul. 29, 2010, now U.S. Pat. No. RE44,242, issued on May 28, 2013, which is a Continuation of U.S. application Ser. No. 11/265,744, filed on Nov. 3, 2005, now U.S. Pat. No. RE41,638, issued on Sep. 7, 2010, which is a Reissue of U.S. application Ser. No. 10/350,221, filed on Jan. 24, 2003, now U.S. Pat. No. 6,643,167, issued on Nov. 4, 2003, which is a Continuation of U.S. application Ser. No. 09/900,917, filed on Jul. 10, 2001, now U.S. Pat. No. 6,529,401, issued on Mar. 4, 2003.

This application is also a Reissue of U.S. application Ser. No. 10/350,221, filed on Jan. 24, 2003, now U.S. Pat. No. 6,643,167, issued on Nov. 4, 2003.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor memory and, in particular, to a memory cell structure having improvements in resistance to soft error of a MOS static RAM.

2. Description of the Background Art

As the miniaturization of memory cells proceeds, the following soft error problem becomes noticeable. Specifically, the data stored in a storage node is inverted due to electrons generated from alpha rays released from a package and neutron beams from outer space. Particularly, as power supply voltage is lowered, malfunction becomes more significant. Attempts to reduce soft error are being pursued.

FIG. **37** is a circuit diagram illustrating a structure equivalent to a SRAM memory cell disclosed in, for example, Japanese Patent No. 2589949. As shown in FIG. **37**, a memory cell **100** is made up of PMOS transistors PT**1** and PT**2**, and NMOS transistors NT**5** to NT**8**, NT**11**, NT**12**, NT**21** and NT**22**.

The sources of the PMOS transistors PT**1** and PT**2** are both connected to a power supply voltage V_{cc}. The drain of the PMOS transistor PT**1** is connected through a node **101** to the gate of the PMOS transistor PT**2** and to the gates of the NMOS transistors NT**21** and NT**22**. The drain of the PMOS transistor PT**2** is connected through a node **111** to the gate of the PMOS transistor PT**1** and to the gates of the NMOS transistors NT**11** and NT**12**.

The sources of the NMOS transistors NT**11** and NT**12** are both grounded. The drain of the NMOS transistor NT**11** is

connected through the node **101** to the drain of the PMOS transistor PT**1**. The drain of the NMOS transistor NT**12** is connected through the nodes **101** and **102** to the drain of the PMOS transistor PT**1**.

The sources of the NMOS transistors NT**21** and NT**22** are both grounded. The drain of the NMOS transistor NT**21** is connected through the node **111** to the drain of the PMOS transistor PT**2**. The drain of the NMOS transistor NT**22** is connected through the nodes **111** and **112** to the drain of the PMOS transistor PT**2**.

The NMOS transistor NT**5** is interposed between a bit line BL**50** and the node **101**, and its gate is connected to a word line WL**50**. The NMOS transistor NT**6** is interposed between a bit line BL**60** and the node **101**, and its gate is connected to a word line WL**60**. The NMOS transistor NT**7** is interposed between a bit line BL**51** and the node **111**, and its gate is connected to the word line WL**50**. The NMOS transistor NT**8** is interposed between a bit line BL**61** and the node **111**, and its gate is connected to the word line WL**60**.

In such a configuration, the word line WL**50** or WL**60** is brought into the active state and the NMOS transistors NT**5** and NT**6**, or the NMOS transistors NT**6** and NT**8** are brought into the on state, thereby to provide access to the nodes **101** and **111**, each being a storage node. This enables to obtain the data from the paired bit lines BL**50** and BL**51** or the paired bit lines BL**60** and BL**61**.

In this configuration, a NMOS driver transistor that is usually made up of a single NMOS transistor is divided into two NMOS transistors (which is divided into the NMOS transistors NT**11** and NT**12**, and NT**21** and NT**22**).

In order to divide the storage node serving as the drain of the PMOS transistor PT**1** (PT**2**) into the node **101** (**111**) and the node **102** (**112**), the NMOS transistor NT**11** (NT**21**) and the NMOS transistor NT**12** (NT**22**) are oppositely disposed so as to interpose therebetween an N well region where the PMOS transistor PT**1** is to be formed.

Therefore, the N well region prevents that a depletion region on the opposite side of the N well region is adversely affected by electrons or holes generated from energy particles colliding with one side of the N well region. This enables to lower incidence of soft error.

However, even with the foregoing SRAM memory cell, a reduction in soft error is insufficient. Further, there is the problem that the circuit configuration is complicated by using two driver transistors, although it can be generally configured by using one.

SUMMARY OF THE INVENTION

According to a first aspect of the invention, a semiconductor memory having a memory cell containing first and second inverters subjected to cross connection, a first conductivity type being defined by first kind, and a second conductivity type being defined by second kind, is characterized in that: the first inverter consists of a first field effect transistor of the first kind and a first field effect transistor of the second kind; that the second inverter consists of a second field effect transistor of the first kind and a second field effect transistor of the second kind; and that the first and second field effect transistors of the first kind are disposed in separate first and second well regions of the second kind, respectively.

According to a second aspect of the invention, the semiconductor memory of the first aspect is characterized in that: an output part of the first inverter includes a connecting part between one electrode of the first field effect transistor of the first kind and one electrode of the first field effect transistor

of the second kind, an input part thereof includes a connecting part between a control electrode of the first field effect transistor of the first kind and a control electrode of the first field effect transistor of the second kind; an output part of the second inverter includes a connecting part between one electrode of the second field effect transistor of the first kind and one electrode of the second field effect transistor of the second kind, and an input part thereof includes a connecting part between a control electrode of the second field effect transistor of the first kind and a control electrode of the second field effect transistor of the second kind; that the memory cell further includes: (i) a third field effect transistor of the first kind, one electrode of which is connected to a first storage terminal electrically connected to the output part of the first inverter and the input part of the second inverter, and the other electrode of which is connected to a first bit line, and a control electrode of which is connected to a word line; and (ii) a fourth field effect transistor of the first kind, one electrode of which is connected to a second storage terminal electrically connected to the output part of the second inverter and the input part of the first inverter, and the other electrode of which is connected to a second bit line, and a control electrode of which is connected to a word line; and that the third and fourth field effect transistors of the first kind are disposed in second and first well regions of the second kind, respectively.

According to a third aspect of the invention, the semiconductor memory of the second aspect is characterized in that the respective one electrodes in the first to fourth field effect transistors of the first kind are disposed separately.

According to a fourth aspect of the invention, the semiconductor memory of the second aspect is characterized in that: the first and third field effect transistors of the first kind and the first field effect transistor of the second kind are arranged in an approximately straight line along the direction of formation of the word line; and that the second and fourth field effect transistors of the first kind and the second field effect transistor of the second kind are arranged in an approximately straight line along the direction of formation of the word line.

According to a fifth aspect of the invention, the semiconductor memory of the first aspect is characterized in that the first and second field effect transistors of the first kind are arranged so as to be point symmetry with respect to the central point of the memory cell.

According to a sixth aspect of the invention, the semiconductor memory of the second aspect is characterized in that the third and fourth field effect transistors of the first kind are arranged so as to be point symmetry with respect to the central point of the memory cell.

According to a seventh aspect of the invention, the semiconductor memory of the second aspect is characterized in that the width of the control electrode of the first and second field effect transistors of the first kind is set so as to be larger than the width of the control electrode of the third and fourth field effect transistors of the first kind.

According to an eighth aspect of the invention, the semiconductor memory of one of the foregoing aspects is characterized in that the memory cell further includes (i) a first resistance component interposed between the input part of the first inverter and the second storage terminal, and (ii) a second resistance component interposed between the input part of the second inverter and the first storage terminal.

According to a ninth aspect of the invention, the semiconductor memory of the eighth aspect is characterized in that the first and second resistance components include a high resistance metal wiring formed from a metal material having a higher resistivity than CoSi.

According to a tenth aspect of the invention, the semiconductor memory of the eighth aspect is characterized in that the first and second resistance components include a high resistance polysilicon wiring formed from polysilicon having a higher resistivity than CoSi.

According to an eleventh aspect of the invention, the semiconductor memory of the second aspect is characterized in that the control electrodes of the third and fourth field effect transistors of the first kind and the word line are formed by using a single polysilicon.

According to a twelfth aspect of the invention, the semiconductor memory of the second aspect is characterized in that: the word line includes separate first and second word lines; that the control electrode of the third field effect transistor of the first kind is connected to the first word line; and that the control electrode of the fourth field effect transistor of the first kind is connected to the second word line.

According to a thirteenth aspect of the invention, the semiconductor memory of the twelfth aspect is characterized in that: the first bit line includes first and second partial bit lines forming a pair of bit lines; that the second bit line includes third and fourth partial bit lines forming a pair of bit lines; that the third field effect transistor of the first kind includes fifth and sixth field effect transistors of the first kind, the fifth field effect transistor of the first kind being interposed between the first partial bit line and the second storage terminal, the sixth field effect transistor of the first kind being interposed between the second partial bit line and the first storage terminal; and that the fourth field effect transistor of the first kind includes seventh and eighth field effect transistors of the first kind, the seventh field effect transistor of the first kind being interposed between the third partial bit line and the first storage terminal, the eighth field effect transistor of the first kind being interposed between the fourth partial bit line and the second storage terminal.

According to a fourteenth aspect of the invention, the semiconductor memory of the thirteenth aspect is characterized in that the width of the control electrode of the first and second field effect transistors of the first kind is set so as to be larger than the width of the control electrode of the fifth to eighth field effect transistors of the first kind.

According to a fifteenth aspect of the invention, the semiconductor memory of the second, twelfth or thirteenth aspect is characterized in that a region for forming the control electrode of the first and second field effect transistors of the first kind is disposed so as to form a portion of the second and first storage terminals, respectively.

According to a sixteenth aspect of the invention, the semiconductor memory of one of the foregoing aspects is characterized in that: the first and second field effect transistors of the second kind are disposed in a well region of the first kind; and that the well region of the first kind is disposed between the first and second well regions of the second kind.

In the semiconductor memory of the first aspect, the first and second field effect transistors of the first kind are disposed in the separate first and second well region of the second kind, respectively. Therefore, if carriers generated from alpha rays, etc. are collected into one or the other electrode region of one of the first and second field effect transistor of the first kind, such carriers are cancelled by being released from one or the other electrode region of the other of the first and second field effect transistor of the first kind on which no influence of the carriers is exerted. This enables to increase resistance to soft error.

In addition, since the first and second inverters each consists of a combination of a field effect transistor of the first kind and that of the second kind, a complementary type can be realized by at least sufficient circuit configuration.

In the semiconductor memory of the second aspect, the third and fourth field effect transistors of the first kind are disposed in the second and first well regions of the second kind, respectively. Thereby, the memory cell selecting operation by means of the word line, and the write/read operation to the memory cell via the first and second bit lines, are executable while improving resistance to soft error.

In the semiconductor memory of the third aspect, resistance to soft error can be increased by separately forming one electrode to be connected to the first or second storage terminal in the first to fourth field effect transistors of the first kind.

In the semiconductor memory of the fourth aspect, the degree of integration can be increased by virtue of the layout of the first to fourth field effect transistors of the first kind and the first and second field effect transistors of the second kind.

In the semiconductor memory of the fifth aspect, by disposing the first and second MOS transistors so as to be point symmetry with respect to the central portion of the memory cell, arrangement between adjacent memory cells can be facilitated to increase the degree of integration.

In the semiconductor memory of the sixth aspect, by disposing the third and fourth MOS transistors so as to be point symmetry with respect to the central portion of the memory cell, arrangement between adjacent memory cells can be facilitated to increase the degree of integration.

In the semiconductor memory of the seventh aspect, the stability of the memory cell can be increased by setting such that the control electrode width of the first and second field effect transistors of the first kind is larger than that of the third and fourth field effect transistors of the first kind.

In the semiconductor memory of the eighth aspect, by signal propagation delay due to the first and second resistance components, the response characteristic for inverting the data held in the first and second storage terminals of the memory cell can be elongated, thereby soft error is hard to occur.

The semiconductor memory of the ninth aspect realizes the first and second resistance components by using the high resistance polysilicon wiring.

The semiconductor memory of the tenth aspect realizes the first and second resistance components by using the high resistance polysilicon wiring.

In the semiconductor memory of the eleventh aspect, by using a single polysilicon common to the control electrodes and word lines of the third and fourth MOS transistors, the number of layers to be formed can be reduced, thereby allowing for a reduction in the cost of the semiconductor memory.

In the semiconductor memory of the twelfth aspect, by the presence of two memory cell selecting means composed of the first and second word lines, the memory cell can be used for FIFO memory.

The semiconductor memory of the thirteenth aspect realizes a two-port memory cell composed of the first to fourth partial bit lines and the first and second word lines.

In the semiconductor memory of the fourteenth aspect, the stability of the memory cell can be increased by setting such that the control electrode width of the first and second field effect transistors of the first kind is larger than that of the fifth to eighth field effect transistors of the first kind.

In the semiconductor memory of the fifteenth aspect, with the arrangement such that the region for forming the control electrode of the first and second field effect transistors of the first kind forms a portion of the second and first storage terminals, respectively, the region for forming memory cell can be narrowed to increase the degree of integration.

In the semiconductor memory of the sixteenth aspect, by the well region of the first kind disposed between the first and second well regions of the second kind, it is avoided that carriers generated in the first or second well region of the second kind exert influence on the other well region of the second kind.

It is an object of the present invention to overcome the foregoing problem by providing a semiconductor memory having a memory cell structure capable of reducing soft error without complicating a circuit configuration.

These and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is an explanatory diagram viewed from above the layout configuration in all layers of a SRAM memory cell according to a first preferred embodiment of the invention;

FIG. **2** is an explanatory diagram viewed from above mainly the layout configuration beneath a first aluminum wiring layer in FIG. **1**;

FIG. **3** is an explanatory diagram viewed from above mainly the layout configuration over a second aluminum wiring layer in FIG. **1**;

FIG. **4** is a circuit diagram illustrating an equivalent circuit of the memory cell in the first preferred embodiment;

FIG. **5** is an explanatory diagram viewed from above the layout configuration in all layers of a SRAM memory cell according to a second preferred embodiment of the invention;

FIG. **6** is an explanatory diagram viewed from above mainly the layout configuration beneath a first aluminum wiring layer in FIG. **5**;

FIG. **7** is an explanatory diagram viewed from above the layout configuration beneath the first aluminum wiring layer between adjacent memory cells;

FIG. **8** is an explanatory diagram viewed from above the layout configuration in all layers of a SRAM memory cell according to a third preferred embodiment of the invention;

FIG. **9** is an explanatory diagram viewed from above mainly the layout configuration beneath a first aluminum wiring layer in FIG. **8**;

FIG. **10** is a circuit diagram illustrating an equivalent circuit of the memory cell in the third preferred embodiment;

FIG. **11** is an explanatory diagram viewed from above the layout configuration in all layers of a SRAM memory cell according to a fourth preferred embodiment of the invention;

FIG. **12** is an explanatory diagram viewed from above mainly the layout configuration beneath a first aluminum wiring layer in FIG. **11**;

FIG. **13** is an explanatory diagram viewed from above the layout configuration in all layers of a SRAM memory cell according to a fifth preferred embodiment of the invention;

FIG. **14** is an explanatory diagram viewed from above mainly the layout configuration over a second aluminum wiring layer in FIG. **13**;

FIG. **15** is a circuit diagram illustrating an equivalent circuit of the memory cell in the fifth preferred embodiment;

FIG. **16** is an explanatory diagram viewed from above the layout configuration in all layers of a SRAM memory cell according to a sixth preferred embodiment of the invention;

FIG. **17** is an explanatory diagram viewed from above mainly the layout configuration beneath a first aluminum wiring layer in FIG. **16**;

FIG. **18** is an explanatory diagram viewed from above mainly the layout configuration above a second aluminum wiring layer in FIG. **16**;

FIG. **19** is an explanatory diagram viewed from above the layout configuration in all layers of a SRAM memory cell according to a seventh preferred embodiment of the invention;

FIG. **20** is an explanatory diagram viewed from above mainly the layout configuration beneath a first aluminum wiring layer in FIG. **19**;

FIG. **21** is an explanatory diagram viewed from above mainly the layout configuration over a second aluminum wiring layer in FIG. **19**;

FIG. **22** is an explanatory diagram viewed from above the layout configuration in all layers of a SRAM memory cell according to an eighth preferred embodiment of the invention;

FIG. **23** is an explanatory diagram viewed from above mainly the layout configuration beneath a first aluminum wiring layer in FIG. **22**;

FIG. **24** is an explanatory diagram viewed from above mainly the layout configuration over a second aluminum wiring layer in FIG. **22**;

FIG. **25** is a circuit diagram illustrating an equivalent circuit of the memory cell in the eighth preferred embodiment;

FIG. **26** is an explanatory diagram viewed from above the layout configuration in all layers of a SRAM memory cell according to a ninth preferred embodiment of the invention;

FIG. **27** is an explanatory diagram viewed from above mainly the layout configuration beneath a first aluminum wiring layer in FIG. **26**;

FIG. **28** is an explanatory diagram viewed from above mainly the layout configuration over a second aluminum wiring layer in FIG. **26**;

FIG. **29** is an explanatory diagram viewed from above the layout configuration in all layers of a SRAM memory cell according to a tenth preferred embodiment of the invention;

FIG. **30** is an explanatory diagram viewed from above mainly the layout configuration beneath a first aluminum wiring layer in FIG. **29**;

FIG. **31** is an explanatory diagram viewed from above mainly the layout configuration over a second aluminum wiring layer in FIG. **29**;

FIG. **32** is an explanatory diagram viewed from above the layout configuration in all layers of a SRAM memory cell according to an eleventh preferred embodiment of the invention;

FIG. **33** is an explanatory diagram viewed from above mainly the layout configuration beneath a first aluminum wiring layer in FIG. **32**;

FIG. **34** is an explanatory diagram viewed from above mainly the layout configuration over a second aluminum wiring layer in FIG. **32**;

FIG. **35** is an explanatory diagram viewed from above the layout configuration in all layers of a SRAM memory cell according to a twelfth preferred embodiment of the invention;

FIG. **36** is an explanatory diagram viewed from above mainly the layout configuration over a second aluminum wiring layer in FIG. **35**; and

FIG. **37** is a circuit diagram illustrating a conventional SRAM memory cell.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Preferred Embodiment

FIGS. **1** to **4** are diagrams illustrating a memory cell structure of a SRAM according to a first preferred embodiment of the invention. FIG. **1** is an explanatory diagram viewed from above the layout configuration in all layers. FIG. **2** is an explanatory diagram viewed from above mainly the layout configuration beneath a first aluminum wiring layer in FIG. **1**. FIG. **3** is an explanatory diagram viewed from above mainly the layout configuration over a second aluminum wiring layer in FIG. **1**. Some reference numerals used in FIG. **2** or **3** are omitted in FIG. **1**.

FIG. **4** is a circuit diagram illustrating an equivalent circuit of the SRAM memory cell of the layout configuration shown in FIGS. **1** to **3**. As seen from FIG. **4**, the SRAM memory cell of the first preferred embodiment is made up of NMOS transistors N**1** to N**4** and PMOS transistors P**1** and P**2**.

The PMOS transistors P**1** and P**2**, each being a driver transistor, are disposed within an N well region NW. The NMOS transistor N**1** that is a driver transistor and the NMOS transistor N**4** that is an access transistor are disposed within a P well region PW**0**. The NMOS transistor N**2** that is a driver transistor and the NMOS transistor N**3** that is an access transistor are disposed within a P well region PW**1**. The P well regions PW**0** and PW**1** are oppositely disposed with the N well region NW interposed therebetween.

A first CMOS inverter I**1** is made up of the NMOS transistor N**1** and PMOS transistor P**1**. That is, the gates of the PMOS transistor P**1** and NMOS transistor N**1** are both connected to a storage terminal Nb, and their drains are both connected to a storage terminal Na. The source of the PMOS transistor P**1** is connected to a power supply voltage V_{dd}, and the source of the NMOS transistor N**1** is grounded.

A second CMOS inverter I**2** is made up of the NMOS transistor N**2** and PMOS transistor P**2**. That is, the gates of the PMOS transistor P**2** and NMOS transistor N**2** are both connected to the storage terminal Na, and their drains are both connected to the storage terminal Nb. The source of the PMOS transistor P**2** is connected to the power supply voltage V_{dd}, and the source of the NMOS transistor N**2** is grounded.

Thus, an output part of the inverter I**1** and an input part of the inverter I**2** are electrically connected to the storage terminal Na, and an input part of the inverter I**1** and an output part of the inverter I**2** are electrically connected to the storage terminal Nb, so that the CMOS inverters I**1** and I**2** are subjected to cross section. Thereby, the storage terminals Na and Nb can store information of mutually inverted logical level.

The NMOS transistor N**3** is interposed between a bit line BLA and the storage terminal Na, and its gate is connected to a word line WL. The NMOS transistor N**4** is interposed between a bit line BLB and the storage terminal Nb, and its gate is connected to the word line WL.

In such a configuration, the word line WL is brought into the active state and the NMOS transistors NT**3** and NT**4** are brought into the on state, thereby to provide access (i.e., read or write) to the storage terminals Na and Nb. This enables to obtain the data from the bit line BLA or BLB.

Referring to FIGS. **1** to **3**, description will proceed to the memory cell structure of the first preferred embodiment.

In the N well region NW, the PMOS transistor P1 is made up of P^+ diffusion regions FL**110**, FL**111**, and a polysilicon wiring PL**1**, and the PMOS transistor P**2** is made up of P^+ diffusion regions FL**120**, FL**121**, and a polysilicon wiring PL**2**.

In the P well region PW**0**, the NMOS transistor **N1** is made up of N^+ diffusion regions FL**210**, FL**211**, and the polysilicon wiring PL**1**, and the NMOS transistor N**4** is made up of N^+ diffusion regions FL**240**, FL**241**, and a polysilicon wiring PL**4**. The polysilicon wiring PL**1** extends from the N well region NW to the P well region PW**0**, so as to be used as a gate common to the NMOS transistor N**1** and PMOS transistor P**1**.

In the P well region PW**1**, the NMOS transistor N**2** is made up of N^+ diffusion regions FL**220**, FL**221**, and the polysilicon wiring PL**2**, and the NMOS transistor N**3** is made up of N^+ diffusion regions FL**230**, FL**231**, and a polysilicon wiring PL**3**. The polysilicon wiring PL**2** extends from the N well region NW to the P well region PW**1**, so as to be used as a gate common to the NMOS transistor N**2** and PMOS transistor P**2**.

The foregoing diffusion regions FL**110**, FL**111**, FL**120**, FL**121**, FL**210**, FL**211**, FL**220**, FL**221**, FL**230**, FL**231**, FL**240** and FL**241** are obtainable by implanting and diffusing impurity.

A ground wiring LG**1** (first layer aluminum wiring) over the diffusion region FL**210** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**210**. An aluminum wiring AL**11**, which is a first layer aluminum wiring extending over the diffusion region FL**211**, FL**111** and FL**231**, is electrically connected through a diffusion contact hole **1**C to the diffusion regions FL**211**, FL**111** and FL**231**, respectively. The aluminum wiring AL**11** is also disposed over part of the polysilicon wiring PL**2**, and is electrically connected through a gate contact hole GC to the polysilicon wiring PL**2**. The aluminum wiring AL**11** can be electrically connected with low impedance, and it corresponds to the storage terminal Na.

The diffusion contact hole **1**C means a contact hole between a diffusion region and a first layer (aluminum) wiring. The gate contact hole GC means a contact hole between a polysilicon wiring and a first layer wiring.

The polysilicon wiring PL**4** is electrically connected through a gate contact hole GC to the word line WL**1** (first layer aluminum wiring). A bit line BLB**1** (first layer aluminum wiring) over the diffusion region FL**241** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**241**.

An aluminum wiring AL**12**, which is a first layer aluminum wiring extending over the diffusion regions FL**240**, FL**120** and FL**220**, is electrically connected through a diffusion contact hole **1**C to the diffusion regions FL**240**, FL**120** and FL**220**, respectively. The aluminum wiring AL**12** is also disposed over part of the polysilicon wiring PL**1**, and is electrically connected through a gate contact hole GC to the polysilicon wiring PL**1**. The aluminum wiring AL**12** can be electrically connected with low impedance, and it corresponds to the storage terminal Nb.

A power supply wiring LV**1** (first layer aluminum wiring) over the diffusion region FL**110** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**110**. The power supply wiring LV**1** over the diffusion region FL**121** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**121**.

A bit line BLA**1** (first layer aluminum wiring) over the diffusion region FL**230** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**230**. A word line WL**1** over the polysilicon wiring PL**3** is electrically connected through a gate contact hole GC to the polyslicon wiring PL**3**. A ground wiring LG**1** over the diffusion region FL**221** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**221**.

A ground wiring LG**1** is electrically connected through a via hole **1**T to a ground wiring LG**2** (second layer aluminum wiring (**2**AL)), and the ground wiring LG**2** is electrically connected through a via hole **2**T to a ground wiring LG**3** (third layer aluminum wiring (**3**AL)).

A word line WL**1** is electrically connected through a via hole **1**T to a word line WL**2** (second layer aluminum wiring), and the word line WL**2** is electrically connected through a via hole **2**T to a word line WL**3** (third layer aluminum wiring). The word line WL shown in FIG. **4** is made up of these word lines WL**1** to WL**3**.

The via hole **1**T means a via hole to make connection between a first layer wiring and a second layer (aluminum) wiring. The via hole **2**T means a via hole to make connection between a second layer wiring and a third layer (aluminum) wiring.

The word line WL**3** and ground wiring LG**3** are disposed parallel with each other, across the P well regions PW**0**, PW**1**, and the N well region NW. Two ground wirings LG**3** are disposed with the word line WL**3** interposed therebetween.

A bit line BLA**2** (second layer aluminum wiring) is electrically connected through a via hole **1**T to a bit line BLA**1** (not shown in FIG. **3**). A bit line BLB**2** (second layer aluminum wiring) is electrically connected through a via hole **1**T to a bit line BLB**1** (not shown in FIG. **3**). A power supply wiring LV**2** (second layer aluminum wiring) is electrically connected through a via hole **1**T to a power supply wiring LV**1** (not shown in FIG. **3**). The bit lines BLA and BLB shown in FIG. **4** are made up of the bit lines BLA**1** and BLA**2**, and the bit lines BLB**1** and BLB**2**, respectively.

The bit lines BLA**2**, BLB**2** and the power supply wiring LV**2** are disposed over the P well regions PW**1**, PW**0** and the N well region NW, respectively, so as to be parallel to each other in the longitudinal direction viewing the drawing.

Thus, in the memory cell structure of the SRAM of the first preferred embodiment, with the N well region NW interposed between the P well regions PW**0** and PW**1**, the NMOS transistors N**1** and N**4** are disposed in the P well region PW**0**, and the NMOS transistors N**2** and N**3** are disposed in the P well region PW**1**. Thereby, the N^+ diffusion region FL**211** and the N^+ diffusion region FL**220** that are electrically connected to the storage terminals Na and Nb, respectively, can be separately formed in the different P well regions PW**0** and PW**1**.

As a result, there are the following effects. Firstly, when electrons generated from alpha rays and neutron beams are collected into the N^+ diffusion region formed in one of the P well regions PW**0** and PW**1**, such electrons are released from the N^+ diffusion region formed in the other P well region where the influence of the generated electrons can be avoided by the presence of the N well region NW. This cancels out the occurrence of electrons acting to invert the hold data of the storage terminals Na and Nb, and thus the inversion of data is hard to occur. That is, there is the effect of improving resistance to soft error (This is hereinafter referred to as the first effect.).

Secondly, since the P well regions PW**0** and PW**1** are separately formed in a direction vertical to the direction of formation of the bit lines BLA and BLB, the formation of the two P well regions PW**0** and PW**1** exerts no influence on the wiring length of the bit lines BLA and BLB. Hence, there is

no possibility that the formation of the P well regions PW**0** and PW**1** increases the wiring length of the bit lines, thus maintaining a good access time (This is hereinafter referred to as the second effect.).

Thirdly, since the NMOS transistors N**1** and N**2**, and the NMOS transistors N**3** and N**4**, are respectively arranged so as to be point symmetry with respect to the central part of the memory cell (the central part of the N well region NW), the degree of integration can be increased when a plurality of the memory cells of the first preferred embodiment are disposed adjacent each other (This is hereinafter referred to as the third effect.).

Fourthly, the formation of the polysilicon wirings PL**1** to PL**4** in the same direction (the lateral direction viewing the drawing) facilitates the control of the gate dimension. Further, because the polysilicon wirings PL**1** and PL**3** (NMOS transistors N**1**, N**3**, and PMOS transistor P**1**), and the polysilicon wirings PL**2** and PL**4** (NMOS transistors N**2**, N**4**, and PMOS transistor P**2**) are respectively arranged in a straight line, no waste region is present and a reduction in the circuit area increases the degree of integration (This is hereinafter referred to as the fourth effect.).

Fifthly, by separately forming a region serving as a drain (i.e., a region electrically connected to the storage terminal Na or Nb) in the NMOS transistors N**1** to N**4**, resistance to soft error can be maintained at a high level (a fifth effect).

Sixthly, with the arrangement that each of inverters I**1** and I**2** of a CMOS structure is made up of a combination of a NMOS transistor and a PMOS transistor, the memory cell can be realized by at least sufficient circuit configuration as a CMOS structure (a sixth effect).

Second Preferred Embodiment

FIGS. **5** and **6** are diagrams illustrating a memory cell structure of a SRAM according to a second preferred embodiment of the invention. FIG. **5** is an explanatory diagram viewed from above the layout configuration in all layers. FIG. **6** is an explanatory diagram viewed from above mainly the layout configuration beneath a first aluminum wiring layer in FIG. **5**. An explanatory diagram viewed from above the layout configuration over a second aluminum wiring layer in FIG. **5** is similar to that of FIG. **3** in the first preferred embodiment. A circuit diagram illustrating an equivalent circuit of the second preferred embodiment is similar to that of FIG. **4**. Some reference numerals used in FIG. **6** or **3** are omitted in FIG. **5**.

As seen from these figures, over a rectangular N^+ diffusion region for a NMOS transistor N**1**, a polysilicon wiring PL**1** is formed by bending it from the central part of the N^+ diffusion region, so that a relatively wide diffusion region FL**212** and a relatively narrow diffusion region FL**213** are formed on the outside and inside of the polysilicon wiring PL**1**, respectively. The NMOS transistor N**1** is made up of the diffusion regions FL**212**, FL**213**, and the polysilicon wiring PL**1**.

Likewise, over a rectangular N^+ diffusion region for a NMOS transistor N**2**, a polysilicon wiring PL**2** is formed by bending it from the central part of the N^+ diffusion region, so that a relatively wide diffusion region FL**223** and a relatively narrow diffusion region FL**222** are formed on the outside and inside of the polysilicon wiring PL**2**, respectively. The NMOS transistor N**2** is made up of the diffusion regions FL**222**, FL**223**, and the polysilicon wiring PL**2**.

A ground wiring LG**1** over the diffusion region FL**212** is electrically connected through two diffusion contact holes **1**C to the diffusion region FL**212**. An aluminum wiring AL**11** over the diffusion region FL**213** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**213**.

Likewise, a ground wiring LG**1** over the diffusion region FL**223** is electrically connected through two diffusion contact holes **1**C to the diffusion region FL**223**. An aluminum wiring AL**12** over the diffusion region FL**222** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**222**. Otherwise, the layout configuration is similar to that of the first preferred embodiment, and the description thereof is thus omitted.

The second preferred embodiment having the foregoing layout configuration produces the following effects in addition to the first, second, fifth and sixth effects of the first preferred embodiment.

It is able to increase the gate width (channel width) of the NMOS transistors N**1** and N**2** that are driver transistors. As a result, the operation speed can be increased by quickly removing the carriers of the bit lines BLA and BLB.

Additionally, the ratio of a gate width W to the NMOS transistors N**3** and N**4**, which are the respective access transistors of the NMOS transistors N**1** and N**2** that are driver transistors, can be increased to improve the stability of the memory cell.

FIG. **7** is an explanatory diagram viewed from above the layout configuration between adjacent cells. Like FIG. **6**, FIG. **7** illustrates mainly the layout configuration beneath a first aluminum wiring layer in FIG. **5**.

In FIG. **7**, there are shown an N well region NW and a P well region PW**0** of a memory cell MC**1**, and an N well region NW and a P well region PW**0** of a memory cell MC**2**.

The NMOS transistors N**1** and N**2** are respectively arranged so as to be point symmetry with respect to the central part of the memory cell (the central part of the N well region NW). This corresponds to the third effect of the first preferred embodiment. Referring to FIG. **7**, between the adjacent memory cells MC**1** and MC**2**, the NMOS transistors N**1** (N**2**), each being a driver transistor, can be disposed adjacent each other in line symmetric relation, thereby to increase the gate width W of the NMOS transistors N**1** and N**2**, while increasing the degree of integration by having the diffusion region FL**212**, word line WL**1**, ground wiring LG**1**, diffusion contact hole **1**C and gate contact hole GC share at least their respective portions.

Thus, there is little or no increase of area due to the bending of the polysilicon wirings PL**1** and PL**2** that become the gates of the NMOS transistors N**1** and N**2**, respectively. It is therefore able to obtain a high-density memory cell structure similar to that of the first preferred embodiment.

In addition, the degree of integration can be increased by disposing the NMOS transistors N**1**, N**3** and PMOS transistor P**1**; and the NMOS transistors N**2**, N**4** and PMOS transistor P**2**, in an approximately straight line, respectively. This corresponds to the fourth effect of the first preferred embodiment.

Third Preferred Embodiment

FIGS. **8** to **10** are diagrams illustrating a memory cell structure of a SRAM according to a third preferred embodiment of the invention. FIG. **8** is an explanatory diagram viewed from above the layout configuration in all layers. FIG. **9** is an explanatory diagram viewed from above mainly the layout configuration beneath a first aluminum wiring layer in FIG. **8**. An explanatory diagram viewed from above the layout configuration over a second aluminum wiring layer in FIG. **8** is similar to that of FIG. **3** in the first preferred embodiment. Some reference numerals used in FIG. **9** or **3** are omitted in FIG. **8**.

FIG. 10 is a circuit diagram illustrating an equivalent circuit of the SRAM memory cell having the layout configuration shown in FIGS. 8, 9 and 3. Referring to FIG. 10, a resistance R1 is interposed between a storage terminal Nb and the gate of a NMOS transistor N1 and a PMOS transistor P1. A resistance R2 is interposed between a storage terminal Na and the gate of a NMOS transistor N2 and a PMOS transistor P2. Otherwise, the configuration is similar to that of the first preferred embodiment described with respect to FIG. 4, and the description thereof is thus omitted.

Referring to FIGS. 8, 9 and 3, description will proceed to the memory cell structure of the third preferred embodiment.

As shown in these figures, a polysilicon wiring PL13 (corresponding to the polysilicon wiring PL1 of the first preferred embodiment), which becomes the gate of the NMOS transistor N1 and PMOS transistor P1, is electrically connected to a high resistance metal wiring M00 that becomes the resistance R1. The high resistance metal wiring M00 is electrically connected through a via hole 0T to an aluminum wiring AL12 that is the storage terminal Nb. The via hole 0T means a via hole to make connection between the high resistance metal wiring M00 formed in the same layer as the polysilicon wiring, and a first layer wiring.

Likewise, a polysilicon wiring PL14 (corresponding to the polysilicon wiring PL2 of the first preferred embodiment), which becomes the gate of the NMOS transistor N2 and PMOS transistor P2, is electrically connected to a high resistance metal wiring M01 that becomes the resistance R2. The high resistance metal wiring M01 is electrically connected through a via hole 0T to the aluminum wiring AL11 that is the storage terminal Na.

Examples of material of the high resistance metal wirings M00 and M01 are tungsten, etc., having a higher resistivity than CoSi (cobalt silicon). Otherwise, the configuration is similar to that of the first preferred embodiment described with respect to FIGS. 1 to 3, and the description thereof is thus omitted.

The third preferred embodiment having the foregoing memory cell structure produces the following effect in addition to the first to sixth effects of the first preferred embodiment.

In the memory cell of the third preferred embodiment, the response characteristic for inverting the data held in the cell is elongated due to signal delay propagating the resistances R1 and R2. As a result, even if the potential of one of the storage terminals Na and Nb is inverted by electrons generated from alpha rays and neutron beams, it returns to the initial hold state before the data of the other storage terminal is inverted, thereby soft error becomes much rare.

Fourth Preferred Embodiment

FIGS. 11 and 12 are diagrams illustrating a memory cell structure of a SRAM according to a fourth preferred embodiment of the invention. FIG. 11 is an explanatory diagram viewed from above the layout configuration in all layers. FIG. 12 is an explanatory diagram viewed from above mainly the layout configuration beneath a first aluminum wiring layer in FIG. 11. An explanatory diagram viewed from above the layout configuration over a second aluminum wiring layer in FIG. 11 is similar to that of FIG. 3 in the first preferred embodiment. Some reference numerals used in FIG. 12 or 3 are omitted in FIG. 11. An equivalent circuit of the SRAM memory cell having the layout configuration of the fourth preferred embodiment is similar to that of the third preferred embodiment described with respect to FIG. 10.

Referring to FIGS. 11, 12 and 3, description will proceed to the memory cell structure of the fourth preferred embodiment.

Of polysilicon wirings PL13 and PL17 (corresponding to the polysilicon wiring PL1 of the first preferred embodiment), which become the gate of a NMOS transistor N1 and a PMOS transistor P1, the polysilicon wiring PL17 that becomes a resistance R1 is formed from a material having a higher resistance than the polysilicon wiring PL13. For instance, when the polysilicon wiring PL13 is formed from CoSi, the polysilicon wiring PL17 is formed from a material having a higher resistivity than CoSi.

The polysilicon wiring PL17 is electrically connected through a gate contact hole GC to an aluminum wiring AL12 that is a storage terminal Nb.

Likewise, of polysilicon wirings PL14 and PL18 (corresponding to the polysilicon wiring PL2 of the first preferred embodiment), which become the gate of a NMOS transistor N2 and a PMOS transistor P2, the polysilicon wiring PL18 that becomes a resistance R2 is formed from a material having a higher resistance than the polysilicon wiring PL14. The polysilicon wiring PL18 is electrically connected through a gate contact hole GC to an aluminum wiring AL11 that is a storage terminal Na. Otherwise, the configuration is similar to that of the first preferred embodiment described with respect to FIGS. 1 to 3, and the description thereof is thus omitted.

The fourth preferred embodiment having the foregoing memory cell structure produces the following effect in addition to the first to sixth effects of the first preferred embodiment.

In the memory cell of the fourth preferred embodiment, the response characteristic for inverting the data held in the cell is elongated due to signal delay propagating the resistances R1 and R2. As a result, even if the potential of one of the storage terminals Na and Nb is inverted by electrons generated from alpha rays and neutron beams, it returns to the initial hold state before the data of the other storage terminal is inverted, thereby soft error becomes much rare.

Fifth Preferred Embodiment

FIGS. 13 to 15 are diagrams illustrating a memory cell structure of a SRAM according to a fifth preferred embodiment of the invention. FIG. 13 is an explanatory diagram viewed from above the layout configuration in all layers. FIG. 14 is an explanatory diagram viewed from above mainly the layout configuration over a second aluminum wiring layer in FIG. 13. An explanatory diagram viewed from above the layout configuration beneath a first aluminum wiring layer in FIG. 13 is similar to that of FIG. 2 in the first preferred embodiment, except that the word line WL2 is divided into word lines WLA2 and WLB2. Some reference numerals used in FIG. 14 or 2 are omitted in FIG. 13.

FIG. 15 is a circuit diagram illustrating an equivalent circuit of the SRAM memory cell having the layout configuration shown in FIGS. 13, 14 and 2. Referring to FIG. 15, a word line WLA is connected to the gate of a NMOS transistor N3, and a word line WLB that is independent of the word line WLA is connected to the gate of a NMOS transistor N4. Otherwise, the configuration is similar to that of the first preferred embodiment described with respect to FIG. 4, and the description thereof is thus omitted.

Referring to FIGS. 13, 14 and 2, description will proceed to the memory cell structure of the fifth preferred embodiment.

A polysilicon wiring PL3 is electrically connected through a gate contact hole GC to a word line WLA1 (first

layer aluminum wiring). The word line WLA**1** is electrically connected through a via hole **1**T to a word line WLA**2** (second layer aluminum wiring). The word line WLA**2** is electrically connected through a via hole **2**T to a word line WLA**3** (third layer aluminum wiring). The word line WLA of FIG. **15** is made up of these word lines WLA**1** to WLA**3**.

Likewise, a polysilicon wiring PL**4** is electrically connected through a gate contact hole GC to a word line WLB**1** (first layer aluminum wiring). The word line WLB**1** is electrically connected through a via hole **1**T to a word line WLB**2** (second layer aluminum wiring). The word line WLB**2** is electrically connected through a via hole **2**T to a word line WLB**3** (third layer aluminum wiring). The word line WLB of FIG. **15** is made up of these word lines WLB**1** to WLB**3**.

The word line WLA**3**, WLB**3** and a ground wiring LG**3** are disposed parallel with each other, across P well regions PW**0**, PW**1** and an N well region NW. Two ground wirings LG**3** are disposed with the word lines WLA**3** and WLB**3** interposed therebetween. Otherwise, the layout configuration is similar to that of the first preferred embodiment, and the description thereof is thus omitted.

The fifth preferred embodiment having the foregoing memory cell structure produces the following effect in addition to the first to sixth effects of the first preferred embodiment.

As shown in the equivalent circuit of FIG. **15**, the word line connected to the gate of the NMOS transistors N**3** and N**4** that are access transistors can be divided into the word lines WLA and WLB. This enables to realize a memory cell structure usable in a FIFO memory.

Sixth Preferred Embodiment

FIGS. **16** to **18** are diagrams illustrating a memory cell structure of a SRAM according to a sixth preferred embodiment of the invention. FIG. **16** is an explanatory diagram viewed from above the layout configuration in all layers. FIG. **17** is an explanatory diagram viewed from above mainly the layout configuration beneath a first aluminum wiring layer in FIG. **16**. FIG. **18** is an explanatory diagram viewed from above the layout configuration over a second aluminum wiring layer in FIG. **16**. Some reference numerals used in FIG. **17** or **18** are omitted in FIG. **16**. An equivalent circuit of the SRAM memory cell having the layout configuration of the sixth preferred embodiment is similar to that of FIG. **15** described in the fifth preferred embodiment.

Referring to FIGS. **16** to **18**, description will proceed to the memory cell structure of the sixth preferred embodiment.

In an N^+ diffusion region for NMOS transistors N**3** and N**4**, the direction of formation of a source/drain region is located at an angle of 90° to the direction of formation of a source/drain region of NMOS transistors N**1**, N**2** and PMOS transistors P**1**, P**2**. That is, diffusion regions FL**242** and FL**243** for the NMOS transistor N**3**, and diffusion regions FL**232** and FL**233** for the NMOS transistor N**4**, are disposed in the lateral direction viewing the drawing.

A bit line BLB**1** over the diffusion region FL**243** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**243**. A bit line BLB**2** (second layer aluminum wiring) is electrically connected through a via hole **1**T to the bit line BLB**1** (not shown in FIG. **18**).

Likewise, a bit line BLA**1** over the diffusion region FL**232** constituting the NMOS transistor N**3** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**232**. A bit line BLA**2** (second layer aluminum wiring) is electrically connected through a via hole **1**T to the bit line BLA**1** (not shown in FIG. **18**).

The bit lines BLA**2** and BLB**2** are disposed parallel with each other, across P well regions PW**0**, PW**1** and an N well region NW.

A ground wiring LG**1** is electrically connected through a diffusion contact hole **1**C to diffusion regions FL**210** and FL**221**. A ground wiring LG**2** is electrically connected through a via hole **1**T to the ground wiring LG**1** (not shown in FIG. **18**). A ground wiring LG**3** is electrically connected through a via hole **2**T to the ground wiring LG**2**.

A power supply wiring LV**1** is electrically connected through a diffusion contact hole **1**C to diffusion regions FL**110** and FL**121**. A power supply wiring LV**2** is electrically connected through a via hole **1**T to the power supply wiring LV**1** (not shown in FIG. **18**). A power supply wiring LV**3** is electrically connected through a via hole **2**T to the power supply wiring LV**2**.

A word line WLA**1** is electrically connected through a gate contact hole GC to a polysilicon wiring PL**23**. A word line WLA**2** is electrically connected through a via hole **1**T to the word line WLA**1** (not shown in FIG. **18**). A word line WLA**3** (third layer aluminum wiring) is electrically connected through a via hole **2**T to the word line WLA**2**.

Likewise, a word line WLB**1** is electrically connected through a gate contact hole GC to a polysilicon wiring PL**24**. A word line WLB**2** is electrically connected through a via hole **1**T to the word line WLB**1** (not shown in FIG. **18**). A word line WLB**3** (third layer aluminum wiring) is electrically connected through a via hole **2**T to the word line WLB**2**.

The (first) ground wiring LG**3**, word line WLB**3**, power supply wiring LV**3**, word line WLA**3** and (second) ground wiring LG**3** are disposed parallel with each other in the longitudinal direction viewing the drawing. The (first) ground wiring LG**3** and word line WLB**3** are disposed over the P well region PW**0**. The power supply wiring LV**3** is disposed over the N well region NW. The word line WLA**3** and (second) ground wiring LG**3** are disposed over the P well region PW**1**.

The sixth preferred embodiment having the foregoing memory cell structure produces the effect equivalent to that inherent in the fifth preferred embodiment, in addition to the first to third, fifth and sixth effects of the first preferred embodiment.

Seventh Preferred Embodiment

FIGS. **19** to **21** are diagrams illustrating a memory cell structure of a SRAM according to a seventh preferred embodiment of the invention. FIG. **19** is an explanatory diagram viewed from above the layout configuration in all layers. FIG. **20** is an explanatory diagram viewed from above mainly the layout configuration beneath a first aluminum wiring layer in FIG. **19**. FIG. **21** is an explanatory diagram viewed from above the layout configuration over a second aluminum wiring layer in FIG. **19**. Some reference numerals used in FIG. **20** or **21** are omitted in FIG. **19**. An equivalent circuit of the SRAM memory cell having the layout configuration of the seventh preferred embodiment is similar to that of FIG. **4** in the first preferred embodiment.

Referring to FIGS. **19** to **21**, description will proceed to the memory cell structure of the seventh preferred embodiment.

A common polysilicon wiring PL**5** of NMOS transistors N**3** and N**4** extends over a P well region PW**0**, N well region NW and P well region PW**1**. The common polysilicon wiring PL**5** is used as the word line WL of FIG. **4**.

Otherwise, the configuration is similar to that of the second preferred embodiment described with respect to FIGS. **5**, **6** and **3**, except for the pattern shape of polysilicon

wirings PL**1** and PL**2**, the position of a gate contact hole GC between a polysilicon wiring PL**1** and an aluminum wiring AL**12**, and the position of a gate contact hole GC between a polysilicon wiring PL**2** and an aluminum wiring AL**11**.

The seventh preferred embodiment having the foregoing memory cell structure produces the same effects as the second preferred embodiment. In addition, since the word line WL does not require any of via holes **1**T, **2**T and word lines WL**2**, WL**3**, the number of necessary layers is reduced to lower the cost.

Eighth Preferred Embodiment

FIGS. **22** to **25** are diagrams illustrating a memory cell structure of a SRAM according to an eighth preferred embodiment of the invention. FIG. **22** is an explanatory diagram viewed from above the layout configuration in all layers. FIG. **23** is an explanatory diagram viewed from above mainly the layout configuration beneath a first aluminum wiring layer in FIG. **22**. FIG. **24** is an explanatory diagram viewed from above the layout configuration over a second aluminum wiring layer in FIG. **22**. Some reference numerals used in FIG. **23** or **24** are omitted in FIG. **22**.

FIG. **25** is a circuit diagram illustrating an equivalent circuit of the SRAM memory cell having the layout configuration shown in FIGS. **22** to **24**. Referring to FIG. **25**, the SRAM memory cell of the eighth preferred embodiment is made up of NMOS transistors N**1**, N**2**, N**5** to N**8**, and PMOS transistors P**1** and P**2**.

The NMOS transistor N**5** is interposed between a bit line BLA and a storage terminal Nb. The NMOS transistor N**6** is interposed between a bit line $\overline{BLA}$ and a storage terminal Na. The gates of the NMOS transistors N**5** and N**6** are both connected to a word line WLA.

The NMOS transistor N**7** is interposed between a bit line BLB and a storage terminal Na. The NMOS transistor N**8** is interposed between a bit line $\overline{BLB}$ and a storage terminal Nb. The gates of the NMOS transistors N**7** and N**8** are both connected to a word line WLB.

The PMOS transistors P**1** and P**2** that are driver transistors are disposed within an N well region NW. The NMOS transistor N**1** that is a driver transistor and the NMOS transistors N**7** and N**8** that are access transistors are disposed within a P well region PW**0**. The NMOS transistor N**2** that is a driver transistor and the NMOS transistors N**5** and N**6** that are access transistors are disposed within a P well region PW**1**. The P well regions PW**0** and PW**1** are oppositely disposed with the N well region NW interposed therebetween. Otherwise, the configuration is similar to that of the equivalent circuit of FIG. **15** described in the fifth preferred embodiment.

Referring to FIGS. **22** to **24**, description will proceed to the memory cell structure of the eighth preferred embodiment.

In the N well region NW, the PMOS transistor P**1** is made up of P^+ diffusion regions FL**110**, FL**111** and a polysilicon wiring PL**17**, and the PMOS transistor P**2** is made up of P^+ diffusion regions FL**120**, FL**121** and a polysilicon wiring PL**18**.

In the P well region PW**0**, the NMOS transistor N**1** is made up of N^+ diffusion regions FL**212**, FL**213** and the polysilicon wiring PL**17**. The NMOS transistor N**7** is made up of N^+ diffusion regions FL**244**, FL**245** and a polysilicon wiring PL**20**. The NMOS transistor N**8** is made up of N^+ diffusion regions FL**246**, FL**247** and the polysilicon wiring PL**20**. The polysilicon wiring PL**17** extends from the N well region NW to the P well region PW**0**, so as to be used as a gate common to the NMOS transistor N**1** and PMOS transistor P**1**. The polysilicon wiring PL**20** is common to the NMOS transistors N**7** and N**8**.

In the P well region PW**1**, the NMOS transistor N**2** is made up of N^+ diffusion regions FL**222**, FL**223** and the polysilicon wiring PL**18**. The NMOS transistor N**5** is made up of N^+ diffusion regions FL**234**, FL**235** and a polysilicon wiring PL**19**. The NMOS transistor N**3** is made up of N^+ diffusion regions FL**236**, FL**237** and a polysilicon wiring PL**19**. The polysilicon wiring PL**18** extends from the N well region NW to the P well region PW**1**, so as to be used as a gate common to the NMOS transistor N**2** and PMOS transistor P**2**. The polysilicon wiring PL**18** is common to the NMOS transistors N**5** and N**6**. The foregoing diffusion regions are obtainable by implanting and diffusing impurity.

A ground wiring LG**1** over the diffusion region FL**212** is electrically connected through a diffusion contact hole **11**C to the diffusion region FL**212**. A bit line BLB**1** over the diffusion region FL**245** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**245**. A bit line $\overline{BLB1}$ over the diffusion region FL**247** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**247**.

An aluminum wiring AL**15**, which is a first layer aluminum wiring extending over the diffusion regions FL**244**, FL**213**, FL**111** and FL**237**, is electrically connected through a diffusion contact hole **1**C to the diffusion regions FL**244**, FL**213**, FL**111** and FL**237**, respectively. The aluminum wiring AL**15** is also disposed over part of the polysilicon wiring PL**18**, and is electrically connected through a gate contact hole GC to the polysilicon wiring PL**18**. The aluminum wiring AL**15** can be electrically connected with low impedance, and it corresponds to the storage terminal Na.

A polysilicon wiring PL**20** is electrically connected through a gate contact hole GC to a word line WLB**1**.

A power supply wiring LV**1** over the diffusion region FL**110** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**110**. A power supply wiring LV**1** over the diffusion region FL**121** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**121**.

The ground wiring LG**1** is electrically connected through two diffusion contact holes **1**C to the diffusion region FL**223**. A bit line BLA**1** over the diffusion region FL**234** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**234**. A bit line $\overline{BLA1}$ over the diffusion region FL**236** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**236**.

An aluminum wiring AL**16**, which is a first layer aluminum wiring extending over the diffusion regions FL**235**, FL**222**, FL**120** and FL**246**, is electrically connected through a diffusion contact hole **1**C to the diffusion regions FL**235**, FL**222**, FL**120** and FL**246**, respectively. The aluminum wiring AL**16** is also disposed over part of the polysilicon wiring PL**17**, and is electrically connected through a gate contact hole GC to the polysilicon wiring PL**17**. The aluminum wiring AL**16** can be electrically connected with low impedance, and it corresponds to the storage terminal Nb.

A word line WLA**1** over a polysilicon wiring PL**19** is electrically connected through a gate contact hole GC to the polysilicon wiring PL**19**.

A ground wiring LG**1** is electrically connected through a via hole **1**T to a ground wiring LG**2**, and the ground wiring LG**2** is electrically connected through a via hole **2**T to a ground wiring LG**3**.

The word line WLA**1** is electrically connected through a via hole **1**T to a word line WLA**2**, and the word line WLA**2**

is electrically connected through a via hole **2**T to a word line WLA**3**. The word line WLA of FIG. **25** is made up of these word lines WLA**1** to WLA**3**.

Likewise, a word line WLB**1** is electrically connected through a via hole **1**T to a word line WLB**2**, and the word line WLB**2** is electrically connected through a via hole **2**T to a word line WLB**3**. The word line WLB of FIG. **25** is made up of these word lines WLB**1** to WLB**3**.

The word lines WLA**3**, WLB**3**, and ground wiring LG**3** are disposed parallel with each other, across the P well regions PW**0**, PW**1**, and the N well region NW. Two ground wirings LG**3** are disposed with the word lines WLA**3** and WLB**3** interposed therebetween.

A bit line BLA**2** is electrically connected through a via hole **1**T to a bit line BLA**1**, and a bit line BLB**2** is electrically connected through a via hole **1**T to a bit line BLB**1**.

Likewise, a bit line $\overline{BLA2}$ is electrically connected through a via hole **1**T to a bit line $\overline{BLA1}$, and a bit line $\overline{BLB2}$ is electrically connected through a via hole **1**T to a bit line $\overline{BLB1}$.

A power supply wiring LV**2** is electrically connected through a via hole **1**T to a power supply wiring LV**1**. The bit lines BLA, $\overline{BLA}$, BLB and $\overline{BLB}$, are made up of the bit lines BLA**1** and BLA**2**; $\overline{BLA1}$ and $\overline{BLA2}$; BLB**1** and BLB**2**; and $\overline{BLB1}$ and $\overline{BLB2}$, respectively.

The paired bit lines BLA**2** and $\overline{BLA2}$, paired bit lines BLB**2** and $\overline{BLB2}$, and the power supply wiring LV**2** are disposed over the P well regions PW**1**, PW**0** and N well region NW, respectively, so that these are parallel with each other in the longitudinal direction viewing the drawing.

Thus, in the memory cell structure of the SRAM of the eighth preferred embodiment, with the N well region NW interposed between the P well regions PW**0** and PW**1**, the NMOS transistors N**1**, N**7** and N**8** are disposed in the P well region PW**0**, and the NMOS transistors N**2**, N**5** and N**6** are disposed in the P well region PW**1**. Thereby, the N^+ diffusion region FL**213** and the N^+ diffusion region FL**222** that are electrically connected to the storage terminals Na and Nb, respectively, can be separately formed in the different P well regions PW**0** and PW**1**.

As a result, it is able to increase resistance to soft error, which is the first effect of the first preferred embodiment.

Since the P well regions PW**0** and PW**1** are separately formed in a direction vertical to the direction of formation of the paired bit lines BLA and $\overline{BLA}$, and the paired bit lines BLB and $\overline{BLB}$, the formation of the two P well regions PW**0** and PW**1** exerts no influence on the wiring length of the paired bit lines BLA and $\overline{BLA}$, and the paired bit lines BLB and $\overline{BLB}$. Hence, there is no possibility that the formation of the P well regions PW**0** and PW**1** increases the wiring length of the bit lines, thus maintaining a good access time. This corresponds to the second effect of the first preferred embodiment.

Since the NMOS transistors N**1** and N**2**, the NMOS transistors N**5** and N**7**, and the NMOS transistors N**6** and N**8**, are respectively arranged so as to be point symmetry with respect to the central part of the memory cell (the central part of the N well region NW), the degree of integration can be increased when a plurality of the memory cells of the eighth preferred embodiment are disposed adjacent each other. This corresponds to the third effect of the first preferred embodiment.

The formation of the polysilicon wirings PL**17** to PL**20** in the same direction (the lateral direction viewing the drawing) facilitates the control of the gate dimension. Further, since the polysilicon wirings PL**17** and PL**19**, and the polysilicon wirings PL**18** and PL**20**, are respectively arranged in a straight line, no waste region is present and a reduction in the circuit area increases the degree of integration. This corresponds to the fourth effect of the first preferred embodiment.

By separately forming a region serving as a drain in the NMOS transistors N**1**, N**2** and N**5** to N**8**, resistance to soft error can be maintained at a high level. This corresponds to the fifth effect of the first preferred embodiment.

With the arrangement such that each of inverters I**1** and I**2** of a CMOS structure is made up of a combination of a NMOS transistor and a PMOS transistor, the memory cell can be realized by at least sufficient circuit configuration as a CMOS structure. This corresponds to the sixth effect of the first preferred embodiment.

In addition, the memory cell of the eighth preferred embodiment realizes a two-port memory cell which employs two word lines WLA and WLB, and two pairs of bit lines (the paired bit lines BLA and $\overline{BLA}$, and paired bit lines BLB and $\overline{BLB}$), as shown in FIG. **25**.

Ninth Preferred Embodiment

FIGS. **26** to **28** are diagrams illustrating a memory cell structure of a SRAM according to a ninth preferred embodiment of the invention. FIG. **26** is an explanatory diagram viewed from above the layout configuration in all layers. FIG. **27** is an explanatory diagram viewed from above mainly the layout configuration beneath a first aluminum wiring layer in FIG. **26**. FIG. **28** is an explanatory diagram viewed from above the layout configuration over a second aluminum wiring layer in FIG. **26**. Some reference numerals used in FIG. **27** or **28** are omitted in FIG. **26**.

An equivalent circuit of the SRAM memory cell having the layout configuration of the ninth preferred embodiment is similar to that of FIG. **25** in the eighth preferred embodiment.

Referring to FIGS. **26** to **28**, the memory cell structure of the ninth preferred embodiment will be described particularly with regard to the different points from the eighth preferred embodiment.

In a P well region PW**0**, a NMOS transistor N**1** is made up of N^+ diffusion regions FL**214**, FL**215** and a polysilicon wiring PL**31**. Here, a considerably large gate width than that of other NMOS transistors N**5** to N**8** can be set by forming the polysilicon wiring PL**31** by bending it 90° two times over the N^+ diffusion regions (FL**214**, FL**215**) for the NMOS transistor N**1**.

The NMOS transistor N**7** is made up of N^+ diffusion regions FL**270**, FL**271** and a polysilicon wiring PL**37**. The NMOS transistor N**8** is made up of N^+ diffusion regions FL**280**, FL**281** and a polysilicon wiring PL**38**.

The polysilicon wiring PL**31** extends from an N well region NW to the P well region PW**0**, so as to be used as a gate common to the NMOS transistor N**1** and a PMOS transistor P**1**.

In a P well region PW**1**, the NMOS transistor N**2** is made up of N^+ diffusion regions FL**224**, FL**225** and a polysilicon wiring PL**32**. Here, a considerably large gate width than that of the other NMOS transistors N**5** to N**8** can be set by forming the polysilicon wiring PL**32** by bending it 90° two times over the N^+ diffusion regions (FL**224**, FL**225**) for the NMOS transistor N**2**.

The NMOS transistor N**5** is made up of N^+ diffusion regions FL**250**, FL**251** and a polysilicon wiring PL**35**. The NMOS transistor N**6** is made up of N^+ diffusion regions FL**260**, FL**261** and a polysilicon wiring PL**36**.

The polysilicon wiring PL**32** extends from the N well region NW to the P well region PW**0**, so as to be used as a gate common to the NMOS transistor N**2** and a PMOS

transistor P**2**. The foregoing diffusion regions are obtainable by implanting and diffusing impurity.

Each of two ground wirings LG**1** over the diffusion region FL**214** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**214**. A bit line BLB**1** over the diffusion region FL**271** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**271**. A bit line $\overline{BLB1}$ over the diffusion region FL**280** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**280**.

An aluminum wiring AL**17**, which is a first layer aluminum wiring extending over the diffusion regions FL**281**, FL**215**, FL**111**, and FL**251**, is electrically connected through a diffusion contact hole **1**C to the diffusion regions FL**281**, FL**215**, FL**111** and FL**251**, respectively. The aluminum wiring AL**17** is also disposed over part of the polysilicon wiring PL**32**, and is electrically connected through a gate contact hole GC to the polysilicon wiring PL**32**. The aluminum wiring AL**17** can be electrically connected with low impedance, and it corresponds to a storage terminal Na.

The polysilicon wirings PL**37** and PL**38** are both electrically connected through a gate contact hole GC to a word line WLB**1**.

A power supply wiring LV**1** over the diffusion region FL**110** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**110**. A power supply wiring LV**1** over the diffusion region FL**121** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**121**.

Each of two ground wirings LG**1** over the diffusion region FL**224** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**224**. A bit line BLA**1** over the diffusion region FL**250** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**250**. A bit line $\overline{BLA1}$ over the diffusion region FL**261** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**261**.

An aluminum wiring AL**18**, which is a first layer aluminum wiring extending over the diffusion regions FL**260**, FL**224**, FL**120** and FL**270**, is electrically connected through a diffusion contact hole **1**C to the diffusion regions FL**260**, FL**224**, FL**120** and FL**270**, respectively. The aluminum wiring AL**18** is also disposed over part of the polysilicon wiring PL**31**, and is electrically connected through a gate contact hole GC to the polysilicon wiring PL**31**. The aluminum wiring AL**18** can be electrically connected with low impedance, and it corresponds to a storage terminal Nb.

A word line WLA**1** over the polysilicon wirings PL**35** and PL**36** is electrically connected through a gate contact hole GC to the polysilicon wirings PL**35** and PL**36**, respectively.

A ground wiring LG**1** is electrically connected through a via hole **1**T to a ground wiring LG**2**, and the ground wiring LG**2** is electrically connected through a via hole **2**T to a ground wiring LG**3**.

A word line WLA**1** is electrically connected through a via hole **1**T to a word line WLA**2**, and the word line WLA**2** is electrically connected through a via hole **2**T to a word line WLA**3**. Likewise, a word line WLB**1** is electrically connected through a via hole **1**T to a word line WLB**2**, and the word line WLB**2** is electrically connected through a via hole **2**T to a word line WLB**3**.

A bit line BLA**2** is electrically connected through a via hole **1**T to a bit line BLA**1**. A bit line BLB**2** is electrically connected through a via hole **1**T to a bit line BLB**1**.

Likewise, a bit line $\overline{BLA2}$ is electrically connected through a via hole **1**T to a bit line $\overline{BLA1}$, and a bit line $\overline{BLB2}$ is electrically connected through a via hole **1**T to a bit line $\overline{BLB1}$. A power supply wiring LV**2** is electrically connected through a via hole **1**T to a power supply wiring LV**1**.

Thus, in the memory cell structure of the SRAM of the ninth preferred embodiment, with the N well region NW interposed between the P well regions PW**0** and PW**1**, the NMOS transistors N**1**, N**7** and N**8** are disposed in the P well region PW**0**, and the NMOS transistors N**2**, N**5** and N**6** are disposed in the P well region PW**1**. This enables to increase resistance to soft error, which is the first effect of the first preferred embodiment.

By separately forming the P well regions PW**0** and PW**1** in a direction vertical to the direction of formation of the paired bit lines BLA and $\overline{BLA}$ and the paired bit lines BLB and $\overline{BLB}$, it is able to maintain a good access time, which is the second effect of the first preferred embodiment.

Further, in the ninth preferred embodiment, as in the eighth preferred embodiment, the NMOS transistors N**1** and N**2**, the NMOS transistors N**5** and N**7**, and the NMOS transistors N**6** and N**8**, are respectively arranged so as to be point symmetry with respect to the central part of the memory cell. It is therefore able to increase the degree of integration when a plurality of the memory cells of the ninth preferred embodiment are disposed adjacent each other. This corresponds to the third effect of the first preferred embodiment.

Furthermore, by separately forming a region serving as a drain in the NMOS transistors N**1**, N**2** and N**5** to N**8**, resistance to soft error can be maintained at a high level. This corresponds to the fifth effect of the first preferred embodiment.

By arranging such that each of inverters I**1** and I**2** of a CMOS structure is made up of a combination of a NMOS transistor and a PMOS transistor, the memory cell can be realized by at least sufficient circuit configuration as a CMOS structure. This corresponds to the sixth effect of the first preferred embodiment.

Like the eighth preferred embodiment, the memory cell of the ninth preferred embodiment can be used as a two-port memory cell.

Additionally, as in the second preferred embodiment, it is able to increase the operation speed and the stability of the memory cell by increasing the gate width (channel width) of the NMOS transistors N**1** and N**2**, each being a driver transistor.

Tenth Preferred Embodiment

FIGS. **29** to **31** are diagrams illustrating a memory cell structure of a SRAM according to a tenth preferred embodiment of the invention. FIG. **29** is an explanatory diagram viewed from above the layout configuration in all layers. FIG. **30** is an explanatory diagram viewed from above mainly the layout configuration beneath a first aluminum wiring layer in FIG. **29**. FIG. **31** is an explanatory diagram viewed from above the layout configuration over a second aluminum wiring layer in FIG. **29**. Some reference numerals used in FIG. **30** or **31** are omitted in FIG. **29**.

An equivalent circuit of the SRAM memory cell having the layout configuration of the tenth preferred embodiment is similar to that of FIG. **25** in the eighth preferred embodiment.

Referring to FIGS. **29** to **31**, description will proceed to the memory cell structure of the tenth preferred embodiment.

In an N well region NW, a PMOS transistor P**1** is made up of P^+ diffusion regions FL**110**, FL**111** and a polysilicon wiring PL**41**, and a PMOS transistor P**2** is made up of P^+ diffusion regions FL**120**, FL**121** and a polysilicon wiring PL**42**.

In a P well region PW0, a NMOS transistor N1 is made up of N^+ diffusion regions FL210, FL211 and the polysilicon wiring PL41, a NMOS transistor N7 is made up of N^+ diffusion regions FL270, FL271 and a polysilicon wiring PL47, and a NMOS transistor N8 is made up of N^+ diffusion regions FL280, FL281 and the polysilicon wiring PL47. The polysilicon wiring PL41 extends from the N well region NW to the P well region PW0, so as to be used as a gate common to the NMOS transistor N1 and PMOS transistor P1. The polysilicon wiring PL47 is common to the NMOS transistors N7 and N8.

In a P well region PW1, a NMOS transistor N2 is made up of N^+ diffusion regions FL220, FL221 and the polysilicon wiring PL42, a NMOS transistor N5 is made up of N^+ diffusion regions FL250, FL251 and a polysilicon wiring PL45, and a NMOS transistor N6 is made up of N^+ diffusion regions FL260, FL261 and the polysilicon wiring PL45. The polysilicon wiring PL42 extends from the N well region NW to the P well region PW1, so as to be used as a gate common to the NMOS transistor N2 and PMOS transistor P2. The polysilicon wiring PL42 is common to the NMOS transistors N5 and N6. The foregoing diffusion regions are obtainable by implanting and diffusing impurity.

A ground wiring LG1 over the diffusion region FL210 is electrically connected through a diffusion contact hole 1C to the diffusion region FL210. A bit line BLB1 over the diffusion region FL271 is electrically connected through a diffusion contact hole 1C to the diffusion region FL271. A bit line $\overline{BLB1}$ over the diffusion region FL281 is electrically connected through a diffusion contact hole 1C to the diffusion region FL281.

An aluminum wiring AL17, which is a first layer aluminum wiring extending over the diffusion region FL270 (FL211) and the diffusion region FL111, is electrically connected through a diffusion contact hole 1C to the diffusion regions FL270 (FL211) and FL111, respectively.

The aluminum wiring AL17 is also electrically connected to the polysilicon wiring PL42. The polysilicon wiring PL42 is electrically connected through a shared contact SC to the diffusion regions FL111 and FL261, respectively. As used herein, the term "shared contact" means a common contact electrically connecting a diffusion region and polysilicon.

The aluminum wiring AL17 can be electrically connected with low impedance. The aluminum wiring AL17, two shared contacts SC and polysilicon wiring PL42 correspond to a storage terminal Na.

The polysilicon wiring PL47 is electrically connected through a gate contact hole GC to a word line WLB1.

A power supply wiring LV1 over the diffusion region FL110 is electrically connected through a diffusion contact hole 1C to the diffusion region FL110. A power supply wiring LV1 over the diffusion region FL121 is electrically connected through a diffusion contact hole 1C to the diffusion region FL121.

A ground wiring LG1 is electrically connected through a diffusion contact hole 1C to the diffusion region FL221. A bit line BLA1 over the diffusion region FL250 is electrically connected through a diffusion contact hole 1C to the diffusion region FL250. A bit line $\overline{BLA1}$ over the diffusion region FL260 is electrically connected through a diffusion contact hole 1C to the diffusion region FL260.

An aluminum wiring AL18, which is a first layer aluminum wiring extending over the diffusion region FL251 (FL220) and the diffusion region FL120, is electrically connected through a diffusion contact hole 1C to the diffusion regions FL251 (FL220).

The aluminum wiring AL18 is also electrically connected to the polysilicon wiring PL41. The polysilicon wiring PL41 is electrically connected through a shared contact SC to the diffusion regions FL120 and FL280, respectively.

The aluminum wiring AL18 can be electrically connected with low impedance. The aluminum wiring AL18, two shared contacts SC and polysilicon wiring PL41 correspond to a storage terminal Nb.

A word line WLA1 over the polysilicon wiring PL45 is electrically connected through a gate contact hole GC to the polysilicon wiring PL45.

A word line WLA1 is electrically connected through a via hole 1T to a word line WLA2, and the word line WLA2 is electrically connected through a via hole 2T to a word line WLA3. Likewise, a word line WLB1 is electrically connected through a via hole 1T to a word line WLB2, and the word line WLB2 is electrically connected through a via hole 2T to a word line WLB3.

The word lines WLA3 and WLB3 are disposed parallel with each other, across the P well regions PW0, PW1, and the N well region NW.

A bit line BLA2 is electrically connected through a via hole 1T to a bit line BLA1. A bit line BLB2 is electrically connected through a via hole 1T to a bit line BLB1.

Likewise, a bit line $\overline{BLA2}$ is electrically connected through a via hole 1T to a bit line $\overline{BLA1}$. A bit line $\overline{BLB2}$ is electrically connected through a via hole 1T to a bit line $\overline{BLB1}$.

A power supply wiring LV2 is electrically connected through a via hole 1T to a power supply wiring LV1. A ground wiring LG1 is electrically connected through a via hole 1T to a ground wiring LG2.

The paired bit lines BLA2 and $\overline{BLA2}$, paired bit lines BLB2 and $\overline{BLB2}$, ground wiring LG2 and power supply wiring LV2 are disposed parallel with each other in the longitudinal direction viewing the drawing.

The paired bit lines BLA2 and $\overline{BLA2}$ and the ground wiring LG2 are disposed over the P well region PW1. The paired bit lines BLB2 and $\overline{BLB2}$ and the ground wiring LG2 are disposed over the P well region PW0. The power supply wiring LV2 is disposed over the N well region NW.

Thus, in the memory cell structure of the SRAM of the tenth preferred embodiment, with the N well region NW interposed between the P well regions PW0 and PW1, the NMOS transistors N1, N7 and N8 are disposed in the P well region PW0, and the NMOS transistors N2, N5 and N6 are disposed in the P well region PW1. This enables to increase resistance to soft error, which is the first effect of the first preferred embodiment.

By separately forming the P well regions PW0 and PW1 in a direction vertical to the direction of formation of the paired bit lines BLA and $\overline{BLA}$ and the paired bit lines BLB and $\overline{BLB}$, it is able to maintain a good access time, which is the second effect of the first preferred embodiment.

Further, in the tenth preferred embodiment as in the eighth preferred embodiment, the NMOS transistors N1 and N2, the NMOS transistors N5 and N7, and the NMOS transistors N6 and N8, are respectively arranged so as to be point symmetry with respect to the central part of the memory cell. It is therefore able to increase the degree of integration when a plurality of the memory cells of the tenth preferred embodiment are disposed adjacent each other. This corresponds to the third effect of the first preferred embodiment.

The memory cell of the tenth preferred embodiment realizes a two-port memory cell, as in the eighth preferred embodiment.

The formation of the polysilicon wirings PL**41**, PL**42**, PL**47** and PL**48** in approximately the same direction (the lateral direction viewing the drawing) facilitates the control of the gate dimension. Further, because the polysilicon wirings PL**41** and PL**45**, and the polysilicon wirings PL**42** and PL**47**, are respectively disposed in a straight line, no waste region is present and a reduction in the circuit area increases the degree of integration. This corresponds to the fourth effect of the first preferred embodiment.

By arranging such that each of inverters I**1** and I**2** of a CMOS structure is made up of a combination of a NMOS transistor and a PMOS transistor, the memory cell can be realized by at least sufficient circuit configuration as a CMOS structure. This corresponds to the sixth effect of the first preferred embodiment.

In addition, with the arrangement that the storage terminal Na is made up of the aluminum wiring AL**17**, shared contacts SC and polysilicon wiring PL**42**, and the storage terminal Nb is made up of the aluminum wiring AL**18**, shared contacts SC and polysilicon wiring PL**41**, it is able to increase the degree of integration by the amount that the well forming width in the longitudinal direction viewing the drawing can be formed by a two-transistor pitch.

Eleventh Preferred Embodiment

FIGS. **32** to **34** are diagrams illustrating a memory cell structure of a SRAM according to an eleventh preferred embodiment of the invention. FIG. **32** is an explanatory diagram viewed from above the layout configuration in all layers. FIG. **33** is an explanatory diagram viewed from above mainly the layout configuration beneath a first aluminum wiring layer in FIG. **32**. FIG. **34** is an explanatory diagram viewed from above the layout configuration over a second aluminum wiring layer in FIG. **32**. Some reference numerals used in FIG. **33** or **34** are omitted in FIG. **32**.

An equivalent circuit of the SRAM memory cell having the layout configuration of the eleventh preferred embodiment is similar to that of FIG. **4** in the first preferred embodiment.

Referring to FIGS. **32** to **34**, description will proceed to the memory cell structure of the eleventh preferred embodiment.

In an N well region NW, a PMOS transistor P**1** is made up of P^+ diffusion regions FL**110**, FL**111** and a polysilicon wiring PL**51**, and a PMOS transistor P**2** is made up of P^+ diffusion regions FL**120**, FL**121** and a polysilicon wiring PL**52**.

In a P well region PW**0**, a NMOS transistor N**1** is made up of N^+ diffusion regions FL**210** (FL**210**A, FL**210**B), FL**211** and the polysilicon wiring PL**51**, and a NMOS transistor N**4** is made up of N^+ diffusion regions FL**240**, FL**241** and a polysilicon wiring PL**54**. The polysilicon wiring PL**51** extends from the N well region NW to the P well region PW**0**, so as to be used as a gate common to the NMOS transistor N**1** and PMOS transistor P**1**.

In a P well region PW**1**, a NMOS transistor N**2** is made up of N^+ diffusion regions FL**220** (FL**220**A, FL**220**B), FL**221** and the polysilicon wiring PL**52**, and a NMOS transistor N**3** is made up of N^+ diffusion regions FL**230**, FL**231** and a polysilicon wiring PL**53**. The polysilicon wiring PL**52** extends from the N well region NW to the P well region PW**1**, so as to be used as a gate common to the NMOS transistor N**2** and PMOS transistor P**2**. The foregoing diffusion regions are obtainable by implanting and diffusing impurity.

A ground wiring LG**1** over the diffusion region FL**210**A and FL**210**B is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**210**A and FL**210**B, respectively. A bit line BLB**1** over the diffusion region FL**241** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**241**.

An aluminum wiring AL**17**, which is a first layer aluminum wiring extending over the diffusion region FL**211** and the diffusion region FL**111**, is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**211**.

The aluminum wiring AL**17** is also electrically connected to the polysilicon wiring PL**52**. The polysilicon wiring PL**52** is electrically connected through a shared contact SC to the diffusion regions FL**111** and FL**231**, respectively.

The aluminum wiring AL**17** can be electrically connected with low impedance. The aluminum wiring AL**17**, two shared contacts SC and polysilicon wiring PL**52** correspond to a storage terminal Na.

The polysilicon wiring PL**54** is electrically connected through a gate contact hole GC to a word line WL**1**.

A power supply wiring LV**1** over the diffusion region FL**110** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**110**. A power supply wiring LV**1** over the diffusion region FL**121** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**121**.

A ground wiring LG**1** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**221**. A bit line BLA**1** over the diffusion region FL**230** is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**230**.

An aluminum wiring AL**18**, which is a first layer aluminum wiring extending over the diffusion region FL**220** and the diffusion region FL**120**, is electrically connected through a diffusion contact hole **1**C to the diffusion region FL**220**.

The aluminum wiring AL**18** is also electrically connected to the polysilicon wiring PL**51**. The polysilicon wiring PL**51** is electrically connected through a shared contact SC to the diffusion regions FL**120** and FL**240**, respectively.

The aluminum wiring AL**18** can be electrically connected with low impedance. The aluminum wiring AL**18**, two shared contacts SC and polysilicon wiring PL**51** correspond to a storage terminal Nb.

A word line WL**1** over the polysilicon wiring PL**53** is electrically connected through a gate contact hole GC to the polysilicon wiring PL**53**.

A word line WL**1** is electrically connected through a via hole **1**T to a word line WL**2**, and the word line WL**2** is electrically connected through a via hole **2**T to a word line WL**3**. The word line WL**3** is disposed across the P well regions PW**0**, PW**1** and the N well region NW.

A bit line BLA**2** is electrically connected through a via hole **1**T to a bit line BLA**1**. A bit line BLB**2** is electrically connected through a via hole **1**T to a bit line BLB**1**.

A power supply wiring LV**2** is electrically connected through a via hole **1**T to a power supply wiring LV**1**. A ground wiring LG**1** is electrically connected through a via hole **1**T to a ground wiring LG**2**.

The bit lines BLA**2**, BLB**2**, ground wiring LG**2** and power supply wiring LV**2** are disposed parallel with each other in the longitudinal direction viewing the drawing.

The bit lines BLA**2** and ground wiring LG**2** are disposed over the P well region PW**1**. The bit lines BLB**2** and ground wiring LG**2** are disposed over the P well region PW**0**. The power supply wiring LV**2** is disposed over the N well region NW.

Thus, in the memory cell structure of the SRAM of the eleventh preferred embodiment, with the N well region NW interposed between the P well regions PW**0** and PW**1**, the NMOS transistors N**1** and N**4** are disposed in the P well

region PW0, and the NMOS transistors N2 and N3 are disposed in the P well region PW1. This enables to increase resistance to soft error, which is the first effect of the first preferred embodiment.

By separately forming the P well regions PW0 and PW1 in a direction vertical to the direction of formation of the bit lines BLA and BLB, it is able to maintain a good access time, which is the second effect of the first preferred embodiment.

Further, in the eleventh preferred embodiment, as in the first preferred embodiment, the NMOS transistors N1 and N2, and the NMOS transistors N3 and N4, are respectively arranged so as to be point symmetry with respect to the central part of the memory cell. It is therefore able to increase the degree of integration when a plurality of the memory cells of the eleventh preferred embodiment are disposed adjacent each other. This corresponds to the third effect of the first preferred embodiment.

The formation of the polysilicon wirings PL51 to PL54 in approximately the same direction (the lateral direction viewing the drawing) facilitates the control of the gate dimension. Further, because the polysilicon wirings PL51 and PL53, and the polysilicon wirings PL52 and PL54, are respectively disposed in a straight line, no waste region is present and a reduction in the circuit area increases the degree of integration. This corresponds to the fourth effect of the first preferred embodiment.

By separately forming a region serving as a drain in the NMOS transistors N1 to N4, resistance to soft error can be maintained at a high level. This corresponds to the fifth effect of the first preferred embodiment.

With the arrangement such that each of inverters I1 and I2 of a CMOS structure is made up of a combination of a NMOS transistor and a PMOS transistor, the memory cell can be realized by at least sufficient circuit configuration as a CMOS structure. This corresponds to the sixth effect of the first preferred embodiment.

In addition, with the arrangement that the storage terminal Na is made up of the aluminum wiring AL17, shared contacts SC and polysilicon wiring PL52, and the storage terminal Nb is made up of the aluminum wiring AL18, shared contacts SC and polysilicon wiring PL51, it is able to increase the degree of integration by the amount that the well forming width in the longitudinal direction viewing the drawing can be formed by a two-transistor pitch.

Twelfth Preferred Embodiment

FIGS. 35 and 36 are diagrams illustrating a memory cell structure of a SRAM according to a twelfth preferred embodiment of the invention. FIG. 35 is an explanatory diagram viewed from above the layout configuration in all layers. FIG. 36 is an explanatory diagram viewed from above mainly the layout configuration over a second aluminum wiring layer in FIG. 35. An explanatory diagram viewed from above the layout configuration beneath a first aluminum wiring layer in FIG. 35 is similar to that of FIG. 33 described in the eleventh preferred embodiment, except that the word line WL2 is divided into word lines WLA2 and WLB2. Some reference numerals used in FIG. 36 or 33 are omitted in FIG. 35. An equivalent circuit of the SRAM memory cell having the layout configuration of the twelfth preferred embodiment is similar to that of FIG. 15 in the fifth preferred embodiment.

Referring to FIGS. 35, 36 and 33, description will proceed to the memory cell structure of the twelfth preferred embodiment.

A polysilicon wiring PL53 is electrically connected through a gate contact hole GC to a word line WLA1 (corresponding to the word line WL1 at the right end in FIG. 33). The word line WLA1 is electrically connected through a via hole 1T to the word line WLA2. The word line WLA2 is electrically connected through a via hole 2T to a word line WLA3. The word line WLA of FIG. 15 is made up of these word lines WLA1 to WLA3.

Likewise, a polysilicon wiring PL54 is electrically connected through a gate contact hole GC to a word line WLB1 (corresponding to the word line WL1 at the left end in FIG. 33). The word line WLB1 is electrically connected through a via hole 1T to a word line WLB2. The word line WLB2 is electrically connected through a via hole 2T to a word line WLB3. The word line WLB of FIG. 15 is made up of these word lines WLB1 to WLB3.

The word lines WLA3 and WLB3 are disposed parallel with each other, across P well regions PW0, PW1 and an N well region NW. Otherwise, the layout configuration is similar to that of the eleventh preferred embodiment, and the description thereof is thus omitted.

The twelfth preferred embodiment having the foregoing memory cell structure produces the effects of the eleventh preferred embodiment, and also realizes a memory cell structure usable in FIFO memory, as in the fifth preferred embodiment.

Other Embodiments

If every conductivity type is reversed in the foregoing first to twelfth preferred embodiments, the same effects are obtainable. Further, these embodiments are applicable with the same effects to field effect transistors such as MIS transistors, without limiting to MOS transistors.

While the invention has been shown and described in detail, the foregoing description is in all aspects illustrative and not restrictive. It is therefore understood that numerous modifications and variations can be devised without departing from the scope of the invention.

What is claimed is:

[1. A semiconductor memory comprising:
- a memory cell having first and second storage terminals storing information of logic levels complementary to each other;
- a power supply wiring supplying a predetermined power supply voltage to said memory cell;
- first and second pairs of bit lines each electrically connected to said first and second storage terminals of said memory cell, when selected; and
- first and second word lines connected to said memory cell, said first pair of bit lines connected to said memory cell and at least reading out data stored at said first and second storage terminals from said memory cell in response to a signal on said first word line, and said second pair of bit lines connected to said memory cell and at least reading out data stored at said first and second storage terminals from said memory cell in response to a signal on said second word line, wherein
  - said first and second pairs of bit lines and said power supply wiring are provided in parallel to each other, with said power supply wiring interposed between said first and second pairs of bit lines.]

[2. The semiconductor memory according to claim 1, further comprising:
- first and second ground wirings each supplying a predetermined ground potential to said memory cell, wherein
  - said first pair of bit lines and said first ground wiring are provided in parallel to each other, with said first ground wiring interposed between said first pair of bit lines, and

said second pair of bit lines and said second ground wiring are provided in parallel to each other, with said second ground wiring interposed between said second pair of bit lines.]

[3. The semiconductor memory according to claim **1**, wherein

said memory cell is formed on first and second P wells and an N well interposed between said first and second P wells in a first direction, and said power supply wiring extending along a second direction vertical to said first direction is formed on said N well.]

4. A semiconductor device having a two-port type static random access memory, one memory cell of which includes first and second inverters, the first inverter comprises first and third transistors and the second inverter comprises second and fourth transistors, comprising:

first and second well regions of a first conductivity type;

a third well region of a second conductivity type disposed between the first and second well regions in a plane view;

a first pair of impurity regions of the first conductivity type provided in the third well region, functioning as two electrodes of the first transistor;

a second pair of impurity regions of the first conductivity type provided in the third well region, functioning as two electrodes of the second transistor;

a third pair of impurity regions of the second conductivity type provided in the first well region, functioning as two electrodes of the third transistor;

a fourth pair of impurity regions of the second conductivity type provided in the first well region, functioning as two electrodes of the fourth transistor;

a fifth pair of impurity regions of the second conductivity type provided in the first well region, functioning as two electrodes of a fifth transistor;

a sixth pair of impurity regions of the second conductivity type provided in the second well region, functioning as two electrodes of a sixth transistor;

a seventh pair of impurity regions of the second conductivity type provided in the second well region, functioning as two electrodes of a seventh transistor;

an eighth pair of impurity regions of the second conductivity type provided in the second well region, functioning as two electrodes of an eighth transistor;

a first conductive layer provided over the first and third well regions, functioning as a gate electrode common to the first and third transistors;

a second conductive layer provided over the second and third well regions, functioning as a gate electrode common to the second and fourth transistors;

a third conductive layer provided over the first well region, functioning as a gate electrode common to the fifth and sixth transistors;

a fourth conductive layer provided over the second well region, functioning as a gate electrode common to the seventh and eighth transistors;

a fifth conductive layer electrically connected to the second conductive layer, one of the first pair of impurity regions, one of the third pair of impurity regions, one of the fifth pair of impurity regions and one of the eighth pair of impurity regions, and functioning as one storage terminal of the one memory cell;

a sixth conductive layer electrically connected to the first conductive layer, one of the second pair of impurity regions, one of the fourth pair of impurity regions, one of the seventh pair of impurity regions and one of the sixth pair of impurity regions, and functioning as another storage terminal of the one memory cell;

a first word line electrically connected to the third conductive layer;

a second word line electrically connected to the fourth conductive layer;

a first bit line electrically connected to the other of the fifth pair of impurity regions;

a second bit line electrically connected to the other of the sixth pair of impurity regions;

a third bit line electrically connected to the other of the seventh pair of impurity regions; and

a fourth bit line electrically connected to the other of the eighth pair of impurity regions.

5. The semiconductor device according to claim 4, wherein

a first supply voltage is supplied to the other of the first pair of impurity regions and the other of the second pair of impurity regions, and

a second supply voltage is supplied to the other of the third pair of impurity regions and the other of the fourth pair of impurity regions.

6. The semiconductor device according to claim 4, wherein

the ones of the third and fifth pairs of impurity regions are a common impurity region, and

the ones of the fourth and seventh pairs of impurity regions are a common impurity region.

7. The semiconductor device according to claim 4, wherein

the one of the first pair of impurity regions is electrically connected to the fifth conductive layer via a first contact hole disposed between overlapped portions of the fifth conductive layer and the one of the first pair of impurity regions in the plane view,

the one of the third pair of impurity regions is electrically connected to the fifth conductive layer via a second contact hole disposed between overlapped portions of the fifth conductive layer and the one of the third pair of impurity regions in the plane view,

the one of the eighth pair of impurity regions is electrically connected to the fifth conductive layer via a third contact hole disposed between overlapped portions of the fifth conductive layer and the one of the eighth impurity regions in the plane view,

the one of the second pair of impurity regions is electrically connected to the sixth conductive layer via a fourth contact hole disposed between overlapped portions of the sixth conductive layer and the one of the second pair of impurity regions in the plane view,

the one of the fourth pair of impurity regions is electrically connected to the sixth conductive layer via a fifth contact hole disposed between overlapped portions of the sixth conductive layer and the one of the sixth pair of impurity regions in the plane view, and

the one of the sixth pair of impurity regions is electrically connected to the sixth conductive layer via a sixth contact hole disposed between overlapped portions of the sixth conductive layer and the one of the fifth pair of impurity regions in the plane view.

8. The semiconductor device according to claim 4, wherein

the second conductive layer is electrically connected to the fifth conductive layer via a seventh contact hole disposed between overlapped portions of the second and fifth conductive layers in the plane view, and

the first conductive layer is electrically connected to the sixth conductive layer via an eighth contact hole disposed between overlapped portions of the first and sixth conductive layers in the plane view.

9. The semiconductor device according to claim 4, wherein

the one of the first pair of impurity regions and the second conductive layer are electrically connected to the fifth conductive layer via a first shared contact disposed between overlapped portions of the fifth conductive layer and the one of the first pair of impurity regions in the plane view,

the one of the third pair of impurity regions is an impurity region common to the one of the fourth pair of impurity regions, and is electrically connected to the fifth conductive layer via a first contact hole disposed between overlapped portions of the fifth conductive layer and the one of the third pair of impurity regions in the plane view,

the one of the eighth pair of impurity regions is electrically connected to the second conductive layer via a second shared contact,

the one of the second pair of impurity regions and the first conductive layer are electrically connected to the sixth conductive layer via a third shared contact disposed between overlapped portions of the sixth conductive layer and the one of the second pair of impurity regions in the plane view,

the one of the fourth pair of impurity regions is an impurity region common to the one of the seventh pair of impurity regions, and is electrically connected to the sixth conductive layer via a second contact hole disposed between overlapped portions of the sixth conductive layer and the one of the sixth impurity regions in the plane view, and

the one of the sixth pair of impurity regions is electrically connected to the first conductive layer via a fourth shared contact.

10. The semiconductor memory according to claim 4, wherein the respective one electrodes in the first to fourth conductive layers are disposed separately.

11. The semiconductor memory according to claim 4, wherein

the first and third conductive layers are arranged in an approximately straight line along the direction of formation of the first word line, and

the second and fourth conductive layers are arranged in an approximately straight line along the direction of formation of the second word line.

* * * * *