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Li et al.

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(54) **BACK-TO-BACK METAL/SEMICONDUCTOR/METAL (MSM) SCHOTTKY DIODE**

(58) **Field of Classification Search**
CPC H01L 29/66143; H01L 29/872; H01L 27/2463; H01L 27/2409; H01L 27/101; G11C 13/0007

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(Continued)

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(56) **References Cited**

U.S. PATENT DOCUMENTS

4,980,546 A * 12/1990 Berger H01L 27/14609 250/208.1

5,484,686 A * 1/1996 Maeda et al. 430/270.13

(Continued)

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OTHER PUBLICATIONS

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Ex Parte Quayle Action on U.S. Appl. No. 11/893,402, dated Apr. 21, 2009.

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Primary Examiner — Leonardo Andujar

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(74) *Attorney, Agent, or Firm* — Foley & Lardner LLP

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U.S. Applications:

(60) Division of application No. 11/435,669, filed on May 17, 2006, now Pat. No. 7,446,010, which is a (Continued)

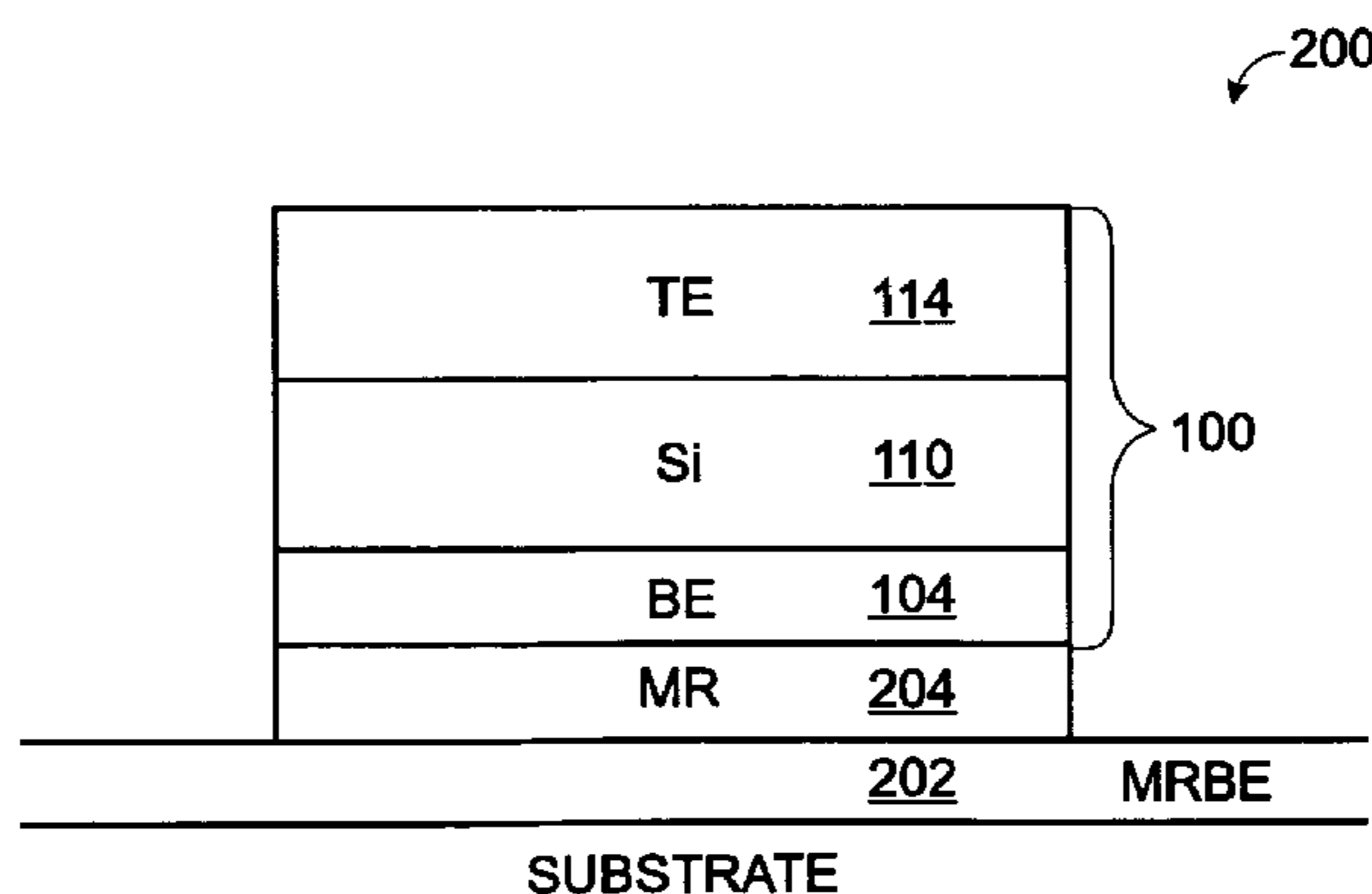
(51) **Int. Cl.**
H01L 21/20 (2006.01)
H01L 27/24 (2006.01)
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(52) **U.S. Cl.**
CPC **H01L 21/20** (2013.01); **G11C 13/0007** (2013.01); **H01L 27/2409** (2013.01);
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(57) **ABSTRACT**

A method is provided for forming a metal/semiconductor/metal (MSM) back-to-back Schottky diode from a silicon (Si) semiconductor. The method deposits a Si semiconductor layer between a bottom electrode and a top electrode, and forms a MSM diode having a threshold voltage, breakdown voltage, and on/off current ratio. The method is able to modify the threshold voltage, breakdown voltage, and on/off current ratio of the MSM diode in response to controlling the Si semiconductor layer thickness. Generally, both the threshold and breakdown voltage are increased in response to increasing the Si thickness. With respect to the on/off current ratio, there is an optimal thickness. The method is able to form an amorphous Si (a-Si) and polycrystalline Si (polySi) semiconductor layer using either chemical vapor deposition (CVD) or DC sputtering. The Si semiconductor can be doped with a Group V donor material, which decreases the threshold voltage and increases the breakdown voltage.

24 Claims, 11 Drawing Sheets



Related U.S. Application Data

continuation-in-part of application No. 11/184,660,
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(2013.01); **H01L 45/04** (2013.01); **H01L**
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H01L 45/147 (2013.01)

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See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,489,774 A * 2/1996 Akamine G01Q 60/06
250/234
5,496,759 A 3/1996 Yue et al.
5,534,711 A 7/1996 Ovshinsky et al.
5,616,947 A * 4/1997 Tamura H01L 21/28264
257/289
5,687,112 A 11/1997 Ovshinsky
5,838,608 A 11/1998 Zhu et al.
5,973,335 A * 10/1999 Shannon H01L 27/24
257/196
6,013,950 A 1/2000 Nasby
6,281,142 B1 * 8/2001 Basceri H01L 21/3105
257/103
6,331,944 B1 * 12/2001 Monsma et al. 365/171
6,532,050 B1 * 3/2003 Kim G02F 1/133514
349/106
6,534,326 B1 3/2003 Hsu et al.

6,753,561 B1 * 6/2004 Rinerson et al. 257/295
6,914,810 B2 7/2005 Hosotani
7,029,924 B2 4/2006 Hsu et al.
7,126,841 B2 10/2006 Rinerson et al.
7,149,108 B2 12/2006 Rinerson et al.
7,271,081 B2 * 9/2007 Li et al. 438/570
7,303,971 B2 * 12/2007 Hsu et al. 438/381
7,446,010 B2 * 11/2008 Li et al. 438/328
7,608,514 B2 * 10/2009 Hsu et al. 438/288
7,968,419 B2 * 6/2011 Li et al. 438/381
2002/0130312 A1 9/2002 Yu et al.
2004/0160804 A1 8/2004 Rinerson et al.
2004/0227203 A1 11/2004 Wu

OTHER PUBLICATIONS

Ex parte Quayle Action on U.S. Appl. No. 12/234,663, dated Dec.
14, 2009.
Ex Parte Quayle Action on U.S. Appl. No. 11/261,398, dated Apr.
24, 2007.
Non-Final Office Action on U.S. Appl. No. 11/184,660, dated Aug.
16, 2007.
Non-Final Office Action on U.S. Appl. No. 11/900,999, dated Jan.
12, 2009.
Non-Final Office Action on U.S. Appl. No. 11/295,778, dated Sep.
22, 2008.
Non-Final Office Action on U.S. Appl. No. 11/435,669, dated Jun.
23, 2008.
Notice of Allowance on U.S. Appl. No. 11/184,660, dated Oct. 11,
2007.
Notice of Allowance on U.S. Appl. No. 11/261,398, dated Jun. 18,
2007.
Notice of Allowance on U.S. Appl. No. 11/435,669, dated Sep. 5,
2008.
Notice of Allowance on U.S. Appl. No. 11/893,402, dated Aug. 27,
2009.
Notice of Allowance on U.S. Appl. No. 11/900,999, dated Jun. 26,
2009.
Notice of Allowance on U.S. Appl. No. 12/234,663, dated Feb. 23,
2011.

* cited by examiner

Fig. 1

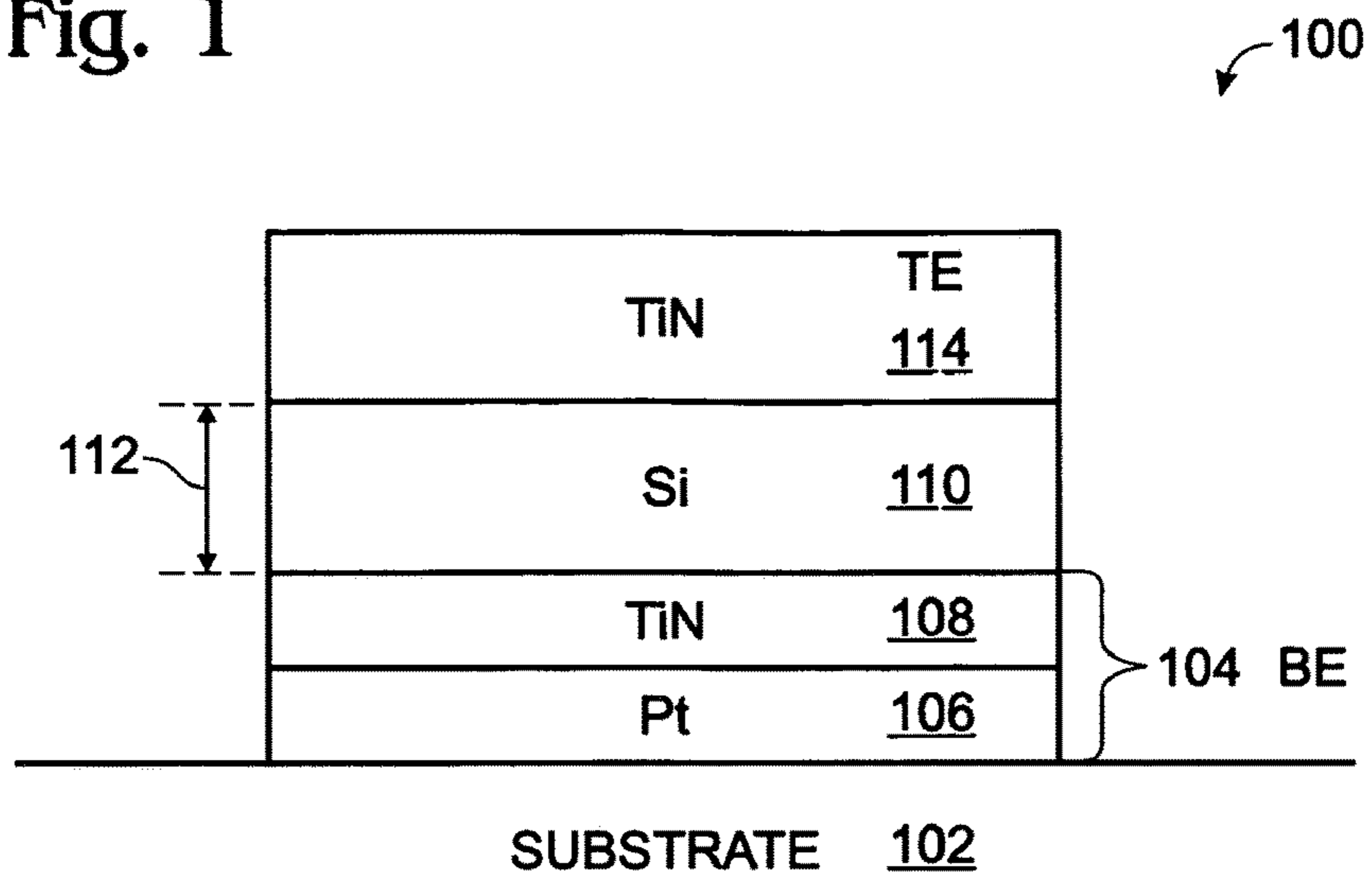


Fig. 2

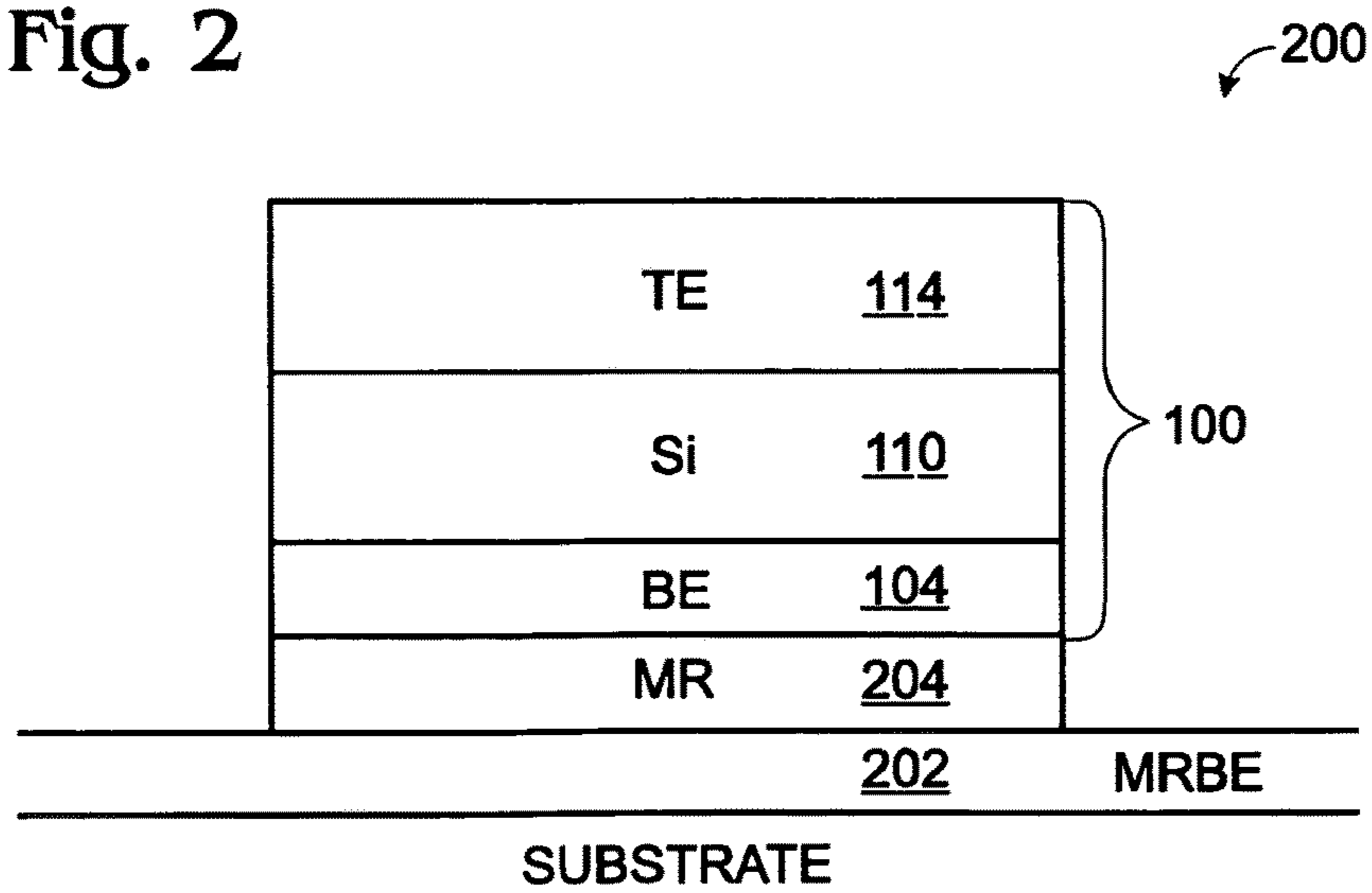


Fig. 3A

WAFER #2741, DC-SPUTTERING Si, 10nm, TiN(150nm)/
 A-Si(10nm)TiN(150nm)/Pt(150nm)/Si, BOTTOM (Pt) TO TOP (TiN)
 ELECTRODES, AREA: 100X100 μ m

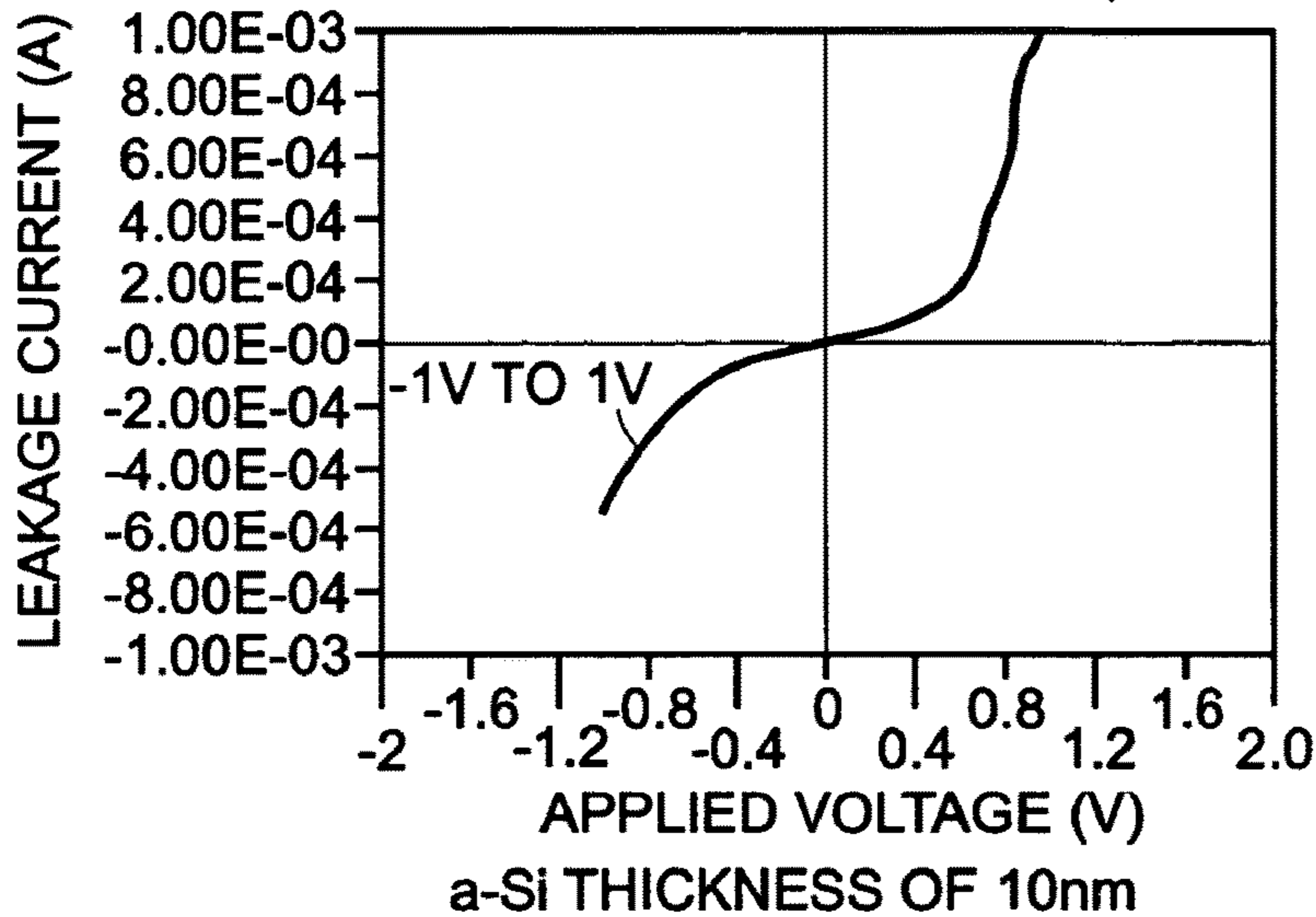


Fig. 3B

WAFER #2984, DC-SPUTTERING Si, 15nm, TiN(150nm)/
 A-Si(15nm)TiN(150nm)/Pt(150nm)/Si, BOTTOM (Pt) TO TOP (TiN)
 ELECTRODES, AREA: 100X100 μ m

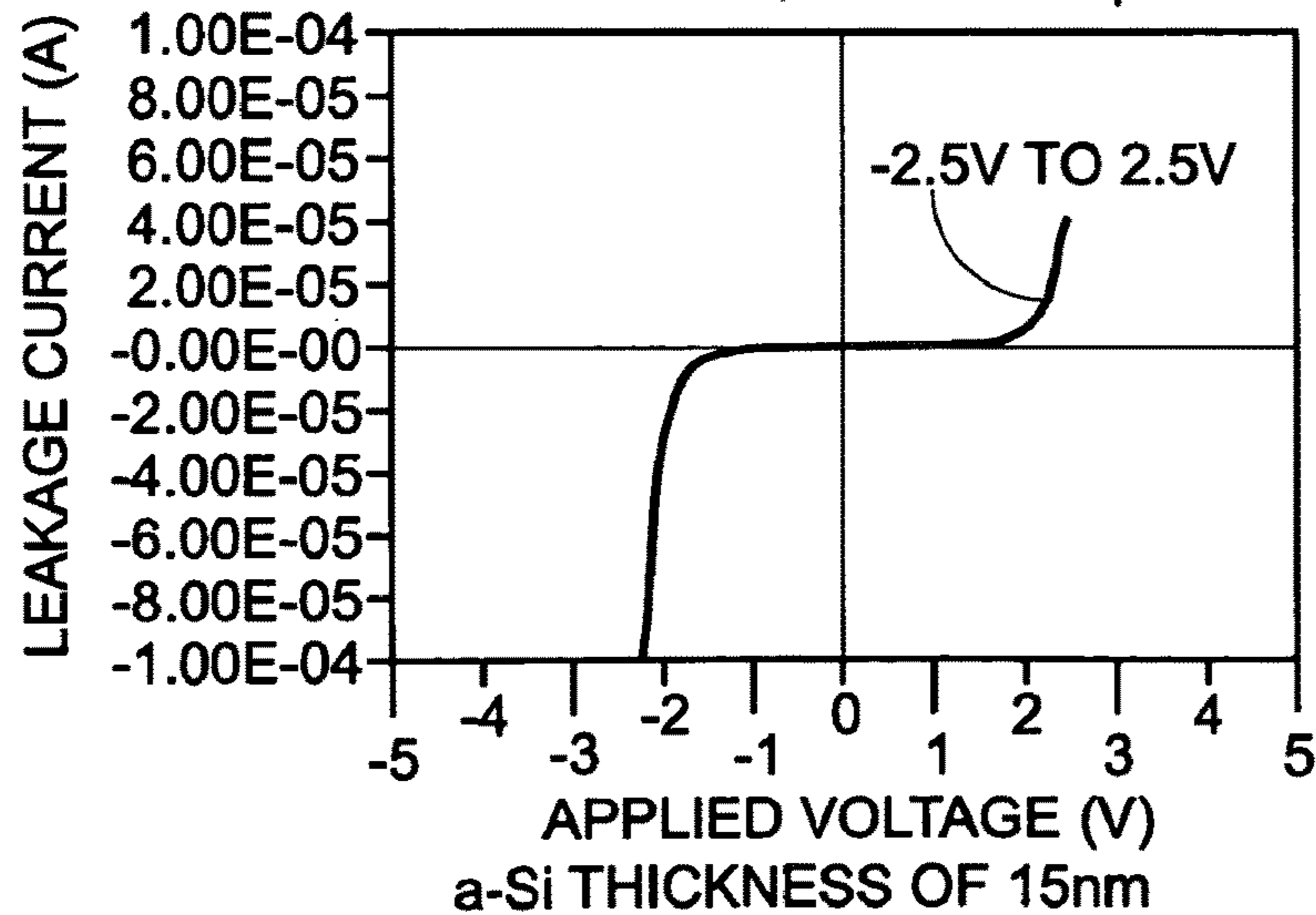
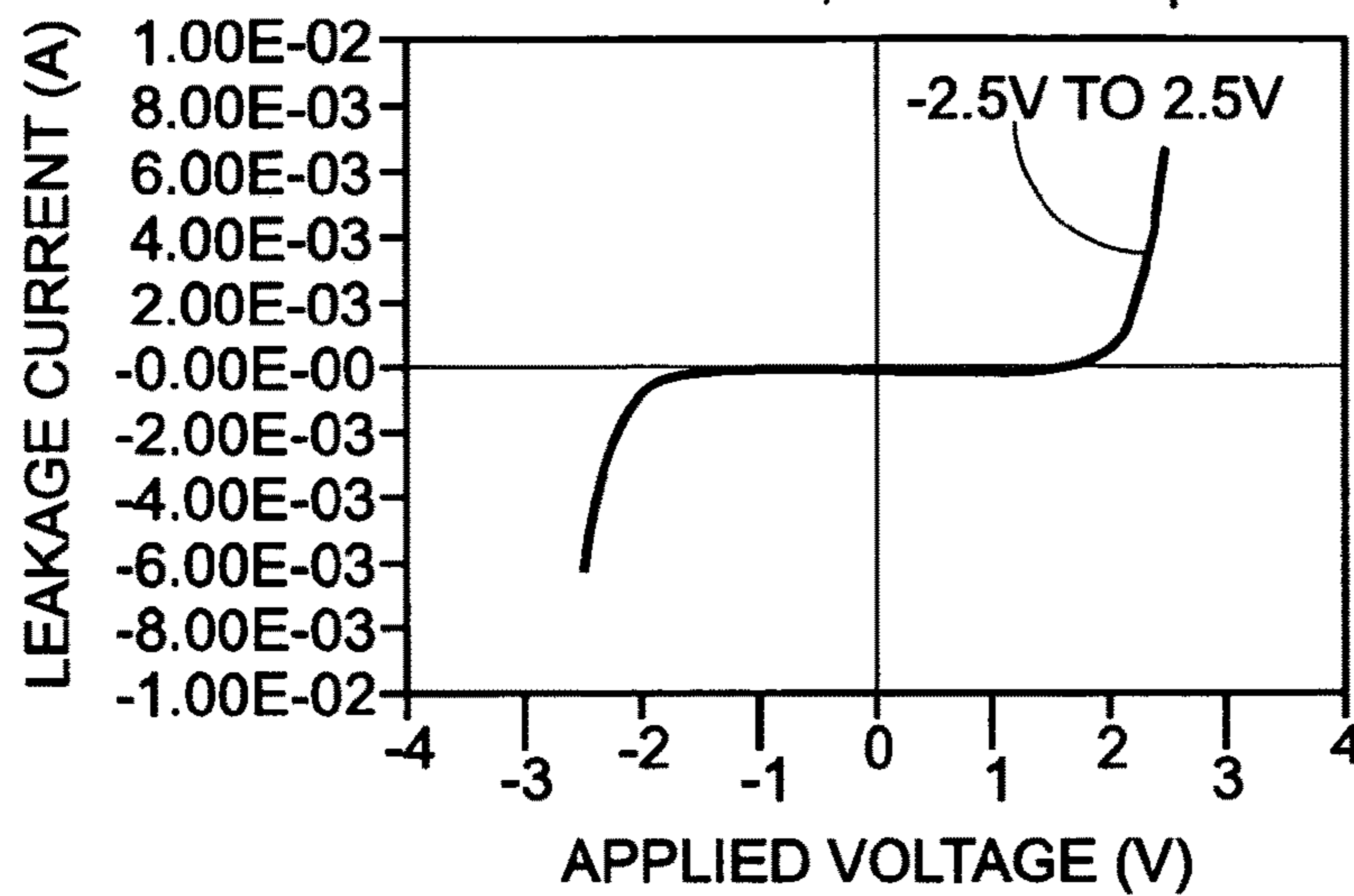


Fig. 3C

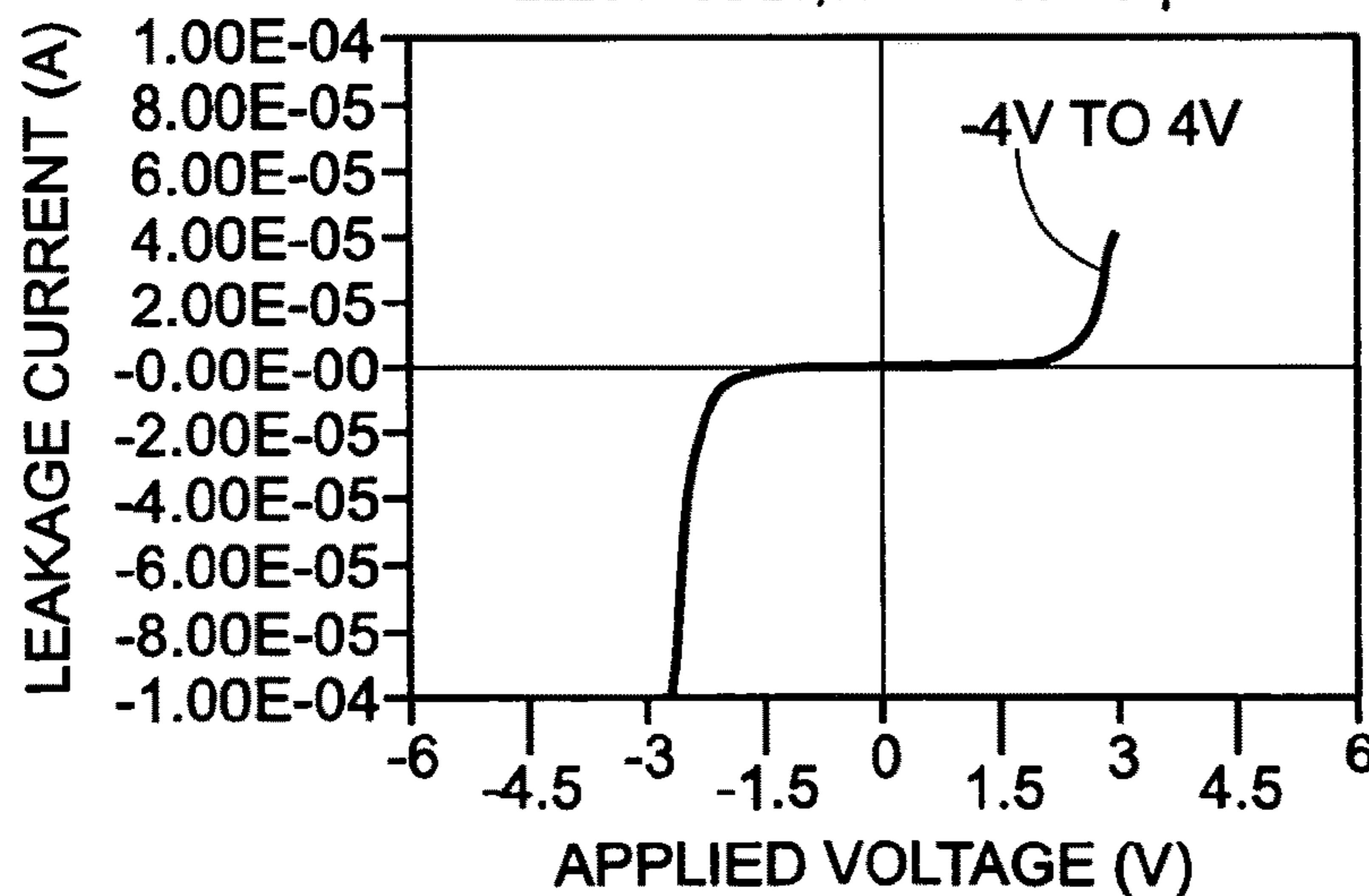
WAFER #2559, DC-SPUTTERING Si, 20nm, TiN(150nm)/
 A-Si(20nm)TiN(150nm)/Pt(150nm)/Si, BOTTOM (Pt) TO TOP (TiN)
 ELECTRODES, AREA: 100X100 μ m



a-Si THICKNESS OF 20nm

Fig. 3D

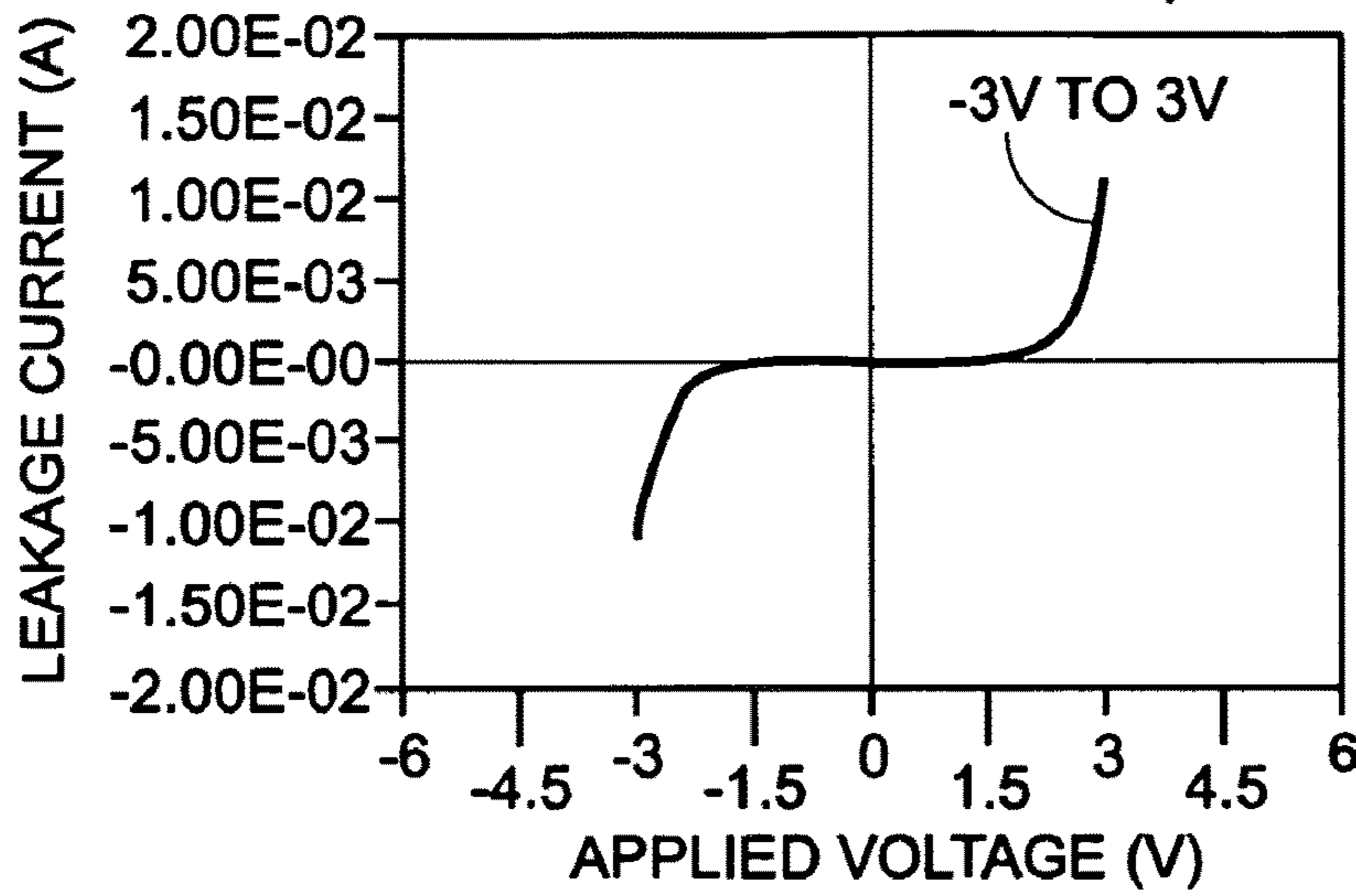
WAFER #2812, DC-SPUTTERING Si, 25nm, TiN(150nm)/
 A-Si(25nm)TiN(150nm)/Pt(150nm)/Si, BOTTOM (Pt) TO TOP (TiN)
 ELECTRODES, AREA: 100X100 μ m



a-Si THICKNESS OF 25nm

Fig. 3E

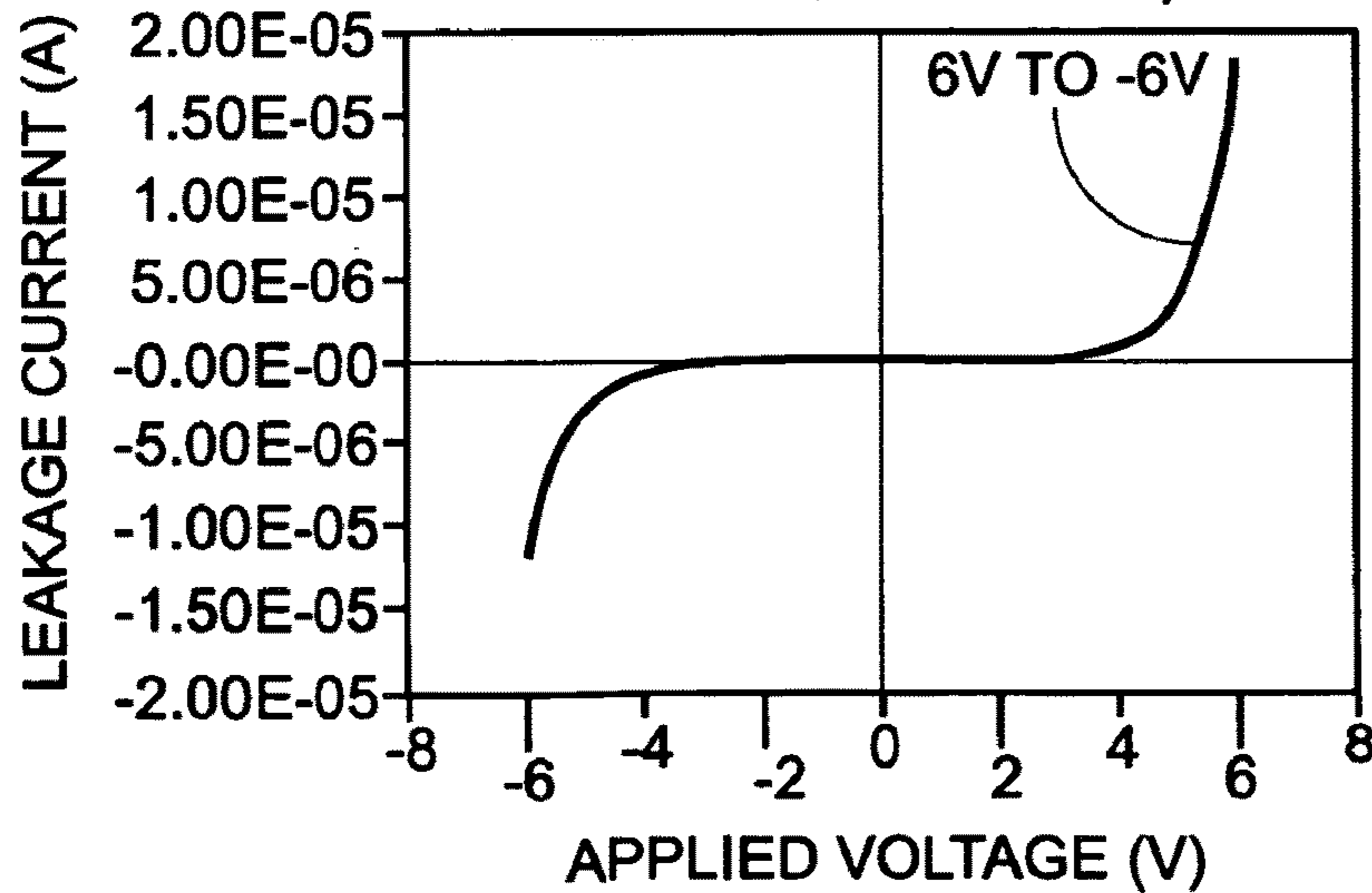
WAFER #2549, DC-SPUTTERING Si, 30nm, TiN(150nm)/
A-Si(30nm)TiN(150nm)/Pt(150nm)/Si, BOTTOM (Pt) TO TOP (TiN)
ELECTRODES, AREA: 100X100 μ m



a-Si THICKNESS OF 30nm

Fig. 3F

WAFER #2528, DC-SPUTTERING Si, 50nm, TiN(150nm)/
A-Si(50nm)TiN(150nm)/Pt(150nm)/Si, BOTTOM (Pt) TO TOP (TiN)
ELECTRODES, AREA: 100X100 μ m



a-Si THICKNESS OF 50nm

Fig. 4

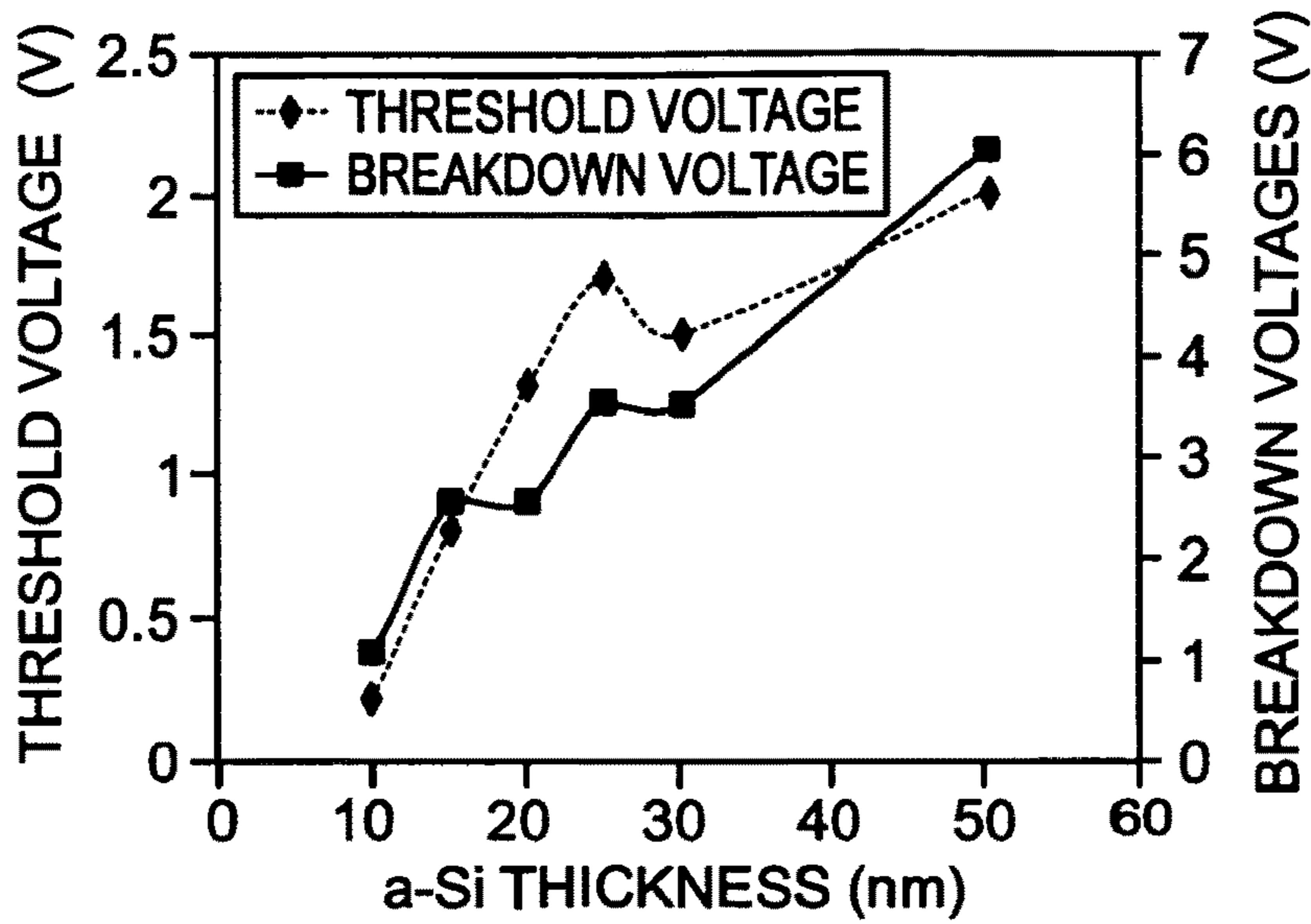


Fig. 5A

WAFER #2281, DC-SPUTTERING, AS IMPLANTATION 30keV, 1E12, 600C
FOR 10 m, TiN(150nm)/A-Si(30nm)/TiN(150nm)/Pt/Si, Pt TO TiN TOP
ELECTRODES, AREA: 100X100 μ m

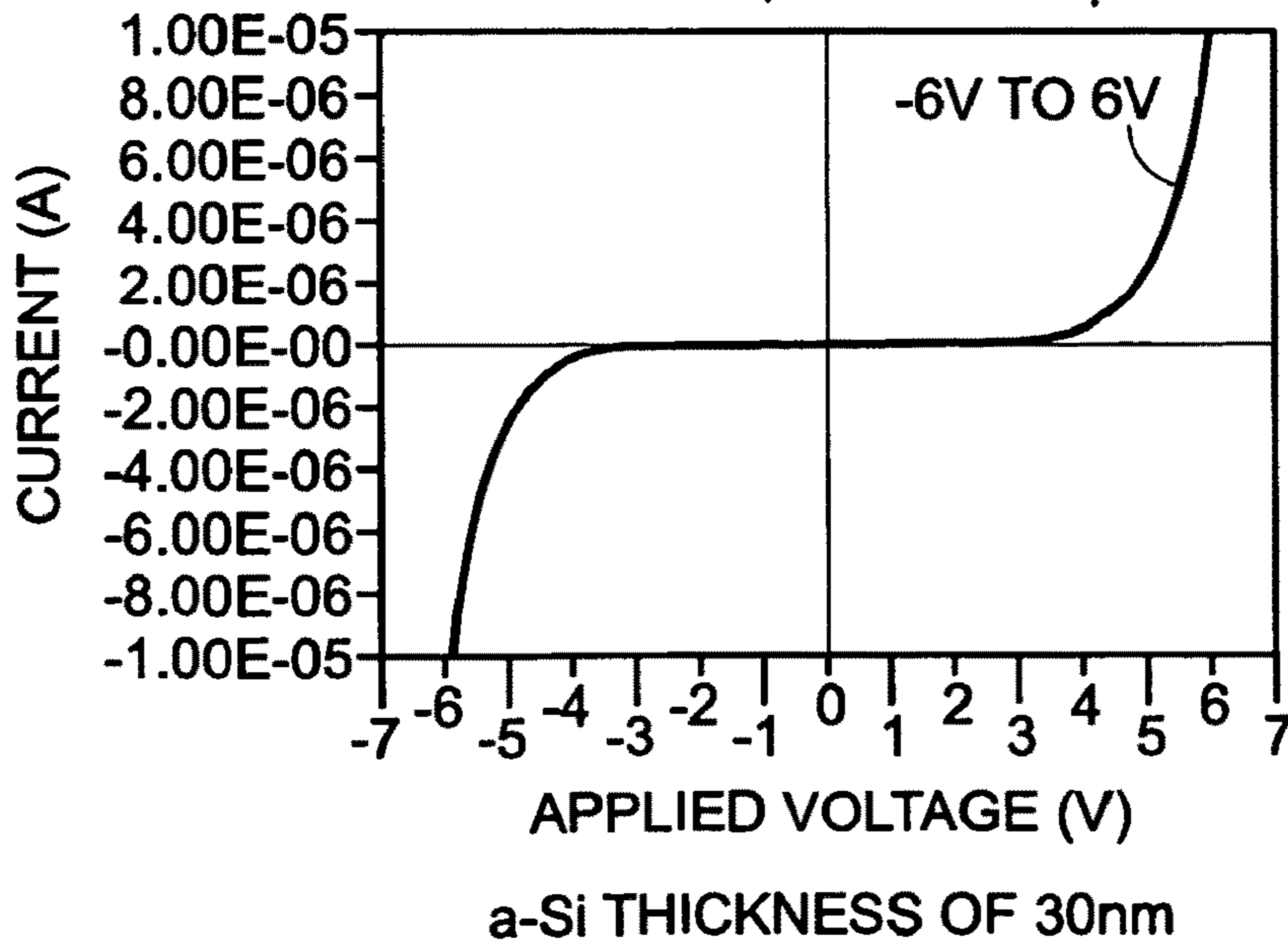
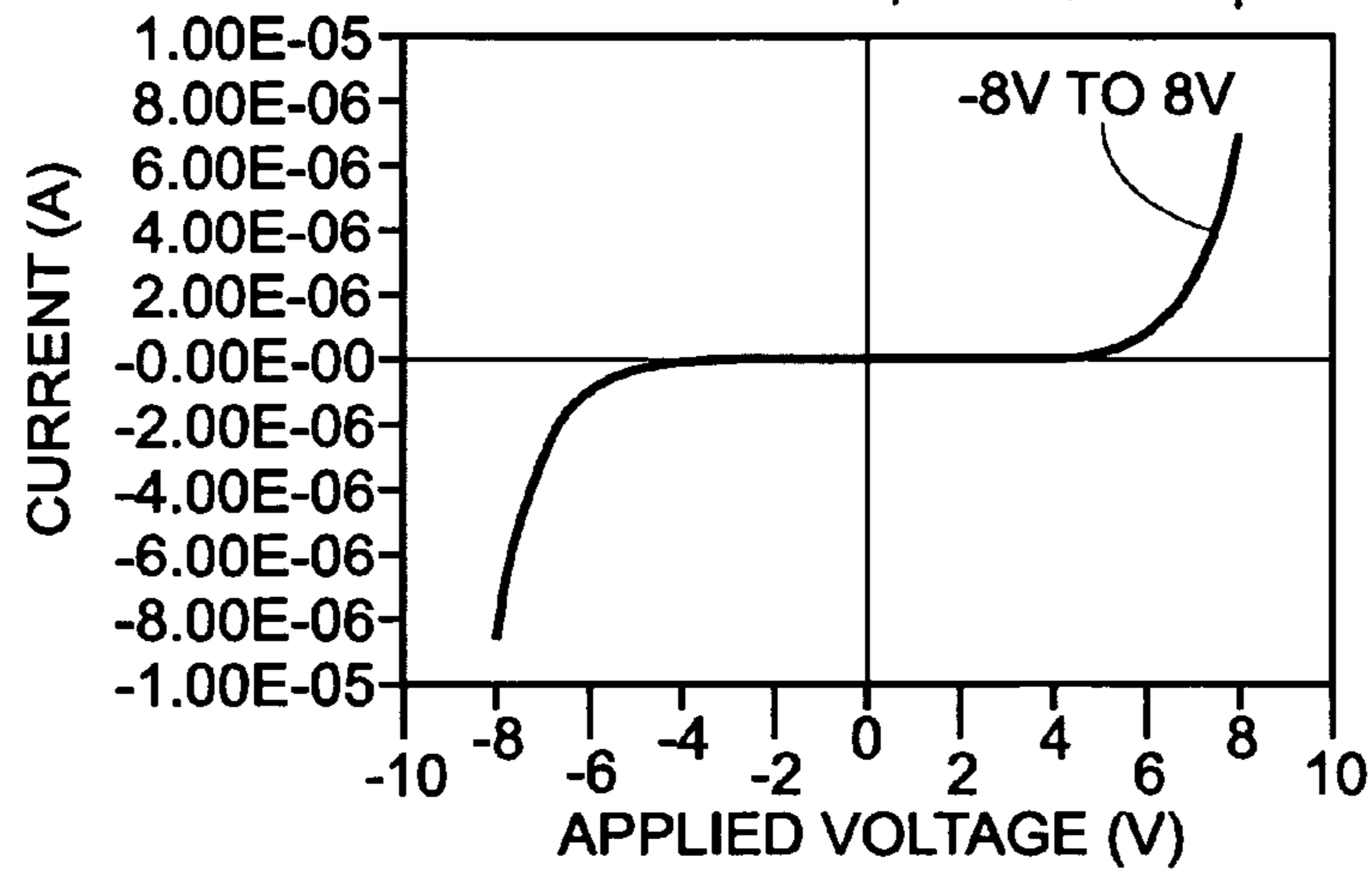


Fig. 5B

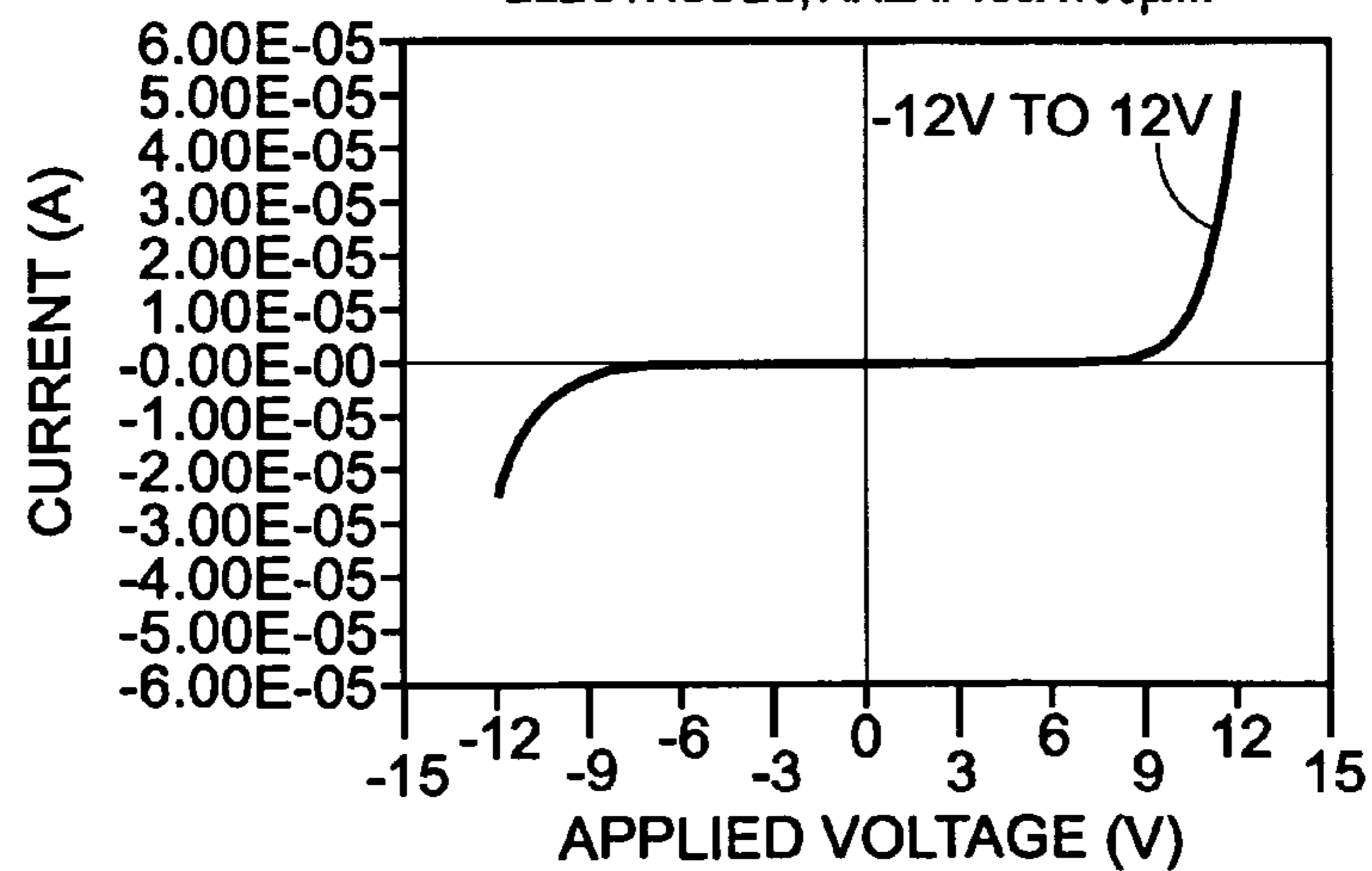
WAFER #3508, DC-SPUTTERING, AS IMPLANTATION 30keV, 1E12,
500C FOR 10 m, TiN(150nm)/A-Si(50nm)/TiN(150nm)/Pt/Si, Pt TO
TiN TOP ELECTRODES, AREA: 100X100 μ m



a-Si THICKNESS OF 50nm

Fig. 5C

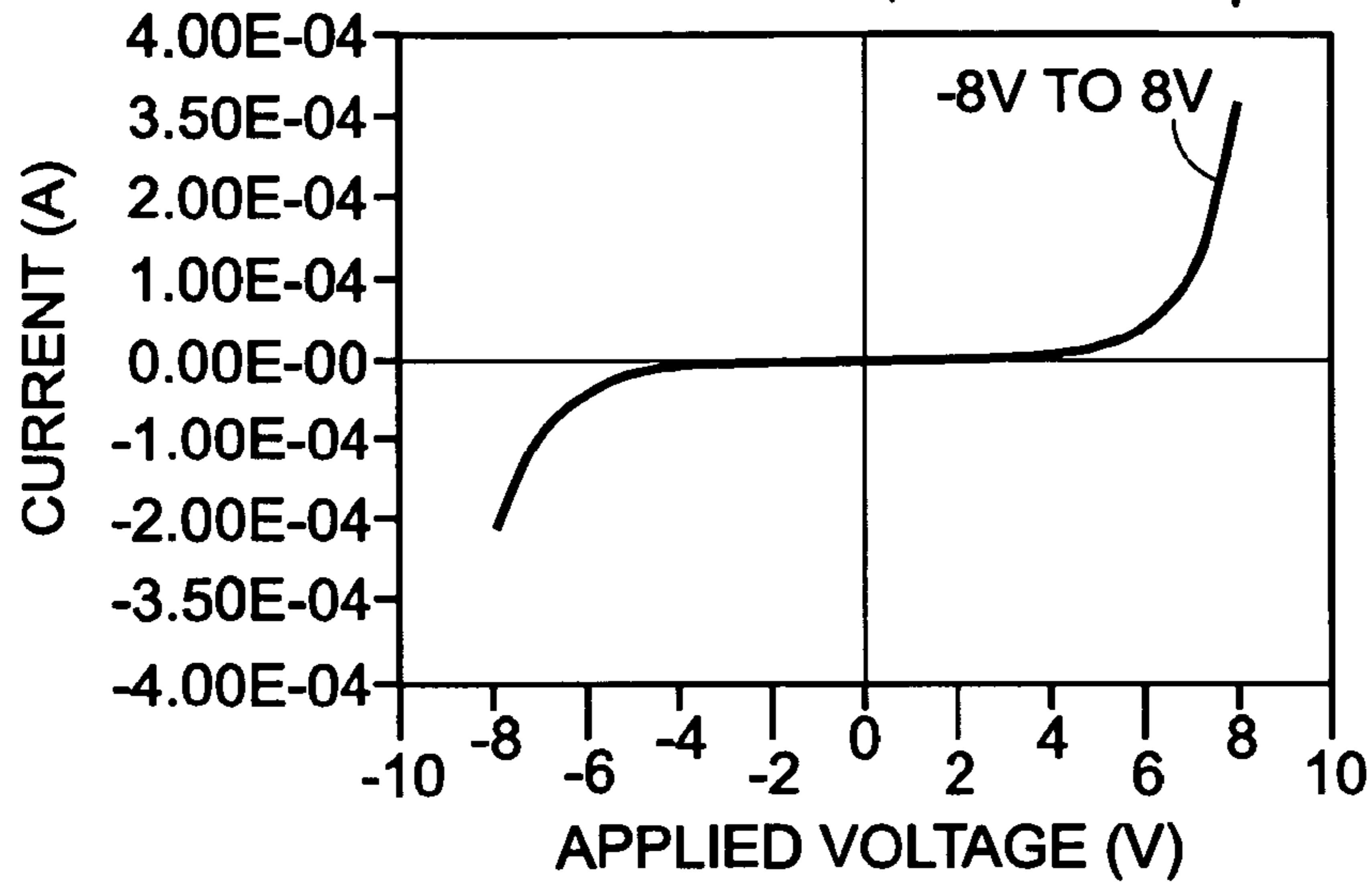
WAFER #2913, DC-SPUTTERING, AS IMPLANTATION 30keV, 1E12, 500C
FOR 10 m, TiN(150nm)/A-Si(65nm)/TiN(150nm)/Pt/Si, Pt TO TiN TOP
ELECTRODES, AREA: 100X100 μ m



a-Si THICKNESS OF 65nm

Fig. 5D

WAFER #2970, DC-SPUTTERING, AS IMPLANTATION 30keV, 1E12,
500C FOR 10 m, TiN(150nm)/A-Si(80nm)/TiN(150nm)/Pt/Si, Pt TO
TiN TOP ELECTRODES, AREA: 100X100 μ m



a-Si THICKNESS OF 80nm

Fig. 6

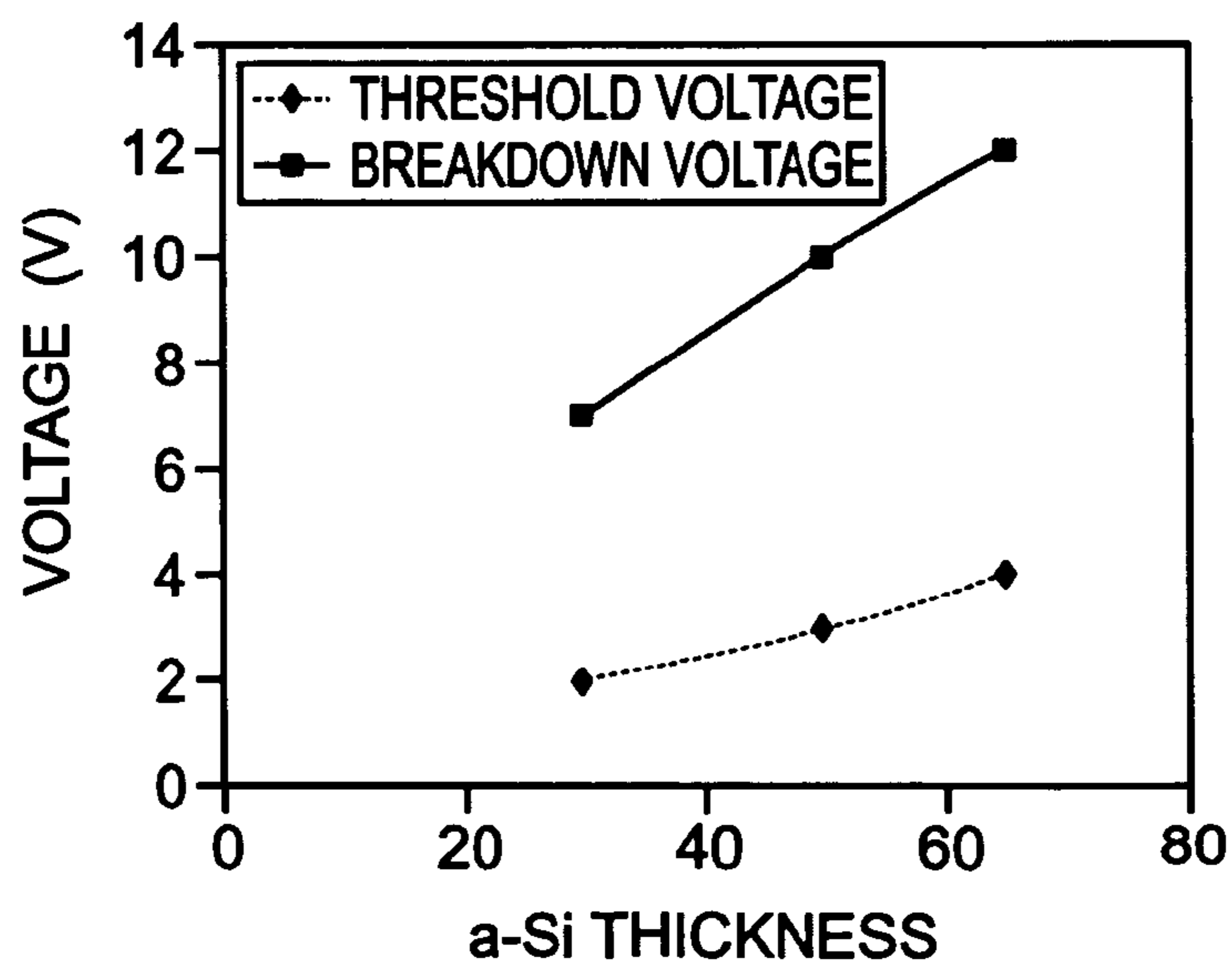
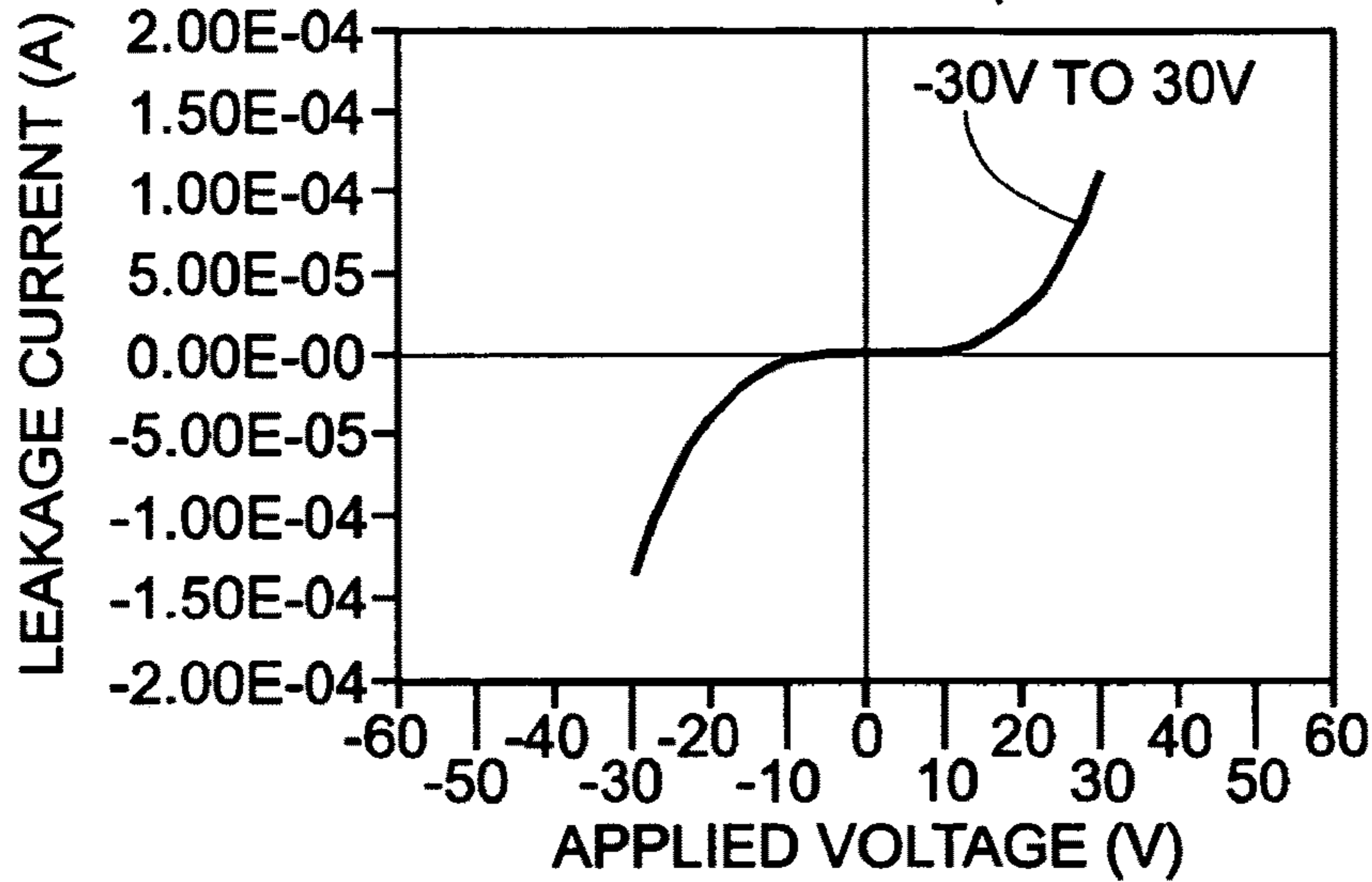


Fig. 7A

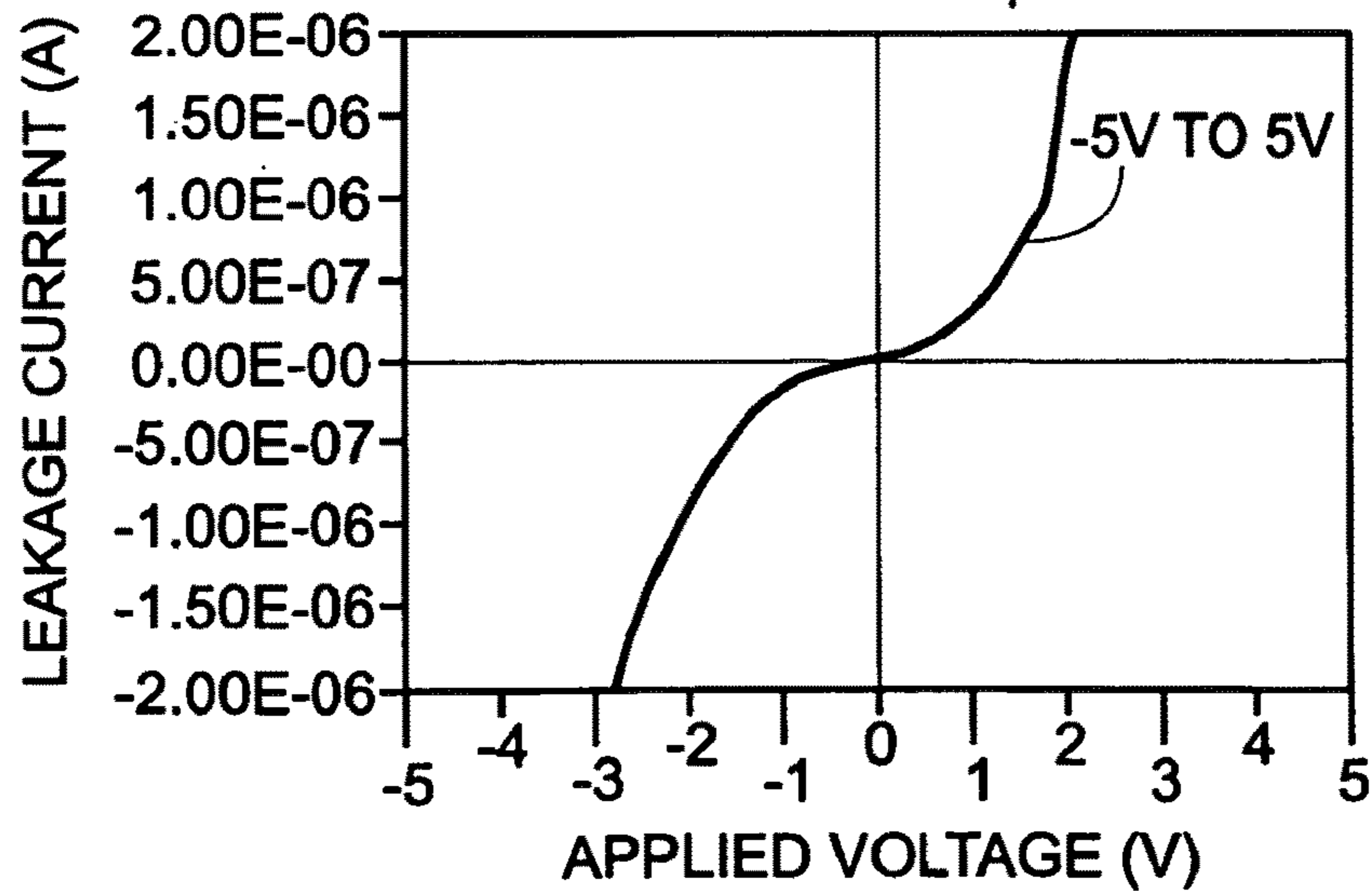
WAFER #3481, DC-SPUTTERING Si, 1.2 μ m, Pt(150nm)/
A-Si(1.2 μ m)/Pt(150nm)/Si, BOTTOM (PT) TO TOP (Pt) ELECTRODES,
AREA: 200X200 μ m



LARGE APPLIED VOLTAGE RANGE

Fig. 7B

WAFER #3481, DC-SPUTTERING Si, 1.2 μ m, Pt(150nm)/
A-Si(1.2 μ m)/Pt(150nm)/Si, BOTTOM (PT) TO TOP (Pt) ELECTRODES,
AREA: 200X200 μ m



SMALL APPLIED VOLTAGE RANGE

Fig. 8A

WAFER #3481, DC-SPUTTERING Si, 1.2 μ m, Pt(150nm)/
A-Si(1.2 μ m)/Pt(150nm)/Si, Si SUBSTRATE TO TOP (Pt) ELECTRODES,
AREA: 200X200 μ m

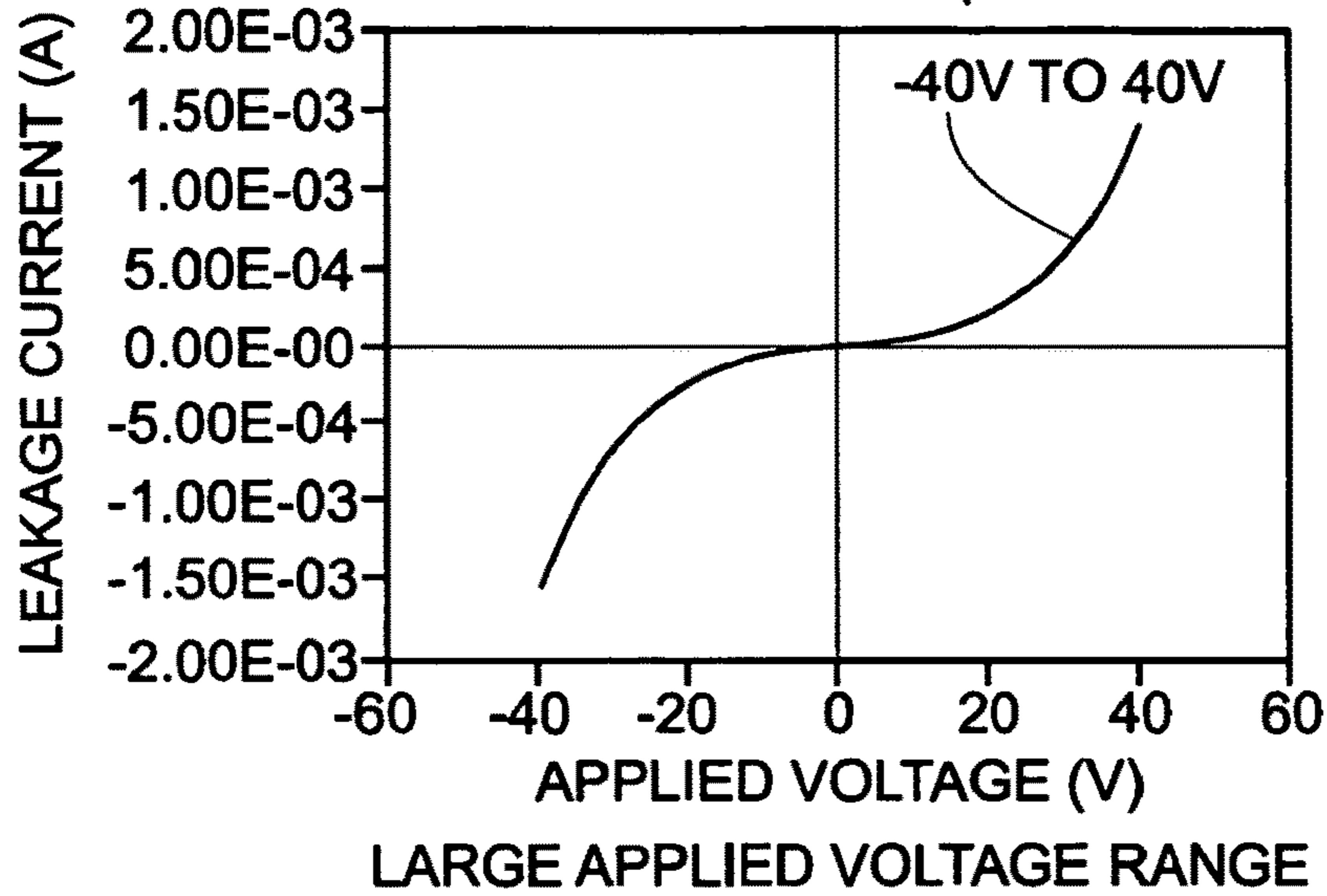


Fig. 8B

WAFER #3481, DC-SPUTTERING Si, 1.2 μ m, Pt(150nm)/
A-Si(1.2 μ m)/Pt(150nm)/Si, Si SUBSTRATE TO TOP (Pt) ELECTRODES,
AREA: 200X200 μ m

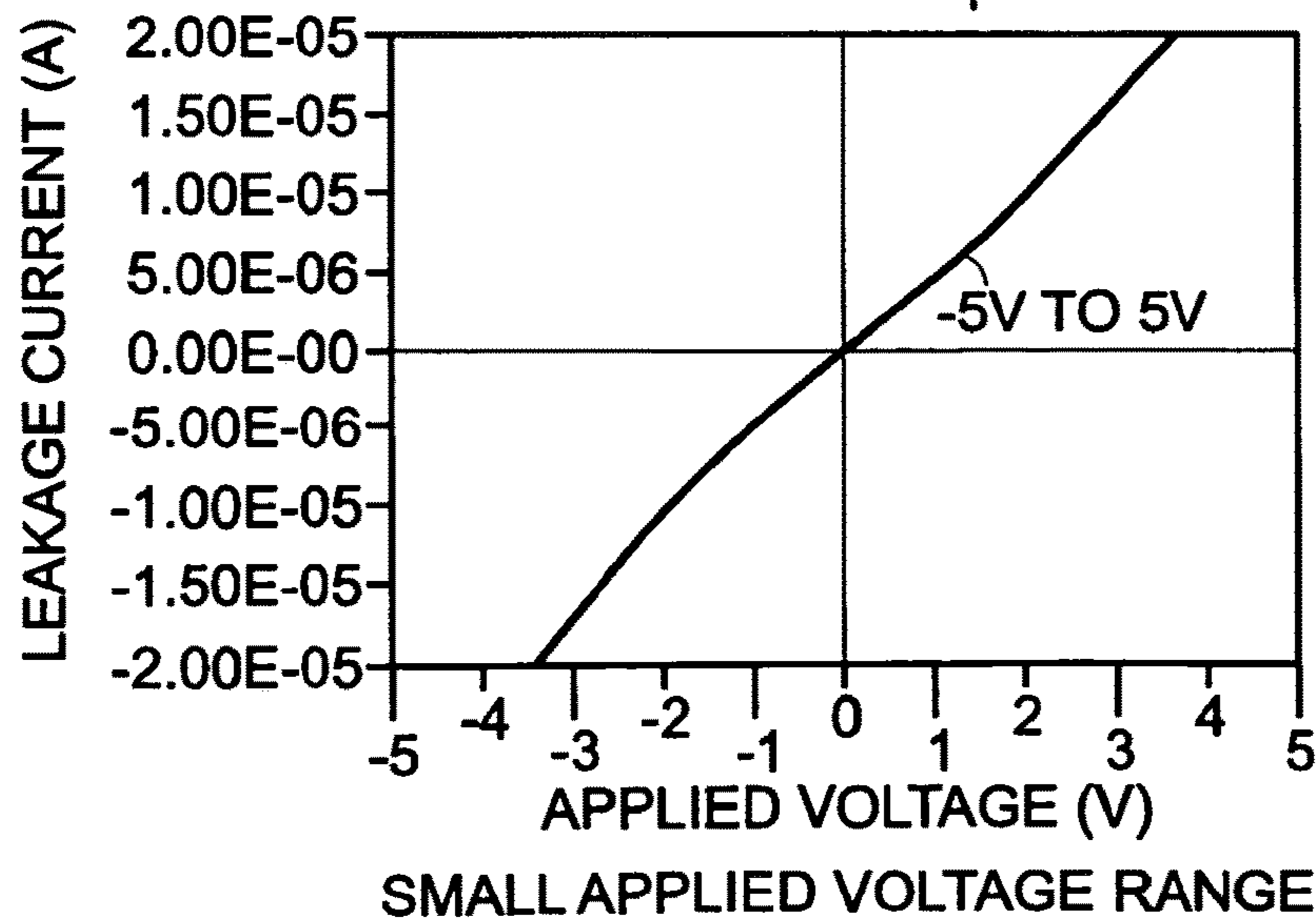


Fig. 9

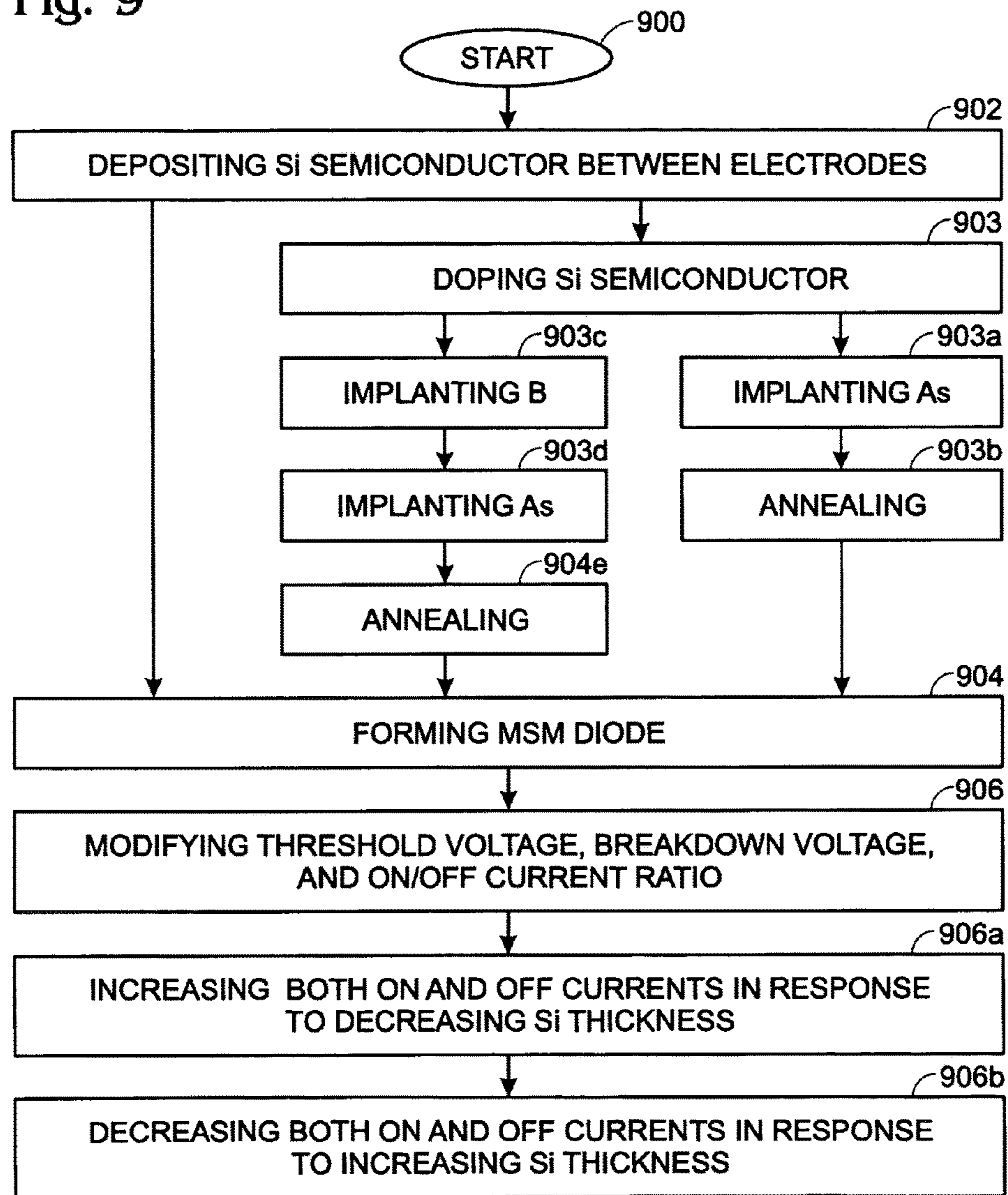
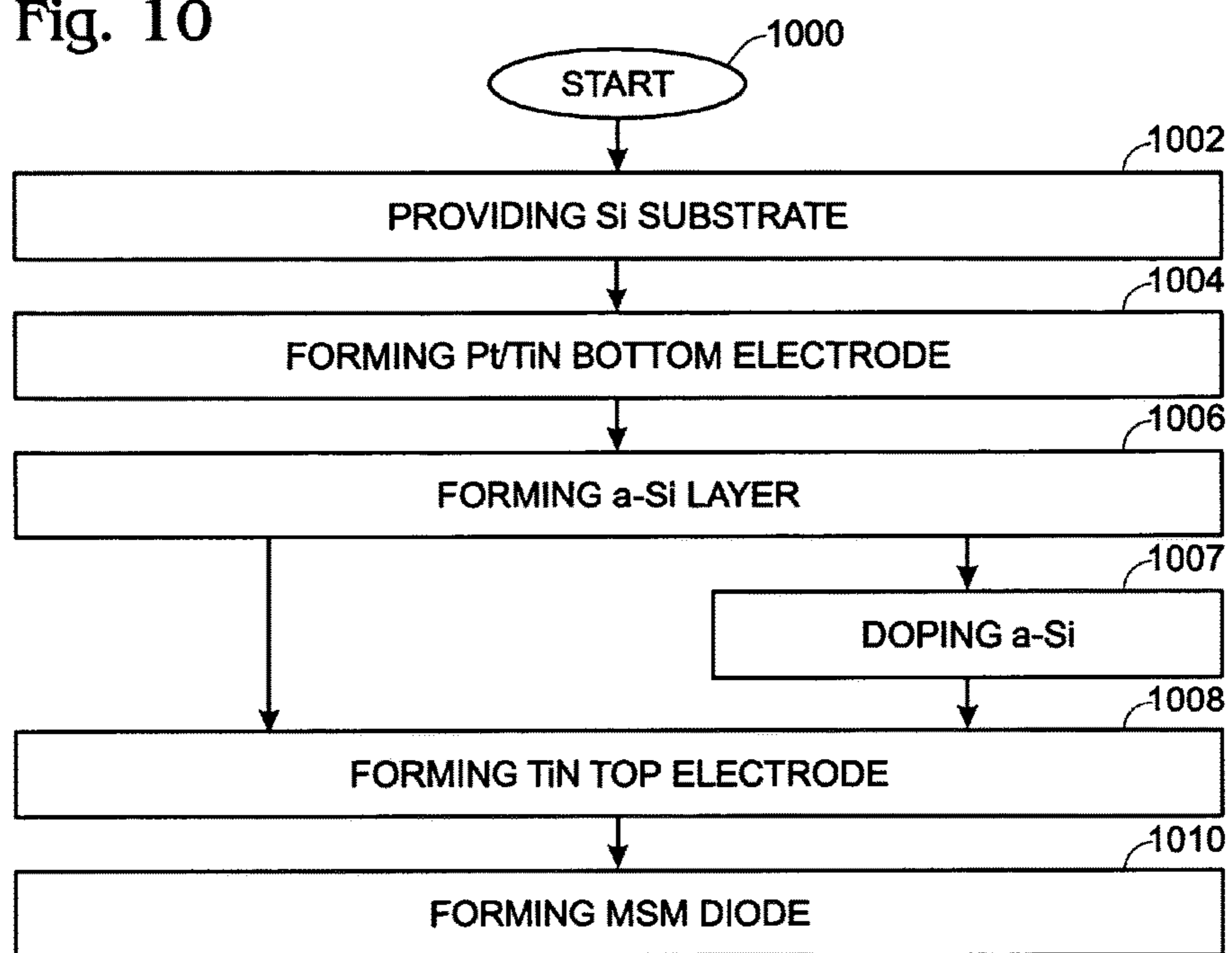


Fig. 10



**BACK-TO-BACK
METAL/SEMICONDUCTOR/METAL (MSM)
SCHOTTKY DIODE**

Matter enclosed in heavy brackets [] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue; a claim printed with strikethrough indicates that the claim was canceled, disclaimed, or held invalid by a prior post-patent action or proceeding.

This application is a reissue of U.S. patent application Ser. No. 12/234,663, filed Sep. 21, 2008 (now U.S. Pat. No. 7,968,419), entitled, *BACK-TO-BACK METAL/SEMICONDUCTOR/METAL (MSM) SCHOTTKY DIODE* which is a Divisional of a patent application entitled, METAL/SEMICONDUCTOR/METAL (MSM) BACK-TO-BACK SCHOTTKY DIODE, invented by Tingkai Li et al., Ser. No. 11/435,669, filed May 17, 2006 issued as U.S. Pat. No. 7,446,010; which is a Continuation-in-Part of a patent application entitled, MSM BINARY SWITCH MEMORY DEVICE, invented by Sheng Teng Hsu et al., Ser. No. 11/184,660, filed Jul. 18, 2005 issued as U.S. Pat. No. 7,303,971. This application is a Continuation-in-Part of a patent application entitled, METAL/ZnOx/METAL CURRENT LIMITER, invented by Tingkai Li et al., Ser. No. 11/216,398, filed Aug. 31, 2005 now U.S. Pat. No. 7,271,081. This application is a Continuation-in-Part of a patent application entitled, CROSSPOINT RESISTOR MEMORY DEVICE WITH BACK-TO-BACK SCHOTTKY DIODE, invented by Sheng Teng Hsu et al., Ser. No. 11/295,778, filed Dec. 7, 2005 now abandoned].

The above-mentioned applications are expressly incorporated herein by reference, and both claim priority under 35 U.S.C. §120. All of the above-referenced applications are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention generally relates to an integrated circuit (IC) fabrication process and, more particularly, to an MSM device, made with a silicon semiconductor, that acts as a back-to-back Schottky diode.

2. Description of the Related Art

A cross-point memory array is a matrix of memory elements, with electrical contacts arranged along x-axes (i.e., word lines) and along y-axes (i.e., bit lines). In some aspects, a digital value is stored as a memory resistance (high or low). The memory state of a memory cell can be read by supplying a voltage to the word line connected to the selected memory element. The resistance or memory state can be read as an output voltage of the bit line connected to the selected memory cell.

Cross-point resistor memory arrays are prone to read disturbance problems. As part of the read operation, electric current flows from a selected word line, through a selected memory cell, to a bit line. However, current also flows into unselected word lines that happen to cross over the selected bit line. The conduction of current into unselected word lines acts to decrease the output impedance and, hence, reduce the output voltage. To clearly distinguish memory states, the output voltage must be clearly distinguishable.

The undesired flow of current through a resistance memory cell can be addressed through the use of series-

connected diodes, since reverse biased diodes are poor conductors. However, this same feature makes a one-diode/one resistor (1D1R) memory difficult to program. Programming voltages cannot be used that reverse bias the diode.

Therefore, 1D1R cells are better suited for unipolar programming. Further, diodes are preferable formed from single crystal silicon, for optimal performance. However, large crystal grains are difficult to form using thin-film deposition processes.

Many cross-point resistor memory array structures have been proposed in attempts to minimize cross-talk problems during read operations in a large area cross-point resistor memory array. IRID memory cell are well suited for a mono-polarity programming memory array. However, high performance diodes can only be fabricated on single crystal silicon. For multi-layer three-dimensional arrays, the upper layer of a diode is formed by re-crystallization of deposited silicon, and the resulting diode usually exhibits poor electrical properties. In addition, the diode must be formed from a silicon film that is fairly thick.

Rinerson et al., U.S. Pat. No. 6,753,561, have proposed a memory cell of a metal/insulator/metal (MIM) structure in series with a resistor memory. The MIM device is non-conductive at low biases. When the bias voltage is higher than a certain value, the conductivity drastically increases. This voltage is called either the "current rise-up voltage" or "varistor voltage". The high field generated in response to the MIM high current region is associated with impact ionization. MIM devices are well known to be unstable if subjected to high current density stress. This is due to deep trap states in the insulator and the local avalanche breakdown when a high electric field is applied to the insulator. As a result, the current voltage characteristics are reversible only at relatively low current conditions. Therefore, MIM non-ohmic devices are not suitable for cross-point memory cells, which require a large numbers of programming operations. In addition, Rinerson does not teach specific MIM materials, or how a MIM device is fabricated.

It would be advantageous if a back-to-back Schottky diode device could be easily fabricated at relatively low temperatures that was highly conductive when forward biased, poorly conductive when reversed biased at relatively low voltages, but highly conductive when reversed biased at higher voltages.

It would be advantageous if the above-mentioned diode could be fabricated with a resistance memory device, to build 1R1D crosspoint memory arrays that have low leakage current, but are capable of programming using bipolar voltages.

SUMMARY OF THE INVENTION

Described herein is a back-to-back diode device that permits current flow in both forward and reverse directions under higher voltage (forward and reverse) bias conditions, but blocks current in under lower voltage bias conditions. The current limiter can be added to a resistance memory cell, to permit high voltage bipolar programming, without the penalty of flowing current into unselected word lines during lower voltage read operations.

Many conventional cross-point resistor memory arrays suffer from read disturbance problems, as electric current flows from a selected word line, through a selected memory cell to a bit line, and then into unselected word lines which cross over the bit line. A cross-point array made with a

current limiter in the memory cells minimizes the current flow into the unselected word lines, maximizing the output (read) voltage.

A metal/semiconductor/metal (MSM) back-to-back Schottky barrier device exhibits a symmetrical non-ohmic property with respect to both positive and negative bias voltages. This device can be used as memory cell current limiter in a resistor cross-point memory array. Since the conductivity of the semiconductor is high, and the capture cross-section of trap state is small, the device is stable operating at high fields. The current density of MSM devices can be several orders of magnitude higher than that of MIM devices.

In addition to 1R1D crosspoint memory applications, the MSM can be used in other applications and circuits that use a current limiting diode. In one aspect, details of an amorphous Si MSM diode (e.g., a TiN/A-Si/TiN structure) are presented, fabricated using DC-sputtering, B and As implantations, and post-annealing processes.

Accordingly, a method is provided for forming a MSM back-to-back Schottky diode from a silicon (Si) semiconductor. The method deposits a Si semiconductor layer between a bottom electrode and a top electrode, and forms a MSM diode having a threshold voltage, breakdown voltage, and on/off current ratio. The method is able to modify the threshold voltage, breakdown voltage, and on/off current ratio of the MSM diode in response to controlling the Si semiconductor layer thickness. Generally, both the threshold and breakdown voltage are increased in response to increasing the Si thickness. With respect to the on/off current ratio, there is an optimal thickness.

The method is able to form an amorphous Si (a-Si) and polycrystalline Si (polySi) semiconductor layer using either chemical vapor deposition (CVD) or DC sputtering. For example, DC sputtering can be used to form an a-Si film. The a-Si can then be annealed to form polySi. Increases in the DC sputtering power or substrate temperature, result in a decrease in threshold voltage, an increase in breakdown voltage, and a decrease in the on/off current ratio. Likewise, the threshold voltage and breakdown voltage increase in response to increasing the oxygen partial pressure. If the semiconductor layer is deposited to the optimal thickness, then the on/off current ratio is decreased when the Si thickness is made thinner, as both the on and off currents increase. Likewise, if the Si thickness is made greater than the optimal thickness, then the on/off current ratio also decreases, as both the on and off currents decrease.

Fabrication details are also presented for the deposition of semiconductor material using the CVD process. In addition, the Si semiconductor can be doped with a Group V donor material. Doping decreases the threshold voltage and increases the breakdown voltage. There is also an on/off current ratio optimal thickness to consider when doping is used.

Additional details of the above-described method of forming an MSM back-to-back Schottky diode, and an MSM diode device are provided below.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a partial cross-sectional view of a metal/semiconductor/metal (MSM) back-to-back Schottky diode fabricated from a silicon (Si) semiconductor.

FIG. 2 is a partial cross-sectional view of a resistance memory device with a MSM back-to-back Schottky diode.

FIG. 3A through 3F are IV curves of MSM devices with various a-Si thicknesses.

FIG. 4 is a graph depicting the relationship between threshold voltages, breakdown voltage, and a-Si thicknesses.

FIGS. 5A through 5D are graphs depicting the IV behavior of MSM devices with As-implanted Si thin films.

FIG. 6 is a graph depicting the relationship between threshold voltage, breakdown voltage, and a-Si thickness when the a-Si is implanted with As dopant.

FIGS. 7A and 7B are graphs depicting IV curves of MSM devices with a-Si thicknesses of 1200 nm and device sizes of 200 μm \times 200 μm .

FIGS. 8A and 8B are graphs depicting the IV curves of MSM devices with a-Si thicknesses of 1200 nm and device sizes of 200 μm \times 200 μm .

FIG. 9 is a flowchart illustrating a method for forming a MSM back-to-back Schottky diode from a Si semiconductor.

FIG. 10 is a flowchart illustrating another method for forming a MSM back-to-back Schottky diode from a Si semiconductor.

DETAILED DESCRIPTION

FIG. 1 is a partial cross-sectional view of a metal/semiconductor/metal (MSM) back-to-back Schottky diode fabricated from a silicon (Si) semiconductor. The MSM diode 100 comprises a Si substrate 102, and a bottom electrode (BE) 104 with a Pt layer 106 overlying the substrate 102, and a TiN layer 108 overlying the Pt layer 106. An amorphous Si (a-Si) semiconductor layer 110 overlies the bottom electrode 104. The a-Si semiconductor layer 110 has a thickness 112 in the range of 10 to 80 nanometers (nm). A TiN top electrode (TE) 114 overlies the a-Si semiconductor layer 110.

The a-Si semiconductor range of thickness may be considered unconventional, and even unexpected. As described in more detail below, the optimal device performance is dependent upon a thickness that must be balanced against considerations of threshold voltage, breakdown voltage, and on/off current ratio.

As described in more detail below, generally the MSM diode 100 has a threshold voltage in the range of about 0.8 to 2 volts and a breakdown voltage in the range of about 2.5 to 6 volts. If the a-Si semiconductor layer 110 has a thickness 112 of about 30 nm, then the MSM diode has a threshold voltage of about 1.5 volts, a breakdown voltage of about 3.5 volts, and an on/off current ratio of about 1.5×10^2 amperes per square centimeters (A/cm^2) at 3 volts, to 6×10^{-2} A/cm^2 at 1 volt, which is 3.5 orders of magnitude.

When the a-Si semiconductor layer 110 includes a Group V donor dopant material, the MSM diode 100 has a threshold voltage in the range of about 2 to 3.5 volts and a breakdown voltage in the range of about 6 to 12 volts. If the doped a-Si semiconductor layer 110 has a thickness 112 of about 30 nm, then the MSM diode 100 has a threshold voltage of about 2.5 volts and a breakdown voltage of about 6 volts.

Besides the materials specifically mentioned above, the top electrode 114 and bottom electrode 104 can be made from the following materials: Pt, Ir, Au, Ag, TiN, AlCu, Pd, W, Ti, Cr, Si, Al, Rh, Ta, Ru, TaN, YBCO, indium tin oxide (ITO), InO₃, ZnO, RuO₂, and La_{1-x}Sr_xCoO₃. However, other unnamed electrode materials are also known in the art that may be used. The substrate 102 is not limited to Si, and may be a material such as Ge, SiO₂, GeAs, glass, quartz, or plastic. Further, although an a-Si semiconductor material has been presented, in other aspects the semiconductor material is polySi.

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FIG. 2 is a partial cross-sectional view of a resistance memory device with a MSM back-to-back Schottky diode. The device 200 comprises a memory resistor bottom electrode (MRBE) 202 and a memory resistor (MR) material 204 overlying the memory resistor bottom electrode 202. A MSM diode 100 overlies the memory resistor material 204. The MSM diode is shown in FIG. 1 and described above, and will not be repeated here in the interest of brevity.

The memory resistor material 204 overlying the memory resistor bottom electrode 202 may be a material such as $\text{Pr}_{0.3}\text{Ca}_{0.7}\text{MnO}_3$ (PCMO), colossal magnetoresistive (CMR) film, transition metal oxides, Mott insulators, high-temperature super conductor (HTSC), or perovskite materials.

The MSM top electrode 114 may be a word line in an array of connected memory devices. In a memory array, a plurality of devices 200 would be attached to each bit line and word line, as is well understood in the art. Then, the MR bottom electrode 202 would be a bit line connected to other memory devices (not shown) in the array. In other aspects not shown, the MSM diode 100 is formed “under” the MR cell, as opposed to “over” the memory cell as shown. That is, the MSM bottom metal electrode 104 would be the bit line, with the memory resistor bottom electrode 202 formed overlying the MSM top electrode 114. Then, an MR top electrode over the MR material 204 (not shown) would be a word line. Materials such as Pt, Ir, Au, Ag, Ru, TiN, Ti, Al, AlCu, Pd, Rh, W, Cr, conductive oxides, Ag, Au, Pt, Ir, or TiN, may potentially be used as the MR top and bottom electrodes.

Functional Description

As described above, the present invention MSM current limiter can be used for crosspoint resistance random access memory (RRAM) arrays and other applications. To that end, amorphous Si MSM structures were studied, especially TiN/a-Si/TiN with a-Si thickness ranging from about 10 nm to 80 nm, with and without As implantation, using DC-sputtering methods. The current/voltage (IV) curves of the MSM devices with a-Si thin films exhibit non-linear characteristics. The threshold voltage and breakdown voltage increase, and the current decreases, as the a-Si film thickness increases. Interesting data is observed from MSM devices having an a-Si thickness in the range of about 30 and 50 nm.

Experimental Methods

The substrate is a P-type Si (100) wafer. After SC1, SC2 cleaning and HF 20:1 dip etching, 100 nm Pt and 150 nm TiN layers are deposited on the Si wafer to form the bottom electrode. The bottom and top electrodes can be any metals such as Pt, Ir, Al, AlCu, Au, Ag, Pd, Rh, W, Ti, Cr, and Si, to name a few materials. The bottom and top electrodes can also be conductive oxides such YBCO, ITO, InO₃, ZnO, RuO₂, and $\text{La}_{1-x}\text{Sr}_x\text{CoO}_3$. Interesting data is obtained from TiN/a-Si/TiN structures.

Amorphous Si thin films with various thicknesses from 10 nm to 80 nm can be deposited on TiN using DC-sputtering and CVD methods. The DC-sputtering and CVD process conditions are listed in Table 1 and 2. As an experiment, half of the wafers with various thicknesses are implanted with As, at 30 keV, with dose of 1E12, and annealed at 500° C. for 10 minutes. MSM diodes with polySi films thickness of 1200 nm are also formed, with double ion implantations of B at 200 keV and 1E13, and an As-implantation of 30 keV and 2E15, with post-annealing at temperatures from about 700-900° C. for 30-90 minutes. Finally, top electrodes of TiN, with thickness of 150 nm are deposited and patterned

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on the a-Si to make MSM device structures. The device structure is Si/Pt (100 nm)/TiN(150 nm)/a-Si/TiN(150 nm).

The phases of the a-Si films can be identified using x-ray diffraction. A Scanning Electron Microscope can be used to measure the thickness and surface morphologies of the films. The properties of the MSM devices with various a-Si thickness can be measured using a HP 4156A precision semiconductor parameter analyzer.

TABLE 1

The DC sputtering process conditions for a-Si thin films					
Target	Power (W)	Dep. Temp.	Dep. Pres.	Atmosphere	Dep. Time
Si	100-300	20-200° C.	7-9 mtorr	Ar	7-150 m

TABLE 2

The process conditions for CVD polysilicon deposition			
Silane flow	Deposition temp.	Deposition pressure	Deposition time
40-200 sccm	500-600° C.	150-250 mtorr	10 min.-6 hours

Experimental Results

FIG. 3A through 3F are IV curves of MSM devices with various a-Si thicknesses. The device size is about 100 $\mu\text{m} \times 100 \mu\text{m}$. The IV measurements are from the top electrode of TiN, to bottom electrode Pt layer. The IV curves of the devices with a-Si of 10 nm exhibit non-linear characteristics when the applied voltage is equal to, or smaller than 1 V. The threshold voltage is around 0.2 V and the breakdown voltage is about 1 V, as shown in FIG. 3A. After breakdown, the MSM device loses its non-linear characteristics. With increasing a-Si film thickness, the threshold voltage and breakdown voltage increase, and the current decreases at the same applied voltage. On the other hand, by increasing the a-Si film thickness, the a-Si MSM devices show much better non-linear characteristics for current limiter applications.

In FIG. 3B the a-Si film thickness is 15 nm, the threshold voltage is about 0.8 V, and the breakdown voltage is larger than 2.5 V.

In FIG. 3C the a-Si film thickness is 20 nm, the threshold voltage is about 1.3 V, and the breakdown voltage is larger than 2.5 V. The a-Si MSM devices show very nice non-linear characteristics, suitable for current limiter applications.

In FIG. 3D the a-Si film thickness is 25 nm, the threshold voltage is about 1.7 V, and the breakdown voltage is larger than 3.5 V.

In FIG. 3E the a-Si film thickness is 30 nm, the threshold voltage is around 1.5 V, and the breakdown voltage is larger than 3.5 V.

In FIG. 3F the a-Si film thickness is 50 nm, the threshold voltage is around 2 V, and the breakdown voltage is larger than 6 V.

FIG. 4 is a graph depicting the relationship between threshold voltages, breakdown voltage, and a-Si thicknesses. The MSM device of FIG. 3F, with an a-Si thickness of 30 nm, shows interesting current limiting characteristics. The “on” current density at an applied voltage of 3 V is about $1.5 \times 10^2 \text{ A/cm}^2$, and the “off” current density at an applied voltage of 1 V is about $6 \times 10^{-2} \text{ A/cm}^2$. The ratio of “on” current density to “off” current density is of the order of 3.5.

FIGS. 5A through 5D are graphs depicting the IV behavior of MSM devices with As-implanted Si thin-films. Arsenic implanted Si thin-films, with thicknesses from 30 nm to 80 nm, are investigated to further explore the non-linear characteristics of a-Si MSM devices for current limiter applications. In FIG. 5A the a-Si film thickness is 30 nm, the threshold voltage is about 2.5 V and the breakdown voltage is larger than 6V.

In FIG. 5B the a-Si film thickness is 50 nm, the threshold voltage is around 3 V, and the breakdown voltage is larger than 8 V.

In FIG. 5C the a-Si film thickness is 65 nm, the threshold voltage is around 4 V, and the breakdown voltage is larger than 12 V.

In FIG. 5D the a-Si film thickness is 80 nm, the threshold voltage is round 3.5 V, and the breakdown voltage is larger than 10 V.

FIG. 6 is a graph depicting the relationship between threshold voltage, breakdown voltage, and a-Si thickness when the a-Si is implanted with As dopant. Compared to MSM devices without implantation, the MSM device with As-implanted Si thin films show very good nonlinear characteristics, higher threshold and breakdown voltages, but lower currents. The reason may due to the formation of surface oxide on amorphous Si during the implantation and post-annealing.

FIGS. 7A and 7B are graphs depicting IV curves of MSM devices with a-Si thicknesses of 1200 nm and device sizes of 200 μm \times 200 μm . The IV measurements are from top electrode of Pt, to bottom electrode of Pt. From the experiment results, further increasing of a-Si thickness up to 1200 nm, result in threshold voltage increases and breakdown voltage increases over 50 V. The currents decrease with increasing a-Si thickness, which means that the resistances of the MSM devices increase. The threshold voltage is very small when low applied voltages are used. But the threshold voltage can be increased after higher voltage training, which switches the devices at higher voltages, before using a lower operation voltage to measure the IV curves. The threshold voltages increase with increases in applied voltages, which is non-ideal for current limiter applications.

FIGS. 8A and 8B are graphs depicting the IV curves of MSM devices with a-Si thicknesses of 1200 nm and device sizes of 200 μm \times 200 μm . The devices are measured from the top electrode of Pt, to the Si substrate. For the high applied voltages, the IV curves exhibit non-linear characteristics, as shown in FIG. 8A. But the IV curves tend to be linear when the low voltages are applied, as shown in FIG. 8B. The threshold voltages also increase with increases in applied voltages. The experimental results show that the MSM devices with thick a-Si films are non-ideal for current limiter applications.

In summary, the IV curves of the MSM devices with a-Si thin films exhibit non-linear characteristics. The threshold voltage and breakdown voltage increase, and the current decreases, with increases in the a-Si film thickness. Compared with MSM devices without implantation, MSM devices with As implanted in the Si thin-films show very good nonlinear characteristics, higher threshold and breakdown voltages, but lower currents. The reason may due to the formation of surface oxide on amorphous Si during the implantation and post-annealing, which may be cured with an HF surface cleaning. Good current limiter data is obtained from MSM devices with an a-Si thickness of 30

current density at applied an voltage of 1V is about 6×10^{-2} A/cm², which is a ratio of about 3.5.

A crosspoint resistor memory array requires a current limiting device, such as diode, in series with the bit memory resistor, to minimize the programming interference, programming disturbance, and read disturbances. A crosspoint memory array with a diode in series with the memory resistance bit cells can only be programmed using mono-polarity voltage pulses. Since a high quality (single-crystal) diode cannot be fabricated onto metal multi-layers, the integration of a resistor cross-point memory array with a diode/resistor cell is not feasible. A MIM current limiter cannot be used in place of diode, as a metal-insulator-metal device is not reliable, even in a very small current density operation. The reliability problems are due to the deep trap states in the insulator and the local catastrophic breakdown in the insulator. However, if the insulator is replaced with a semiconductor material, a back-to-back Schottky structure can be formed.

The MSM device functions as a back-to-back Schottky diode. The current density is dependent upon the barrier height of the metal, with respect to the semiconductor. The series resistance of the MSM device may be decreased, by reducing the thickness and the resistivity of the semiconductor material. If the semiconductor is too thin, the leakage current of the device increases and the low bias voltage current may be too large for some practical memory cell applications. Since the purpose of MSM device is to limit the current flow through the unselected cells in an array, the IV properties of the MSM device do not have to be symmetric around the zero bias voltage. Therefore, the MSM electrodes need not be the same material.

FIG. 9 is a flowchart illustrating a method for forming a MSM back-to-back Schottky diode from a Si semiconductor. Although the method is depicted as a sequence of numbered steps for clarity, the numbering does not necessarily dictate the order of the steps. It should be understood that some of these steps may be skipped, performed in parallel, or performed without the requirement of maintaining a strict order of sequence. The method starts at Step 900.

Step 902 deposits a Si semiconductor layer between a bottom electrode and a top electrode. Depositing the Si semiconductor layer in Step 902 includes forming a semiconductor layer selected from a-Si or polySi materials, using a CVD or DC sputtering process. Step 904 forms a MSM diode having a threshold voltage, breakdown voltage, and on/off current ratio. Step 906 modifies the threshold voltage, breakdown voltage, and on/off current ratio of the MSM diode in response to controlling the Si semiconductor layer thickness.

Generally, increasing the Si thickness in Step 902 leads to an increase in the threshold voltage and an increase the breakdown voltage (Step 906). With respect to the on/off ratio, however, there is an optimal thickness. The optimal thickness is associated with a large on/off current ratio. If the Si semiconductor layer is deposited to this so-called optimal thickness in Step 902, then modifying the on/off current ratio of the MSM diode in Step 906 includes substeps. Step 906a increases both the on and off currents in response to decreasing the Si thickness below optimal thickness. Step 906b decreases both the on and off currents in response to increasing the Si thickness above the optimal thickness.

In one aspect, Step 902 forms an a-Si semiconductor with the DC sputtering process as follows:

using a Si target;
sputtering with a power in the range of about 100 to 300 watts (W);

heating a substrate to a temperature of about 20° to 200° C.;

creating a deposition pressure in the range of about 7.0 to 9 mtorr;

using an atmosphere of Ar;

depositing for a duration in the range of about 7 to 150 minutes; and,

forming a-Si.

Step 902 forms a polySi semiconductor with the DC sputtering process, following the formation of the a-Si, by annealing at a temperature greater than 550° C., and forming polySi as a result.

In one aspect, increasing the DC sputtering power or substrate temperature in Step 902 results in (Step 906) decreasing the threshold voltage, increasing the breakdown voltage, and decreasing the on/off current ratio.

If Step 902 forms the a-Si semiconductor with a DC sputtering process that uses an oxygen partial pressure in the range of 0 to 5%, then Step 906 increases the threshold voltage and breakdown voltage in response to increasing the oxygen partial pressure. In considering the thickness of the Si semiconductor deposited in Step 902, Step 906 modifies the on/off current ratio of the MSM diode in response to increasing the oxygen partial pressure as follows. The on/off current ratio decreases when the Si thickness is less than the optimal (defined with respect to the on/off ratio) thickness. Likewise, the on/off current ratio decreases when the Si thickness is greater than the optimal thickness.

Alternately, Step 902 forms the Si semiconductor layer using a CVD process as follows:

flowing silane at a rate in the range of about 40 to 200 standard cubic centimeters (sccm);

heating the substrate to a temperature in the range of about 500 to 600° C.;

creating a deposition pressure in the range of about 150 to 250 milliTorr (mtorr); and,

depositing for a duration in the range of about 10 minutes to 6 hours.

In another aspect of the method, Step 903 dopes the Si semiconductor layer with a Group V donor material. Then, modifying the threshold voltage, breakdown voltage, and on/off current ratio of the MSM diode in Step 906 includes decreasing the threshold voltage and increasing the breakdown voltage in response to increasing the doping the Si semiconductor layer.

In considering the thickness of the Si semiconductor deposited in Step 902, the on/off current ratio of the MSM diode is modified (Step 906) in response to doping the Si semiconductor layer as follows. The on/off current ratio decreases when the Si thickness is less than the optimal (as defined with respect to the on/off ratio) thickness. Likewise, the on/off current ratio decreases when the Si thickness is greater than the optimal thickness.

In one aspect, doping the Si semiconductor layer in Step 903 includes substeps. Step 903a implants As with an energy of about 30 keV and a dose of about 1×10^{12} . Step 903b anneals at a temperature of about 500° C. for about 10 minutes. In another aspect, Step 902 forms a polysi semiconductor layer having a thickness in the range of about 600 to 1200 nm. Then, doping the Si semiconductor layer in Step 903 includes alternate substeps. Step 903c implants B with an energy of about 200 keV and a dose of about 1×10^{13} . Step 903d implants As with an energy of about 30 keV and a dose of about 2×10^{15} . Step 903e anneals at a temperature in the range of about 700° to 900° C. for about 30 to 90 minutes.

FIG. 10 is a flowchart illustrating another method for forming a MSM back-to-back Schottky diode from a Si

semiconductor. The method starts at Step 1000. Step 1002 provides a Si substrate. Step 1004 forms a bottom electrode with a Pt layer overlying the substrate, and a TiN layer overlying the Pt layer. Step 1006 forms an a-Si semiconductor layer overlying the bottom electrode, having a thickness in the range of 10 to 80 nm. Step 1008 forms a TiN top electrode overlying the a-Si semiconductor layer. Step 1010 forms a MSM diode having a threshold voltage in the range of about 0.8 to 2 volts, and a breakdown voltage in the range of about 2.5 to 6 volts.

In one aspect, forming the a-Si semiconductor layer in Step 1006 includes forming an a-Si layer with a thickness of about 30 nm. Then, Step 1010 forms an MSM diode with a threshold voltage of about 1.5 volts and a breakdown voltage of about 3.5 volts. Step 1010 also forms an MSM diode with an on/off current ratio of about 1.5×10^2 amperes per square centimeters (A/cm^2) at 3 volts, to $6 \times 10^{-2} A/cm^2$ at 1 volt, which is 3.5 orders of magnitude.

In another aspect, Step 1007 dopes the a-Si semiconductor layer with a Group V donor material. Then, Step 1010 forms an MSM diode with a threshold voltage in the range of about 2 to 3.5 volts and a breakdown voltage in the range of about 6 to 12 volts. If the a-Si semiconductor layer is formed to a thickness of about 30 nm (Step 1006), then Step 1010 forms an MSM diode with a threshold voltage of about 2.5 volts and a breakdown voltage of about 6 volts.

A MSM back-to-back Schottky diode made with a Si semiconductor, and corresponding fabrication processes have been provided. Examples of process details have been presented to illustrate the invention. Likewise, a resistance memory device has been presented as an example of an application. However, the invention is not limited to merely these examples. Other variations and embodiments of the invention will occur to those skilled in the art.

We claim:

1. A method for forming a metal/semiconductor/metal (MSM) back-to-back Schottky diode from a silicon (Si) semiconductor, *the method* comprising:

providing a Si substrate;

forming a bottom electrode with a *platinum* (Pt) layer overlying the Si substrate, and a *titanium nitride* (TiN) layer overlying the Pt layer;

forming an amorphous Si (a-Si) semiconductor layer overlying the bottom electrode, having a thickness in [the] a range of about 10 nm to 80 [nanometers (nm)] nm;

forming a TiN top electrode overlying the a-Si semiconductor layer; and,

forming a MSM diode having] wherein the formed MSM diode has a threshold voltage in [the] a range of about 0.8 volts to 2 volts, and a breakdown voltage in the range of about 2.5 volts to 6 volts.

2. The method [for forming a MSM back-to-back Schottky diode from a Si semiconductor according to] of claim 1, wherein said forming [the] an a-Si semiconductor layer [includes] comprises forming an a-Si layer with a thickness of about 30 nm; and], and wherein said forming [the] a MSM diode [includes] comprises forming an MSM diode with a threshold voltage of about 1.5 volts and a breakdown voltage of about 3.5 volts.

3. The method [for forming a MSM back-to-back Schottky diode from a Si semiconductor according to] of claim 2, wherein said forming [the] a MSM diode [includes] comprises forming an MSM diode with an on/off current ratio of about 1.5×10^2 amperes per square centimeters (A/cm^2) at 3 volts, to about $6 \times 10^{-2} A/cm^2$ at 1 volt.

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4. [The method for forming a MSM back-to-back Schottky diode from a Si semiconductor according to claim 1 further comprising:] *A method for forming a metal/semiconductor/metal (MSM) back-to-back Schottky diode from a silicon (Si) semiconductor, the method comprising:*

providing a Si substrate;

forming a bottom electrode with a platinum (Pt) layer overlying the Si substrate, and a titanium nitride (TiN) layer overlying the Pt layer;

forming an amorphous Si (a-Si) semiconductor layer overlying the bottom electrode, having a thickness in a range of about 10 to 80 nanometers (nm);

forming a TiN top electrode overlying the a-Si semiconductor layer;

doping the a-Si semiconductor layer with a Group V donor material; and

wherein forming the MSM diode includes forming an MSM diode with] wherein the formed MSM diode has a threshold voltage in [the] a range of about 2 volts to 3.5 volts and a breakdown voltage in [the] a range of about 6 volts to 12 volts.

5. The method [for forming a MSM back-to-back Schottky diode from a Si semiconductor according to] of claim 4, wherein *said forming [the] an a-Si semiconductor layer [includes] comprises forming an a-Si layer with a thickness of about 30 nm; and], and wherein said forming [the] a MSM diode [includes] comprises forming an MSM diode with a threshold voltage of about 2.5 volts and a breakdown voltage of about 6 volts.*

6. A metal/semiconductor/metal (MSM) back-to-back Schottky diode fabricated from a silicon (Si) semiconductor, comprising:

a Si substrate;

a bottom electrode with a *platinum* (Pt) layer overlying the Si substrate, and a *titanium nitride* (TiN) layer overlying the Pt layer;

an amorphous Si (a-Si) semiconductor layer overlying the bottom electrode, having a thickness in [the] a range of 10 nm to 80 [nanometers (nm)] nm; and

a TiN top electrode overlying the a-Si semiconductor layer,

wherein the MSM diode has a threshold voltage in a range of about 0.8 volts to 2 volts and a breakdown voltage in a range of about 2.5 volts to 6 volts.

[7. The MSM back-to-back Schottky diode from a Si semiconductor according to claim 6 wherein the MSM diode has a threshold voltage in the range of about 0.8 ; to 2 volts and a breakdown voltage in the range of about 2.5 to 6 volts.]

8. [The MSM back-to-back Schottky diode from a Si semiconductor according to claim 6] *A metal/semiconductor/metal (MSM) back-to-back Schottky diode fabricated from a silicon (Si) semiconductor, comprising:*

a Si substrate;

a bottom electrode with a platinum (Pt) layer overlying the Si substrate, and a titanium nitride (TiN) layer overlying the Pt layer;

an amorphous Si (a-Si) semiconductor layer overlying the bottom electrode, having a thickness in a range of 10 nm to 80 nm; and

a TiN top electrode overlying the a-Si semiconductor layer,

wherein the a-Si semiconductor layer has a thickness of about 30 nm; and], and wherein the MSM diode has a threshold voltage of about 1.5 volts, a breakdown voltage of about 3.5 volts, and an on/off current ratio of about 1.5×10^2 amperes per square centimeters (A/cm^2) at 3 volts, to about 6×10^{-2} A/cm^2 at 1 volt.

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9. [The MSM back-to-back Schottky diode from a Si semiconductor according to claim 6] *A metal/semiconductor/metal (MSM) back-to-back Schottky diode fabricated from a silicon (Si) semiconductor, comprising:*

a Si substrate;

a bottom electrode with a platinum (Pt) layer overlying the Si substrate, and a titanium nitride (TiN) layer overlying the Pt layer;

an amorphous Si (a-Si) semiconductor layer overlying the bottom electrode, having a thickness in a range of 10 nm to 80 nm; and

a TiN top electrode overlying the a-Si semiconductor layer,

wherein the a-Si semiconductor layer [includes] comprises a Group V donor dopant material; and], and wherein the MSM diode has a threshold voltage in [the] a range of about 2 volts to 3.5 volts and a breakdown voltage in [the] a range of about 6 volts to 12 volts.

10. The MSM back-to-back Schottky diode [from a Si semiconductor according to] of claim 9, wherein the a-Si semiconductor layer has a thickness of about 30 nm; and], and wherein the MSM diode has a threshold voltage of about 2.5 volts and a breakdown voltage of about 6 volts.

11. *A method for forming a diode, the method comprising: forming a bottom electrode on a substrate, wherein the bottom electrode includes a first electrically-conductive layer and a second electrically-conductive layer overlying the first electrically-conductive layer;*

forming a deposited amorphous material overlying the bottom electrode, wherein the deposited amorphous material has a thickness in a range of about 10 nm to 80 nm; and

forming a top electrode overlying the deposited amorphous material, wherein the top electrode comprises a third electrically-conductive layer; and

wherein the formed diode has a threshold voltage in a range of about 0.8 volts to 2 volts and a breakdown voltage in a range of about 2.5 volts to 6 volts;

forming a metal/semiconductor/metal diode having a threshold voltage in a range of about 0.8 volts to 2 volts and a breakdown voltage in a range of about 2.5 volts to 6 volts.

12. *The method of claim 11, wherein the first electrically-conductive layer comprises platinum, and wherein the second electrically-conductive layer comprises titanium nitride.*

13. *The method of claim 12, wherein the third electrically-conductive layer comprises titanium nitride.*

14. *The method of claim 11, wherein the first electrically-conductive layer and the second electrically-conductive layer each comprise at least one of Ir, Au, Ag, TiN, AlCu, Pd, W, Ti, Cr, Si, Al, Rh, Ta, Ru, TaN, YBCO, indium tin oxide, InO₃, ZnO, RuO₂, and La_{1-x}Sr_xCoO₃.*

15. *The method of claim 14, wherein the third electrically-conductive layer comprises at least one of Ir, Au, Ag, TiN, AlCu, Pd, W, Ti, Cr, Si, Al, Rh, Ta, Ru, TaN, YBCO, indium tin oxide, InO₃, ZnO, RuO₂, and La_{1-x}Sr_xCoO₃.*

16. *The method of claim 11, further comprising doping the deposited amorphous material with a Group V donor material.*

17. *An apparatus comprising:*

a substrate;

a bottom electrode including a first electrically-conductive layer overlying the substrate, and a second electrically-conductive layer overlying the first electrically-conductive layer;

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a deposited amorphous material overlying the bottom electrode, wherein the deposited amorphous material has a thickness in a range of about 10 to 80 nanometers (nm); and

a top electrode overlying the deposited amorphous material, wherein the top electrode includes a third electrically-conductive layer,

wherein the apparatus comprises a metal/semiconductor/metal diode having a threshold voltage in a range of about 0.8 to 2 volts and a breakdown voltage in a range of about 2.5 volts to 6 volts.

18. The apparatus of claim 17, wherein the first electrically-conductive layer comprises platinum, and wherein the second electrically-conductive layer comprises titanium nitride.

19. The apparatus of claim 18, wherein the third electrically-conductive layer comprises titanium nitride.

20. The apparatus of claim 17, wherein the first electrically-conductive layer and the second electrically-conductive layer each comprise at least one of Ir, Au, Ag, TiN, AlCu, Pd, W, Ti, Cr, Si, Al, Rh, Ta, Ru, TaN, YBCO, indium tin oxide, InO₃, ZnO, RuO₂, and La_{1-x}Sr_xCoO₃.

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21. The apparatus of claim 20, wherein the third electrically-conductive layer comprises at least one of Ir, Au, Ag, TiN, AlCu, Pd, W, Ti, Cr, Si, Al, Rh, Ta, Ru, TaN, YBCO, indium tin oxide, InO₃, ZnO, RuO₂, and La_{1-x}Sr_xCoO₃.

22. The apparatus of claim 17, wherein the substrate comprises silicon.

23. The apparatus of claim 17, wherein the substrate comprises at least one of Ge, SiO₂, GeAs, glass, quartz, or plastic.

24. The apparatus of claim 17, wherein the deposited amorphous material is doped with a Group V donor material.

25. The apparatus of claim 17, wherein the bottom electrode, the deposited amorphous material, and the top electrode are components of a metal/semiconductor/metal (MSM) diode, wherein the apparatus further comprises a memory resistor bottom electrode and a memory resistor material overlying the memory resistor bottom electrode, and wherein the MSM diode overlies the memory resistor material.

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