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(54) **VOLTAGE-PROGRAMMING SCHEME FOR CURRENT-DRIVEN AMOLED DISPLAYS**

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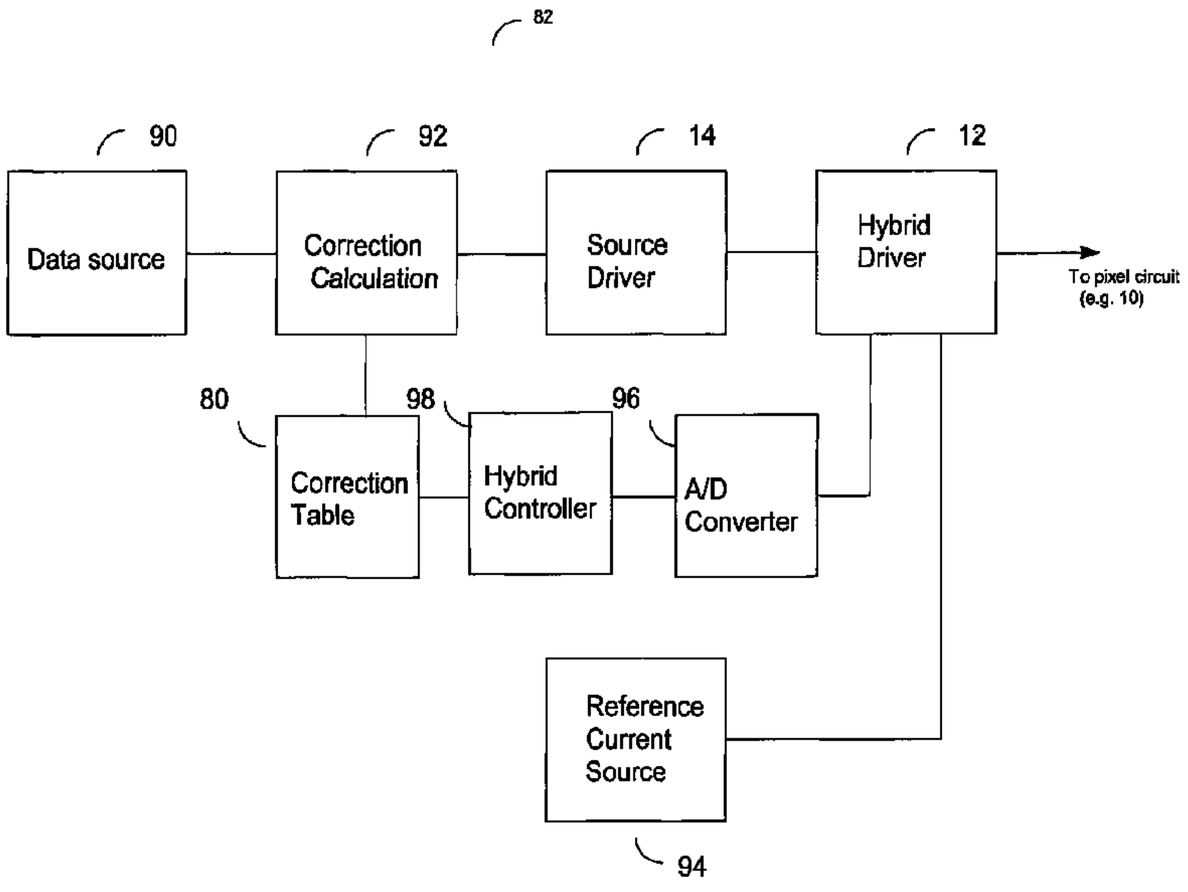
(57) **ABSTRACT**

A system and method for driving an AMOLED display is provided. The AMOLED display includes a plurality of pixel circuits. A voltage-programming scheme, a current-programming scheme or a combination thereof is applied to drive the display. Threshold shift information, and/or voltage necessary to obtain hybrid driving circuit may be acquired. A data sampling may be implemented to acquire a current/voltage relationship. A feedback operation may be implemented to correct the brightness of the pixel.

5 Claims, 23 Drawing Sheets



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application for the reissue of Pat. No. 8,232,939, which is a continuation of application No. 11/571,480, filed as application No. PCT/CA2005/001007 on Jun. 28, 2005, now Pat. No. 8,115,707.

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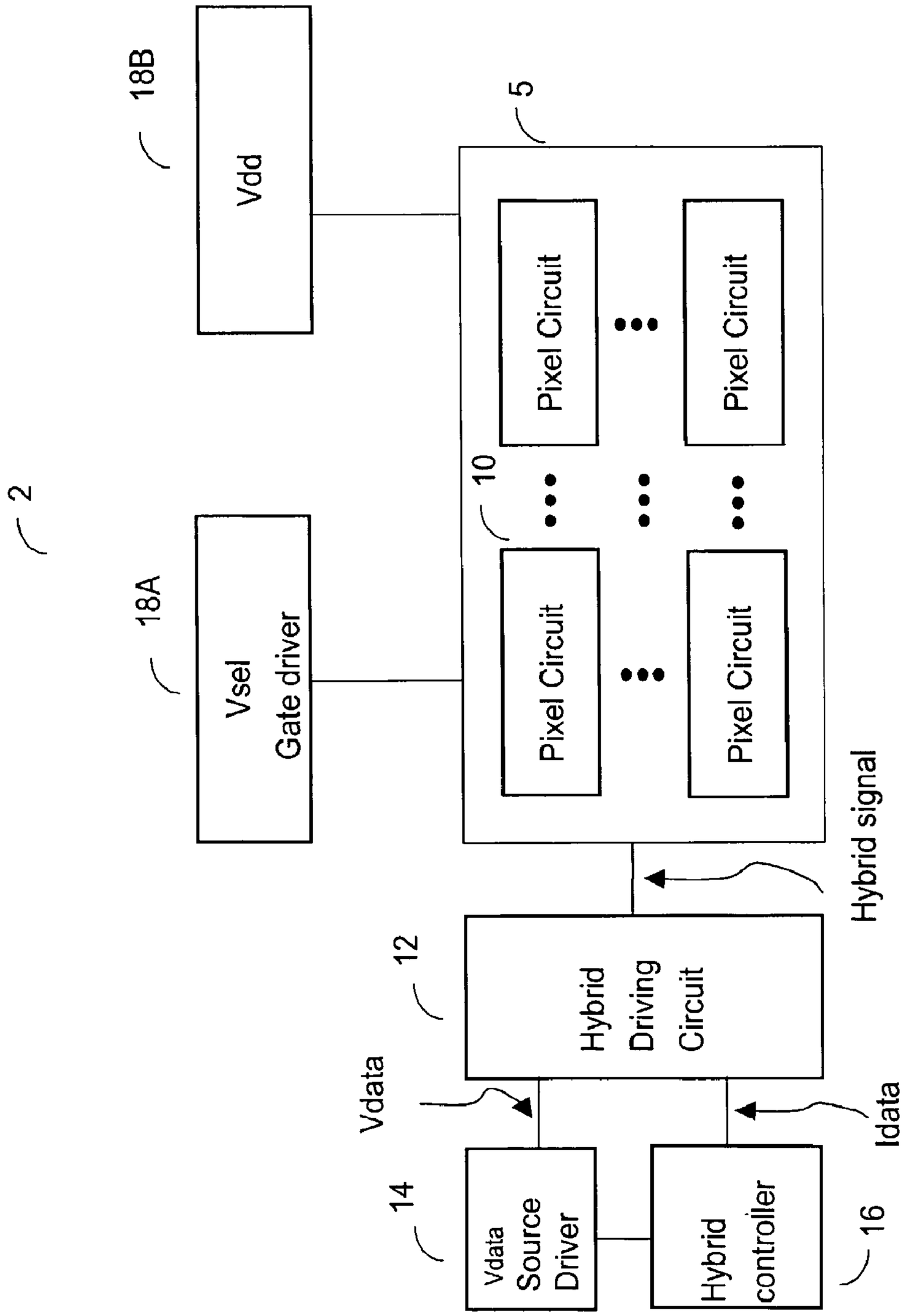
2
18B
Vdd
5
18A
Vsel
Gate driver
10
Pixel Circuit
Pixel Circuit
Pixel Circuit
Pixel Circuit
Hybrid signal
12
Hybrid
Driving
Circuit
Vdata
Idata
14
Vdata
Source
Driver
Hybrid
controller
16

FIG.1

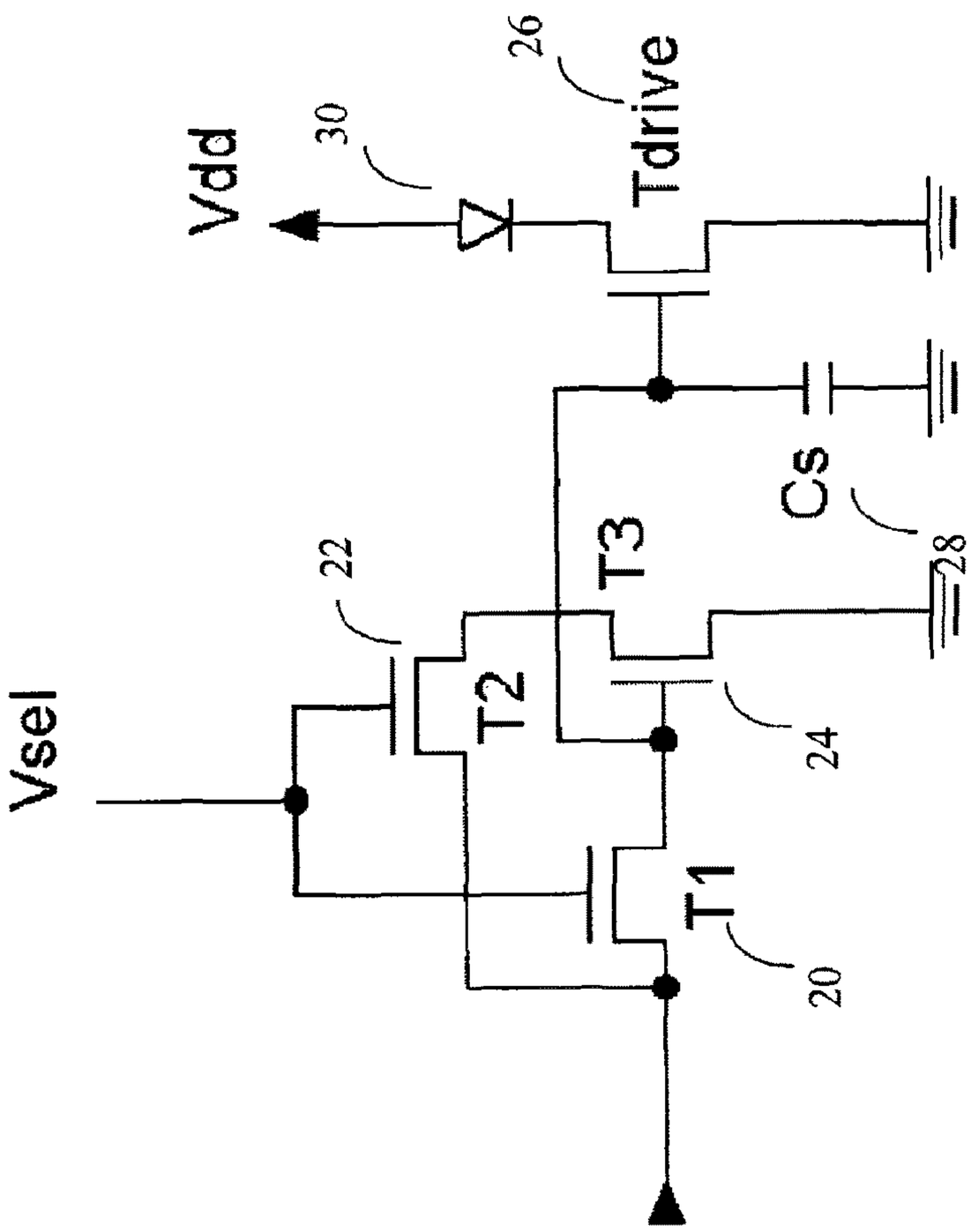

FIG.2

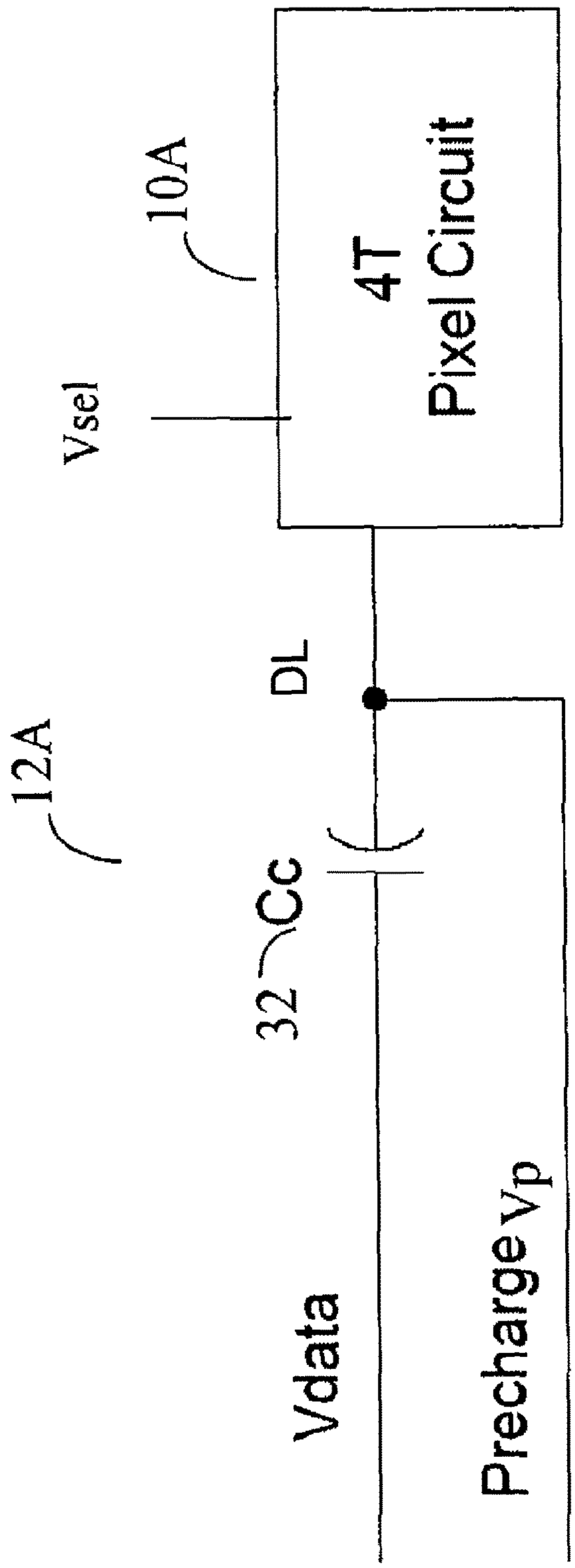

FIG.3

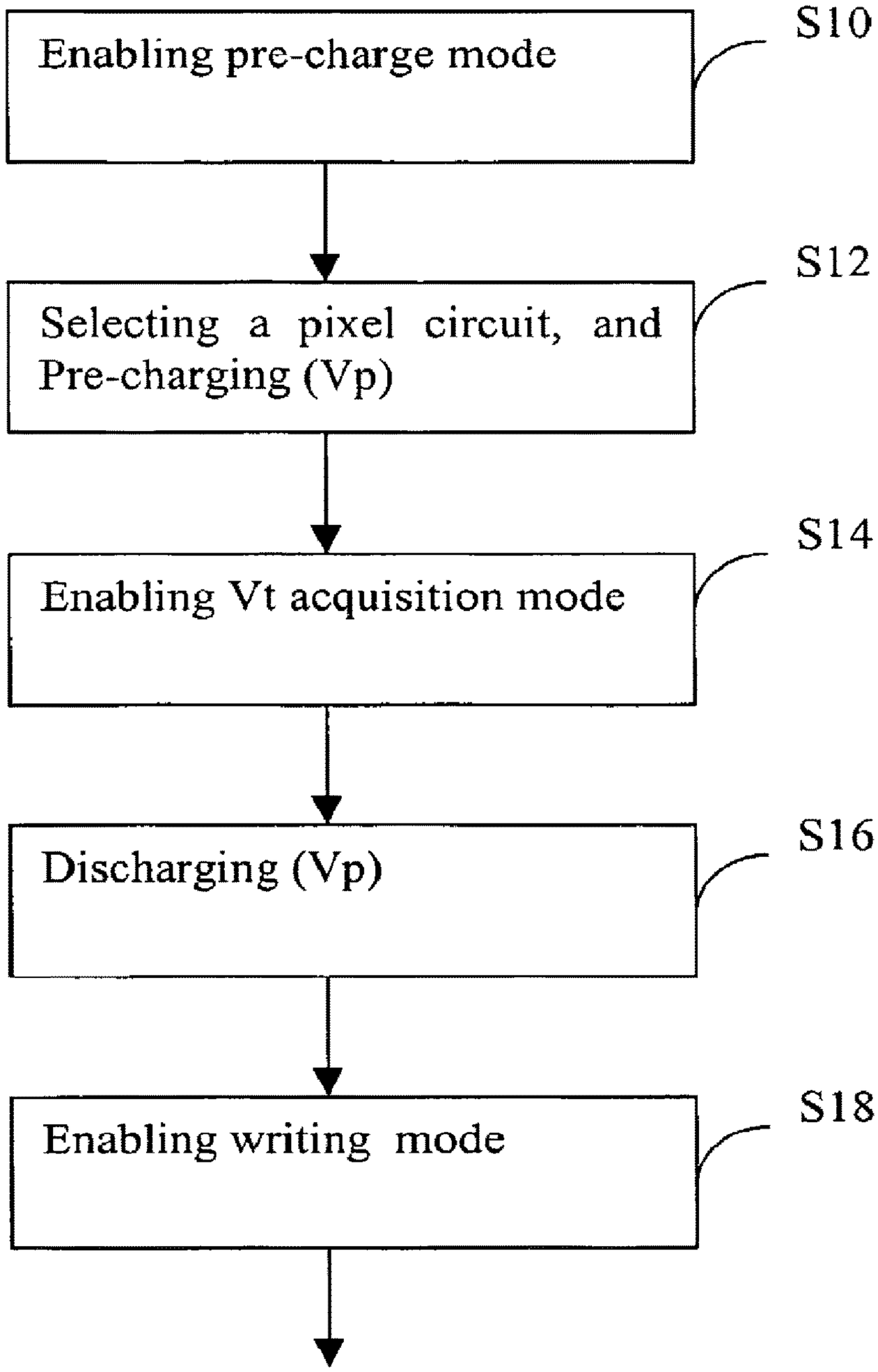
Enabling pre-charge mode
S10
Selecting a pixel circuit, and Pre-charging (Vp)
S12
Enabling Vt acquisition mode
S14
Discharging (Vp)
S16
Enabling writing mode
S18

FIG. 4

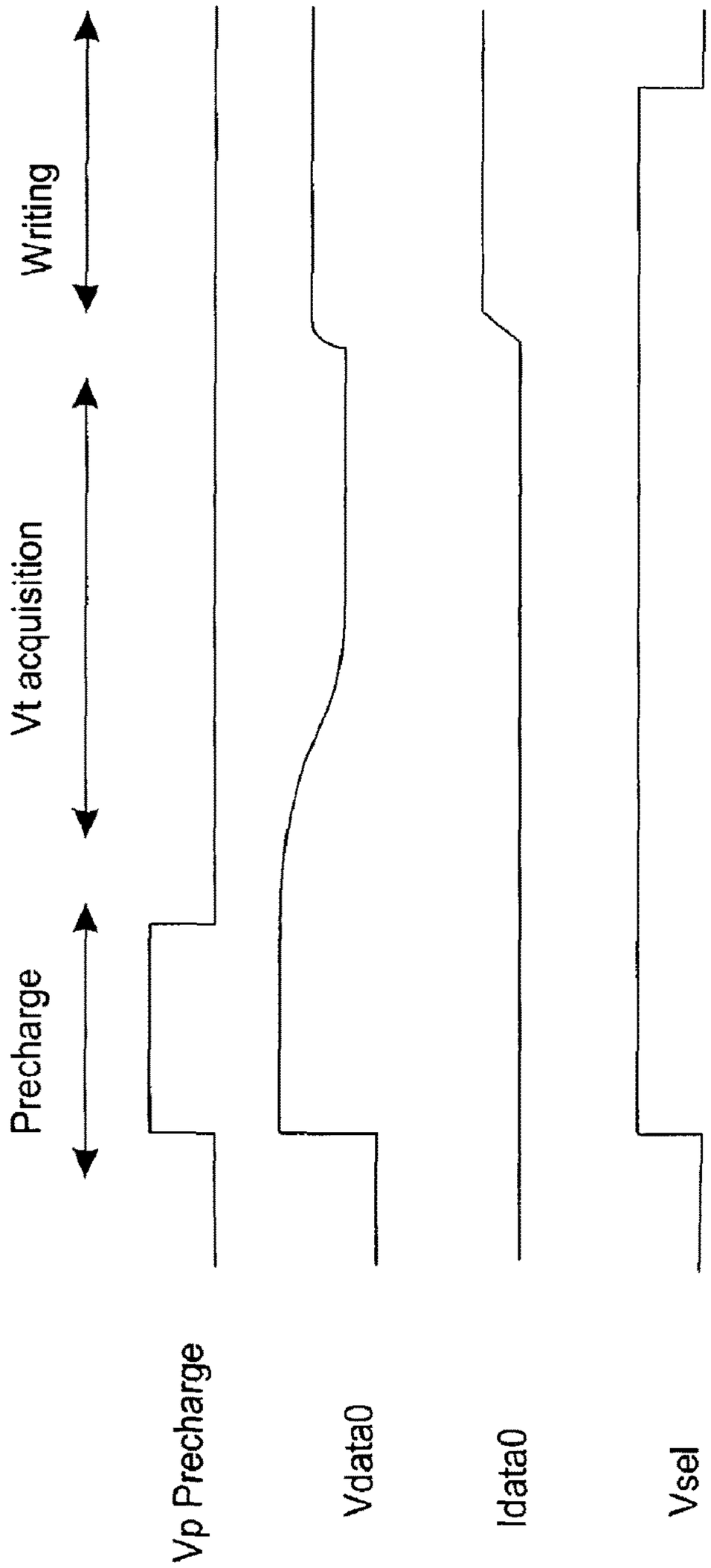
Writing
Vt acquisition
Precharge
Vp Precharge
Vdata0
Idata0
Vsel

FIG.5

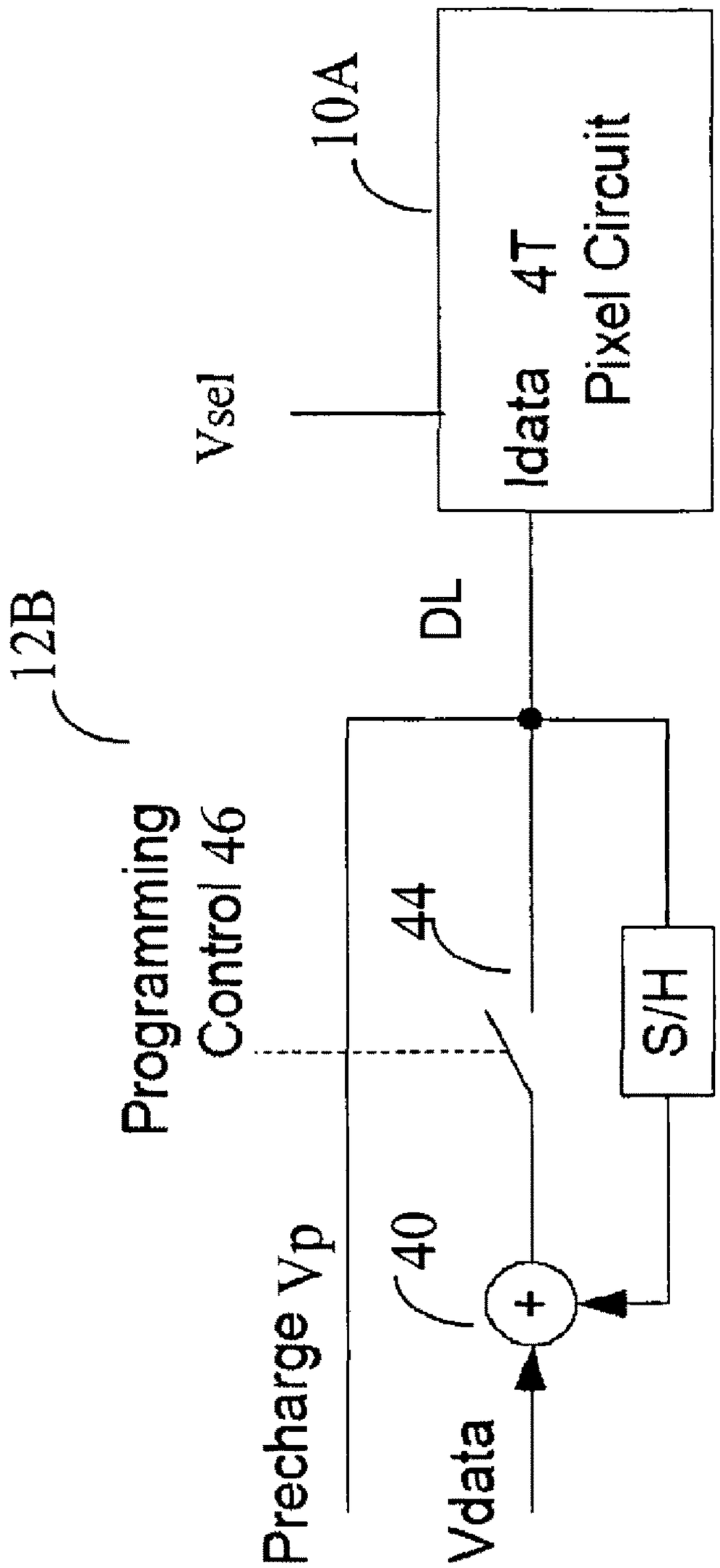
10A
4T Pixel Circuit
Idata
Vsel
DL
12B
Programming Control 46
44
S/H
42
40
+
Vdata
Precharge Vp

FIG.6

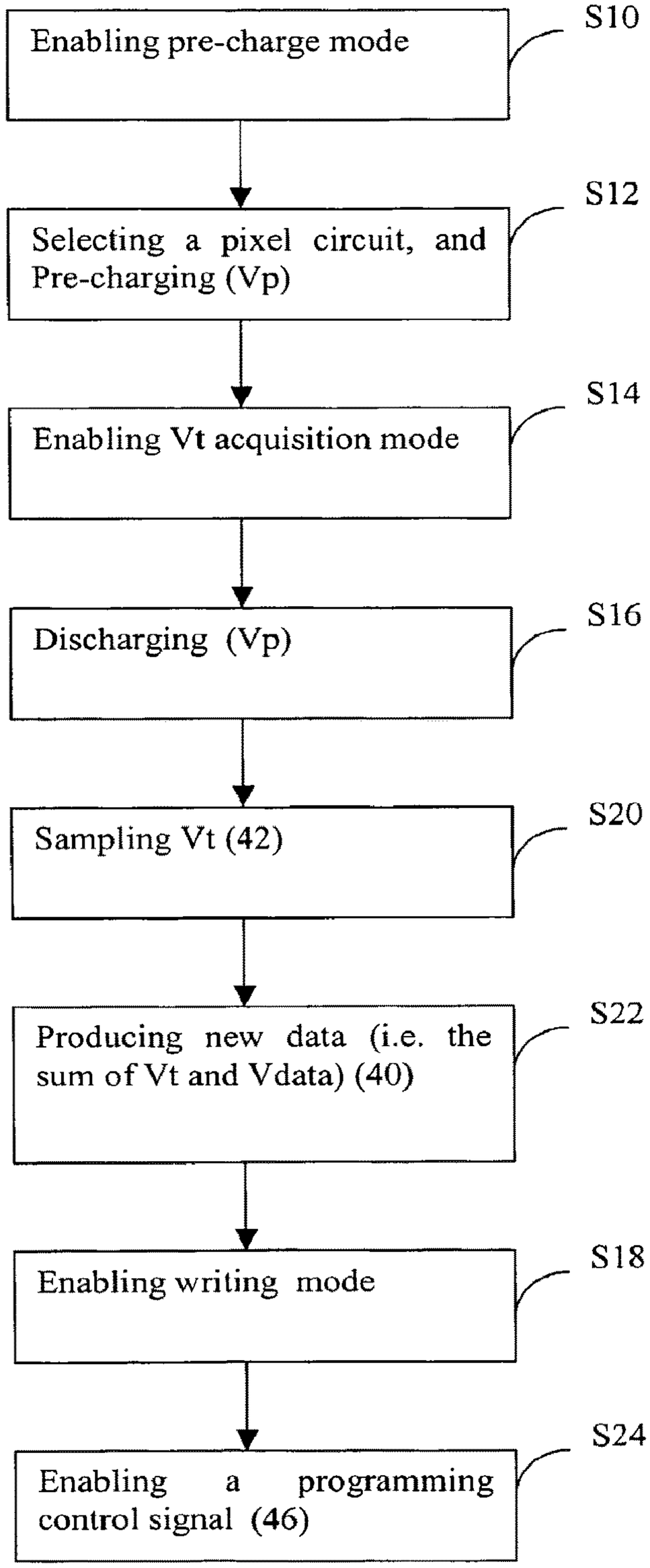
Enabling pre-charge mode
S10
Selecting a pixel circuit, and Pre-charging (Vp)
S12
Enabling Vt acquisition mode
S14
Discharging (Vp)
S16
Sampling Vt (42)
S20
Producing new data (i.e. the sum of Vt and Vdata) (40)
S22
Enabling writing mode
S18
Enabling a programming control signal (46)
S24

FIG. 7

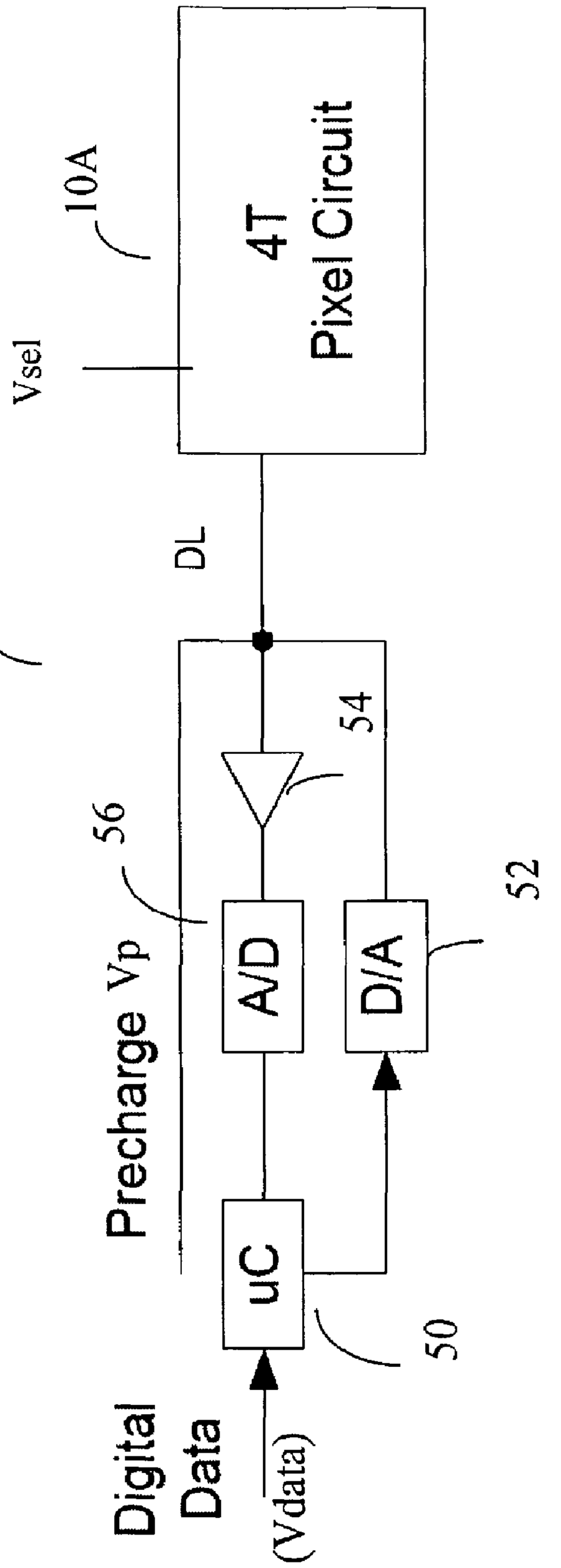
10A
4T
Pixel Circuit
Vsel
12C
DL
54
56
52
Precharge Vp
A/D
D/A
uC
50
Digital
Data
(Vdata)

FIG.8

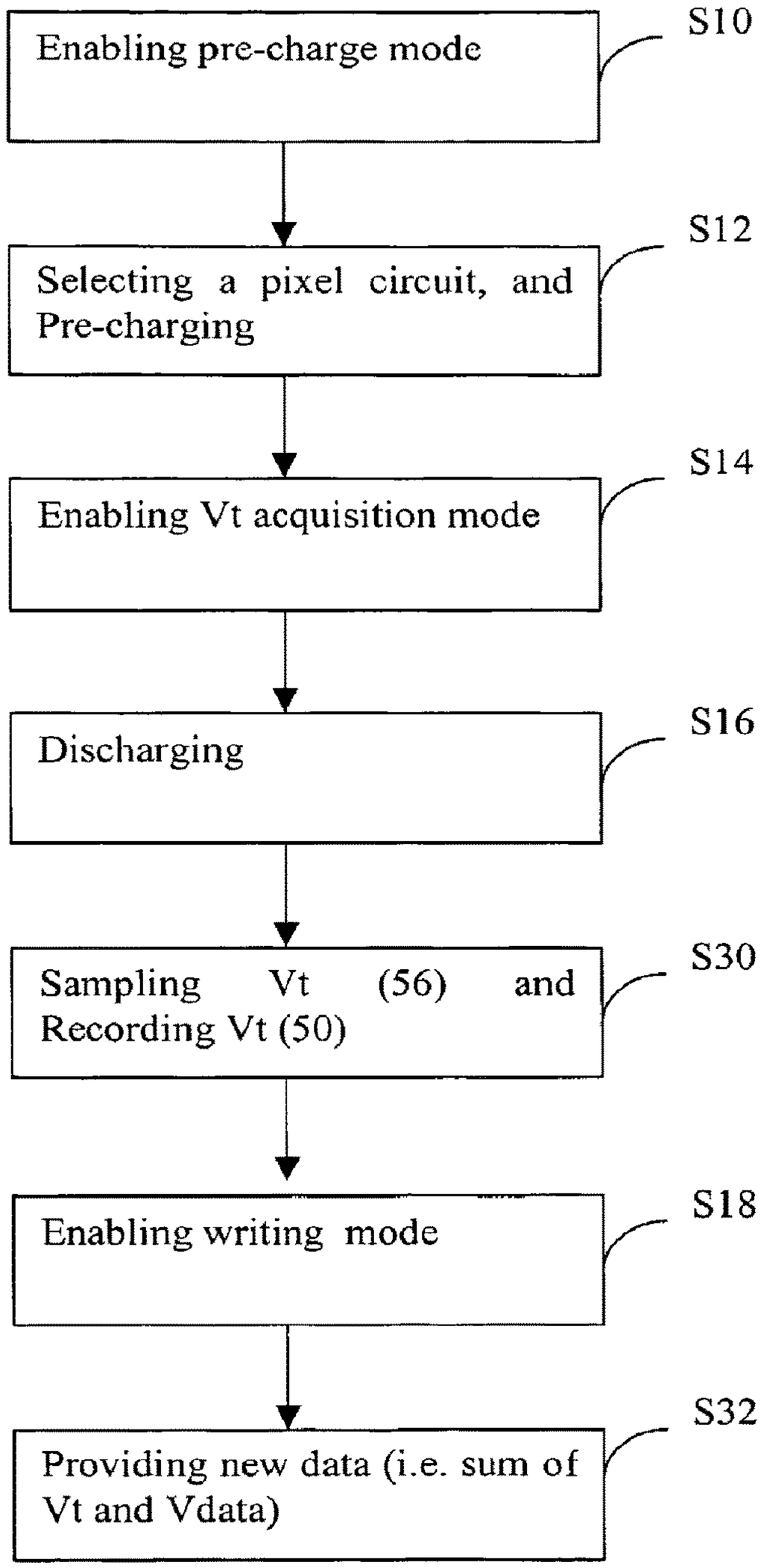
Enabling pre-charge mode
S10
Selecting a pixel circuit, and Pre-charging
S12
Enabling Vt acquisition mode
S14
Discharging
S16
Sampling Vt (56) and Recording Vt (50)
S30
Enabling writing mode
S18
Providing new data (i.e. sum of Vt and Vdata)
S32

FIG. 9

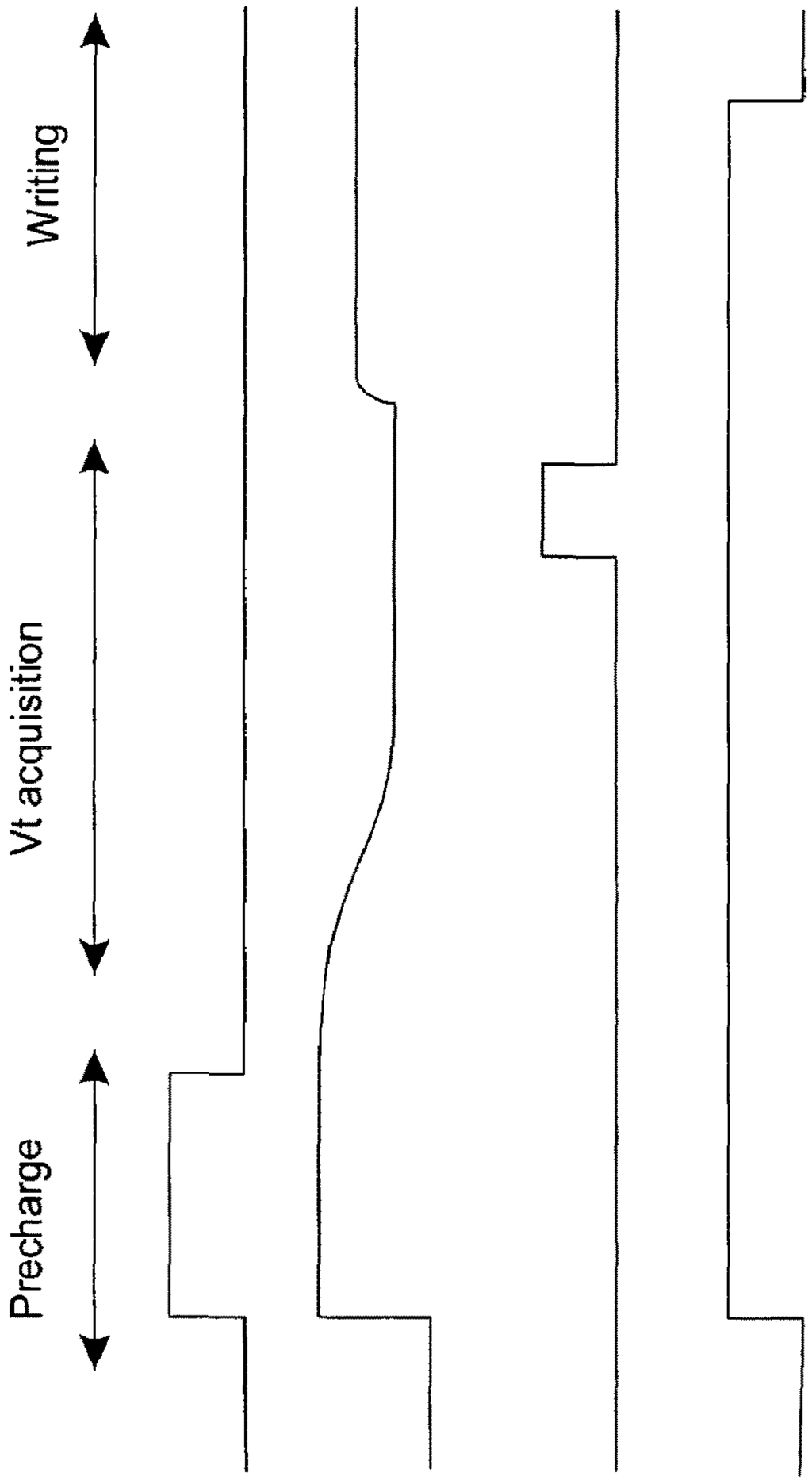
Writing
Vt acquisition
Precharge
Vp Precharge
Vdata0
A/D Sample
Vsel

FIG.10

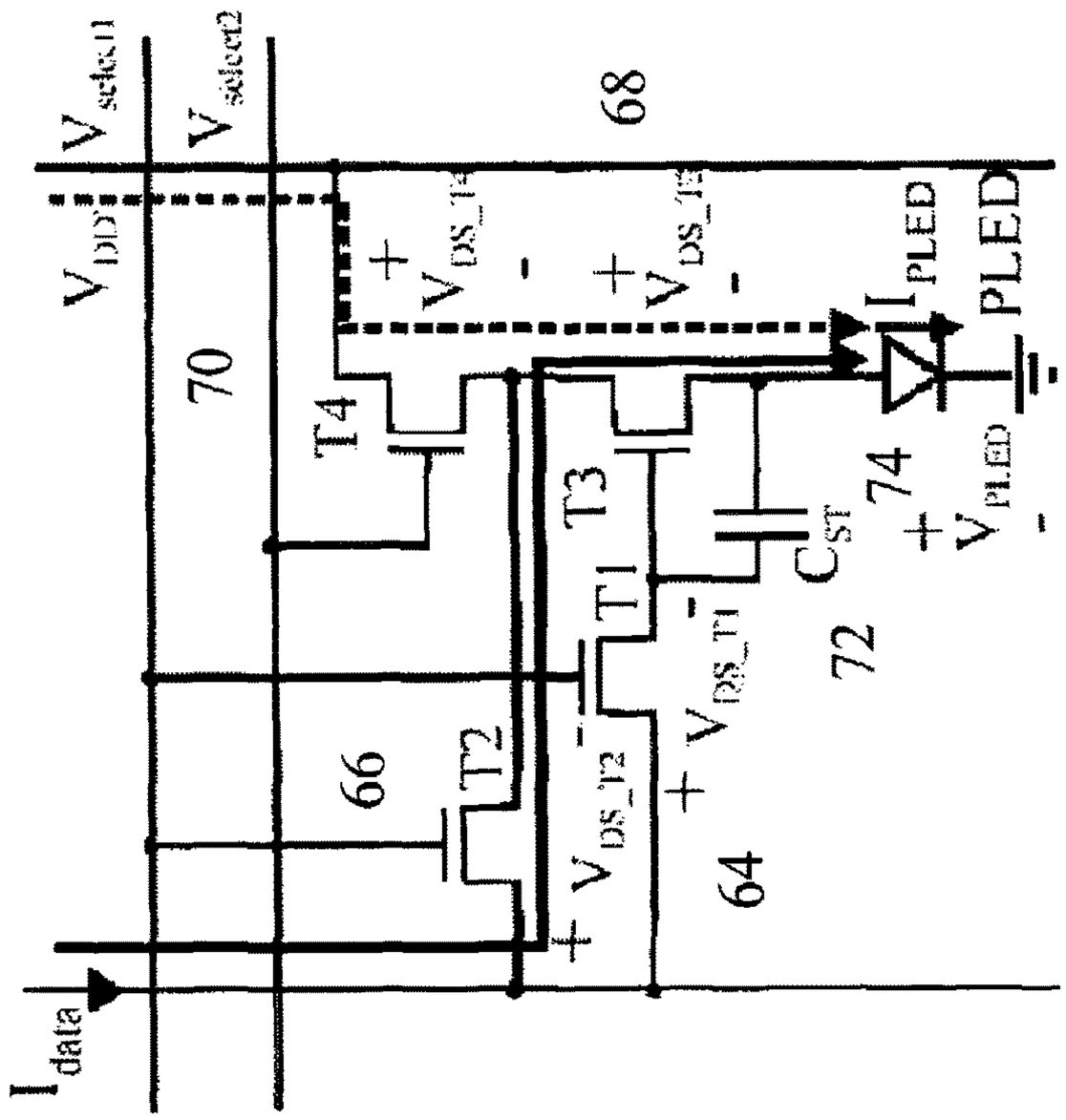
$V_{select1}$
$V_{select2}$
V_{DD}
68
70
V_{DS_T4}
V_{DS_T3}
T4
T3
T2
T1
66
64
72
74
C_{ST}
V_{DS_T2}
V_{DS_T1}
I_{PLED}
V_{PLED}
PLED
I_{data}

FIG.11

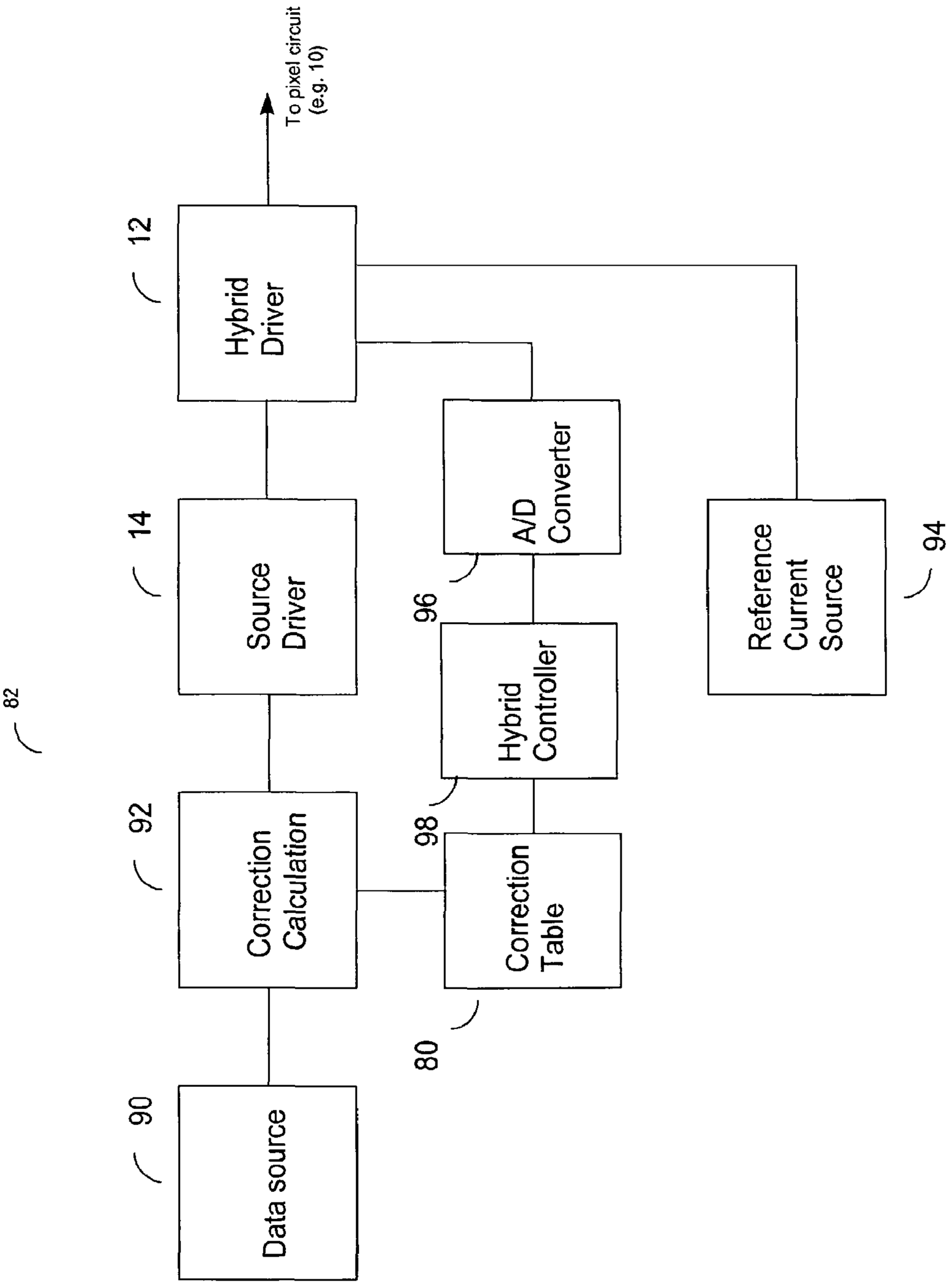
82
To pixel circuit (e.g. 10)
12
Hybrid Driver
14
Source Driver
A/D Converter
96
Hybrid Controller
Reference Current Source
94
92
Correction Calculation
98
Correction Table
80
90
Data source

FIG. 12

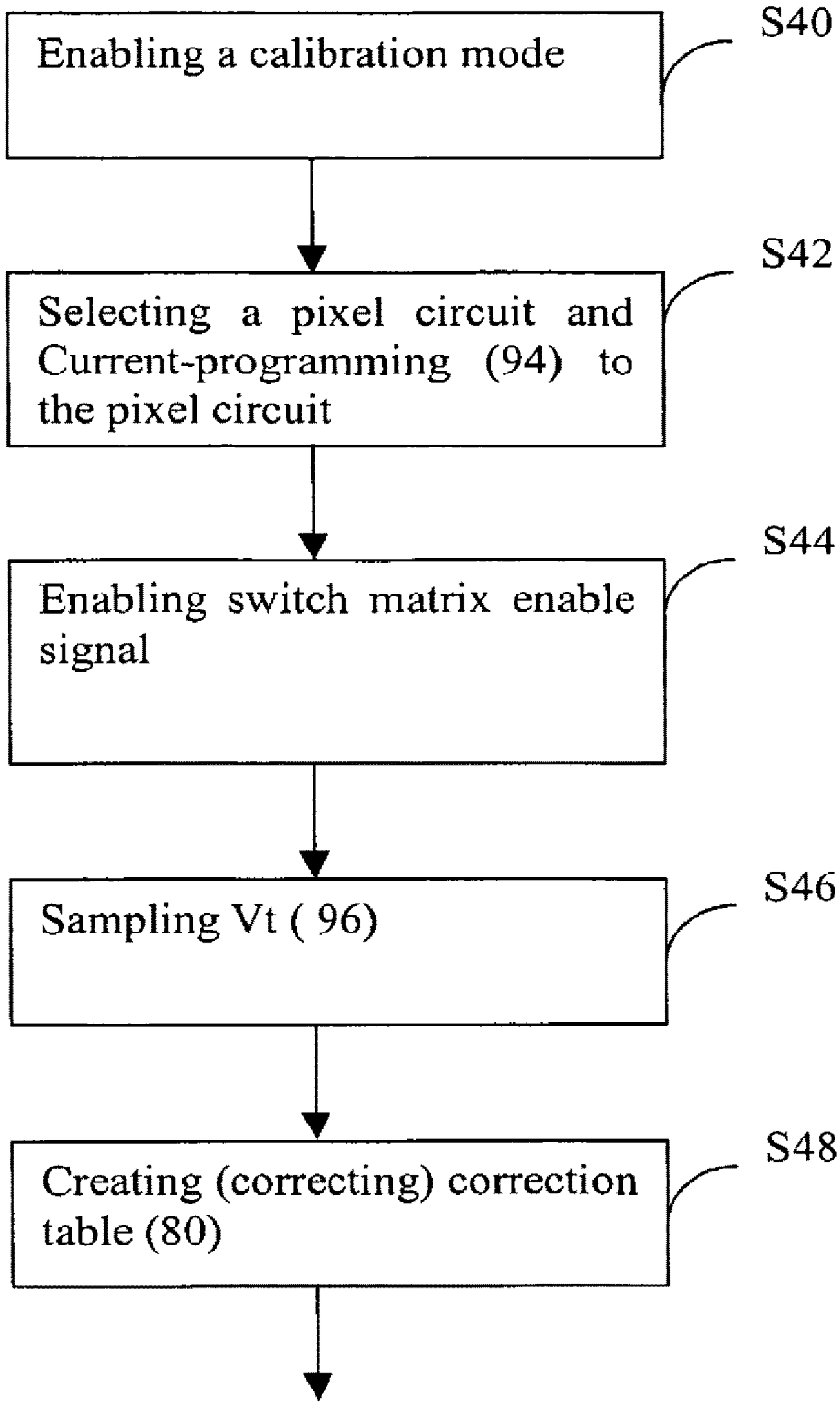
Enabling a calibration mode
S40
Selecting a pixel circuit and Current-programming (94) to the pixel circuit
S42
Enabling switch matrix enable signal
S44
Sampling Vt (96)
S46
Creating (correcting) correction table (80)
S48

FIG. 13

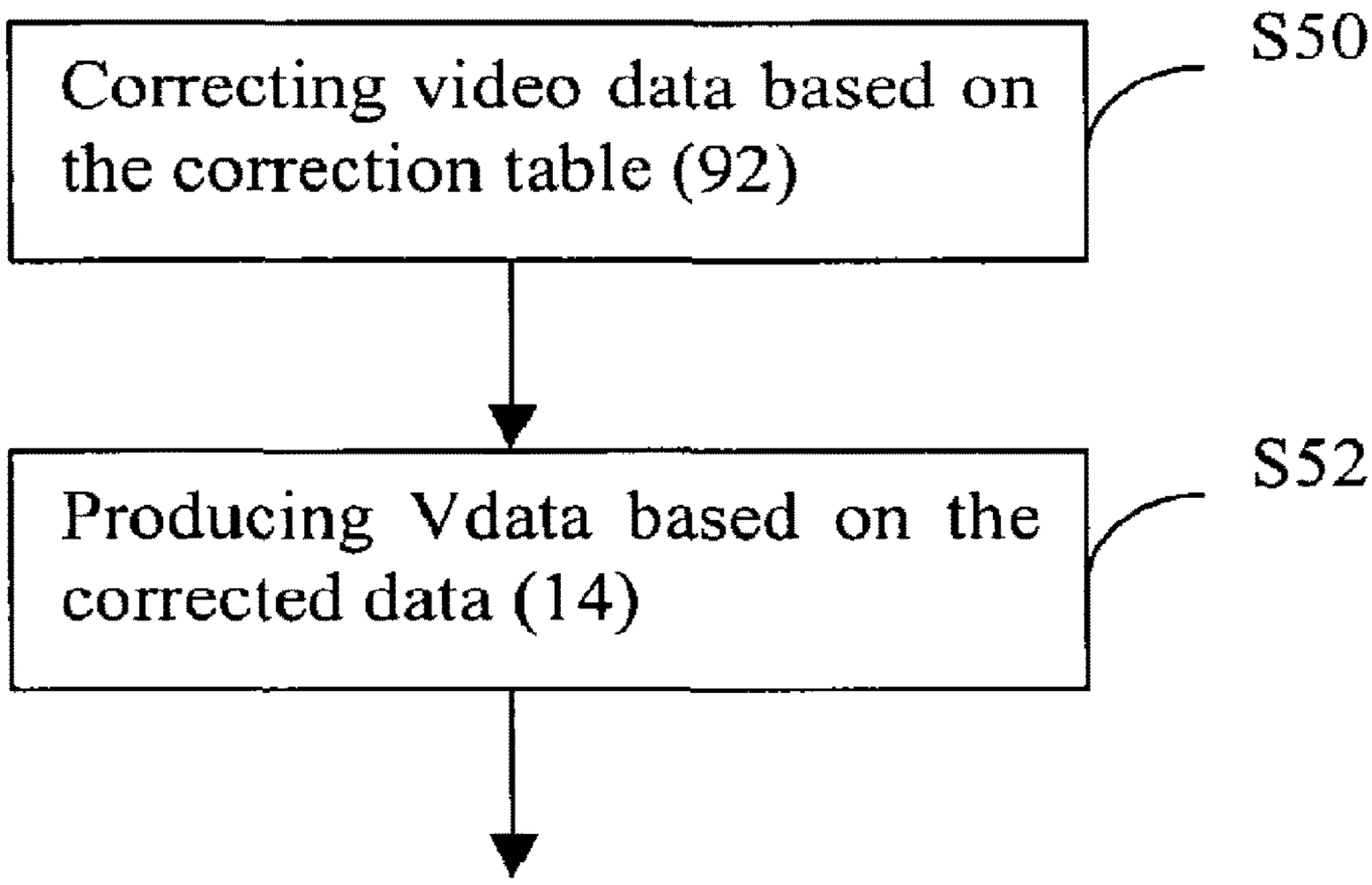
Correcting video data based on the correction table (92)
S50
Producing Vdata based on the corrected data (14)
S52

FIG. 14

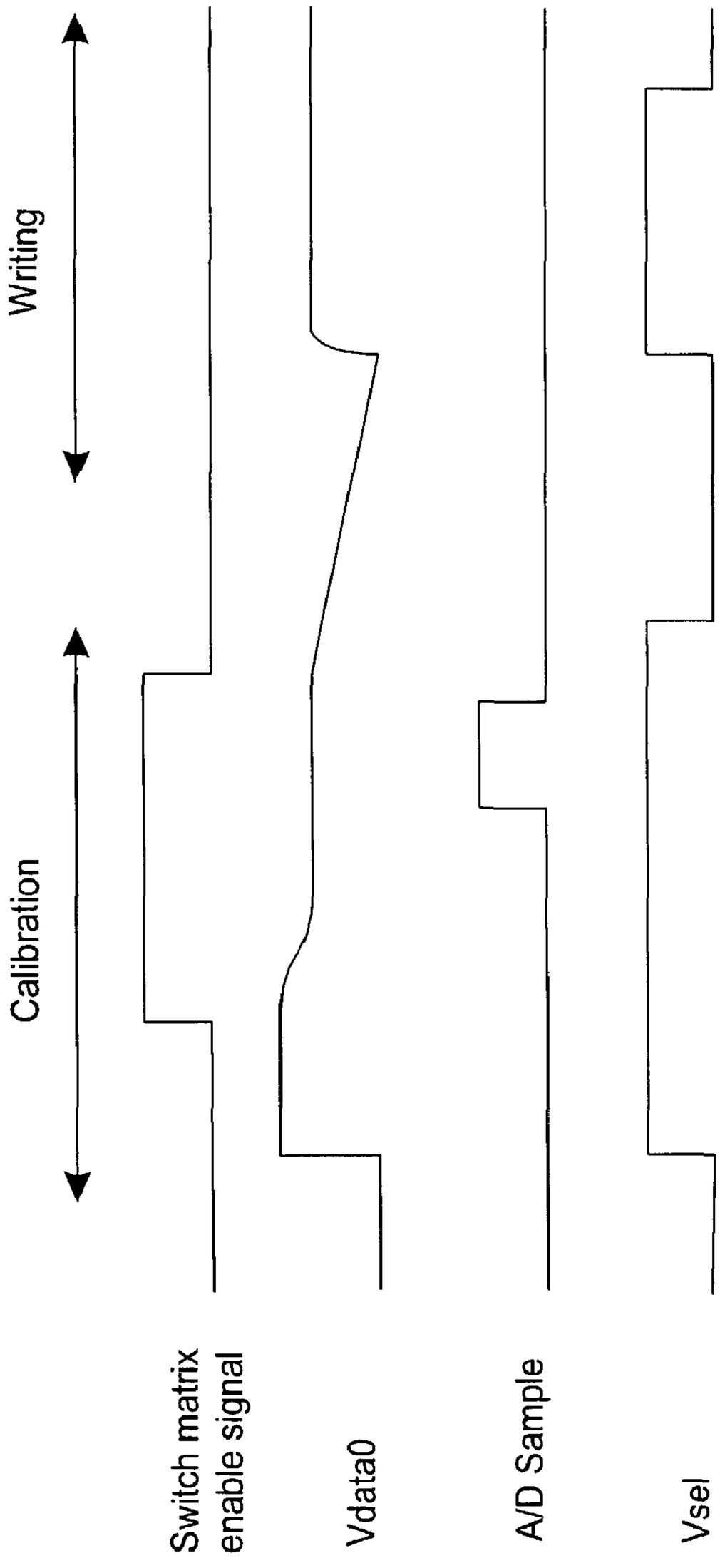
Writing
Calibration
Switch matrix enable signal
Vdata0
A/D Sample
Vsel

FIG. 15

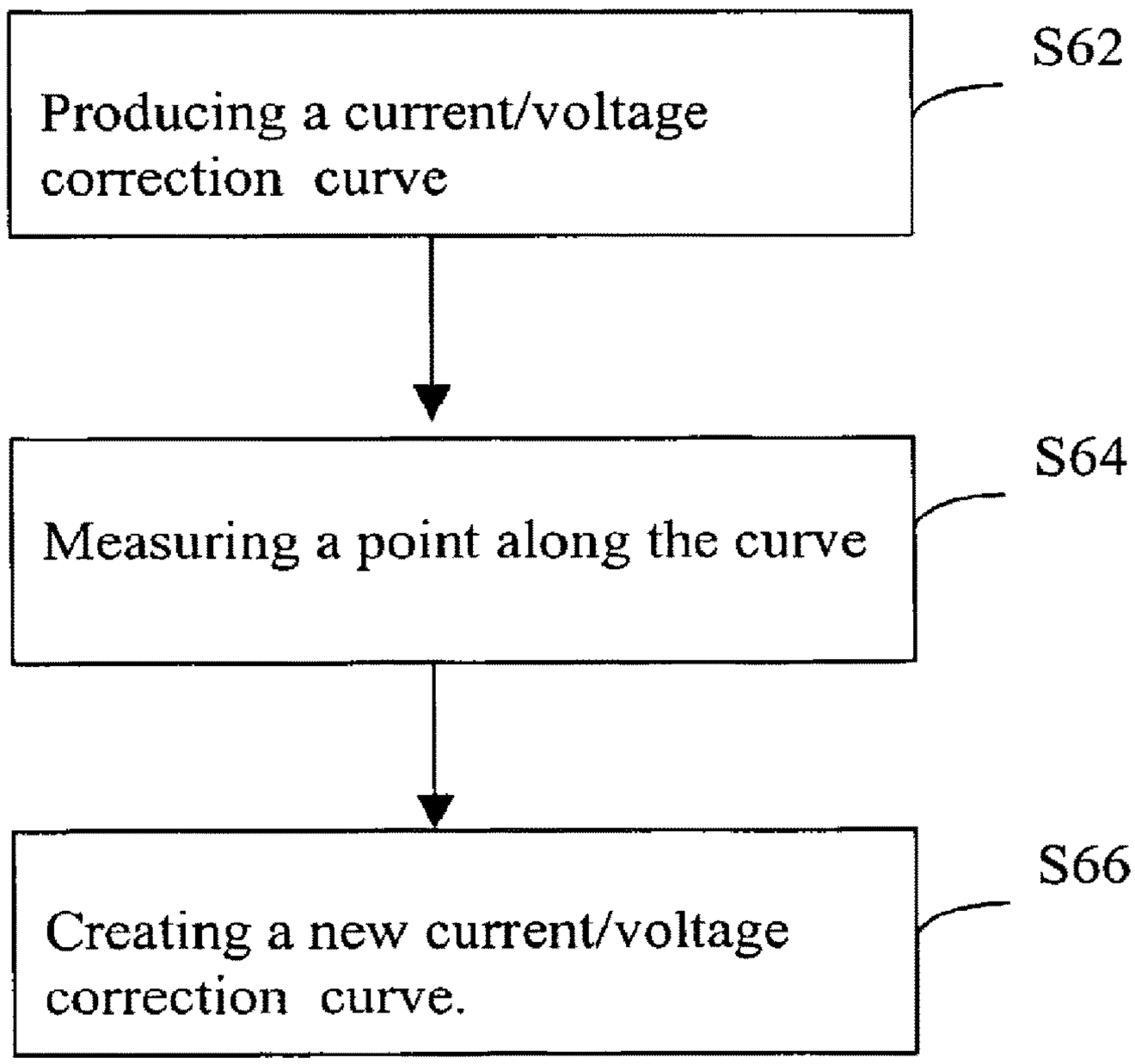
Producing a current/voltage correction curve
S62
Measuring a point along the curve
S64
Creating a new current/voltage correction curve.
S66

FIG.16

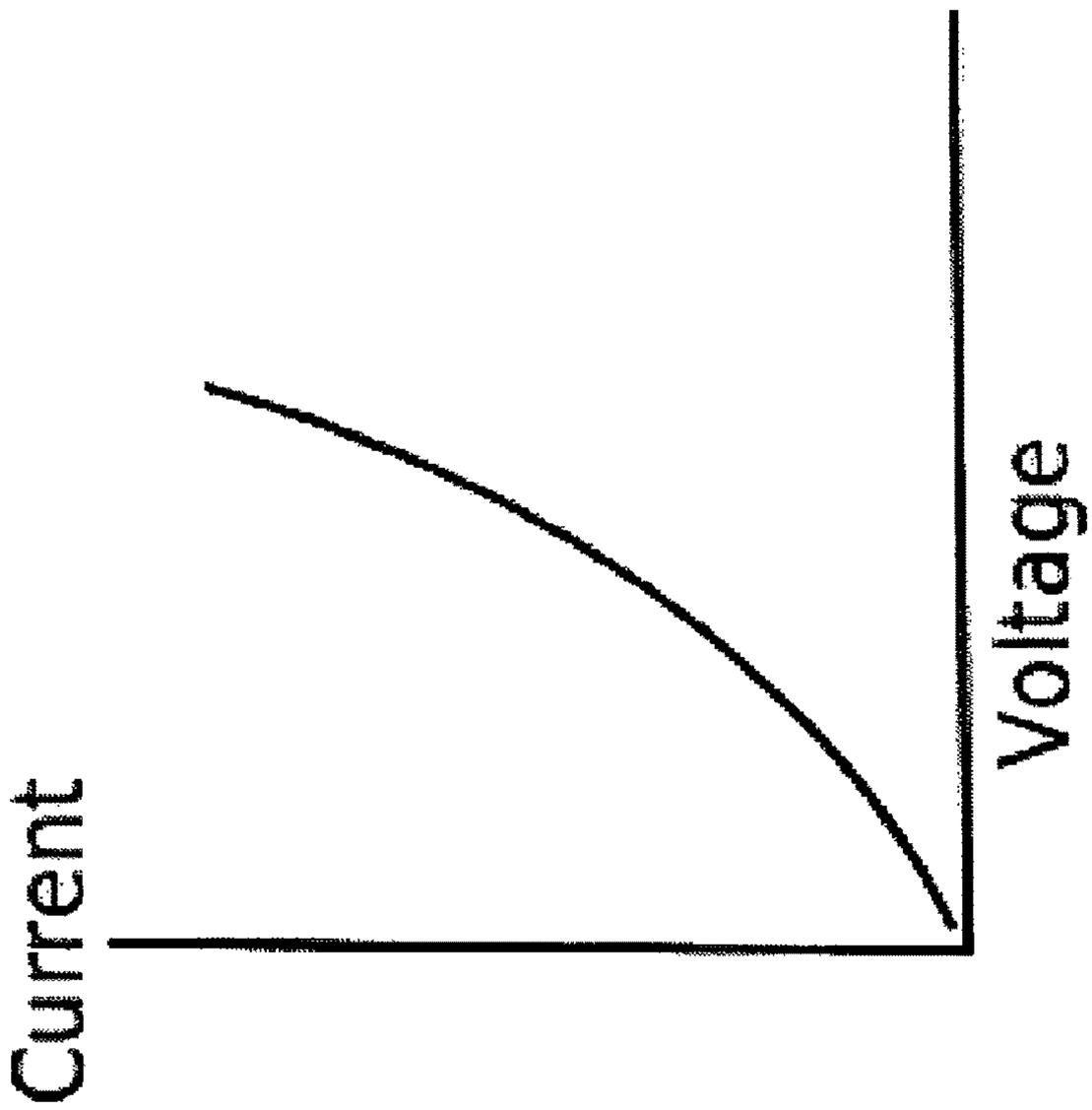

FIG. 17

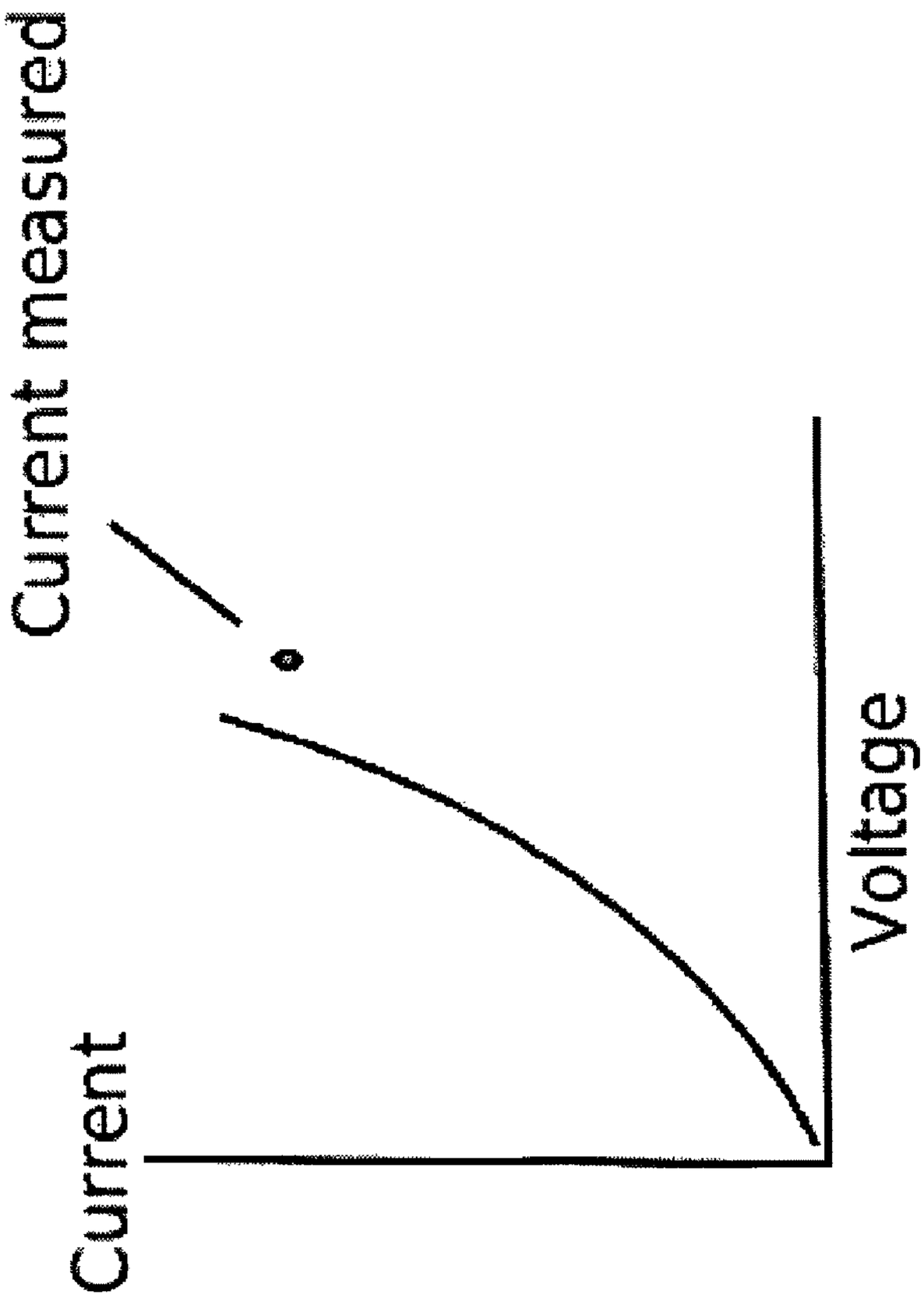

FIG. 18

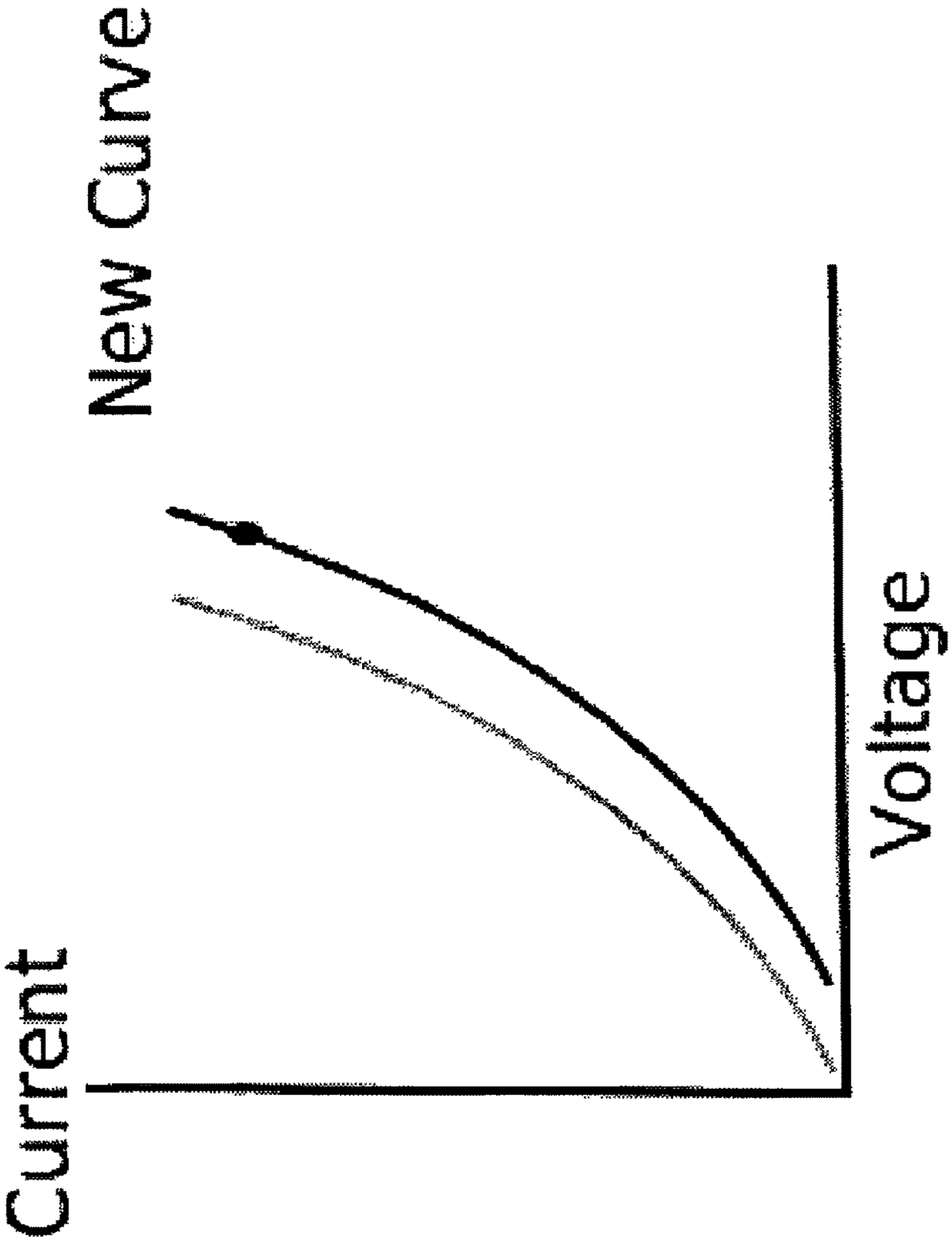

FIG. 19

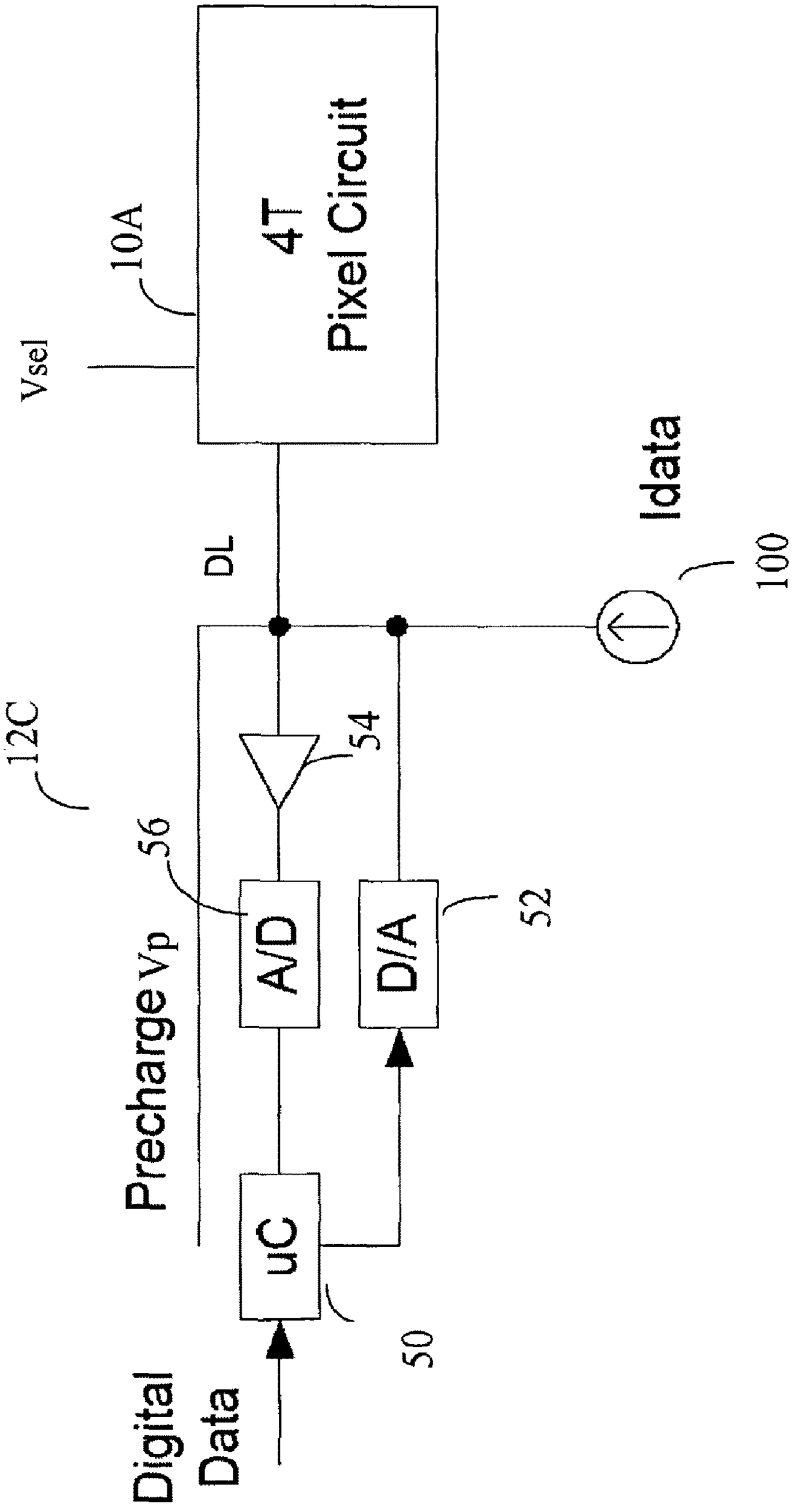
Vsel
10A
4T
Pixel Circuit
DL
Idata
100
12C
54
56
A/D
D/A
52
Precharge Vp
uC
Digital
Data
50

FIG. 20

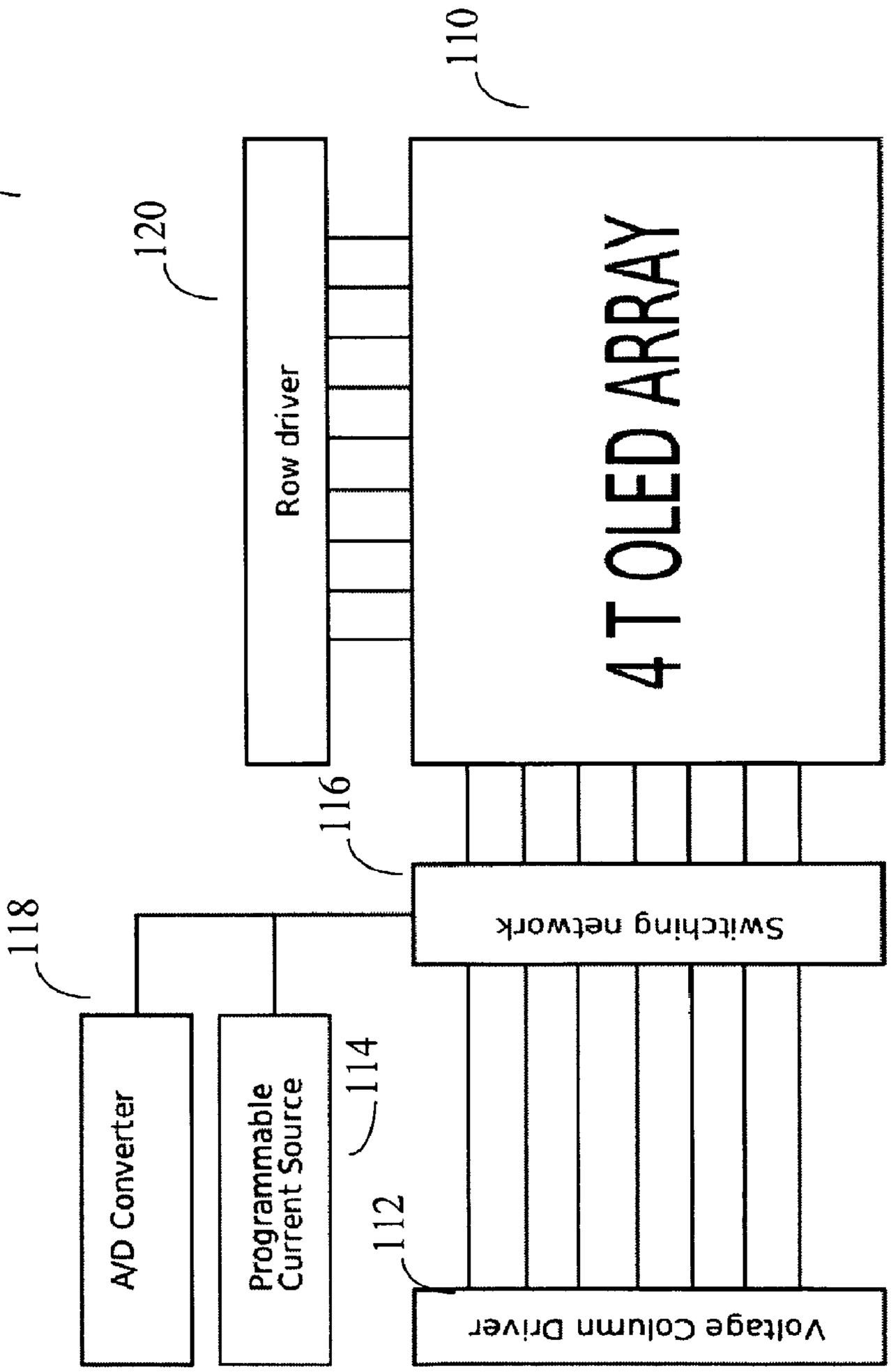
105
110
120
Row driver
4 T OLED ARRAY
116
Switching network
118
A/D Converter
Programmable Current Source
114
112
Voltage Column Driver

FIG. 21

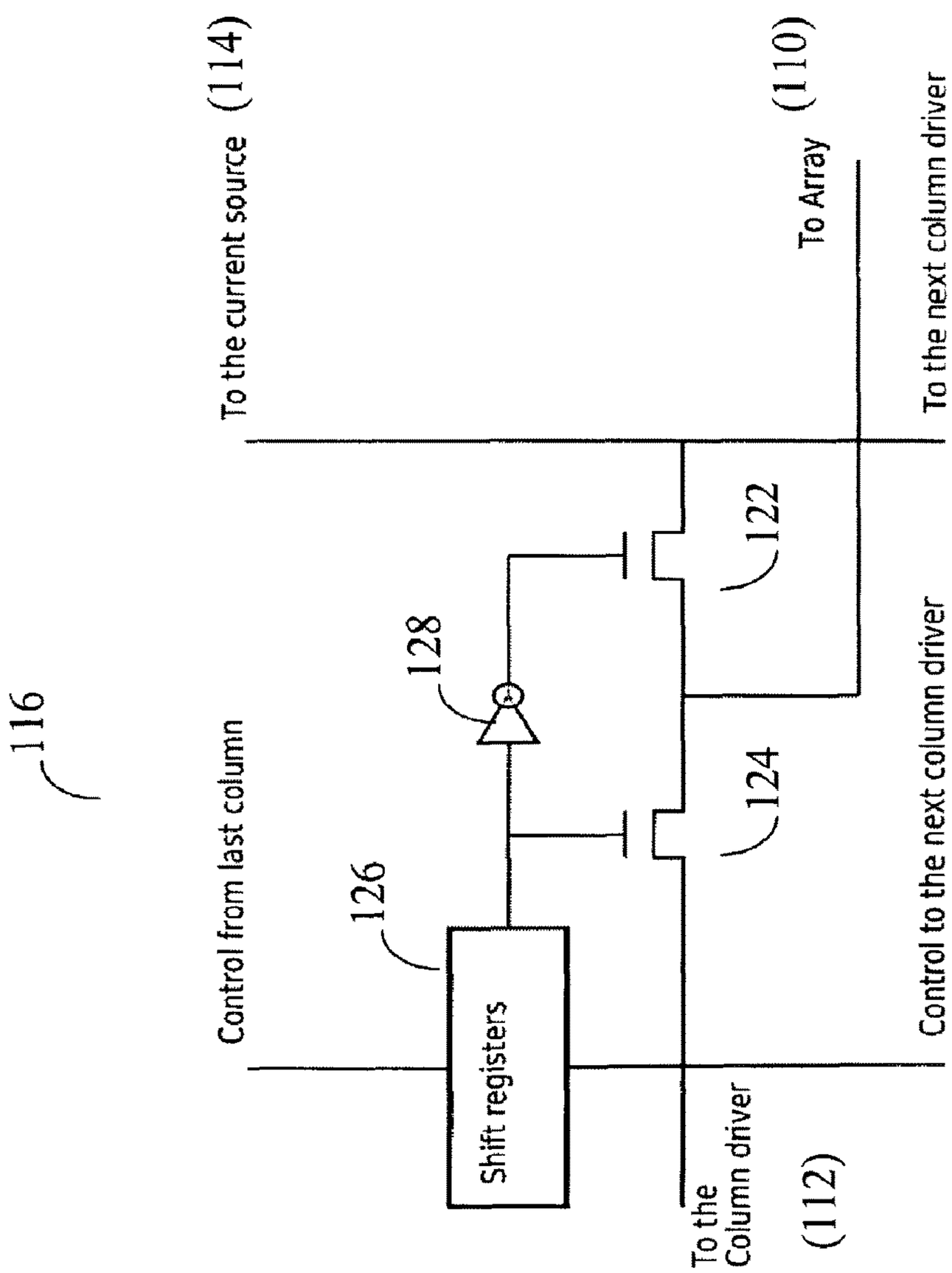
116
(114)
(110)
To the current source
To Array
To the next column driver
To the next column d
From last column
128
126
122
124
Shift registers
Control from
Control to th
To the
Column driver
(112)

FIG. 22

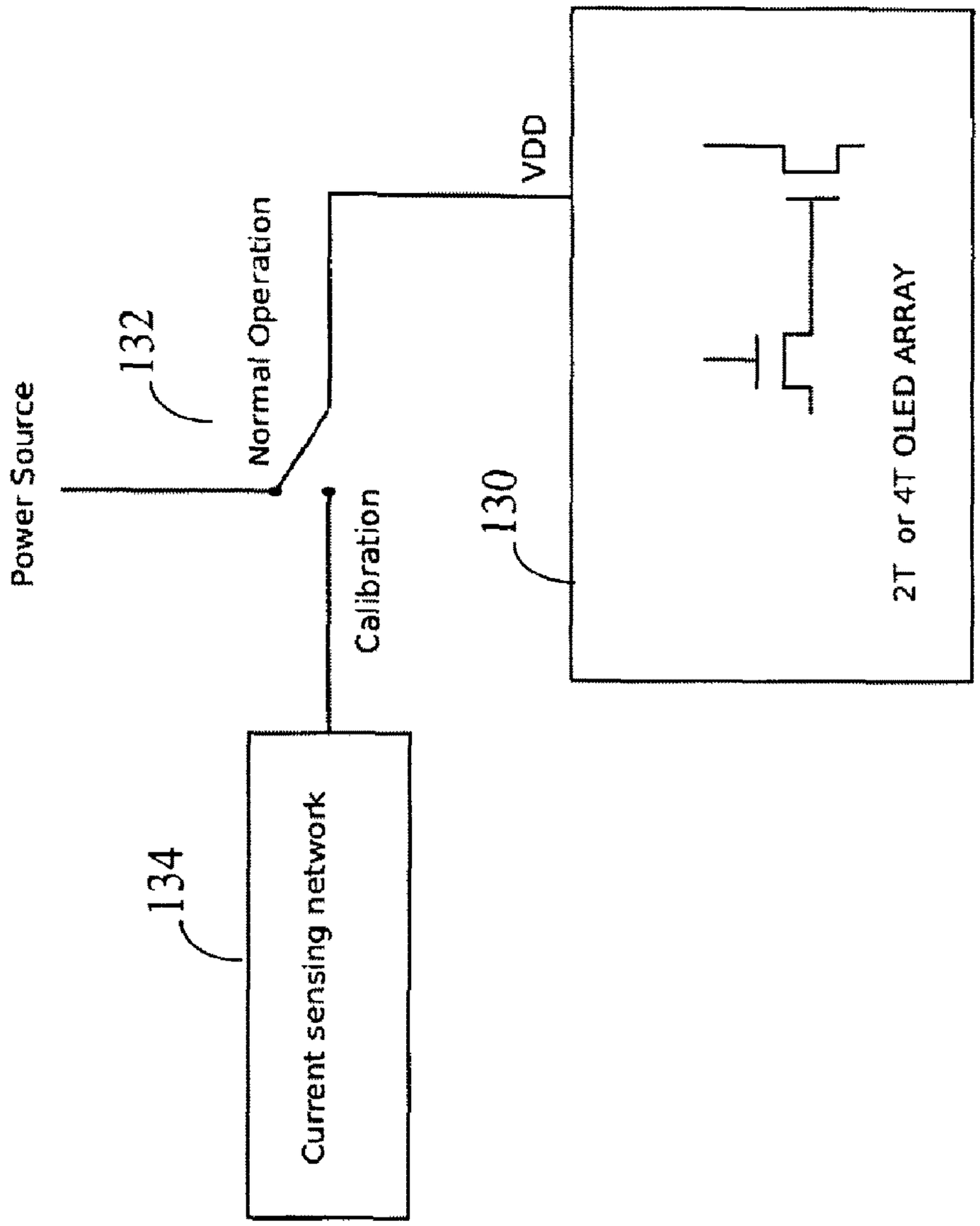
Power Source
132
Normal Operation
Calibration
130
VDD
2T or 4T OLED ARRAY
134
Current sensing network

FIG. 23

VOLTAGE-PROGRAMMING SCHEME FOR CURRENT-DRIVEN AMOLED DISPLAYS

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue; a claim printed with strikethrough indicates that the claim was canceled, disclaimed, or held invalid by a prior post-patent action or proceeding.

Notice: More than one reissue application has been filed for the reissue of U.S. Pat. No. 8,232,939. The reissue applications are (1) Ser. No. 14/090,320, which is an application for reissue of U.S. Pat. No. 8,232,939 and has been reissued as U.S. Pat. No. RE45,291 E, (2) application Ser. No. 14/326,705 (the present application), which is a continuation reissue of U.S. Pat. No. 8,232,939, and (3) application Ser. No. 14/326,677, which is a divisional reissue of U.S. Pat. No. 8,232,939.

CROSS REFERENCE TO RELATED APPLICATIONS

This is a continuation of U.S. patent application Ser. No. 11/571,480, which is a national stage application of international application no. PCT/CA2005/001007, filed Jun. 28, 2005, which claims the benefit of and priority to Canadian Patent Application No. 2,472,671, filed on Jun. 29, 2004, each of these applications being incorporated herein by reference in its entirety.

FIELD OF INVENTION

The present invention relates to a display technique, and more specifically to technology for driving pixel circuits.

BACKGROUND OF THE INVENTION

Active matrix organic light emitting diode (AMOLED) displays are well known in the art. The AMOLED displays have been increasingly used as a flat panel in a wide variety of tools.

The AMOLED displays are classified as either a voltage-programmed display or a current-programmed display. The voltage-programmed display is driven by a voltage-programmed scheme where data is applied to the display as a voltage. The current-programmed display is driven by a current-programmed scheme where data is applied to the display as a current.

The advantage of the current-programming scheme is that it can facilitate pixel designs where the brightness of the pixel remains more constant over time than with voltage programming. However, the current-programming requires longer time of charging capacitors associated with the column.

Therefore, there is a need to provide a new scheme for driving a current-driven AMOLED display, which ensures high speed and high quality.

SUMMARY OF THE INVENTION

The present invention relates to a system and method of driving a pixel circuit in an AMOLED display.

The system and method of the present invention uses Voltage-Programming Scheme For Current-Driven AMOLED Displays.

In accordance with an aspect of the present invention there is provided a system for driving a display which includes a plurality of pixel circuits, each having a plurality of thin film transistors (TFTs) and an organic light emitting diode (OLED), which includes: a voltage driver for generating a voltage to program the pixel circuit; a programmable current source for generating a current to program the pixel circuit; and a switching network for selectively connecting the data driver or the current source to one or more pixel circuits.

In accordance with a further aspect of the present invention there is provided a system for driving a pixel circuit having a plurality of thin film transistors (TFTs) and an organic light emitting diode (OLED), which includes: a pre-charge controller for pre-charging and discharging a data node of the pixel circuit to acquire threshold voltage information of the TFT from the data node; and a hybrid driving circuit for programming the pixel circuit based on the acquired threshold voltage information and video data information displayed on the pixel circuit.

In accordance with a further aspect of the present invention there is provided a system for driving a pixel circuit having a plurality of thin film transistors (TFTs) and an organic light emitting diode (OLED), which includes: a sampler for sampling, from a data node of the pixel circuit, a voltage required to program the pixel circuit; and a programming circuit for programming the pixel circuit based on the sampled voltage and video data information displayed on the pixel circuit.

In accordance with a further aspect of the present invention there is provided a method of driving a pixel circuit having a plurality of thin film transistors (TFTs) and an organic light emitting diode (OLED), which includes the steps of: selecting a pixel circuit and pre-charging a data node of the pixel circuit; allowing the pre-charged data node to be discharged; extracting a threshold voltage of the TFT through the discharging step; and programming the pixel circuit, including compensating a programming data based on the extracted threshold voltage.

This summary of the invention does not necessarily describe all features of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features of the invention will become more apparent from the following description in which reference is made to the appended drawings wherein:

FIG. **1** is a block diagram showing a system for driving an AMOLED display in accordance with an embodiment of the present invention;

FIG. **2** is a schematic diagram showing one example of a pixel circuit of FIG. **1**;

FIG. **3** is a schematic diagram showing an example of a hybrid driving circuit, which is applicable to FIG. **1**;

FIG. **4** is an exemplary flow chart for showing the operation of the hybrid driving circuit of FIG. **3**;

FIG. **5** is an exemplary timing chart for showing the operation of the hybrid driving circuit of FIG. **3**;

FIG. **6** is a schematic diagram showing a further example of a hybrid driving circuit, which is applicable to FIG. **1**;

FIG. **7** is an exemplary flow chart for showing the operation of the hybrid driving circuit of FIG. **6**;

FIG. **8** is a schematic diagram showing a further example of a hybrid driving circuit, which is applicable to FIG. **1**;

FIG. **9** is an exemplary flow chart for showing the operation of the hybrid driving circuit of FIG. **8**;

FIG. **10** is an exemplary timing chart for showing the operation of the hybrid driving circuit of FIG. **8**;

FIG. **11** is a schematic diagram showing a further example of the pixel circuit of FIG. **1**;

FIG. **12** is a block diagram showing a system for driving an AMOLED display in accordance with a further embodiment of the present invention;

FIG. **13** is an exemplary flow chart for showing the operation of the system of FIG. **12**;

FIG. **14** is an exemplary flow chart for showing the operation of the system of FIG. **12**;

FIG. **15** is an exemplary timing chart for showing the operation of the system of FIG. **12**;

FIG. **16** is an exemplary flow chart for a hidden refresh operation of the system of FIG. **12**;

FIG. **17** is a diagram showing an example of a sample of the current/voltage correction curve;

FIG. **18** is a diagram showing the current/voltage correction curve of FIG. **17** and an example of a newly measured data point:

FIG. **19** is a diagram showing an example of a new current/voltage correction curve based on the measured point of FIG. **18**;

FIG. **20** is a block diagram showing a further example of a programming circuit for implementing a combined current and voltage-programming technique;

FIG. **21** is a block diagram showing a system for driving an AMOLED display in accordance with a further embodiment of the invention;

FIG. **22** is a schematic diagram showing an example of a switch network of FIG. **21**; and

FIG. **23** is a schematic diagram showing a system for correcting the current/voltage information of the pixel circuit.

DETAILED DESCRIPTION

Embodiments of the present invention are described using an AMOLED display. Drive scheme described below is applicable to a current programmed (driven) pixel circuit and a voltage programmed (driven) pixel circuit.

In addition, hybrid technique described below can be applied to any existing driving scheme, including a) any drive schemes that use sophisticated timing of the data, select, or power inputs to the pixels to achieve increased brightness uniformity, b) any drive schemes that use current or voltage feedback, c) any drive schemes that use optical feedback.

The light emitting material of the pixel circuit can be any technology, specifically organic light emitting diode (OLED) technology, and in particular, but not limited to, fluorescent, phosphorescent, polymer, and dendrimer materials.

Referring to FIG. **1**, there is illustrated a system **2** for driving an AMOLED display **5** in accordance with an embodiment of the present invention. The AMOLED display **5** includes a plurality of pixel circuits. In FIG. **1**, four pixel circuits **10** are shown as an example.

The system **2** includes a hybrid driving circuit **12**, a voltage source driver **14**, a hybrid programming controller **16**, a gate driver **18**A and a power-supply **18**B. The pixel circuit **10** is selected by the gate driver **18**A (Vsel), and is programmed by either voltage mode using a node Vdata or current mode using a node Idata. The hybrid driving circuit **12** selects the mode of programming, and connects it to the pixel circuit **10** through a hybrid signal. A pre-charge signal (Vp) is applied to the pixel circuit **10** to acquire threshold Vt information (or Vt shift information) from the pixel circuit **10**. The hybrid driving circuit **12** controls the pre-charging, if pre-charging technique is used. The pre-charge signal (Vp) may be generated within the hybrid driving circuit **12**, which depends on the operation condition. The power-supply **18**B (Vdd) supplies the current required to energize the display **5** and to monitor the power consumption of the display **5**.

The hybrid controller **16** controls the individual components that make up the entire hybrid programming circuit. The hybrid controller **16** handles timing and controls the order in which the required functions occur. The hybrid controller **16** may generate data Idata and supplied to the hybrid driving circuit **12**. The system **2** may have a reference current source, and the Idata may be supplied under the control of the hybrid controller **16**.

The hybrid driver **12** may be implemented either as a switching matrix, or as the hybrid driving circuit(s) of FIG. **3**, **6**, **8** or **20** or combination thereof.

In the description, Vdata refers to data, a data signal, a data line or a node for supplying the data or data signal Vdata, or a voltage on the data line or the node. Similarly, Idata refers to data, a data signal, a data line or a node for supplying the data or data signal Idata, or a current on the data line or the node. Vp refers to a pre-charge signal, a pre-charge pulse, a pre-charge voltage for pre-charging/discharging, a line or a node for supplying the pre-charge signal, pre-charge pulse or pre-charge voltage Vp. Vsel refers to a pulse or a signal for selecting a pixel circuit or a line or a node for supplying the pulse or signal Vs. The terms "hybrid signal", "hybrid signal node", and "hybrid signal line" may be used interchangeably.

The pixel circuit **10** includes a plurality of TFTs, and an organic light emitting diode (OLED). The TFT may be an n-type TFT or a p-type TFT. The TFT is, for example, but not limited to, an amorphous silicon (a-Si:H) based TFT, a polycrystalline silicon based TFT, a crystalline silicon based TFT, or an organic semiconductor based TFT. The OLED may be regular (P-I-N) stack or inverted (N-I-P) stack. The OLED can be located in the source or the drain of one or more driving TFTs.

FIG. **2** illustrates an example of the pixel circuit **10** of FIG. **1**. The pixel circuit of FIG. **2** includes four thin film transistors (TFTs) **20-26**, a capacitor Cs **28** and an organic light emitter diode (OLED) **30**. The TFT (Tdrive) **26** is a drive TFT that is connected to the OLED **30** and the capacitor Cs **28**. The pixel circuit of FIG. **2** is selected by the select line Vsel, and is programmed by a data line DL. The data line DL is controlled by the hybrid signal output from the hybrid driving circuit **12** of FIG. **1**.

In FIG. **2**, four TFTs are illustrated. However, the pixel circuit **10** of FIG. **1** may include less than four TFTs or more than four TFTs.

In the description, the terms "data line DL" and "data node DL" may be used interchangeably.

Referring to FIGS. **1-2**, the data node DL is pre-charged and discharged to acquire the threshold Vt of a drive TFT (e.g., Tdrive **26** of FIG. **2**) or the threshold Vt shift. In the description, Vt shift, Vt shift information, Vt, and Vt information may be used interchangeably. The pixel circuit **10** is then consecutively programmed by the source driver **14** using voltage-programming. The acquired Vt shift information is utilized to compensate for degradation of the pixel circuit **10**, thus maintaining uniform brightness of the display **5**.

The process of acquiring Vt starts by applying Vsel to T1 **20** and T2 **22** to the pixel circuit illustrated in FIG. **2**. Such action causes the drain and gate of T3 **24** to be at the same voltage. This allows the Vt of T3 **24** to be extracted by first applying the pre-charge voltage Vp to the data line DL, which is than allowed to be discharged. The rate of discharge is a function of Vt. Thus, by measure of the rate of discharge, Vt can be obtained.

FIG. **3** illustrates an example of a hybrid driving circuit, which is applicable to the hybrid driving circuit **12** of FIG. **1**. The hybrid driving circuit **12**A of FIG. **3** implements voltage programming technique.

The hybrid driving circuit **12**A of FIG. **3** includes a charge programming capacitor Cc **32**. The charge programming capacitor Cc **32** is provided between the data line Vdata and the data node DL. The pre-charge line Vp is also connected to the data node DL.

The hybrid driving circuit **12**A is provided to a pixel circuit **10**A having four TFTs (such as the pixel circuit of FIG. **2**). However, the pixel circuit **10**A may include more than four TFTs or less than four TFTs.

The charge programming capacitor Cc **32** is provided to program the pixel circuit **10**A with a voltage that is equal to the sum of threshold Vt of the TFT and Vdata, scaled by a constant K. The constant is determined by the voltage division network formed by the charge storage capacitor (e.g. Cs **28** of FIG. **2**) and the charge programming capacitor Cc **32**.

FIG. **4** illustrates an exemplary flow chart for showing the operation of the hybrid driving circuit **12**A of FIG. **3**. At step S**10**, pre-charge mode is enabled. At step S**12**, a pixel circuit is selected and pre-charging (Vp) is started. At step S**14**, Vt acquisition mode is enabled, and at step S**16**, discharging (Vp) starts. The Vt information is acquired through Cc **32**. Then at step S**18**, writing mode is enabled.

FIG. **5** illustrates an exemplary timing chart for showing the operation of the hybrid driving circuit **12**A of FIG. **3**. In the drawings, Vdata**0** represents voltage at the data node (e.g. DL of FIG. **2**) of the pixel circuit; Idata**0** represents current at the data node (e.g. DL of FIG. **2**) of the pixel circuit.

The programming procedure starts by selecting the pixel to be programmed with the pulse Vsel. At the same time, the pre-charge pulse Vp is applied to the pixel circuit's data input (e.g. DL of FIG. **2**).

During the Vt acquisition phase, voltage on the data line (DL) is allowed to be discharged through the pixel circuit, which is in a current mirror connection with the Vsel line held high. The data line (DL) is discharged to a certain voltage, and the Vt of a drive TFT is extracted from that voltage. The voltage at Vdata is at ground.

During the programming (writing) phase, the calculated compensated voltage is applied to the data input line (DL) of the pixel circuit. The programming routine finishes with the lowering of the Vsel signal.

The calculated compensated voltage is obtained through analog means of a charge programming capacitor Cc**32**. However, any other analog means for obtaining compensated voltage may be used. Further, any (external) digital circuit (e.g. **50** of FIG. **7**) may be used to obtain the calculated compensated voltage.

The source driver (**14** of FIG. **1**) supplies Vdata to the capacitor Cc **32**. When Vdata is increased from ground to the desired voltage level, the voltage at Idata is equal to (Vt+Vdata)*K.

The structure of FIG. **3** is simple, and is easily implemented.

FIG. **6** illustrates a further example of a hybrid driving circuit, which is applicable to the hybrid driving circuit **12** of FIG. **1**. The hybrid driving circuit **12**B of FIG. **6** implements voltage programming technique.

The hybrid driving circuit **12**B includes a summer **40**, a sample and hold (S/H) circuit **42** and a switching element **44**. The S/H circuit **42** samples Idata and holds it for a certain period. The summer **40** receives Vdata and the output of the S/H circuit **42**. The switching element **44** connects the output of the summer **40** to the data node DL in response to a programming control signal **46**.

The hybrid driving circuit **12**B utilizes the summer **40**, instead of the charge coupling capacitor Cc **32**, to produce programming voltage that is equal to the sum of Vt and Vdata. As the hybrid driving circuit **12**B does not utilize a capacity, programming voltage is not affected by the parasitic capacitance, and it has less charge feed-through effect. As the hybrid driving circuit **12**B does not utilize a charge storage capacitor, programming voltage is not affected by the charge storage capacitance. As the hybrid driving circuit **12**B does not utilize a charge programming capacitor, it achieves faster Vt acquisition time. Removal of the charge programming capacitor eliminates the charge dependency of the programming scheme. Thus the programming voltage is not affected by the charge being shared between the charge storage capacitor and the parasitic capacitance of the system. This results in a higher effective programming voltage.

FIG. **7** illustrates an exemplary flow chart for showing the operation of the hybrid driving circuit **12**B of FIG. **6**. During the Vt acquisition mode, the Vt is sampled at step S**20**, and new data is produced at step S**22**. When writing mode is enabled, the new data is supplied to the pixel circuit in response to the programming control signal (**46**) at S**24**. It is noted that the operation of the system having the hybrid driving circuit **12**B is not limited to FIG. **7**. The new data may be produced after step S**18**. The control signal **46** may be enabled before step S**18**.

During the Vt acquisition cycle, Vdata is at ground, and the voltage at the data node DL is equal to Vt of the TFT by the pre-charging/discharging operation (Vp). The voltage on the data node DL is sampled and holed by the S/H circuit **42**. The Vt is provided to the summer **40** through the S/H circuit **42**. When Vdata is increased from ground to the desired voltage level, the summer **40** outputs the sum of Vt and Vdata. The switch **44** turns on in response to the programming control signal **46**. The voltage at the data node DL goes to (Vt+Vdata). Timing chart for showing the operation of the system **2** having the hybrid driving circuit **12**B is similar to that of FIG. **5**.

FIG. **8** illustrates a further example of a hybrid driving circuit, which is applicable to the hybrid driving circuit **12** of FIG. **1**. The hybrid driving circuit **12**C of FIG. **8** implements voltage programming technique.

The hybrid driving circuit **13**C is a direct digital hybrid driving circuit. The direct digital programming circuit **13**C includes a microComputer uC **50** which receives digital data (Vdada), a digital to analog (D/A) converter **52**, a voltage follower **54** for increasing current without affecting voltage, and an analog to digital (A/D) converter **56**.

The threshold Vt of the drive TFT may increase slowly. Thus, it may not be necessary to acquire the threshold Vt of the drive TFT every programming cycle. This effectively hides the Vt acquisition for the majority of the programming cycle. In the direct digital hybrid driving circuit **13**C, the threshold Vt acquired from the pixel circuit **10**A is digitalized at the A/D converter **56**, and is stored in memory contained in the uC **50**. The digital data that defines the

brightness of the pixel is added to the Vt in the uC **50**. The resulting voltage is then converted back to an analog value at the D/A **52**, which is programmed into the pixel circuit **10**A. This programming method is designed to compensate for the slow process of the Vt acquisition.

FIG. **9** illustrates an exemplary flow chart for showing the operation of the hybrid driving circuit **12**C of FIG. **8**. At the Vt acquisition mode, the Vt is sampled and recorded at step S**30**. When writing mode is enabled, new data is provided based on the recorded data. It is noted that the operation of the system having the hybrid driving circuit **12**C of FIG. **8** is not limited to FIG. **9**. At the writing mode, the data which have been recorded may be used without implementing the Vt acquisition.

FIG. **10** illustrates an exemplary timing chart for showing the operation of the hybrid driving circuit **12**C of FIG. **8**. During the Vt acquisition, sampling by the A/D converter **56** is implemented. In a next cycle, the hybrid driving circuit **13**C may use the Vt that has been previously acquired and has been recorded in the uC **50**.

The conversion of the output on the data node DL by A/D can remove the requirements of having to acquire the Vt every programming cycle. The Vt of the pixel circuit **10**A may be acquired once every second or less. Thus, it may acquire Vt for only one row of the display per frame cycle. This effectively increases the amount of time for the pixel programming cycle. Less frequent need of Vt acquisition ensures faster programming time.

In the above description, FIG. **2** is used to describe the pixel circuit **10** of FIG. **1**. However, the pixel circuit **10** is not limited to that of FIG. **2**. The pixel circuit **10** may be a pixel circuit illustrated in FIG. **11** (J. Kanichi, J.-H. Kim, J. Y. Nahm, Y. He and R. Hattori "Amorphous Silicon Thin-Film Transistor Based Active-Matrix Organic Light Emitting Display" Asia Display IDW 2001 pp. 315). The pixel circuit of FIG. **11** includes four TFTs **64**-**70**, a capacitor C_{ST} **72** and an OLED **74**. The TFT **78** is a drive TFT that is connected to the OLED **74** and the capacitor C_{ST} **72**. The pixel circuit of FIG. **11** is selected by Vselect**1** and Vselect**2**, and is programmed by Idata. The voltage acquired is a combination of the voltage across the OLED **74** and T**3** **68**. The technique compensates the voltage change of both the Vt and the OLED **74**. Idata of FIG. **11** corresponds to the data node DL of FIG. **2**.

FIG. **12** illustrates a system for driving an AMOLED display in accordance with a further embodiment of the invention. The system **82** of FIG. **12** includes a hybrid programming circuit having a correction table **80**, a source driver **14** for implementing a voltage-programming scheme and a reference current source **94** for implementing a current-programming scheme. The system **82** drives a display having a plurality of pixel circuits using the voltage-programming scheme and the current-programming scheme.

A hybrid controller **98** is provided to control each component. In FIG. **12**, the hybrid controller **98** is placed between the A/D converter **96** and the correction table **80**, as an example. The hybrid controller **98** is similar to the hybrid controller **16** of FIG. **1**.

The pixel circuit driven by the system **82** may be the pixel circuit **10** of FIG. **1**, and may be a current programmed pixel circuit or a voltage programmed pixel circuit. The pixel circuit driven by the system **82** may be implemented by FIG. **2** or FIG. **11**, however, is not limited to those of FIGS. **2** and **11**.

The hybrid programming circuit includes a correction calculation module **92** for correcting data from the data source **90** based on the correction table **80** and an A/D converter **96**. The data corrected by the correction calculation module **92** is applied to the source driver **14**. The source driver **14** generates Vdata based on the corrected data output from the correction calculation module **92**. Vdata from the source driver **14** and Idata from the reference current source **94** are supplied to the hybrid driver **12**.

The data source **90** is, for example, but not limited to, a DVD. The hybrid driver **12** may be implemented either as a switching matrix, or as the digital programming circuit(s) of FIG. **8**, **20** or combination thereof. The A/D converter **96** may be the A/D converter **56** of FIG. **8**. The system **82** may implement the Vt acquisition technique described above using the A/D converter **96** (**56**).

The correction table **80** is a lookup table. The correction table **80** records the relationship between current required to program the pixel circuit and voltage necessary to obtain that current. The correction table **80** is built for every pixel in the entire display.

In the description, the relationship between the current required to program the pixel circuit and the voltage necessary to obtain that programming current, is referred to as "current/voltage correction information", "current/voltage correction curve", or "current/voltage information", or "current voltage curve".

In FIG. **12**, the correction table **80** is illustrated separately from the correction calculation module **92**. However, the correction table **80** may be included in the correction calculation module **92**.

The operation of the system of FIG. **12** has two modes, namely display mode and calibration mode. In the display mode, the data from the data source **90** is corrected using the data in the correction table **80**, and is applied to the source driver **14**. The hybrid driver **12** is not involved in the display mode. In the calibration mode, the current from the reference current source **94** is applied to the pixel circuit, and the voltage associated with the current is read from the pixel circuit. The voltage is converted to a digital data by the A/D converter **96**. The correction table **80** is updated with the correct value based on the digital data.

During the display mode, a voltage-programming scheme is implemented. The voltage on the data line (e.g. DL of FIG. **2**) of the pixel circuit determines the brightness of the pixels. The voltage required to program the pixel circuit is calculated from the pixel brightness to be displayed (from the incoming video information) combined with the current/voltage correction information stored in the correction table **80**. The information on the correction table **80** is combined with incoming video information to ensure that each pixel will maintain a constant brightness over long-term use.

After the display has been used for a fixed period of time, the display enters the calibration mode. The current source **94** is connected to the data input node (DL) of the pixel circuit via the hybrid driver **12**. Each pixel is programmed through a current-programming scheme (where the level of current on the data line determines the brightness of the pixel), and the voltage required to achieve that current is read by the A/D converter **96**.

The voltage required to program the pixel current is sampled at multiple current points by the A/D converter **96**. The multiple points may be a subset of the possible current levels (e.g. 256 possible levels for 8-bit, or 64 levels for 6-bit). This subset of voltage measurements is used to construct the correction table **80** that is interpolated from the measurement points.

The calibration mode may be entered either through user's command or may be combined with the normal display mode so that the calibration takes place during the display refresh period.

In one example, the entire display may be calibrated at once. The display may stop showing incoming video information for a short period of time while each pixel was programmed with a current and the voltage recorded.

In a further example, a subset of the pixels may be calibrated, such as one pixel every fixed number of frames. This is virtually transparent to the user, and the correction information may still be acquired for each pixel.

When a conventional voltage-programming scheme is utilized, a pixel circuit is programmed in an open loop configuration, where there is no feedback from the pixel circuit regarding the threshold voltage shift of the TFTs. When a conventional current-programming scheme is utilized, the brightness of the pixel may remain constant over time. However, the current programming scheme is slow. Thus, the table lookup technique combines the technique of the current-programming scheme with the technique of the voltage-programming scheme. The pixel circuit is programmed with a current through a current-programming scheme. A voltage to maintain that current is read and is stored at a lookup table. The next time that particular level of current is applied to the pixel circuit, instead of programming with a current, the pixel circuit is programmed based on information on the lookup table. Accordingly, it attains the compensation inherent in the current programming scheme while attaining the fast programming time that is only possible with voltage-programming scheme.

In the above description, the correction table (lookup table) **80** is used to correct the current/voltage correction information. However, the system **82** of FIG. **12** may use the lookup table to correct the Vt shift and the current/voltage correction information at the same time in combination with the hybrid driving circuit of FIG. **3**, **6**, **8** or **20**.

For example, several voltage measurements are captured at many different current points by the A/D converter **96** (**56**). The hybrid controller **98** extracts the Vt shift information by extending the voltage versus current curve to zero current point. The Vt shift information is stored in an array of tables (correction table **80**) which is applied to incoming display data.

The uC **50** of FIG. **8** or **20** may utilize the lookup table to generate appropriate voltage and program the pixel circuit.

The hybrid circuits **12**A of FIGS. **3** and **12**B of FIG. **6** may be integrated into the system of FIG. **12**.

FIGS. **13-14** illustrate exemplary flow charts for showing the operation of the system of FIG. **12**. Referring to FIG. **13**, at step S**40**, calibration mode is enabled. At step S**42**, a pixel circuit is selected and current programming is implemented to the selected pixel circuit. At step S**44**, a switch matrix enable signal is enabled. Then the connection to the pixel circuit is changed. The Vt is sampled at step s**46**, and then the correction table is created/corrected at step S**48**. Referring to FIG. **14**, at step S**50**, video data are corrected based on the correction table. Then at step S**52**, new Vdata is produced based on the corrected data.

It is noted that the writing mode may be implemented based on the previously created correction table without implementing the calibration mode. It is noted that the operation of the system of FIG. **12** is not limited to FIGS. **13-14**.

FIG. **15** illustrates an exemplary timing chart for showing a combination of the Vt shift acquisition and the current/voltage correction. A switch matrix enable signal in FIG. **15** represents a control signal for the hybrid driver **12** of FIG. **12**.

Referring to FIGS. **12** and **15**, the calibration mode (i.e. the current-programming scheme) is enabled when the switch matrix enable signal is high. The programming mode (i.e. the voltage-programming scheme) is enabled when the switch matrix enable signal is low. However, the calibration mode may be enabled when the switch matrix enable signal is low. The programming mode may be enabled when the switch matrix enable signal is high.

A/D sampling is implemented during the calibration mode. During the calibration mode, the current from the reference current source **94** is applied to the pixel circuit. The voltage on the data input node is converted to a digital voltage by the A/D converter **56**. Based on the digital voltage and current associated with the digital voltage, current/voltage correction information is recorded at the lookup table. The Vt shift information is generated based on the data in the correction table **80** or the output from the A/D converter **96**.

The system **82** of FIG. **12** may implement hidden refresh technique for refreshing current/voltage correction information in addition to the table lookup technique described above.

Under the hidden refresh operation, new current/voltage correction information is constructed while completely hidden from user's perception. This technique utilizes the information that is currently displayed on the screen (i.e. the incoming video data). By obtaining the pixel characteristics from the full calibration routine that has been performed during the manufacturing process of the display, the current/voltage correction information for each pixel in the display is known. During the display's usage, the current/voltage correction curve may shift due to the change in Vt. By measuring a single point along the current/voltage correction curve (which is the data currently displayed, that is part of the video image), a new current/voltage correction curve is extrapolated from the point so that it is fitted to the measured point. Based on the new current/voltage correction curve, the Vt shift information is extracted which is used to compensate for the shift in Vt.

FIG. **16** illustrates an exemplary flow chart for the hidden refresh operation of the system of FIG. **12**. First, a current/voltage correction curve is produced during the calibration process that is implemented during the manufacturing of the display (step S**62**). FIG. **17** illustrates an example of a sample of the current voltage correction curve.

Referring to FIG. **16**, the next step is to measure a point along the curve during the usage of the display. This point can be any point along the curve, so any data that the user currently has on the display can be used for calibration (step S**64**). FIG. **18** illustrates the current voltage correction of FIG. **17** and an example of a newly measured data point.

Referring to FIG. **16**, the last step is to shift the current/voltage correction curve to fit the point of voltage verses current relationship that is measured (step S**66**). FIG. **19** illustrates an example of a new current voltage correction curve based on the measured point of FIG. **18**.

The process associated with FIGS. **17-19** is implemented in the hybrid controller **98** of FIG. **12**.

The system **82** of FIG. **12** may implement a combined current and voltage-programming technique. FIG. **20** illustrates one example of a hybrid driving circuit for implementing the combined current and voltage-programming technique. The hybrid driving circuit of FIG. **20** may be included in the hybrid driver **12** of FIG. **12**.

In the hybrid driving circuit of FIG. **20**, the digital hybrid driving circuit **12**C and a current source **100** are provided to the data line DL of the pixel circuit.

To enhance the circuit's ability to compensate for a change in the current/voltage correction curve due to temperature, threshold voltage shift, or other factors, the pixel circuit programming is divided into two phases.

During the writing mode, the pixel circuit **10**A is voltage-programmed first to set the gate voltage of the driving TFT to an approximate value, then followed by a current programming phase. The current programming phase can then fine-tune the output current. The system of FIG. **20** is faster than current programming and has the compensation capabilities of the current programming scheme.

In FIG. **20**, the digital hybrid driving circuit **12**C is provided. However, the combined current and voltage-programming technique may be implemented by combining the hybrid driving circuit **12**A of FIG. **3** or **12**B of FIG. **6** with the current source **100**. The current source **100** may be the reference current source **94** of FIG. **12**.

The system **2** of FIG. **1** may implement the hidden refresh technique described above. The system **2** of FIG. **1** may implement the combined current and voltage-programming technique. The system **2** of FIG. **1** may include the hybrid driving circuit of FIG. **20** to implement the combined current and voltage-programming technique.

Extension of the direct digital programming scheme is now described in detail. The direct digital programming scheme (FIGS. **6**, **8** and **20**) can be extended to drive an OLED array (e.g. a 4T OLED array) using voltage programmed column drivers, such as those used for driving Active Matrix Liquixd Crystal Display (AMLCD), or voltage-programmed Active-Matrix Organic Light Emitting Diode (AMOLED) displays, or any other voltage-output display driver.

FIG. **21** illustrates a system for driving an AMOLED array having a plurality of pixel circuits in accordance with a further embodiment of the invention. The system **105** of FIG. **21** includes a voltage column driver **112**, a programmable current source **114**, a switching network **116**, an A/D converter **118** and a row driver **120**.

The voltage column driver **112** is a voltage programmed column driver. Each of the voltage column driver **112** and the row driver **120** may be any driver that has a voltage output, such as those designed for the AMLCD. The voltage column driver **112** and the programmable current source **114** are connected to an OLED array **110** through the switching network **116**. The OLED array **110** forms an AMOLED display, and contains a plurality of pixel circuits (such as **10** of FIG. **1**). The pixel circuit may be a current programmed pixel circuit or a voltage programmed pixel circuit.

The A/D converter **118** is an interface that allows an analog signal (i.e. current driving the display **110**) to be read back as a digital signal. The digital signal associated with the current can than be processed and/or stored. The A/D converter **118** may be the A/D converter **56** of FIGS. **8** and **20**. The column driver **112** may be the source driver **14** of FIGS. **1** and **12**.

The system **105** of FIG. **21** implements the calibration mode and the display mode as described above.

FIG. **22** illustrates an example of the switch network **116** of FIG. **21**. The switching network **116** of FIG. **22** includes two MOSFET switches **122** and **124** that can switch the column of the display (**110**) from connecting to the column driver (**112**) to the combination of the current source (**114**) and the A/D converter (**118**), and vice versa. A shift register **126** is a source of the digital control signal that controls the operation of the MOS switches **122** and **124**. An inverter **128** inverts an output from the shift register **126**. Thus, when the switch **122** is on (off), the switch **124** is off (on).

The switching network **116** may be located either off the glass in the column driver (**112**) or directly on the glass using TFT switches.

Referring to FIGS. **21-22**, the system **105** uses only one current source **114**. The voltage-programming drivers (such as, AMLCD drivers, or any other voltage-output drivers) drive the rest of the display **110**. The switching matrix (switching network **116**) allows different pixels within the array of pixels to be connected to a single current source (**114**) through a time division method. This allows a single current source to be applied to the entire display. This lowers the cost of the driver circuit and speeds up the programming time for the pixel circuit.

The system **105** uses the A/D converter **118** to convert an analog output of the data node (e.g. DL of FIG. **2**) of the pixel circuit to digital data. The conversion by the A/D converter **118** removes the requirements of having to acquire the Vt every programming cycle. The Vt of the pixel circuit may be acquired once every few minutes. Thus it may acquire one column of the panel every refresh cycle.

Only one A/D **118** may be implemented for all the columns. The circuit acquires only one pixel per frame refresh. For example, for a 320 by 240 panel, the number of pixels is 76, 8000. For a frame rate of 30 Hz, the time required to acquire Vt from all pixels for the entire frame is 43 minutes. This may be acceptable for some applications, providing that Vt does not shift substantially in an hour.

The parasitics only affect the amount of time to discharge the capacitor to acquire Vt. Since the circuit is voltage-programmed, it is not affected by the parasitics. Since Vt is only acquired one column per frame time, it can be long. For example, for a display with 320 columns that has a frame rate of 30 Hz, each frame time is 33 mS. For voltage programming, it is possible to program a pixel in 70 uS. For 320 columns, the time to update the display is 22 mS, which still leave 11 mS to complete a charge/discharge cycle.

The system **105** may implement the lookup table technique to compensate for Vt shift and/or to correct the current/voltage information as described above

The system **105** may implement the hidden refresh technique to acquire the Vt shift information and current/voltage correction information of each pixel circuit (**10**) in the display **110**. This current/voltage correction information is used to populate a lookup table (e.g. a correction table **80** of FIG. **12**) that will then be used to compensate for the degradation in the pixel circuit, which is caused by aging. To reduce cost, the number of current-programmed circuits has been reduced so there is only one per display instead of one per column driver.

The system **105** may implement the combined current and voltage-programming technique as described above.

The current/voltage information of the pixel circuit can be further corrected by implementing a system illustrated in FIG. **23**. FIG. **23** illustrates a system for correcting the current/voltage information of the pixel circuit. In FIG. **23**, a display **130** is depicted as a 2T or 4T OLED array. However, the display **130** may include a plurality of pixel circuits, each having three or more than four transistors. The display **130** may include voltage-driven pixel circuits or current-driven pixel circuits. The system of FIG. **23** is applicable to the systems **2**, **82** and **105** of FIGS. **1**, **12** and **22**.

As illustrated in FIG. **23**, a switch **132** is provided to disconnect the common electrode of the OLED. It is well

known that two electrodes are provided for the OLED. One is connected to the pixel circuit, and the other is a common electrode connected to all OLEDs. It is noted that the common electrode may be Vdd or GND depending on the type of OLED. The switch **132** connects the common electrode of the OLED into a current sensing network **134** utilizing a high side common mode sensor (such as, INA168 by TI). The current sensing network **134** measures the current through the common electrode.

During the calibration phase, each pixel is lit individually and the current consumed is acquired by the sensing network **134**. The acquired current is used to correct the lookup table (e.g. the correction table **80** of FIG. **12**) populated by the direct digital hybrid driving circuit of FIG. **8** or **20**.

A dark display current may be acquired to include the effect of dead pixel and leakage current of the array. During this procedure, all pixels are turned off, and the current (i.e. dark display current) is measured.

According to the embodiments of the present invention, the major issue with current-programmed pixel circuits, which is the slow programming time, is solved. The concept of using feedback to compensate the pixel circuit enhances the uniformity and stability of the display while retaining the fast programming capability of the voltage programmed drive scheme.

The present invention has been described with regard to one or more embodiments. However, it will be apparent to persons skilled in the art that a number of variations and modifications can be made without departing from the scope of the invention as defined in the claims.

What is claimed is:

[1. A system for programming at least one pixel circuit in a display, the system comprising:

a voltage driver for generating a voltage to apply to a data node of the at least one pixel circuit to thereby program the at least one pixel circuit according to the generated voltage;

a programmable current source for providing a first current and a second current to apply to the data node of the at least one pixel circuit;

a sampler for reading a first voltage on the data node while the first current is maintained through the at least one pixel circuit via the programmable current source and for reading a second voltage on the data node while the second current is maintained through the at least one pixel circuit via the programmable current source; and

a controller configured to:

generate a voltage versus current relationship for the at least one pixel circuit based on the first current and the second current and based on the sampled first and second voltages,

extract, based on the voltage versus current relationship for the at least one pixel circuit, a voltage corresponding to a zero current level, and

program the at least one pixel circuit via the data node with a programming voltage generated by the voltage driver that is set according to display data and according to the extracted voltage corresponding to the zero current level.**]**

[2. The system according to claim **1**, wherein the at least one pixel circuit is configured to be alternately programmed by a programming current applied to the data node or by a programming voltage applied to the data node.**]**

[3. The system according to claim **2**, wherein the at least one pixel circuit includes a mirror transistor having a gate coupled to a gate terminal of the driving transistor, the at least one pixel circuit configured such that the data node is coupled to a gate terminal of the mirror transistor via one or more switch transistors, the applied current being conveyed via the one or more switch transistors through the mirror transistor while the gate terminal of the mirror transistor adjusts to a voltage for maintaining the applied current through the mirror transistor.**]**

[4. The system according to claim **3**, wherein the one or more switch transistors include a first switch transistor and a second transistor,

the first switch transistor operated according to a select signal and configured to couple the data node to the gate terminal of the mirror transistor while the first switch transistor is switched on,

the second switch transistor operated according to the select signal and configured to couple the data node to a drain or a source terminal of the mirror transistor while the second switch transistor is switched on.**]**

[5. The system according to claim **2**, wherein the at least one pixel circuit includes one or more switch transistors configured to couple the data node to a drain or a source terminal of the driving transistor while the programming current is applied to the at least one pixel circuit via the data node,

the one or more switch transistors further configured to couple the data node to a gate terminal of the driving transistor while the programming current is applied, such that the gate terminal of the driving transistor adjusts to a voltage for maintaining the applied current through the driving transistor,

the one or more switch transistors further configured to couple the data node to a gate terminal of the driving transistor while the programming voltage is applied to the at least one pixel circuit via the data node.**]**

[6. The system according to claim **1**, wherein the sampler includes an analog to digital converter configured to capture digital information indicative of the first and second voltages on the data node.**]**

[7. The system according to claim **6**, further comprising a memory for storing the digital information indicative of the first and second voltages, the digital information being stored in a lookup table that associates the first and second voltages with the first and second currents to thereby characterize the voltage versus current relationship of the at least one pixel circuit.**]**

[8. The system according to claim **1**, wherein the controller is further configured to instruct the voltage driver to set the programming voltage for the at least one pixel circuit by adding the voltage corresponding to the zero current level to a voltage indicated by the display data.**]**

[9. The system according to claim **1**, wherein the at least one pixel circuit is a plurality of pixel circuits arranged in an array of rows and columns, each of the plurality of pixel circuits having a data node coupled to a data line, and wherein the programmable current source is configured to generate a plurality currents to apply to each of the plurality of pixel circuits and the sampler is configured to read a corresponding plurality of voltages for each of the plurality of pixel circuits while each of the plurality of currents is maintained through respective ones of the plurality of pixel circuits.**]**

[10. The system according to claim **1**, wherein the controller is configured to extract the threshold voltage of the driving transistor of the at least one pixel circuit by extending the voltage versus current relationship for the at least one pixel circuit to the zero current level and determining the voltage corresponding to the zero current level, the voltage

corresponding to the zero current level providing an estimate of the threshold voltage of the driving transistor of the at least one pixel circuit.]

[11. The system according to claim 1, further comprising a memory communicatively coupled to the controller for digitally storing digital information indicative of the first and second voltages.]

[12. The system according to claim 1, wherein the at least one pixel circuit includes an organic light emitting diode for emitting light according to the display data and one or more thin film transistors for conveying a current through the organic light emitting diode according to the display data.]

[13. A method of operating a display having at least one pixel circuit, the at least one pixel circuit having a light emitting device coupled in series with a driving transistor configured to convey a driving current through the light emitting device according to display information, the at least one pixel circuit configured to be alternately programmed according to the display information by a programming current applied to a data node of the at least one pixel circuit or by a programming voltage applied to the data node, the method comprising:

applying a first current to the data node of the at least one pixel circuit;

reading a first voltage on the data node while the first current is maintained through the at least one pixel circuit;

applying a second current to the data node of the at least one pixel circuit;

reading a second voltage on the data node while the second current is maintained through the at least one pixel circuit;

storing digital information indicative of the first and second voltages such that the first and second voltages are associated with the first and second currents;

generating a voltage versus current relationship for the at least one pixel circuit based on the first and second voltages and the first and second currents;

extracting, based on the generated voltage versus current relationship for the at least one pixel circuit, a voltage corresponding to a zero current level; and

programming the at least one pixel circuit by applying, to the data node of the at least one pixel circuit, a programming voltage that is based on the display data and the voltage corresponding to the zero current level.]

[14. The method according to claim 13, wherein the at least one pixel circuit is at least one of a plurality of pixel circuits arranged in an array of rows and columns in the display, and wherein the applying the first and second current, the reading the first and second voltages, the storing, the generating, and the extracting are applied to each of the plurality of pixel circuits such that voltages corresponding to the zero current level are extracted for each of the plurality of pixel circuits.]

[15. The method according to claim 14, wherein the voltage corresponding to the zero current level is an estimate of a threshold voltage of the driving transistor in the at least one pixel circuit, and wherein the programming is applied to each of the plurality of pixel circuits based on the display data for each of the plurality of pixel circuits and based on the estimate of the threshold voltage of the driving transistor for each of the plurality of pixel circuits such that the display is operated to compensate for the threshold voltages of the driving transistors in each of the plurality of pixel circuits.]

[16. The method according to claim 13, wherein the storing is carried out by digitally storing the digital information indicative of the first and second voltages in a lookup table associated with the at least one pixel circuit.]

[17. The method according to claim 13, wherein the applying the first current and the applying the second current are performed during a calibration mode of the display that is distinct from a normal display mode, the calibration mode being a period during which images are not shown on the display.]

[18. The method according to claim 13, wherein at least one of the first current or the second current is a programming current applied to the at least one pixel circuit during a programming operation of a normal display mode to program the at least one pixel circuit to emit light according to the display information.]

[19. The method according to claim 13, wherein the at least one pixel circuit is at least one of a plurality of pixel circuits arranged in an array of rows and columns in the display, and wherein at least one of the first current or the second current is a programming current applied to the at least one pixel circuit during a programming operation of a normal display mode while others of the plurality of pixel circuits are voltage programmed with programming voltages, thereby hiding the applying the at least one of the first current or the second current to the at least one pixel circuit.]

[20. The method according to claim 13, further comprising:

responsive to the extracting, applying a third current to the data node of the at least one pixel circuit;

reading a third voltage on the data node while the third current is maintained through the at least one pixel circuit;

storing digital information indicative of the third voltage such that the third voltage is associated with the third current;

updating the voltage versus current relationship for the at least one pixel circuit based on at least the third voltage and the third current;

extracting, based on the updated voltage versus current relationship for the at least one pixel circuit, a voltage corresponding to a zero current level, the voltage corresponding to the zero current level being an updated estimate of a threshold voltage of the driving transistor in the at least one pixel circuit; and

programming the at least one pixel circuit to compensate for the threshold voltage of the driving transistor by applying, to the data node of the at least one pixel circuit, a programming voltage that is based on the display data and the updated estimated threshold voltage.]

[21. A system for programming at least one pixel circuit in a display, the system comprising:

a voltage driver for generating a voltage to apply to a data node of the at least one pixel circuit to thereby program the at least one pixel circuit according to the generated voltage;

a programmable current source for providing a first current to apply to the data node of the at least one pixel circuit;

a sampler for reading a first voltage on the data node while the first current is maintained through the at least one pixel circuit via the programmable current source; and

a controller configured to:

receive calibration data indicative of a voltage versus current relationship for the at least one pixel circuit;

generate an updated voltage versus current relationship for the at least one pixel circuit based on the first current and the first voltage and based on the received calibration data,

extract, based on the updated voltage versus current relationship for the at least one pixel circuit, a voltage corresponding to a zero current level, and

program the at least one pixel circuit via the data node with a programming voltage generated by the voltage driver that is set according to display data and according to the extracted voltage corresponding to the zero current level.]

[**22**. The system according to claim **21**, wherein the first current is a programming current applied to the at least one pixel circuit during a programming operation of a normal display mode to program the at least one pixel circuit to emit light according to the display information.]

[**23**. The system according to claim **21**, wherein the at least one pixel circuit is configured to be alternately programmed by a programming current applied to the data node or by a programming voltage applied to the data node.]

[**24**. The system according to claim **21**, wherein the at least one pixel circuit is a plurality of pixel circuits arranged in an array of rows and columns, each of the plurality of pixel circuits having a data node coupled to a data line, and wherein the programmable current source is configured to generate a plurality currents to apply to each of the plurality of pixel circuits and the sampler is configured to read a corresponding plurality of voltages for each of the plurality of pixel circuits while each of the plurality of currents is maintained through respective ones of the plurality of pixel circuits.]

[**25**. The system according to claim **21**, wherein the sampler includes an analog to digital converter configured to capture digital information indicative of the first and second voltages on the data node.]

[**26**. The system according to claim **25**, further comprising a memory for storing the digital information indicative of the first voltage, the digital information being stored in a lookup table that associates the first voltage with the first current to thereby characterize the voltage versus current relationship of the at least one pixel circuit.]

[**27**. The system according to claim **21**, wherein the at least one pixel circuit includes an organic light emitting diode for emitting light according to the display data and one or more thin film transistors for conveying a current through the organic light emitting diode according to the display data.]

[**28**. A method of operating a display having at least one pixel circuit, the at least one pixel circuit having a light emitting device coupled in series with a driving transistor configured to convey a driving current through the light emitting device according to display information, the at least one pixel circuit configured to be alternately programmed according to the display information by a programming current applied to a data node of the at least one pixel circuit or by a programming voltage applied to the data node, the method comprising:

applying a first current to the data node of the at least one pixel circuit;

reading a first voltage on the data node while the first current is maintained through the at least one pixel circuit;

storing digital information indicative of the first voltage such that the first voltage is associated with the first current;

receiving calibration data indicative of a voltage versus current relationship for the at least one pixel circuit;

generating an updated voltage versus current relationship for the at least one pixel circuit based on the first voltage, the first current, and the received calibration data;

extracting, based on the updated voltage versus current relationship for the at least one pixel circuit, a voltage corresponding to a zero current level; and

programming the at least one pixel circuit by applying, to the data node of the at least one pixel circuit, a programming voltage that is based on the display data and the voltage corresponding to the zero current level.]

[**29**. The method according to claim **28**, wherein the at least one pixel circuit is at least one of a plurality of pixel circuits arranged in an array of rows and columns in the display, and wherein the applying the first current, the reading the first voltage, the storing, the receiving, the generating, and the extracting are applied to each of the plurality of pixel circuits such that voltages corresponding to the zero current level are extracted for each of the plurality of pixel circuits.]

[**30**. The method according to claim **29**, wherein the voltage corresponding to the zero current level is an estimate of a threshold voltage of the driving transistor in the at least one pixel circuit, and wherein the programming is applied to each of the plurality of pixel circuits based on the display data for each of the plurality of pixel circuits and based on the estimate of the threshold voltage of the driving transistor for each of the plurality of pixel circuits such that the display is operated to compensate for the threshold voltages of the driving transistors in each of the plurality of pixel circuits.]

31. A method of calibrating a display panel having a plurality of pixel circuits, each of the pixel circuits including a drive transistor coupled to an organic light emitting device, comprising:

measuring a degradation of each pixel circuit of a subset of the pixel circuits during a frame while displaying a video image with the pixel circuits on the display panel;

extracting, for each of the pixel circuits of the subset, a current/voltage point for the pixel circuit from the degradation measurement;

determining, for each of the pixel circuits of the subset, corresponding compensation information from a fitting of a previously stored voltage versus current relationship for the pixel circuit to the extracted current/voltage point for the pixel circuit; and

compensating each of the pixel circuits of the subset based on the respective compensation information for each of the pixel circuits of the subset.

32. The method of claim 31, wherein each of the pixel circuits are programmed using current, while the degradation measurement is a voltage measurement.

33. The method of claim 31, wherein the measuring is carried out without stopping video information from being displayed on the display panel.

34. The method of claim 33, wherein the measuring is carried out during a refresh period of the display panel.

35. The method of claim 31, wherein the measuring, extracting, and determining are carried out externally from the pixel circuit.

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