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(54) **INTEGRATED CIRCUIT FOR CLOCK GENERATION FOR MEMORY DEVICES**

(71) Applicant: **TEXAS INSTRUMENTS DEUTSCHLAND GmbH**, Freising (DE)

(72) Inventor: **Joerg Goller**, Zweikirchen (DE)

(73) Assignee: **TEXAS INSTRUMENTS INCORPORATED**, Dallas, TX (US)

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Issued: **Feb. 23, 2010**
Appl. No.: **12/110,684**
Filed: **Apr. 28, 2008**

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(Continued)

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G11C 7/10 (2006.01)
G11C 7/22 (2006.01)

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CPC ***G11C 7/10*** (2013.01); ***G11C 7/22*** (2013.01); ***G11C 7/222*** (2013.01)

(58) **Field of Classification Search**
CPC G11C 7/22
(Continued)

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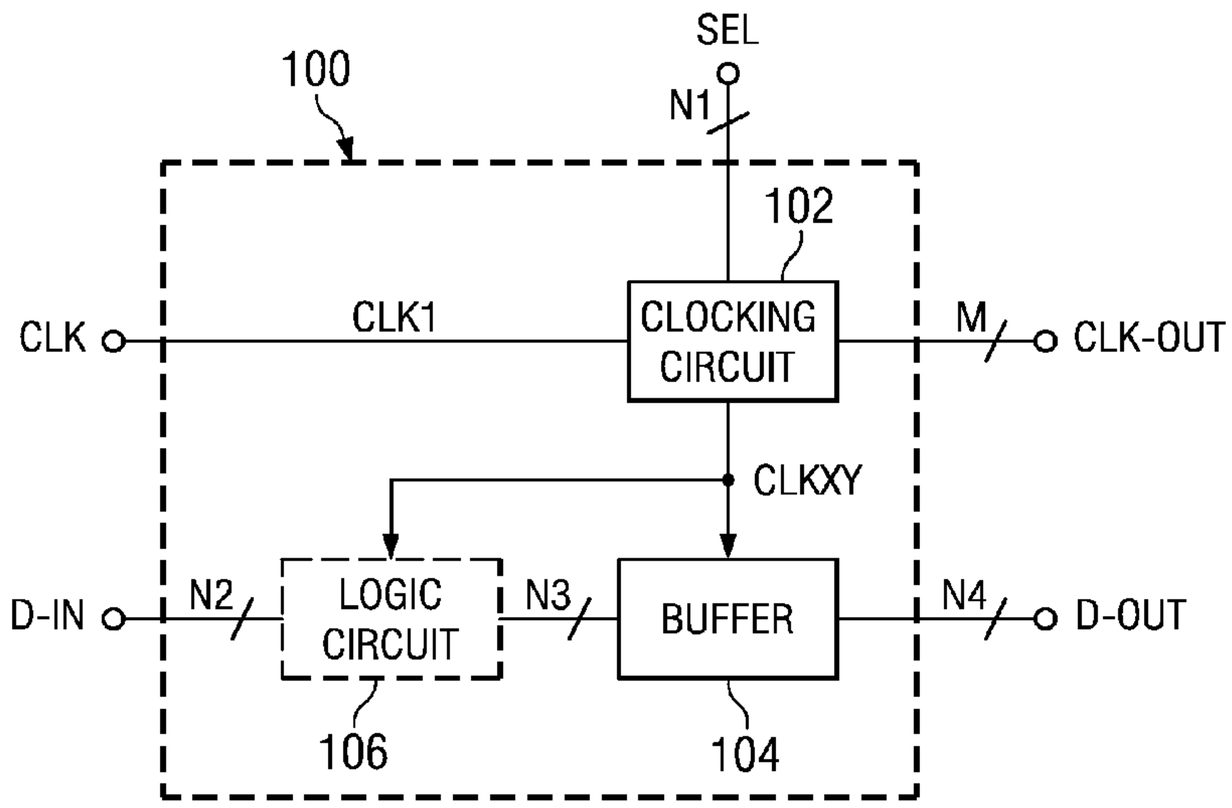
Primary Examiner — Angela M Lie
(74) *Attorney, Agent, or Firm* — Gregory J. Albin; Charles A. Brill; Frank D. Cimino

(57) **ABSTRACT**

A device for generating clock signals for use with a plurality of DDR memory devices on a dual in-line memory module (DIMM) board is provided that has a data buffer for buffering data. A clock divider divides a first clock signal (CLK**1**) having a first clock frequency to generate a second clock signal (CLK**20**) having a second clock frequency which is an integer multiple of the first clock frequency. A shift register (SH) receives the second clock signal as a data input signal, and comprises a plurality flip-flops having clock inputs coupled to receive the first clock signal (CLK**1**), and further coupled so that the data output of a preceding flip-flop is coupled to be the data input of a following flip-flop. The second clock signal is shifted through the shift register (SH) in response to the first clock signal (CLK**1**) to generate a plurality of shifted clock signals (CLK **21**, . . . , CLK**32**) at respective data outputs of the plurality of flip-flops. A multiplexer commonly coupled to the data outputs of the flip-flops selects one of the shifted clock signals (CLK **21**, . . . , CLK**32**) to serve as an output clock signal for transmission of the buffered data to a memory device.

7 Claims, 6 Drawing Sheets

Amended



Related U.S. Application Data

(60) Provisional application No. 61/016,674, filed on Dec. 26, 2007.

(58) **Field of Classification Search**
USPC 365/189.05
See application file for complete search history.

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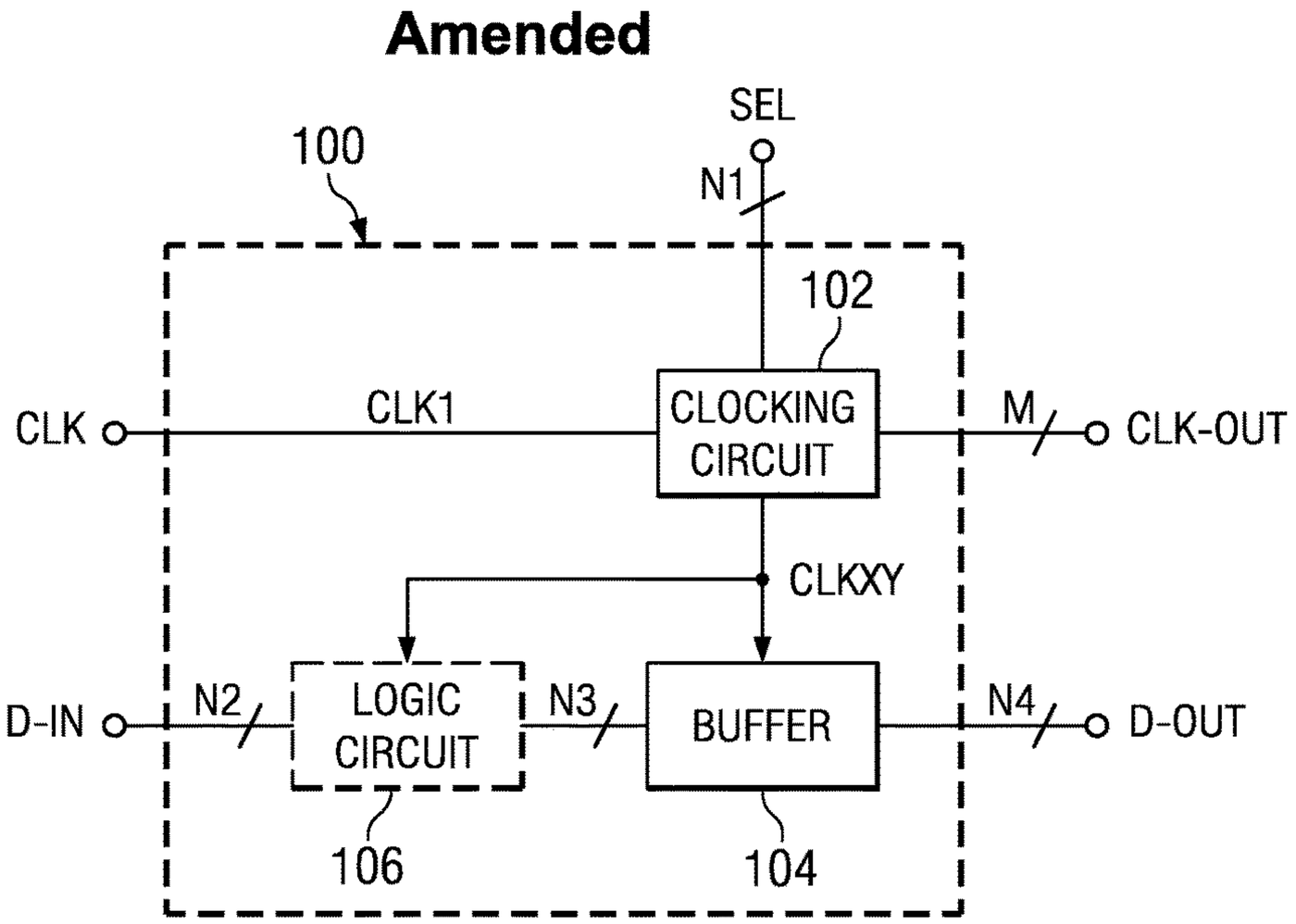

Amended
100
SEL
N1
102
CLK
CLK1
CLOCKING CIRCUIT
M
CLK-OUT
CLKXY
D-IN
N2
LOGIC CIRCUIT
N3
BUFFER
N4
D-OUT
106
104

FIG. 1

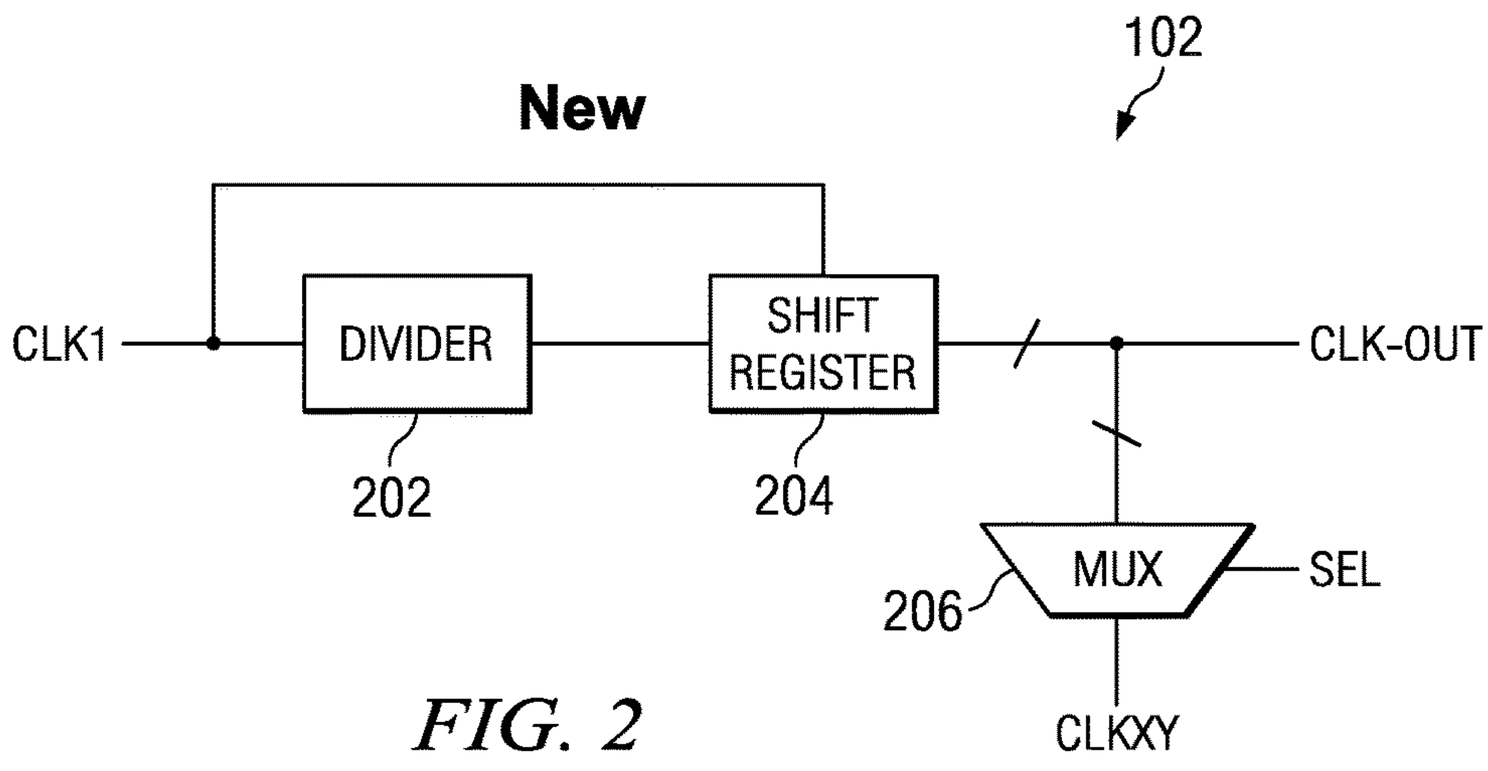
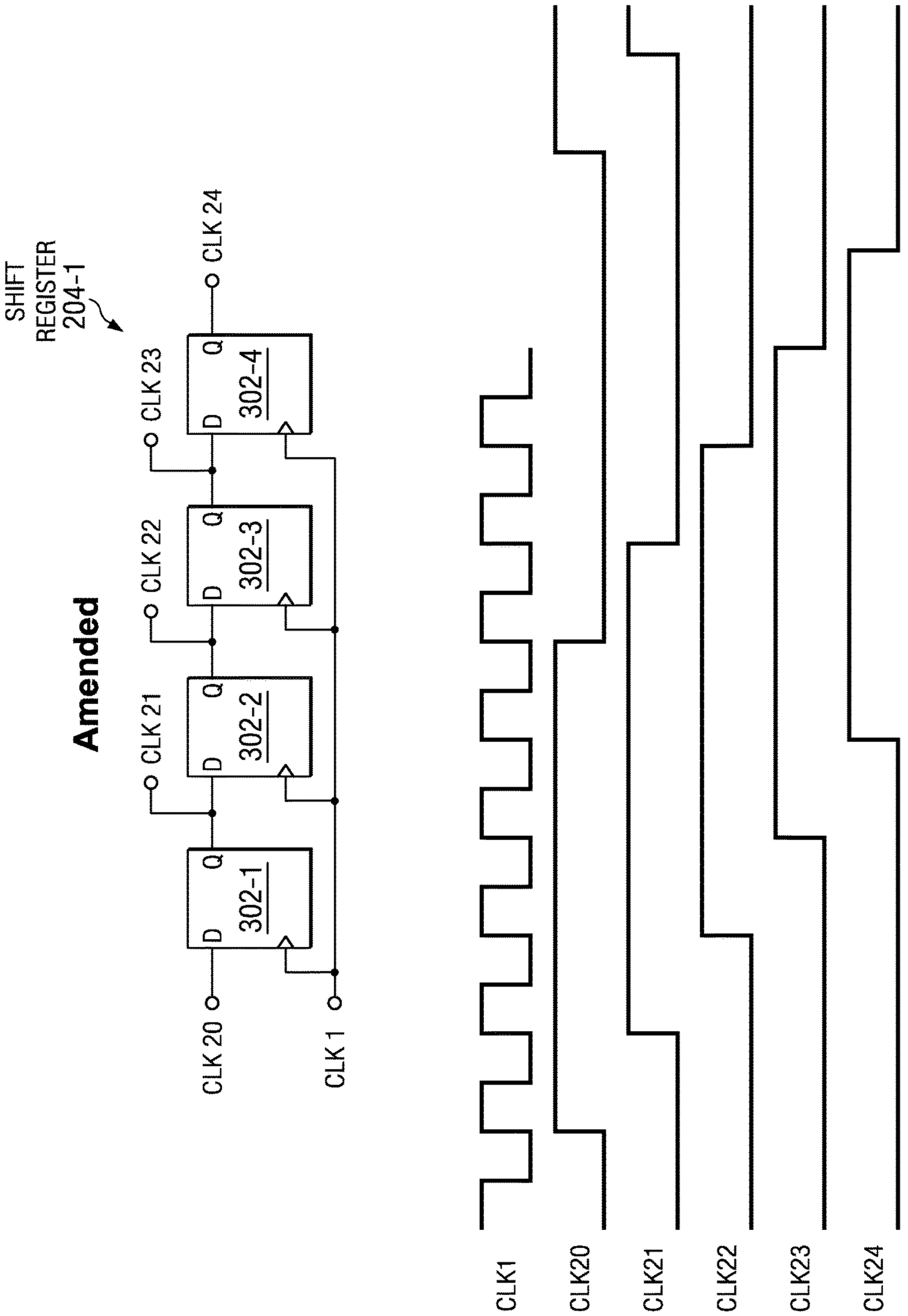

New
102
CLK1
DIVIDER
SHIFT REGISTER
CLK-OUT
202
204
MUX
SEL
206
CLKXY

FIG. 2

FIG. 3

Amended



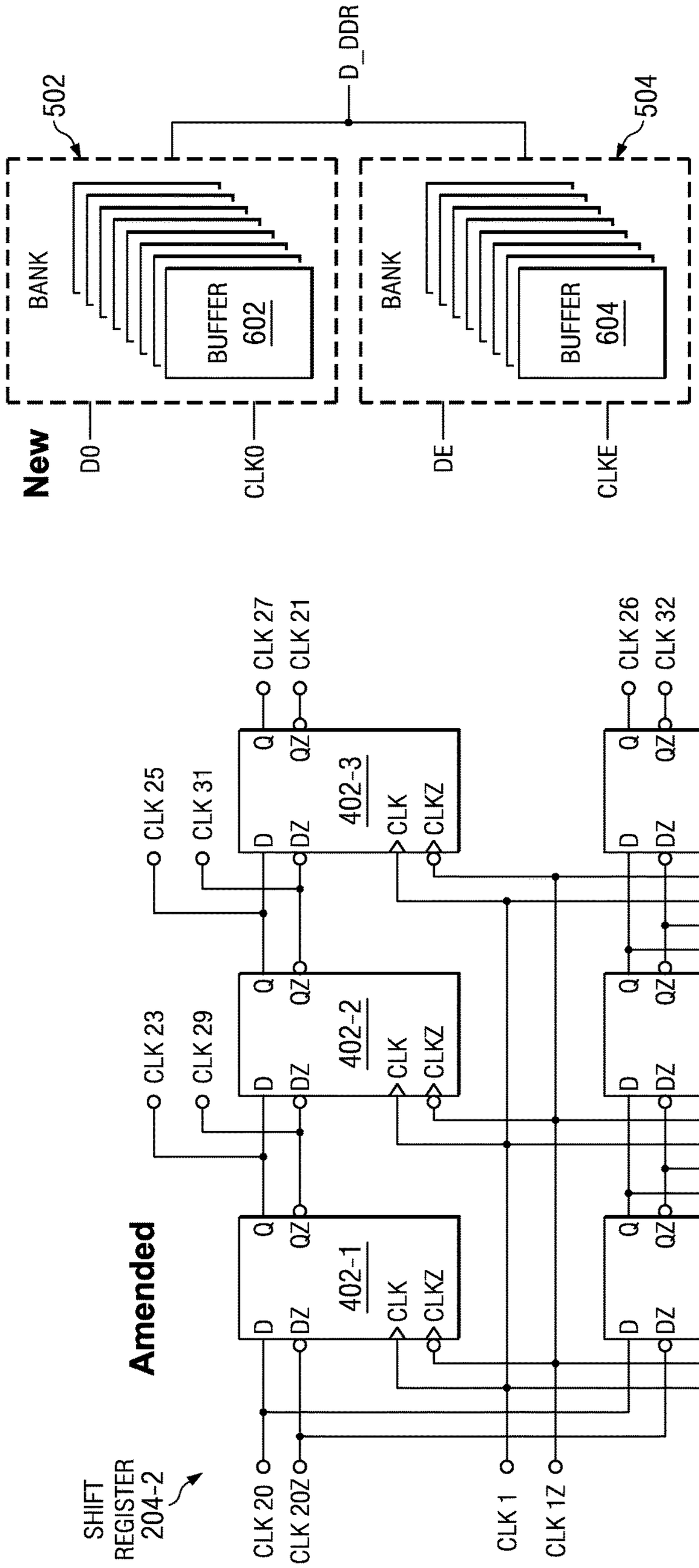


FIG. 5 (PRIOR ART)

FIG. 4

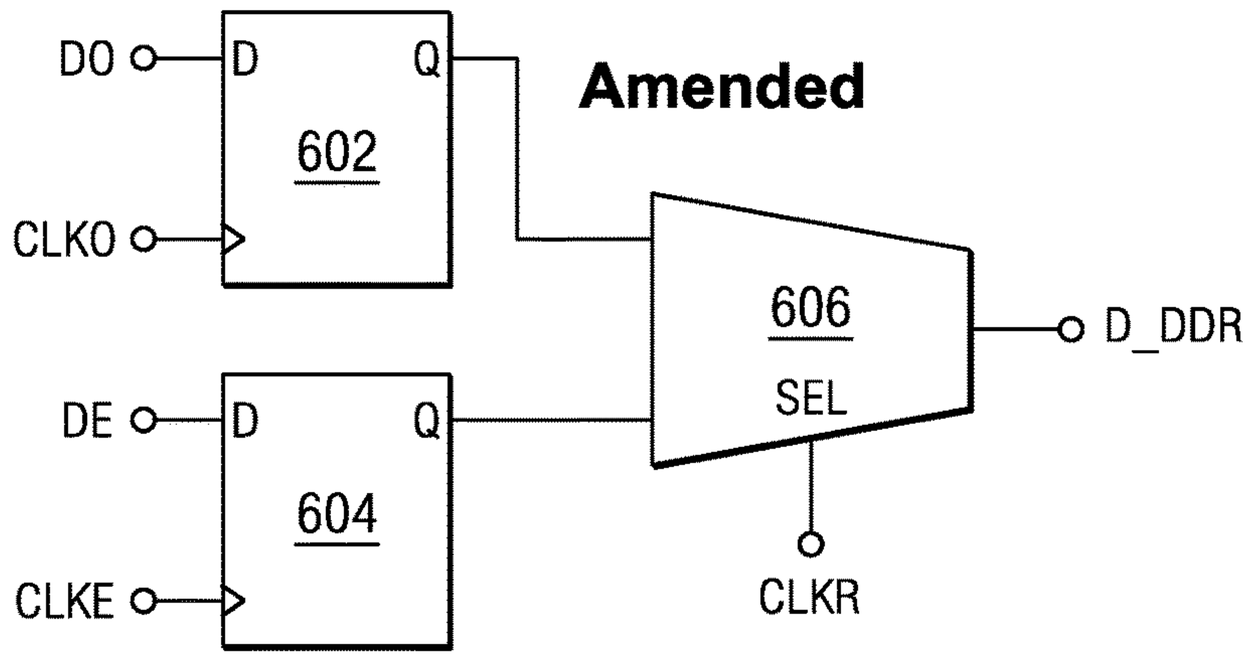


FIG. 6
(PRIOR ART)

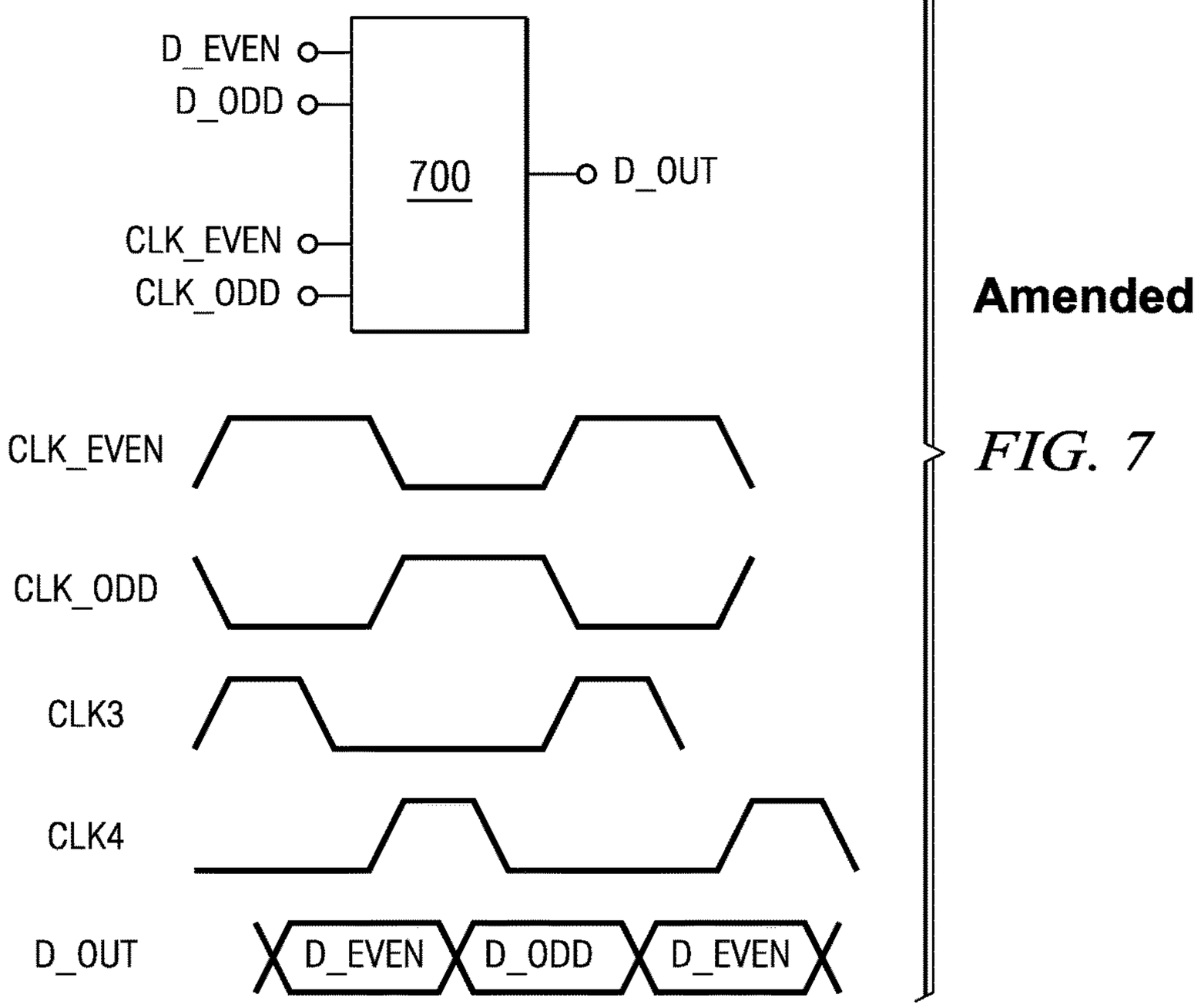


FIG. 7

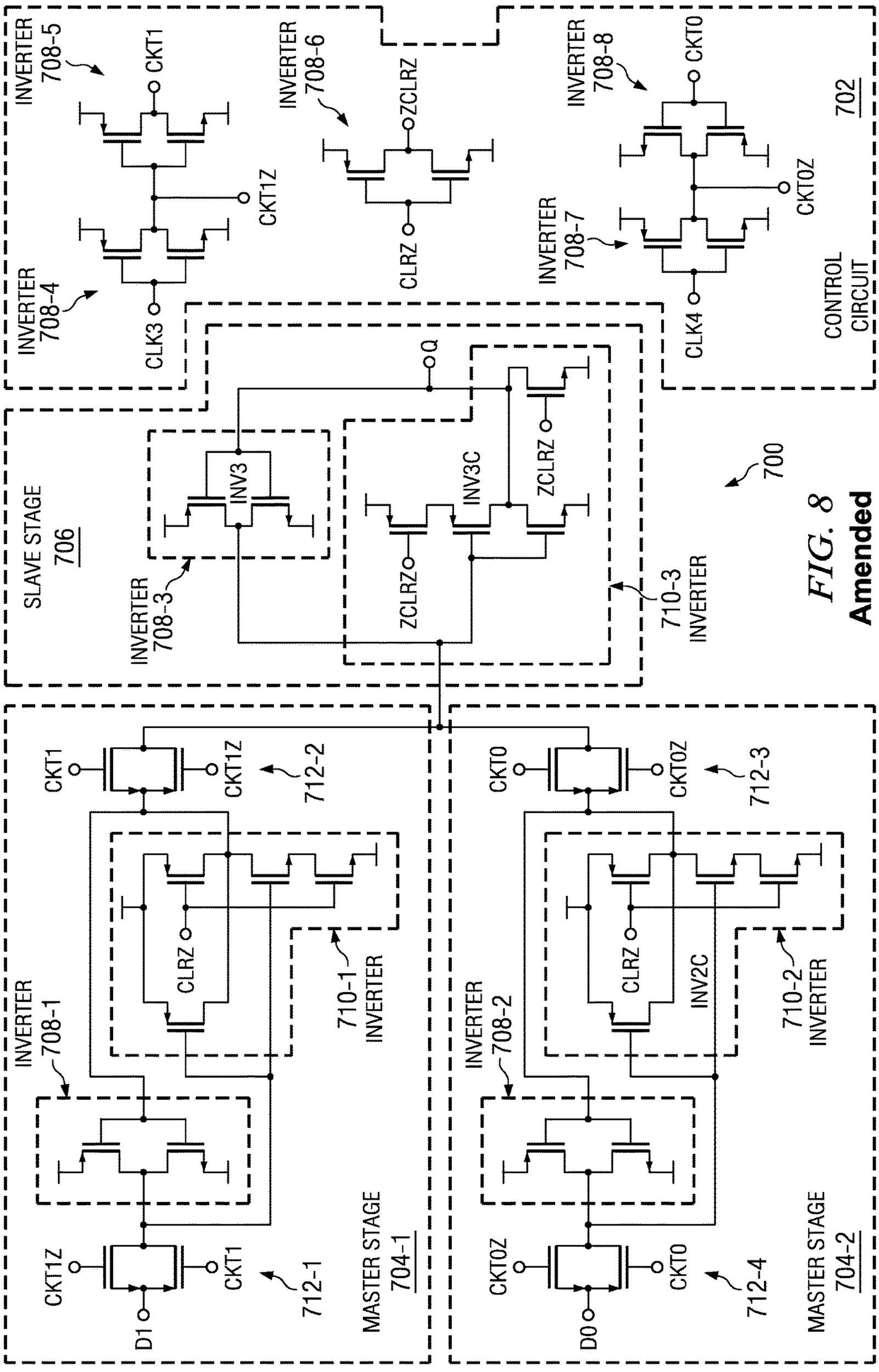


FIG. 8
Amended

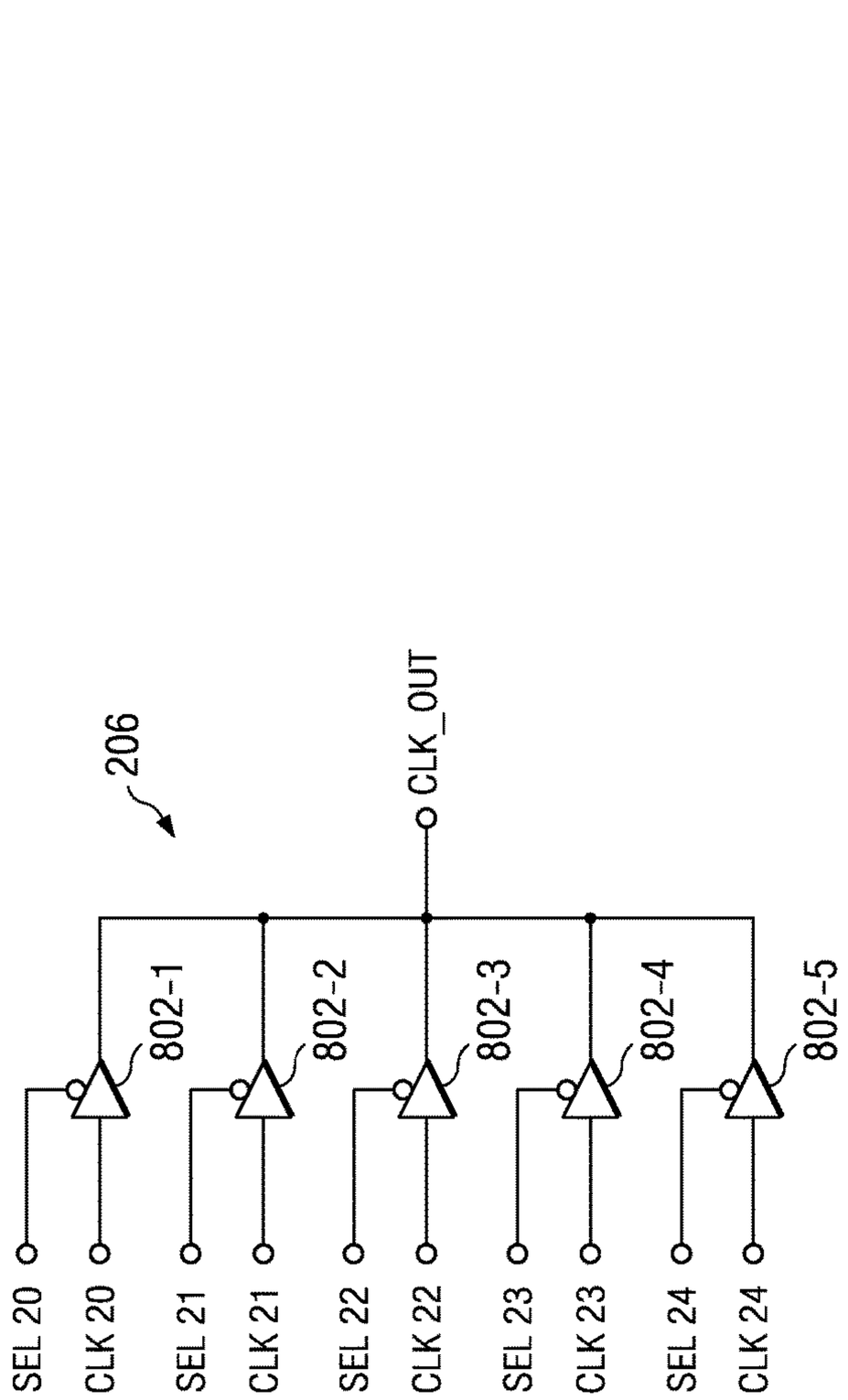


FIG. 9
Amended

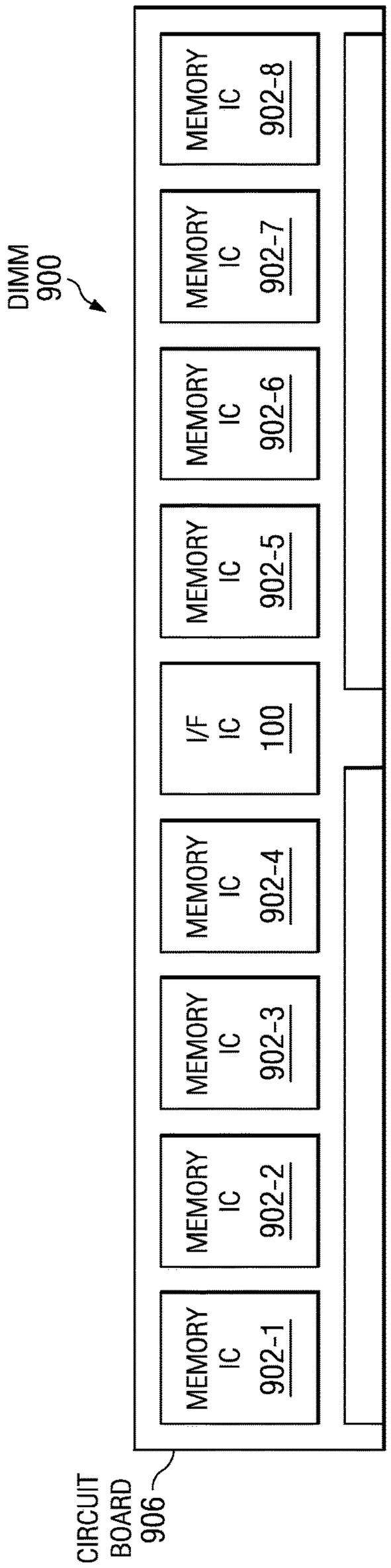


FIG. 10
New

INTEGRATED CIRCUIT FOR CLOCK GENERATION FOR MEMORY DEVICES

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue; a claim printed with strikethrough indicates that the claim was canceled, disclaimed, or held invalid by a prior post-patent action or proceeding.

[This patent application claims priority from German Patent Application No. 10 2007 020 005.8, filed 27 Apr. 2007, and from U.S. Provisional Patent Application No. 61/016,674, filed 26 Dec. 2007.]

PRIORITY/RELATED APPLICATIONS

This Application is a Reissue Divisional of application Ser. No. 13/252,779, which is a Reissue Application of U.S. Pat. No. 7,668,022, Ser. No. 12/110,684, which claims priority from German Patent Application No. 10 2007 020 005.8, filed 27 Apr. 2007, and from U.S. Provisional Patent Application No. 61/016,674, filled 26 Dec. 2007.

FIELD OF THE INVENTION

The invention relates to an integrated electronic device for generating clock signals for [DDR] *double data rate* (*DDR*) memory devices.

BACKGROUND

On a typical buffered dual in-line memory module (DIMM) board, a number of memory modules and a memory buffer are arranged. The memory buffer constitutes the interface between the memory controller and the memory modules spread over the board. The memory modules (as, for example, *Dynamic Random Access Memories or* DRAMs) require a specific and precise timing at their data, address and clock inputs. As the memory boards (DIMM boards) have a dense routing in terms of numerous wires, providing suitable and exact timing of the data and address signals, as well as the corresponding clock signals, places a high requirement on the memory buffers. If the memory buffers fail to meet the requirements, the timing at the inputs to the memory devices may be different from the timing at the corresponding outputs of the controlling devices, which may impair the overall performance of the memory systems. In order to satisfy the different timing requirements, conventional solutions shift the phase of the clock signals. For this purpose, phase locked loops (PLL) with phase mixers or delay locked loops (DLL) are used to optimize the phase relationship of a clock signal with regard to a data signal. However, PLLs and DLLs consume a considerable amount of chip area. Further, as data throughput of the memory buffering devices increases, the power consumption and the heat produced in the memory buffering devices, in particular in the DLLs and PLLs, creates problems.

SUMMARY

It is an object of the invention to provide an electronic device for generating clock signals for DDR memory devices on DIMM boards suitable to flexibly satisfy the timing requirements, while being small in size and having less power consumption and less area consumption.

An electronic device for generating clock signals for DDR memory devices on DIMM boards according to a described example embodiment is adapted to transfer data and clock signals to and/or from a plurality of memory devices on a DIMM board. The electronic device includes a data buffer for buffering data; a clock divider for dividing a first clock signal having a first clock frequency to generate a second clock signal having a second clock frequency, the second clock frequency being an integer multiple of the first clock frequency; and a shift register including multiple flip-flops. The flip-flops have clock inputs for receiving the first clock signal. The shift register receives the second clock signal as a data input signal. In the shift register, the data output of a preceding flip-flop is coupled to the data input of a following flip-flop, so as to shift the second clock signal through the shift register in response to the first clock signal, thereby generating a plurality of shifted clock signals at the outputs of the flip-flops. A multiplexer coupled to the outputs of the flip-flops for selecting a shifted clock signal serves as an output clock signal for transmission of the buffered data to a memory device.

A memory buffer according to a described embodiment exploits the presence of two different clock signals (first and second clock signals) with different clock frequencies to generate a respective phase-shifted clock output signal to be used for data transmission of the buffered data. Clock dividers and shift registers were generally considered to be inappropriate for high speed and high precision clock generation, as the jitter contributed by each flip-flop adds up. The summed jitter of the preceding flip-flops in the clock divider and the shift register may then appear in the output clock signal, rendering the clock signal unsuitable for high speed applications. Yet, based on the recognition that the first clock signal can have a sufficiently small jitter, the invention may be implemented to overcome this prejudice.

The first clock signal is processed in a clock divider, the frequency of which is a fraction of the frequency of the first clock signal. Instead of using a PLL or a DLL architecture to produce a phase-shifted clock signal with an optimum phase relationship to the data to be transmitted, the invention may be implemented to make use of a shift register which is appropriately coupled to the first and the second clock. Each flip-flop of the shift register is clocked by the first clock signal and generates at its output a phase-shifted version of the second clock signal being delayed with respect to the second clock signal by one clock cycle of the first clock for each flip-flop. The so-produced phase-shifted clock signals are fed to a multiplexer, which is adapted to select one phase-shifted clock signal to be used for data transmission of the buffered data. Dependent on the respective requirements for a specific data transmission, an optimum clock signal can be selected. Since the memory buffer according to the described embodiment does not need PLLs or DLLs, power consumption and heat generation is considerably reduced with regard to conventional solutions. The chip area consumed by the shift register is much smaller than the area required by a PLL or DLL.

The electronic device, and in particular the shift register, implemented in accordance with the invention as described, may preferably be adapted to receive, to process and to output differential signals. Accordingly, the first clock signal may be a differential clock signal and the flip-flops of the shift register are preferably adapted to be clocked by the differential first clock signal. Further, the second clock signal may be a differential clock signal and the plurality of

flip-flops of the shift register may be adapted to process the second clock signal as a differential data signal. A first group of the flip-flops of the shift register may be coupled to operate in response to a rising edge of the first clock signal, and a second group of the flip-flops of the shift register may be coupled to operate in response to a falling edge of the first clock signal, by simply interchanging the differential first clock signals at the clock inputs of the second group of flip-flops. An inverter, which would introduce unwanted phase shift, is not required. Further, according to this aspect of the implementation of the invention, only half a period of the fast clock signal is used for generating the phase-shifted derivatives of the second clock signal, which reduces granularity to half the clock period of the first clock signal (i.e., to ½ UI, where UI is a unit interval). By using differential flip-flops, any additional unwanted phase shift or skew due to inverters (or other additional gates) to produce inverted clock signals is avoided. Further, using flip-flops with differential clock and data inputs and differential data outputs allows the phase-shifted output clock signals to be produced using only half the number of flip-flops. If necessary, an electronic device according to the invention may further include clock generating means for recovering the first clock signal from the input data.

According to another aspect of the invention, the electronic device may further include circuitry for generating a third clock signal and a fourth clock signal from the first clock signal, wherein the third clock signal and the fourth clock signal are clock signals that are non-overlapping with respect to each other. Further, an electronic device according to an implementation of the invention may include a special flip-flop, which includes a first master stage for storing a first binary value in response to the third clock signal, a second master stage for storing a second binary value in response to the fourth clock, and a slave stage which is coupled to the first and the second master stages to receive and to store either the first or the second binary value in response to a fifth clock having twice the frequency of the input clock. This aspect of the invention relates to double data rate memory devices (DDR).

Data, which is to be written to the memory devices, is stored in a write FIFO for memory buffer applications. Typically, there are two banks of write FIFOs (for example, one bank for even and another bank for odd clock cycles) which run based on the second clock and an inverted second clock. The even and the odd data stored in the FIFO are re-sampled at twice the core frequency (frequency of the second clock). This usually requires use of a multiplexer, the select line of which is controlled by the core clock and a flip-flop run at twice the frequency. This conventional approach requires an additional clock having twice the clock rate of the core clock. Further, the conventional approach introduces additional latency. The approach according to some embodiments of the invention, in particular a new dual flip-flop architecture, reduces latency by at least six unit intervals (UI)—a unit interval being the length of one clock period of the first clock signal. This advantage is achieved by the newly provided architecture of the flip-flop. Accordingly, two master stages are clocked by two non-overlapping clock signals, such that single bit values are clocked into the two master stages in an alternating manner. A clock having twice the frequency of the input clock is used to clock the data from a selected one of the master stages to the single slave stage which is coupled to both master stages.

The first clock signal is source centered with respect to the data signals. Data signals in the context of the invention include command and address signals, as well as strobe signals or the like. The internal core clock of the memory buffer is preferably one of the shifted clock signals generated by the shift register. The multiplexer is preferably implemented as a tri-state solution comprising a plurality of tri-state buffers. The tri-state buffers are implemented to introduce the same phase shift relative to the respective clock signals. This is typically done by matching the layouts and wire lengths of the interconnections of the tri-state buffers. All clock signals are routed to the interface via a global clock tree with minimum skew and insertion delay, as well as balanced buffers which do not introduce duty cycle distortion. One of the shifted clock signals may be used as a core clock for generating the data as, for example, command and address signals or strobe signals.

The invention also provides a system for digital data processing. The system includes at least a DIMM board with (e.g., DDR) memory modules and an electronic device for generating clock signals and buffering data. The electronic device may be configured as set out above and include a shift register to derive a plurality of clock signals from a second clock by use of first clock, wherein the first clock has a clock frequency which is an integer multiple of the second clock. The relationship between the frequencies of the first and the second clocks may also include fractions of the first clock including, preferably, half a period of the first clock. This can be done by using, for example, rising and falling edges of the first clock.

In another aspect, the invention also provides a method for buffering data and generating clock signals for a plurality of memory modules on a DIMM board. The method according to the invention includes buffering input data for the memory modules, dividing the first clock signal (e.g., by a positive integer) to receive a second clock signal, and deriving a plurality of clock signals from the second clock signal by sequentially shifting the second signal using, e.g., the rising and/or falling edges of the first clock signal.

DETAILED DESCRIPTION OF THE DRAWINGS

Example embodiments of the invention are described below with reference to accompanying drawings, wherein:

FIG. **1** shows a simplified block diagram of an embodiment of the invention;

FIG. 2 show a simplified block diagram of the clocking circuit of FIG. 1;

FIG. **[2]** *3* shows a simplified schematic and a timing diagram of a shift register according to an embodiment of the invention;

FIG. **[3]** *4* shows a simplified schematic of a differential shift register according to an embodiment of the invention;

[FIG. **4** shows a schematic**]** *FIGS. 5 and 6 show diagrams* of **[**a**]** conventional double data rate **[**generator**]** *generators*;

FIG. **[5]** *7* shows a top level block diagram of a flip-flop according to the invention;

FIG. **[6]** *8* shows a detailed schematic of a flip-flop according to the invention; **[**and**]**

FIG. **[7]** *9* shows a clock signal selection circuit according to the invention*; and*

FIG. 10 shows a DIMM according to the invention.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[FIG.**]** *FIGS.* **1** **[**shows a**]** *and 2 show* simplified block **[**diagram**]** *diagrams* of an example implementation of *an interface integrated circuit (IC) 100 in accordance with an embodiment of* the invention. *The interface circuit 100*

generally comprises a clocking circuit 102, a data buffer 104, and an (optional) logic circuit 106. A data input receives data from a memory controller or the like (not shown). The input data D-IN applied at data input terminal has a bus width of N**2**. A clock input CLK receives a **[**first**]** clock signal CLK**1** in the form of a high speed clock. The input data D-IN comprises all kinds of data, address information and control information to be exchanged with memory modules *or ICs 902-1 to 902-8 that are secured* on a DIMM board *or circuit board 906 and are in communication with an interface IC or module 100* (*as shown in FIG. 10*). The **[**first**]**clock signal CLK**1** is divided by a clock divider *202* in **[**block DIV-SH**]** *clocking circuit 102* to derive a **[**second**]**clock signal CLK**20** (not shown in FIG. **1**) having a lower frequency. The frequency of the **[**first**]**clock signal CLK**1** will typically be an integer multiple of the frequency of the **[**second**]** clock signal CLK**20**. **[**Block DIV-SH**]** *Clocking circuit 102* also includes an internal shift register *204* (which may be similar to those described below in connection with FIGS. **[2** and **3]** *3 and 4*). The shift register *204* provides a plurality of phase-shifted derivatives of the second clock signal, a selected one of which may be chosen in response to applied selection signals SEL of bus width N**1** *by way of multiplexer 206* (*an example of which can be seen in greater detail in FIG. 9*). Clock signals CLKXY and CLK-OUT have the specific phase of one (or more in the case of a bus) of the phase-shifted derivatives of clock *signal* CLK**20**, determined according to the applied selection signals SEL.

Clock signal CLKXY is used as a core clock. *Signal* CLKXY has the same frequency as CLK**20** and a specific phase relationship with respect to *clock signals* CLK**20** and CLK**1**. The phase of *signal* CLKXY is selected by one or more of the selection signals SEL. Also, the phase-shifted clock signals at the output pins CLK_OUT of bus width M are selected by selection signals SEL. **[**The block designated by DIGL**]** *Logic circuit 106* represents *an intermediate logic circuit that can include* various additional digital logic, buffers or combinatorial logic which may be coupled between the input D-IN and an output buffer **[**BUF**2]** *104*. The bus width for data, command and address signals will vary according to the specific architecture of a particular implementation. Thus, the reference numbers N**1**, N**2**, N**3**, N**4** and M represent different possible bus width combinations.

FIG. **[2]** *3* shows in more detail an example implementation of a shift register *204-1* of the type implemented in **[**block DIV-SH**]** *clocking circuit 102*. The **[**second**]** clock signal CLK**20** is fed as an input signal to the data input D of a **[**first**]** flip-flop **[**FF**1]** *302-1*. The **[**first**]** clock signal CLK**1**, with a frequency that is an integer multiple of the frequency of the **[**second**]** clock signal *CLK20*, is fed to the clock inputs of the flip-flops *302-1 to 302-4*. The flip-flops **[**FF**1**, FF**2**, FF**3** and FF**4]** *302-1 to 302-4* are coupled in typical shift register configuration, with the output Q of each preceding flip-flop (e.g., Q of **[**FF**1]** *flip-flop 302-1*) coupled to the data input D of each following flip-flop (e.g., D of **[**FF**2]** *flip-flop 302-2*). In this way, a number of phase-shifted clock signals CLK**21**, CLK**22**, CLK**23** and CLK**24** are produced, each being shifted by one clock cycle with respect to a preceding clock signal.

FIG. **[3]** *4* shows a simplified schematic of a differential shift register *204-2* implementation according to an example embodiment of the invention. The differential shift register comprises six flip-flops **[**FF**1** to FF**6]** *402-1 to 402-6*. All flip-flops *402-1 to 402-6* receive differential clock signals CLK**1** and CLK**1**Z, where *signal* CLK**1**Z is the inverted version of *signal* CLK**1**. (A "Z" used at the end of the reference legend of a signal indicates the inverted form of the signal without the "Z"). The frequency of differential clock signals CLK**20**, CLK**20**Z is substantially smaller than the frequency of CLK**1**, CLK**1**Z. In the present embodiment, the frequency of *signal* CLK**1** may, e.g., be six times the frequency of *signal* CLK**20**. *Signal* CLK**20** can be derived from *signal* CLK**1** in known ways using a clock divider *202*. The circuit shown in FIG. **[3]** *4* serves to provide twelve derivative clock signals CLK**21[-]** *to* CLK**32** of the slower clock *signal* CLK**20**. Flip-flops **[**FF**1**, FF**2** and FF**3]** *402-1 to 402-3* are clocked by the rising edge of *signal* CLK**1**, whereas **[**FF**4**, FF**5** and FF**6]** *flip-flops 402-4 to 402-6* are clocked by the falling edge of *signal* CLK**1** (i.e., the rising edge of CLK**1**Z). This is achieved by simply interchanging the differential clock signals CLK**1**, CLK**1**Z at the clock inputs of the two groups of flips-flops. An additional inverter is not needed. Therefore, e.g., for DDR applications, using differential clock signals, such as *signals* CLK**1** and CLK**1**Z, in a fully differential approach without an inverter is particularly useful. The propagation delay of even a single inverter (or any other single gate) would introduce additional and unwanted phase shift in the range of several percent of the period of the clock signals. Because the rising and falling edges of the fast *signal* CLK**1** are used, the **[**derivative**]** *derivative signals* CLK**21**-CLK**32** are shifted with respect to each other by half the period of *signal* CLK**1** (½ UI). So, the granularity of the phase shifter is reduced to ½ UI of the fast clock *signal* CLK**1**.

Preferably, *signal* CLK**20** may be inverted before being fed to the input of the phase shifter *204-2* shown in FIG. **[3]** *4*. This may be helpful to compensate for the delays (including setup and hold times and propagation delays, etc.) of the flip-flops. The phase shifter *204-2* shown in FIG. **[3]** *4* may preferably be used in **[**the DIV-SH stage**]** *clocking circuit 102* shown in FIG. **1**. The phase shifter *204-2* may be adapted to accommodate different numbers of phase-shifted clock derivatives, as needed.

[FIG. **4** shows a simplified schematic **]** *FIGS. 5 and 6 show diagrams* of a configuration used in prior art electronic devices for double data rate data output. In the memory buffer (*similar to buffer 104*), the data to be written to the memory devices (*i.e., memory devices 902-1 to 902-8*) is to be stored in a write **[**FIFO**]** *first-in-first-out* (*FIFO*) for the different memory buffer applications. There are typically two banks *502 and 504* of write **[**first-in first-out (FIFO)**]** *FIFO* buffers **[**FF**03** and FFE**3]** *602 and 604*, which run from the core clock CLKO and the inverted core clock CLKE. The data stored in **[**FF**03** and FFE**3]** *buffers 602 and 604* is alternately fed by multiplexer **[**MUX**]** *606* to the output pin (or pins) D_DDR by a core clock CLKR having twice the frequency of the clock signals CLKO and CLKE used for the FIFOs. Therefore, the approach shown in **[**FIG. **4]** *FIGS. 5 and 6* requires an additional clock at twice the frequency of the core clock rate and adds latency.

FIG. **[5]** *7* shows a simplified block diagram of an example flip-flop *700* according to an aspect of the invention *for the data buffer 104 that can be used to form a write FIFO circuit*. As with the conventional approach *shown in FIG. 4*, two complementary clock signals CLK_EVEN and CLK_ODD are fed to the flip-flop **[**FFD**]** *700*. Further, corresponding data signals D_EVEN and D_ODD are supplied to the flip-flop *700*. In the example implementation according to the invention, the flip-flop *700* (or additional circuitry) generates two non-overlapping clock signals CLK**3** and CLK**4** as illustrated by the waveforms below the

flip-flop, and the data D_EVEN and D_ODD is source centered with respect to either *signals* CLK**3** or CLK**4**.

FIG. **[6]** *8* shows a more detailed schematic of the flip-flop *700* of FIG. **[5]** *7*. The **[**first**]** master stage *704-1* includes two transmission gates **[**T**1** and T**3]** *712-1 and 712-2* being clocked by respective clock signals CKT**1**, CKT**1**Z, where *signal* CKT**1**Z is the inverted clock with respect to *signal* CKT**1**. Further, the **[**first**]** master stage *704-1* includes **[**inverters INV**1]** *inverter 708-1* and clocked inverter **[**INV**1**C**]** *or tri-state inverter 710-1*. The **[**second**]** master stage *704-2* includes the two transmission gates **[**T**0**, T**2]** *712-4 and 712-3* and inverter **[**INV**2]** *708-2*, as well as clocked inverter **[**INV**2**C**]** *710-2*. The slave stage *706* includes **[**inverters INV**3]** *inverter 708-3* and clocked inverter **[**INV**3**C**]** *710-3*. The slave stage *706* is coupled to the outputs of both master stages *704-1 and 704-2* via transmission gates **[**T**3** and T**2]** *712-2 and 712-3*. The master stages *704-1 and 704-2* receive respective data signals D**1** and D**0**, one being the even, the other being the odd data as explained with respect to FIG. **[5]** *7*. Accordingly, the **[**first**]** master stage *704-1* stores the data received via input pin D**1** and the **[**second**]** master stage *704-2* stores the data received via input pin D**0**. The clock signals CKT**1**, CKT**1**Z, CKT**0**, CKT**0**Z may be derived in known ways from the third and the fourth clock signals CLK**3** and CLK**4** shown in FIG. **[5]** *7 using control circuit 702*. Further, an inverted **[**version**]** *signal* ZCLRZ of the clock signal CLRZ (*which can function as a select signal similar to signal CLKR of FIG. 4*) is produced by inverter **[**INV**4]** *708-6*. Inverters **[**INV**5**-INV**8]** *708-4, 708-5, 708-7 and 708-8* are used for clock signals CKT**1**, CKT**1**Z, CKT**0**, CKT**0**Z.

With respect to the prior art circuit shown in **[**FIG. **4]** *FIGS. 5 and 6*, the flip-flop **[**implementation**]** *700* according to the invention saves a considerable amount of chip area. Each of the flip-flops **[**shown in FIG. **5]** *700* includes at least a master and a slave stage. The invention provides the same, or even a better functionality in terms of speed and power dissipation, and saves the multiplexer, the control logic and signals for the multiplexer and a slave stage.

FIG. **[7]** *9* shows an example of a *multiplexer 206 that employs* tri-state **[**buffer**]** *buffers or inverters 802-1 to 802-5* according to the invention. The clock signals CLK**20**, CLK**21**, CLK**22**, CLK**23** and CLK**24** are supplied, respectively, to **[**a number of**]** tri-state buffers *802-1 to 802-5*, each having a corresponding selection input SEL**20**, SEL**21**, SEL**22**, SEL**23** and SEL**24**. The output signal CLK_OUT is selected from the phase-shifted clock input signals CLK**20[-]** *to* CLK**24** in response to the applied selection signals. The *unselected* tri-state buffers **[**of the clock signals which are not selected**]** (*i.e., 802-1*) can be set in a high impedance state. The **[**tri-state buffer**]** *multiplexer 206* may preferably be used in the **[**DIV-SH block of FIG. **1]** *clocking circuit 102*. The tri-state buffer may be adapted to any specific number of phase-shifted derivatives of the clock signals.

Those skilled in the art to which the invention relates will appreciate that the described implementations are merely representative examples, and that many other implementations are possible within the scope of the claimed invention.

What is claimed is:

[1. A device for generating clock signals in association with a plurality of DDR memory devices on a dual in-line memory module (DIMM) board, the electronic device comprising:

a data buffer for buffering data;

a clock divider for dividing a first clock signal having a first clock frequency to generate a second clock signal having a second clock frequency, the second clock frequency being an integer multiple of the first clock frequency;

a shift register coupled to receive the second clock signal as a data input signal; the shift register comprising a plurality flip-flops having clock inputs coupled to receive the first clock signal, and being further coupled so that a data output of a preceding flip-flop is coupled to a data input of a following flip-flop so as to shift the second clock signal through the shift register in response to the first clock signal, thereby generating a plurality of shifted clock signals at the respective data outputs of the plurality of flip-flops; and

a multiplexer commonly coupled to the data outputs of the flip-flops for selecting a shifted clock signal to serve as an output clock signal for transmission of the buffered data to a memory device.**]**

[2. The device of claim **1**, wherein the first clock signal is a differential clock signal and the plurality of flip-flops are coupled to be clocked by the differential first clock signal.**]**

[3. The device of claim **1**, wherein the second clock signal is a differential clock signal and the plurality of flip-flops are coupled to process the second clock signal as a differential data signal.**]**

[4. The device of claim **1**, wherein a first group of the flip-flops is coupled to operate in response to a rising edge of the first clock signal, and a second group of the flip-flops is coupled to operate in response to a falling edge of the first clock signal. by coupling the second group of flip-flops.**]**

[5. The electronic device of claim **1**, further comprising a clock generator for recovering the first clock signal from input data.**]**

[6. The device of claim **1**, further comprising;

circuitry for generating a third clock signal and a fourth clock signal from the first clock signal; wherein the third clock signal and the fourth clock signal are non-overlapping with respect to each other;

a flip-flop circuit comprising a first master stage for storing a first binary value in response to the third clock signal and a second master stage for storing a second binary value in response to the fourth clock signal; and a slave stage coupled to the first and the second master stages, to receive and to store either a first or the second binary value in response to a fifth clock signal having twice the frequency of an input clock.**]**

[7. A system for digital data processing, comprising at least one DIMM board having multiple memory modules and a device for generating clock signals in association with a plurality of DDR memory devices on a dual in-line memory module (DIMM) board, the device comprising:

a data buffer for buffering data;

a clock divider for dividing a first clock signal having a first clock frequency to generate a second clock signal having a second clock frequency, the second clock frequency being an integer multiple of the first clock frequency;

a shift register coupled to receive the second clock signal as a data input signal; the shift register comprising a plurality flip-flops having clock inputs coupled to receive the first clock signal, and being further coupled so that a data output of a preceding flip-flop is coupled to a data input of a following flip-flop so as to shift the second clock signal through the shift register in response to the first clock signal, thereby generating a plurality of shifted clock signals at the respective data outputs of the plurality of flip-flops; and

a multiplexer commonly coupled to the data outputs of the flip-flops for selecting a shifted clock signal to serve as an output clock signal for transmission of the buffered data to a memory device.]

[8. A method for generating clock signals for a plurality of memory modules on a DIMM board, comprising:

buffering input data to be transferred to the memory modules;

dividing a first clock signal to derive a second clock signal; and

deriving a plurality of additional clock signals from the second clock signal by sequentially shifting the second clock signal according to timing established by at least one of the rising edges and falling edges of the first clock signal.]

9. A dual in-line memory module (DIMM) comprising:

a circuit board;

a plurality of memory integrated circuits (ICs), wherein each memory IC is secured to the circuit board; and

an interface IC that is secured to the circuit board and that is in communication with at least one of the memory ICs, wherein the interface IC buffers input data, and wherein the interface IC divides a first clock signal to derive a second clock signal, and wherein the interface IC derives a set of clock signals from the second clock signal by sequentially shifting the second clock signal according to timing established by at least one of the rising edges and falling edges of the first clock signal.

10. The DIMM of claim 9, wherein the interface IC further comprises:

a data buffer;

a clock divider for dividing the first clock signal having a first clock frequency to generate the second clock signal having a second clock frequency, the first clock frequency being an integer multiple of the second clock frequency;

a shift register coupled to receive the second clock signal as a data input signal, wherein the shift register comprising a plurality flip-flops having clock inputs coupled to receive the first clock signal, and being further coupled so that a data output of a preceding flip-flop is coupled to a data input of a following flip-flop so as to shift the second clock signal through the shift register in response to the first clock signal, thereby generating a plurality of shifted clock signals at the respective data outputs of the plurality of flip-flops; and

a multiplexer commonly coupled to the data outputs of the flip-flops for selecting a shifted clock signal to serve as an output clock signal for transmission of the buffered data.

11. The DIMM of claim 10, wherein the first clock signal is a differential clock signal and the plurality of flip-flops are coupled to be clocked by the differential first clock signal.

12. The DIMM of claim 10, wherein the second clock signal is a differential clock signal and the plurality of flip-flops are coupled to process the second clock signal as a differential data signal.

13. The DIMM of claim 10, wherein a first group of the flip-flops is coupled to operate in response to a rising edge of the first clock signal, and a second group of the flip-flops is coupled to operate in response to a falling edge of the first clock signal, by coupling the second group of flip-flops.

14. The DIMM of claim 10, further comprising a clock generator for recovering the first clock signal from input data.

15. The DIMM of claim 10, further comprising:

circuitry for generating a third clock signal and a fourth clock signal from the first clock signal; wherein the third clock signal and the fourth clock signal are non-overlapping with respect to each other;

a flip-flop circuit comprising a first master stage for storing a first binary value in response to the third clock signal and a second master stage for storing a second binary value in response to the fourth clock signal; and

a slave stage coupled to the first and the second master stages, to receive and to store either a first or the second binary value in response to a fifth clock signal having twice the frequency of an input clock.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : RE46,754 E
APPLICATION NO. : 14/568464
DATED : March 13, 2018
INVENTOR(S) : Goller

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification

At Column 1, please delete Lines 13-25 (approx.) in their entirety, and replace with the following:
--CROSS-REFERENCE TO RELATED APPLICATIONS
NOTICE: More than one reissue application has been filed for the reissue of U.S. Patent No. 7,668,022 B2. The reissue applications are U.S. Reissue Patent Application Serial Nos. 14/568,464 (the present application), filed on December 12, 2014, now U.S. Reissue Patent No. RE46,754 E, issued March 3, 2018, which is a divisional reissue application of U.S. Reissue Patent Application Serial No. 13/252,779, filed on October 4, 2022, now U.S. Reissue Patent No. RE45,359 E, issued February 3, 2015, which is a reissue application of U.S. Patent Application Serial No. 12/110,684, filed on April 28, 2008, now U.S. Patent No. 7,668,022 B2, issued February 23, 2010, which claims priority under 35 USC § 119 to each of U.S. Provisional Patent Application No. 61/016,674, filed on December 26, 2007, now expired, and German Patent Application No. DE 10 2007 020 005.8, filed on April 27, 2007.--

Signed and Sealed this
Eighteenth Day of October, 2022

Katherine Kelly Vidal

Katherine Kelly Vidal
Director of the United States Patent and Trademark Office