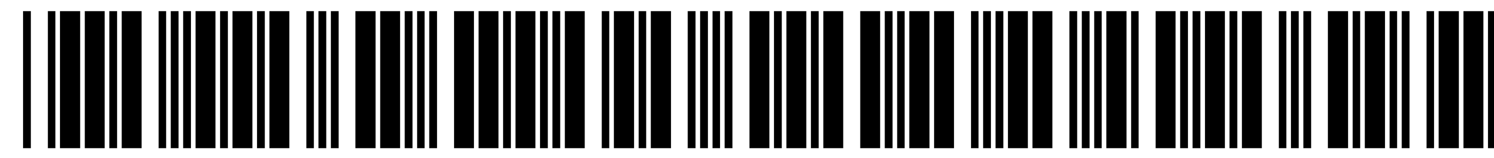
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(54) **SWITCHING DEVICE HAVING A NON-LINEAR ELEMENT**

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(58) **Field of Classification Search**
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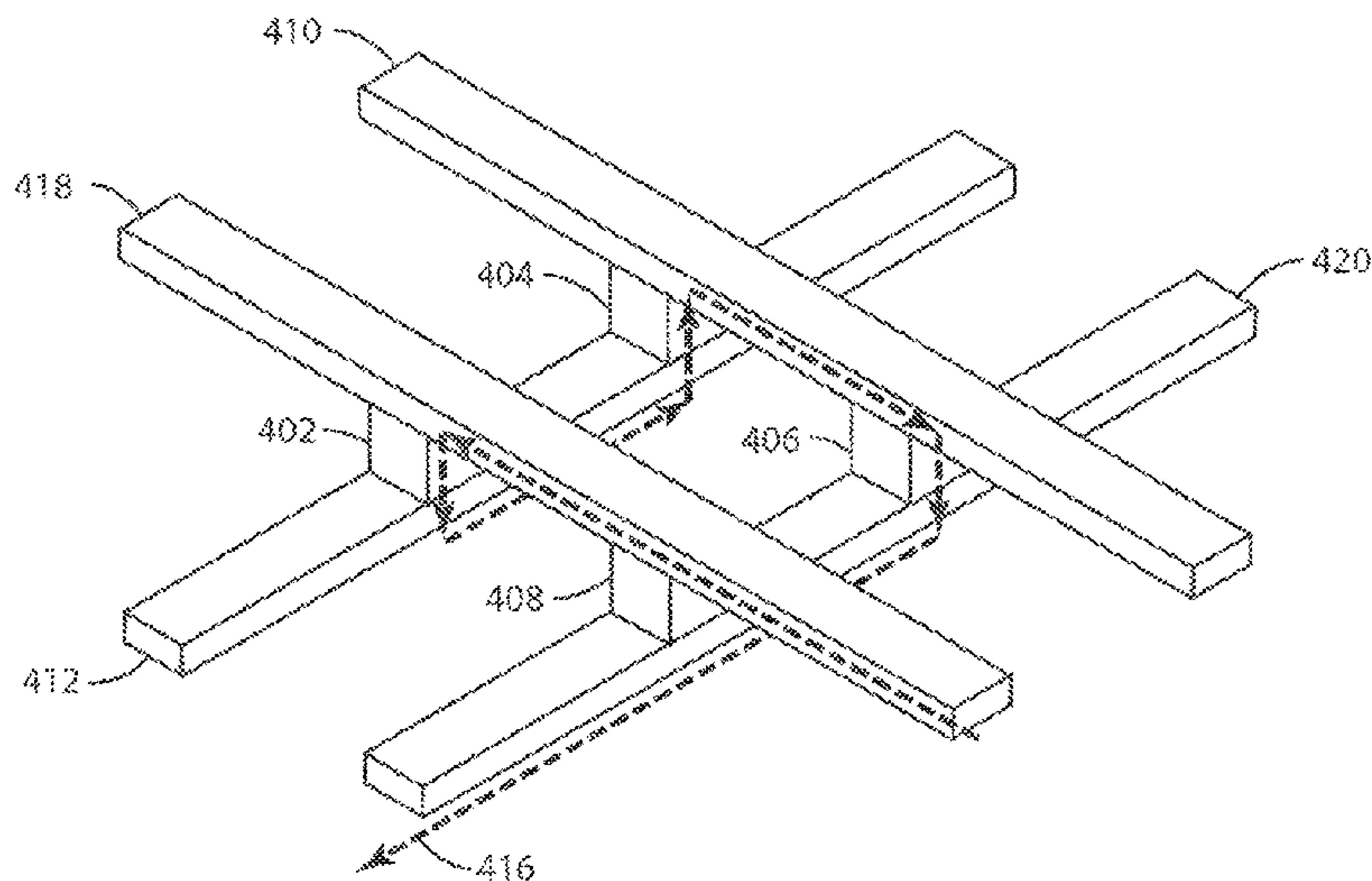
(57) **ABSTRACT**

Method for a memory including a first, second, third and fourth cells include applying a read, program, or erase voltage, the first and second cells coupled to a first top interconnect, the third and fourth cells coupled to a second top interconnect, the first and third cells coupled to a first bottom interconnect, the second and fourth cells are to a second bottom interconnect, each cell includes a switching material overlying a non-linear element (NLE), the resistive switching material is associated with a first conductive threshold voltage, the NLE is associated with a lower, second conductive threshold voltage, comprising applying the read voltage between the first top and the first bottom electrode to switch the NLE of the first cell to conductive, while the NLEs of the second, third, and the fourth cells remain non-conductive, and detecting a read current across the first cell in response to the read voltage.

32 Claims, 9 Drawing Sheets



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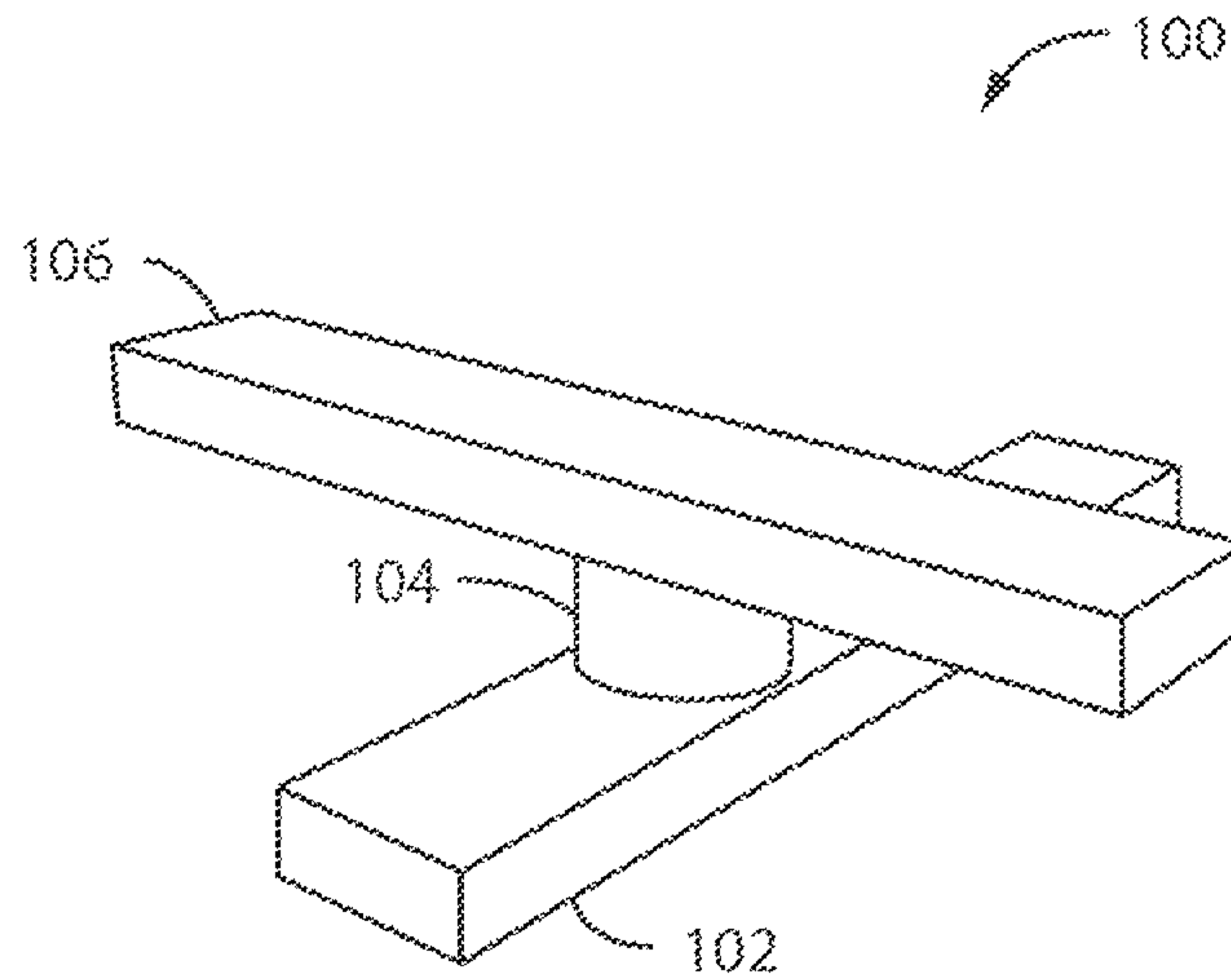

FIG. 1

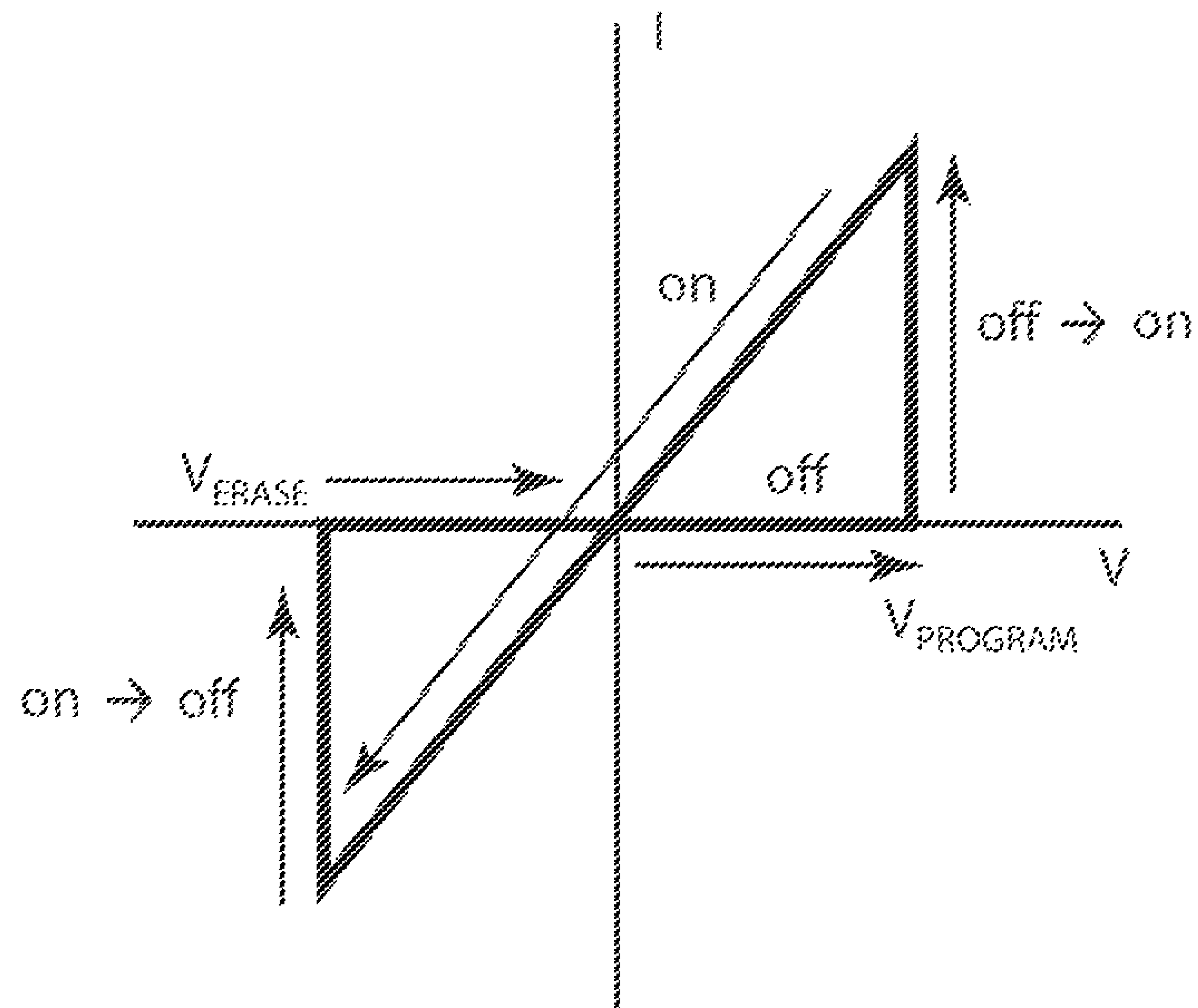

FIG. 2

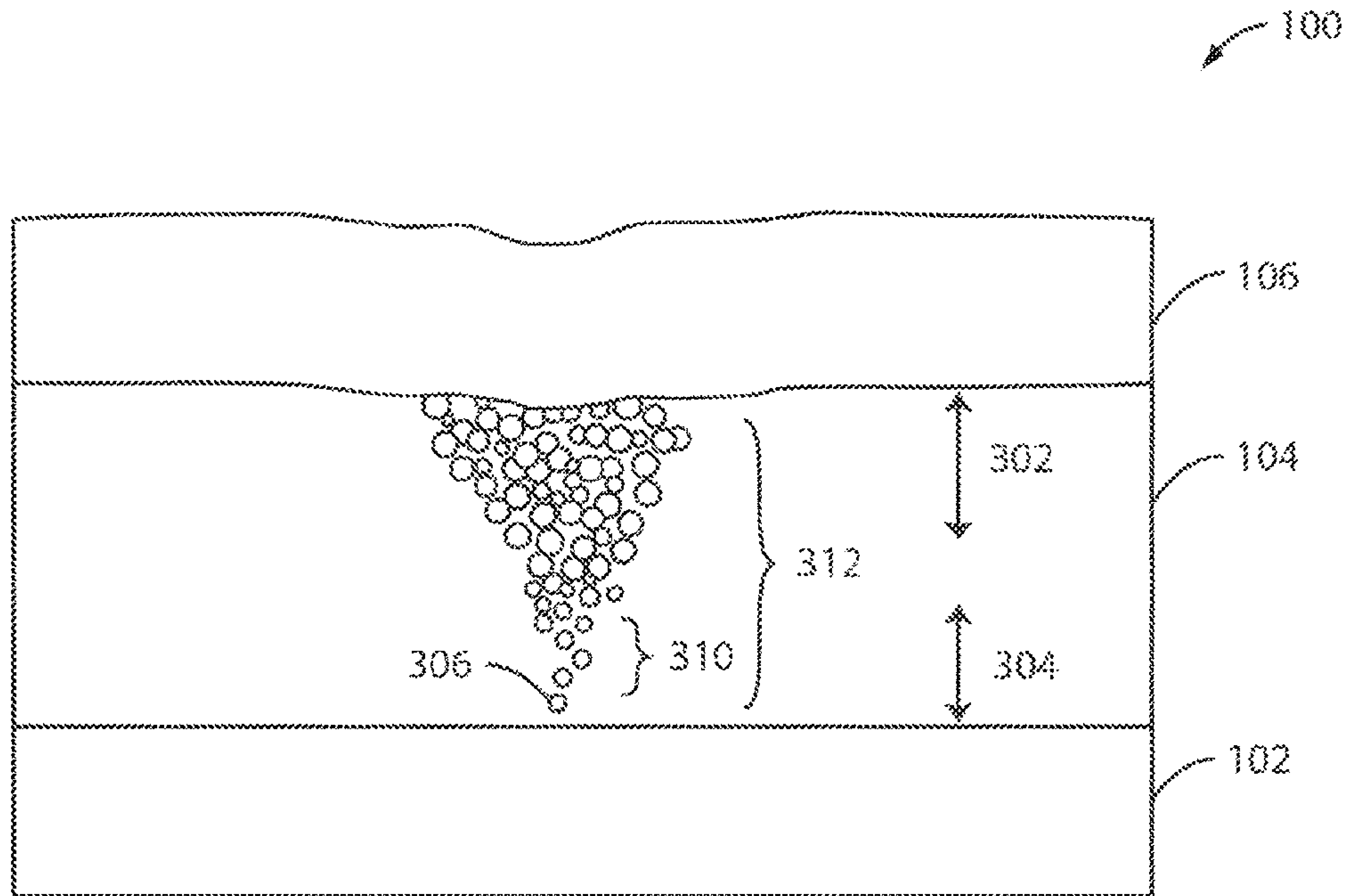

FIG. 3A

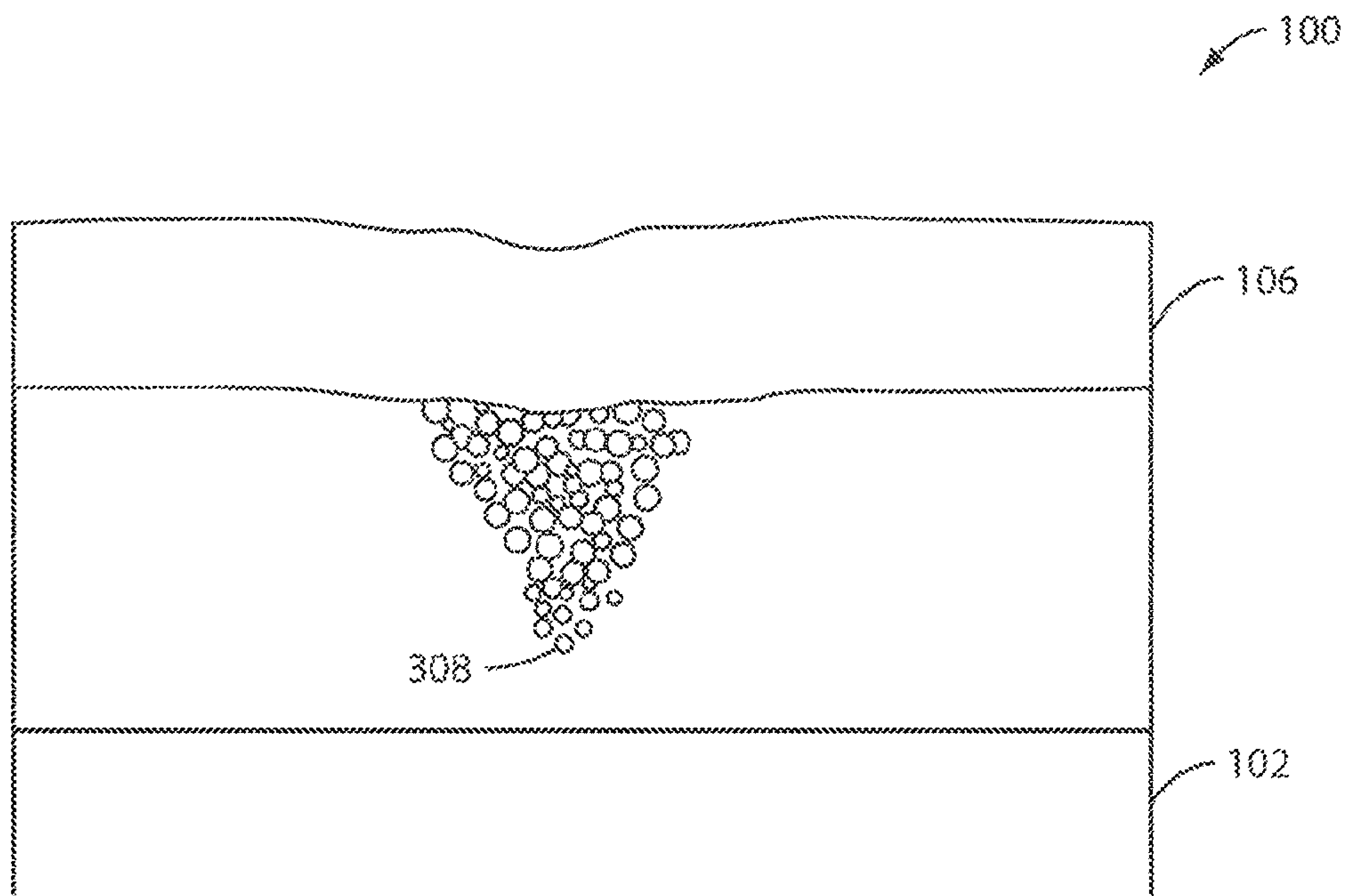

FIG. 3B

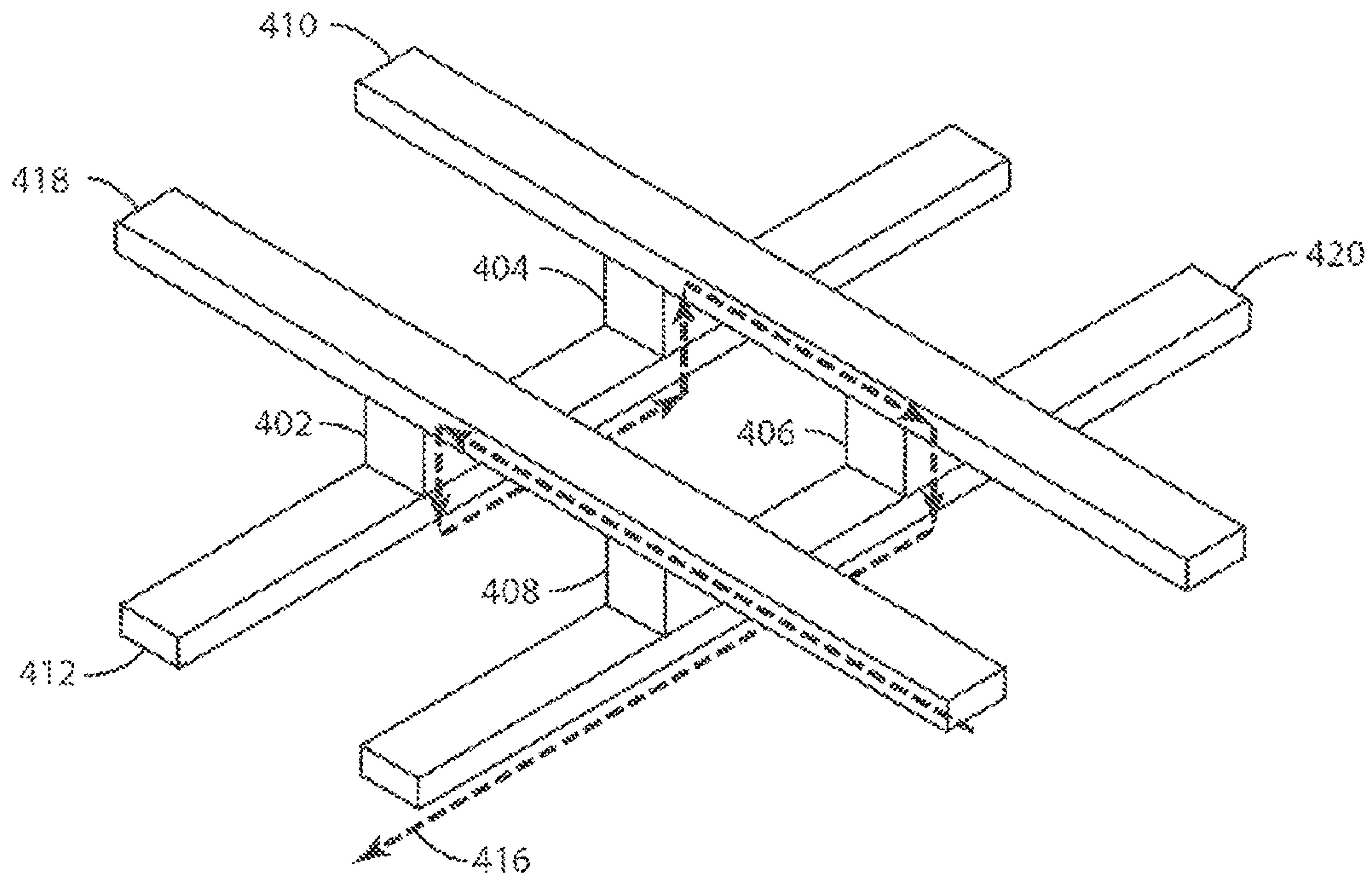

FIG. 4

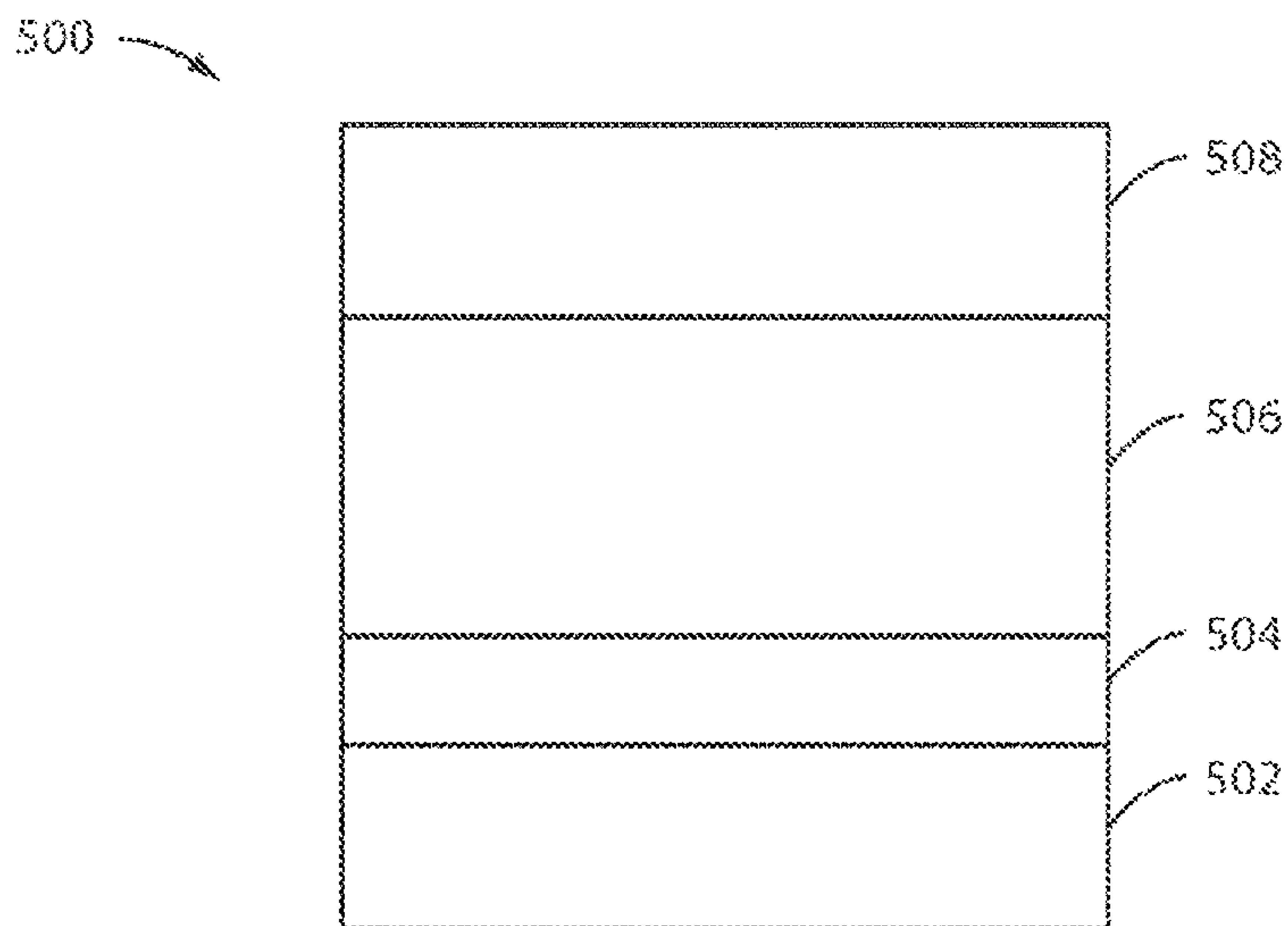

FIG. 5

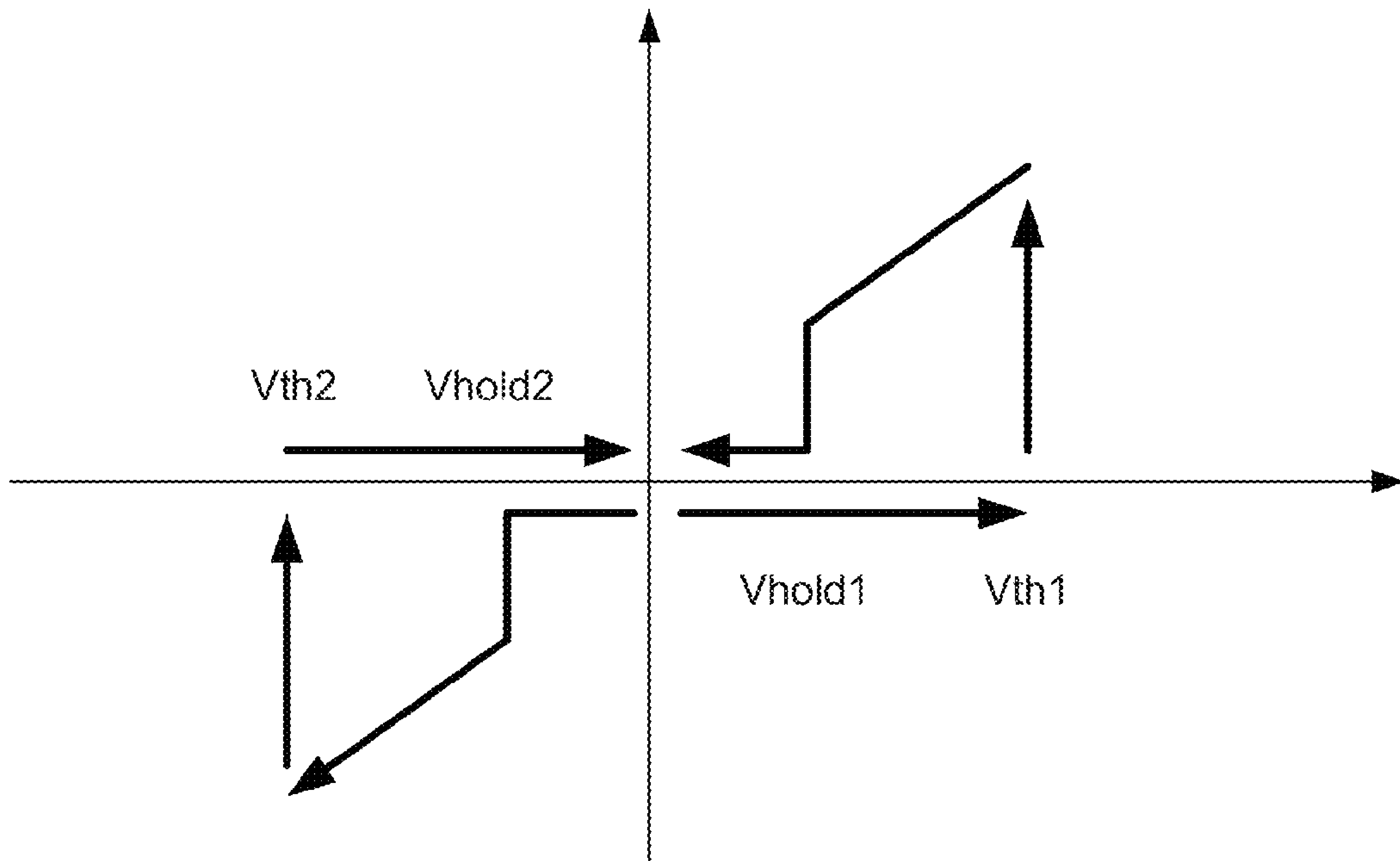

FIG. 6A

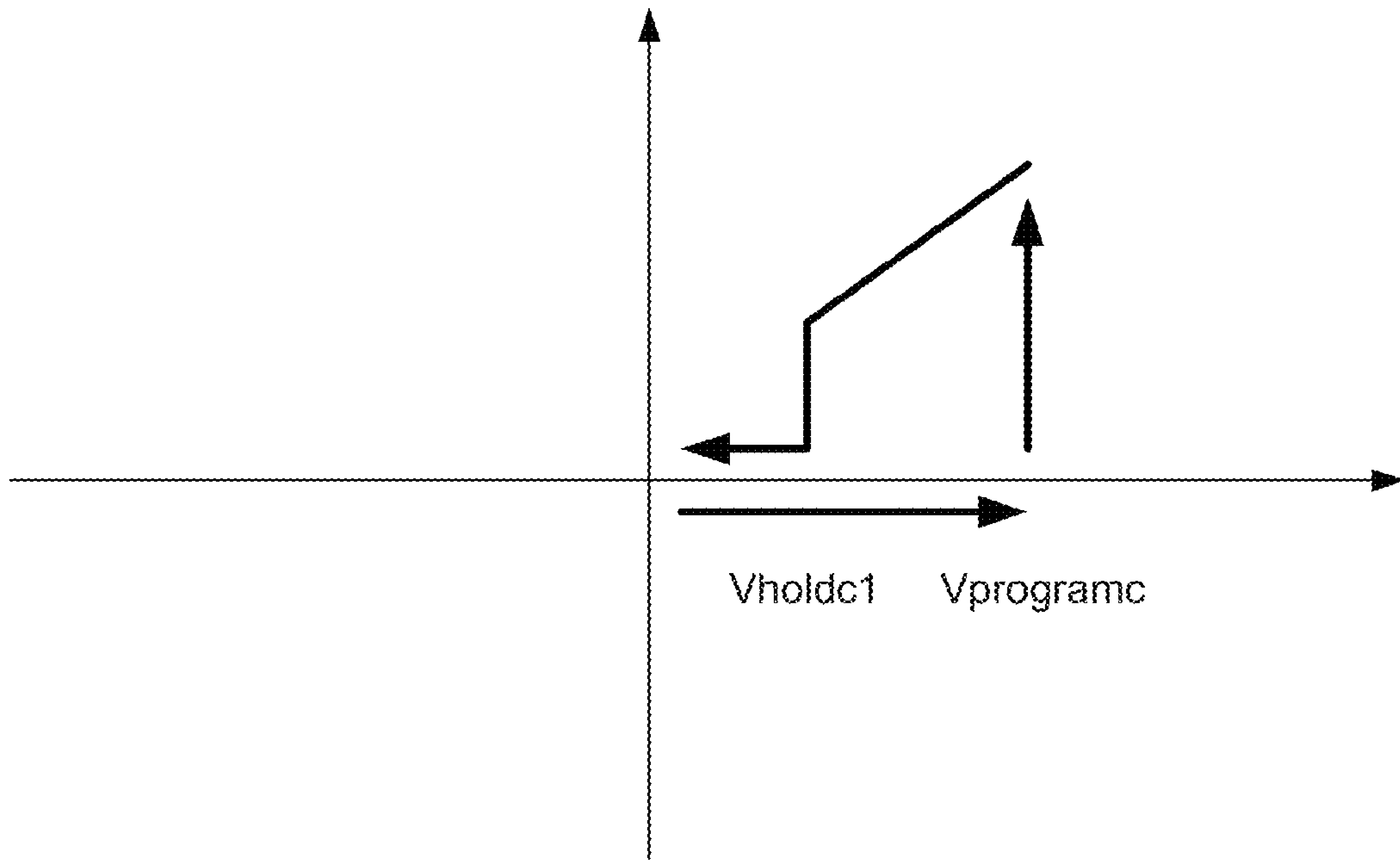

FIG. 6B

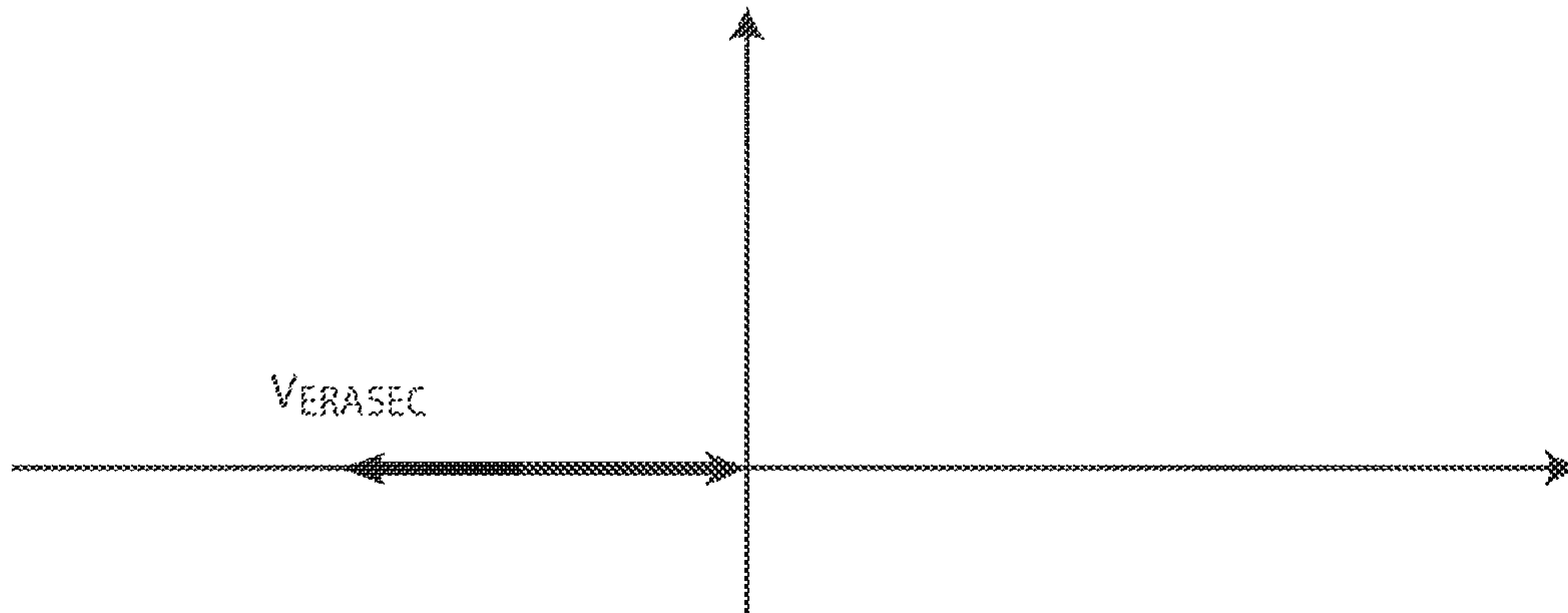

FIG. 6C

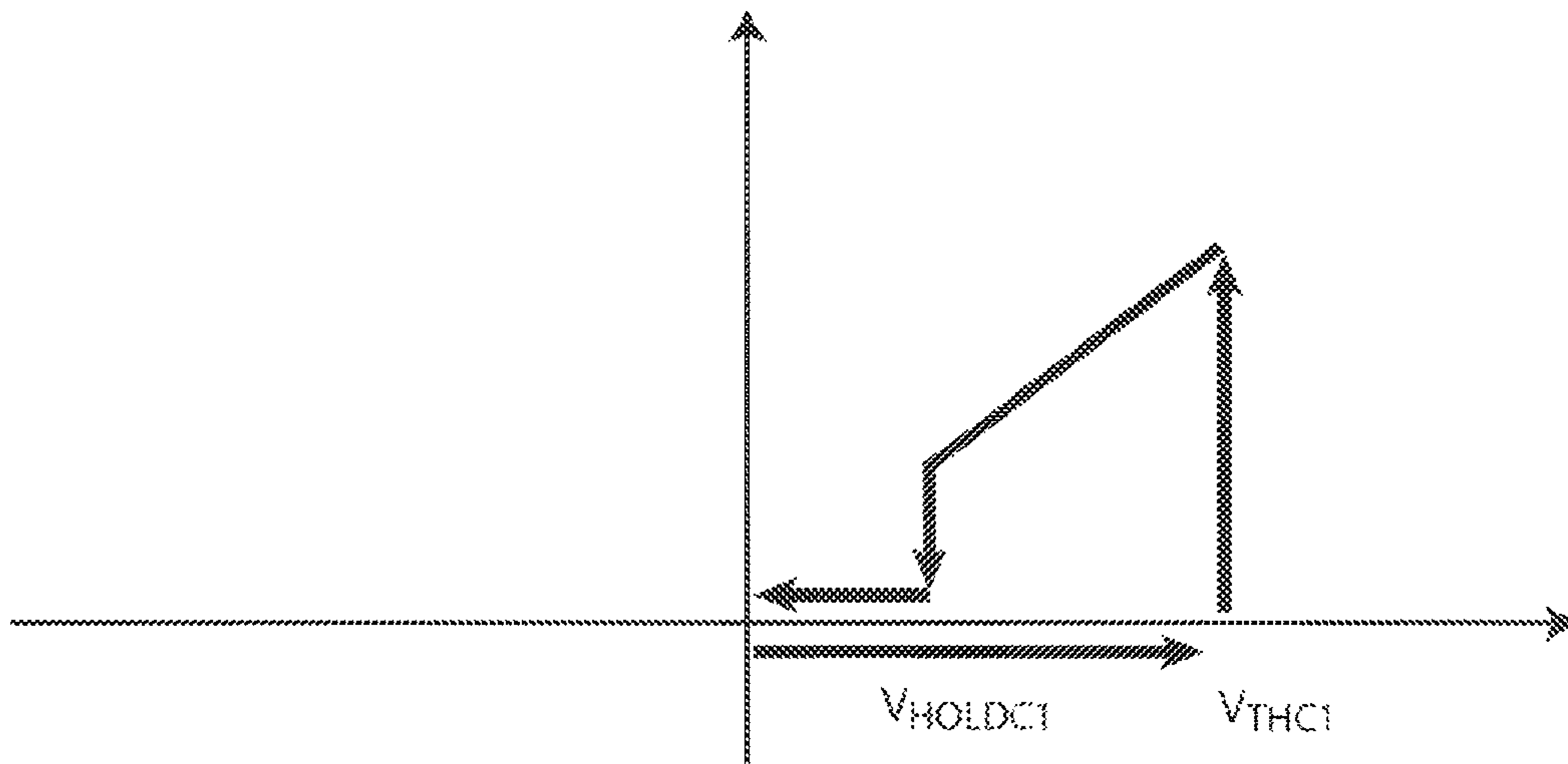

FIG. 6D

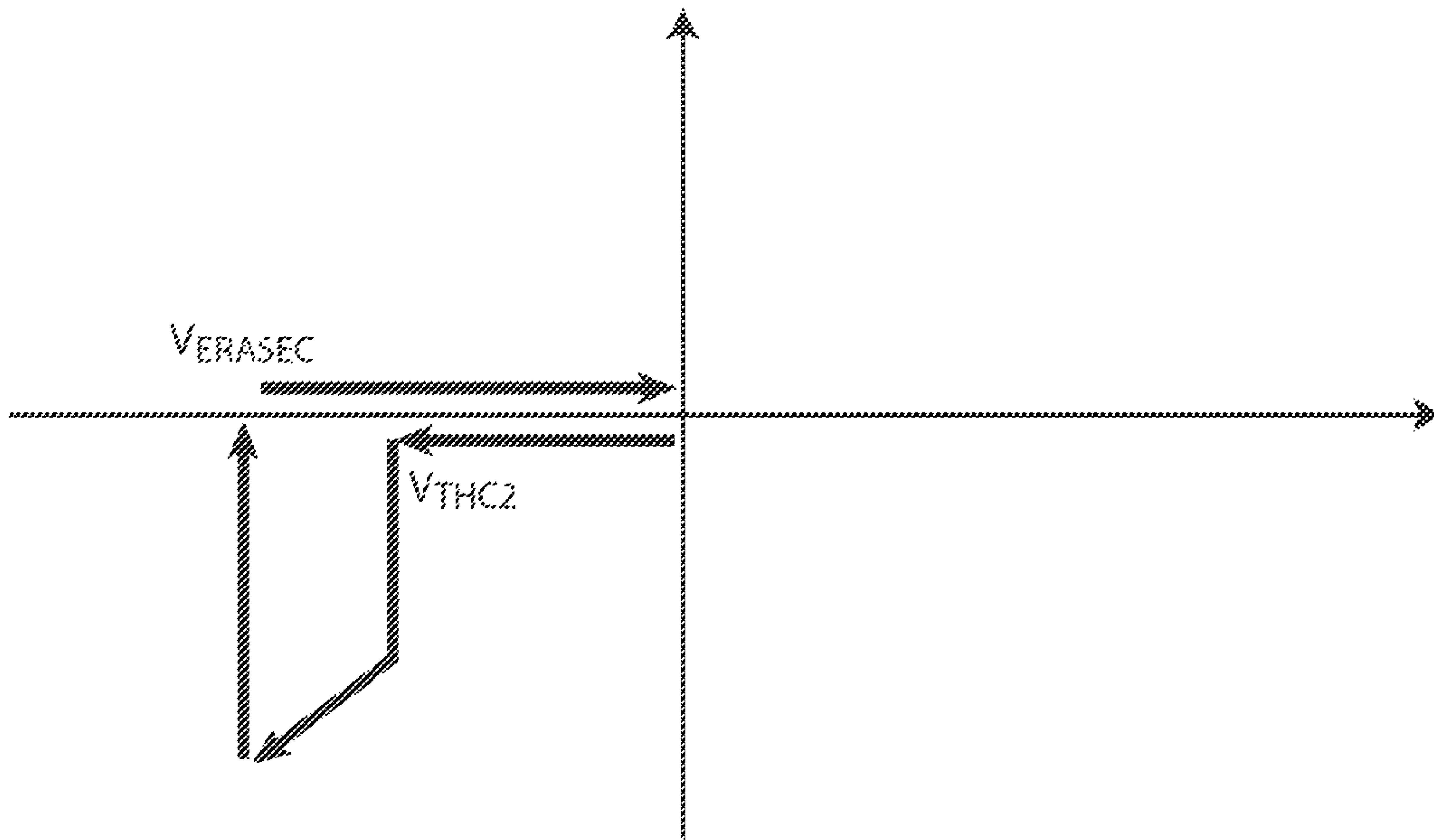

FIG. 6E

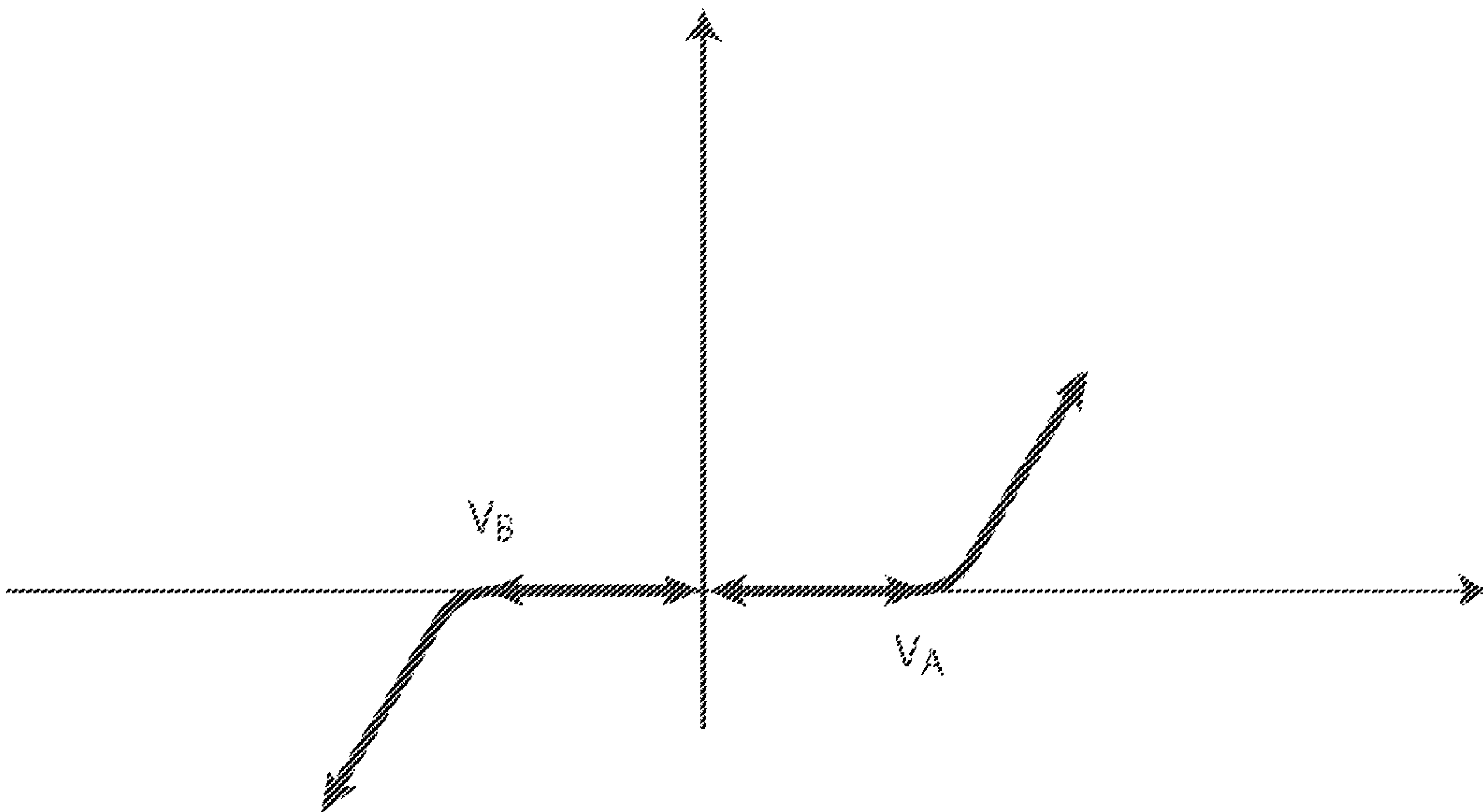

FIG. 7A

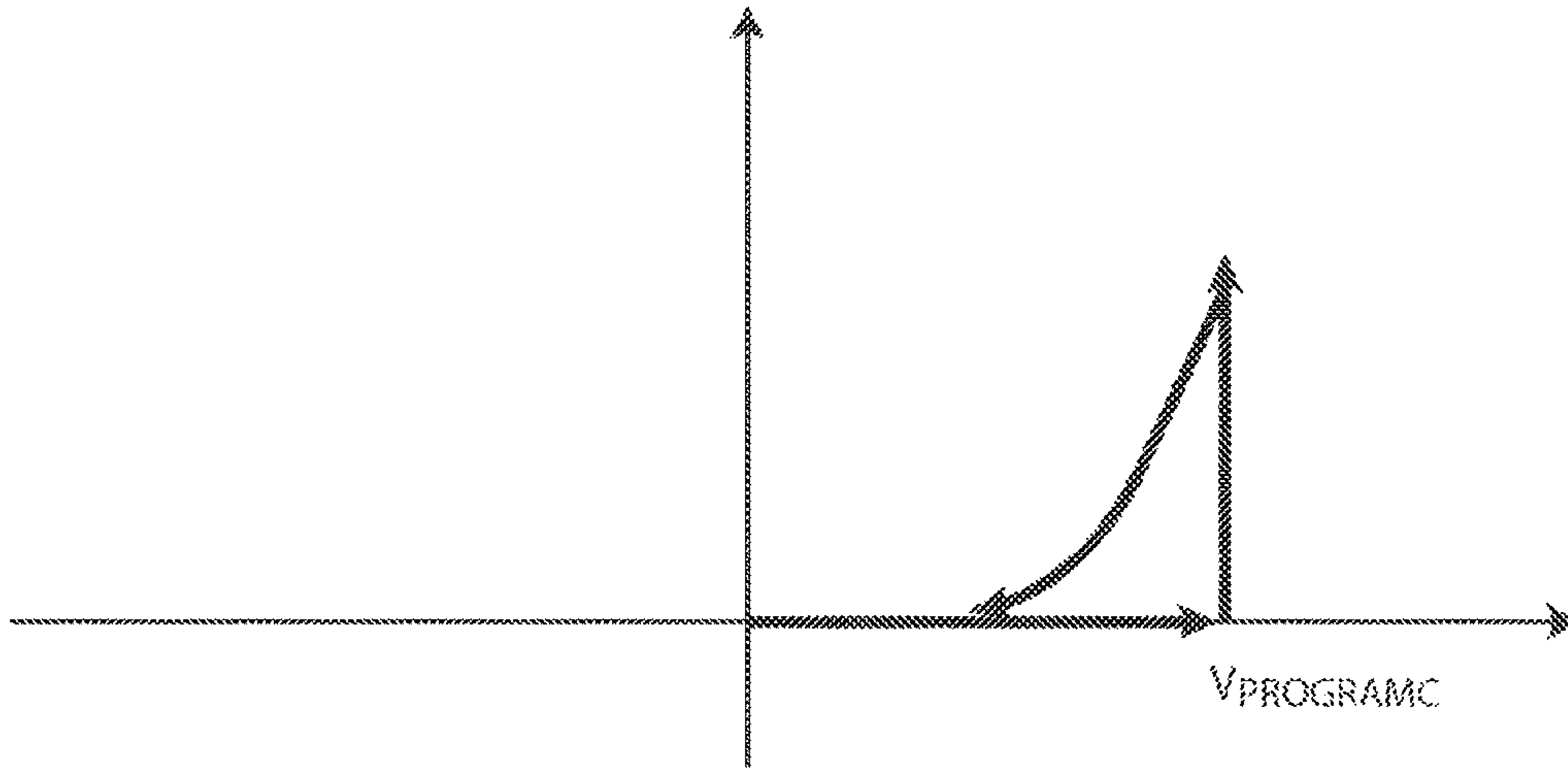

FIG. 7B

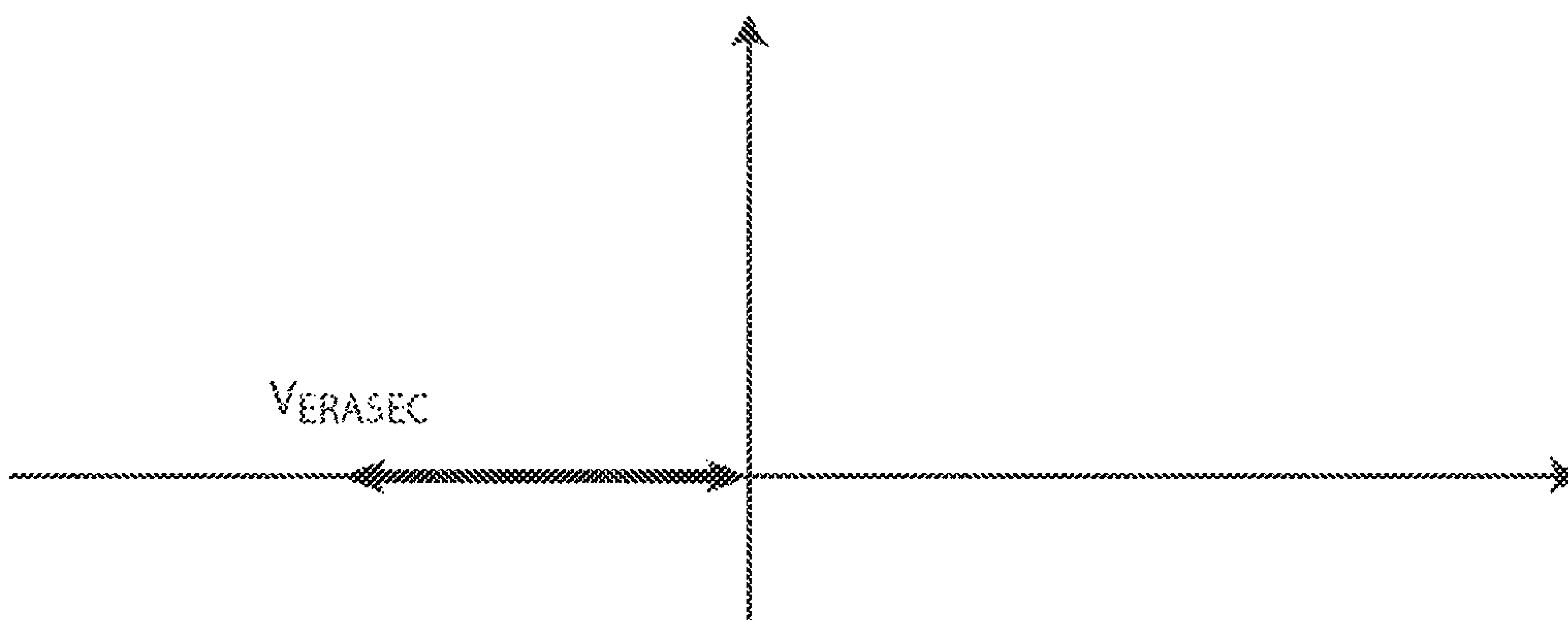

FIG. 7C

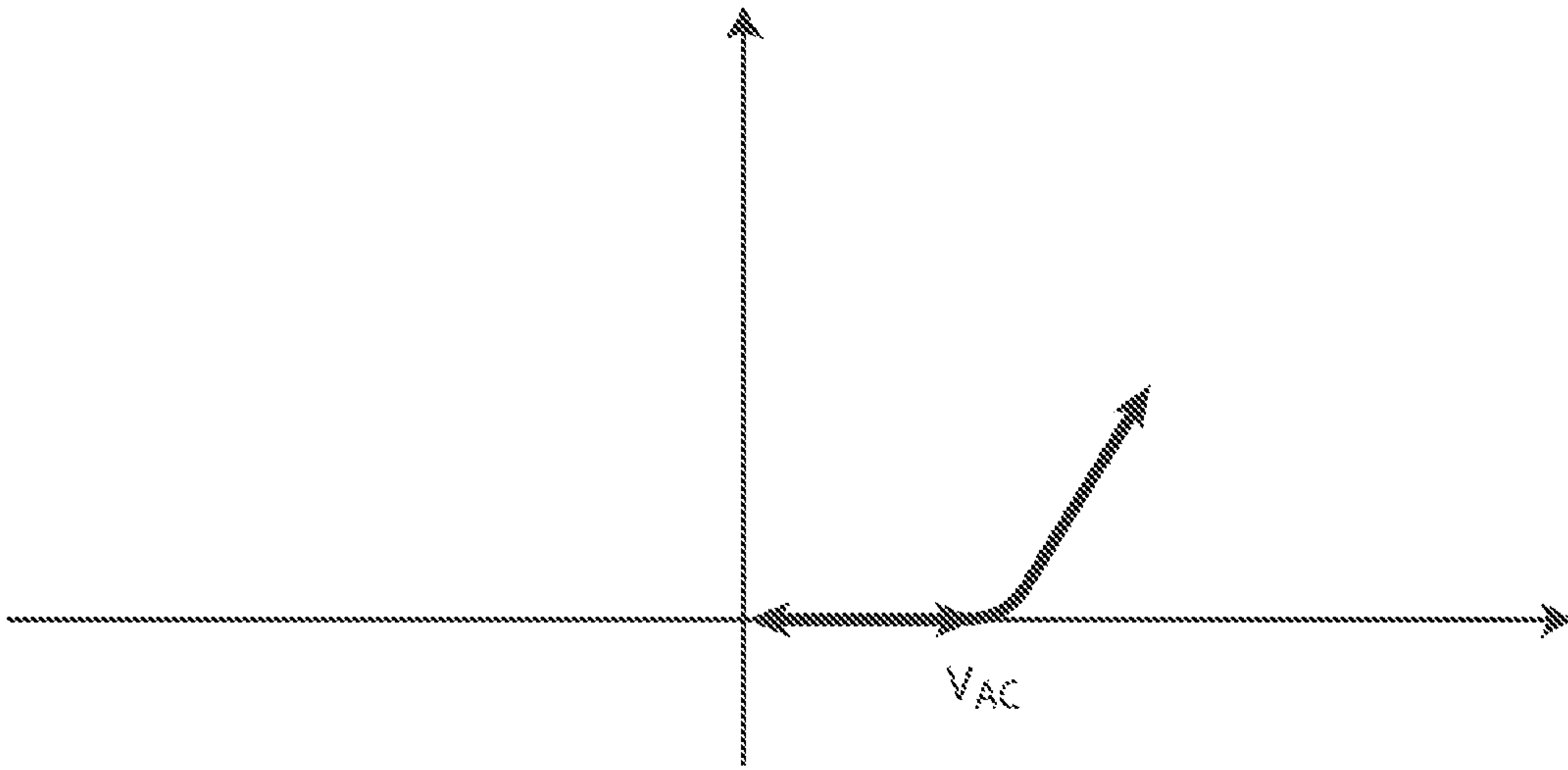

FIG. 7D

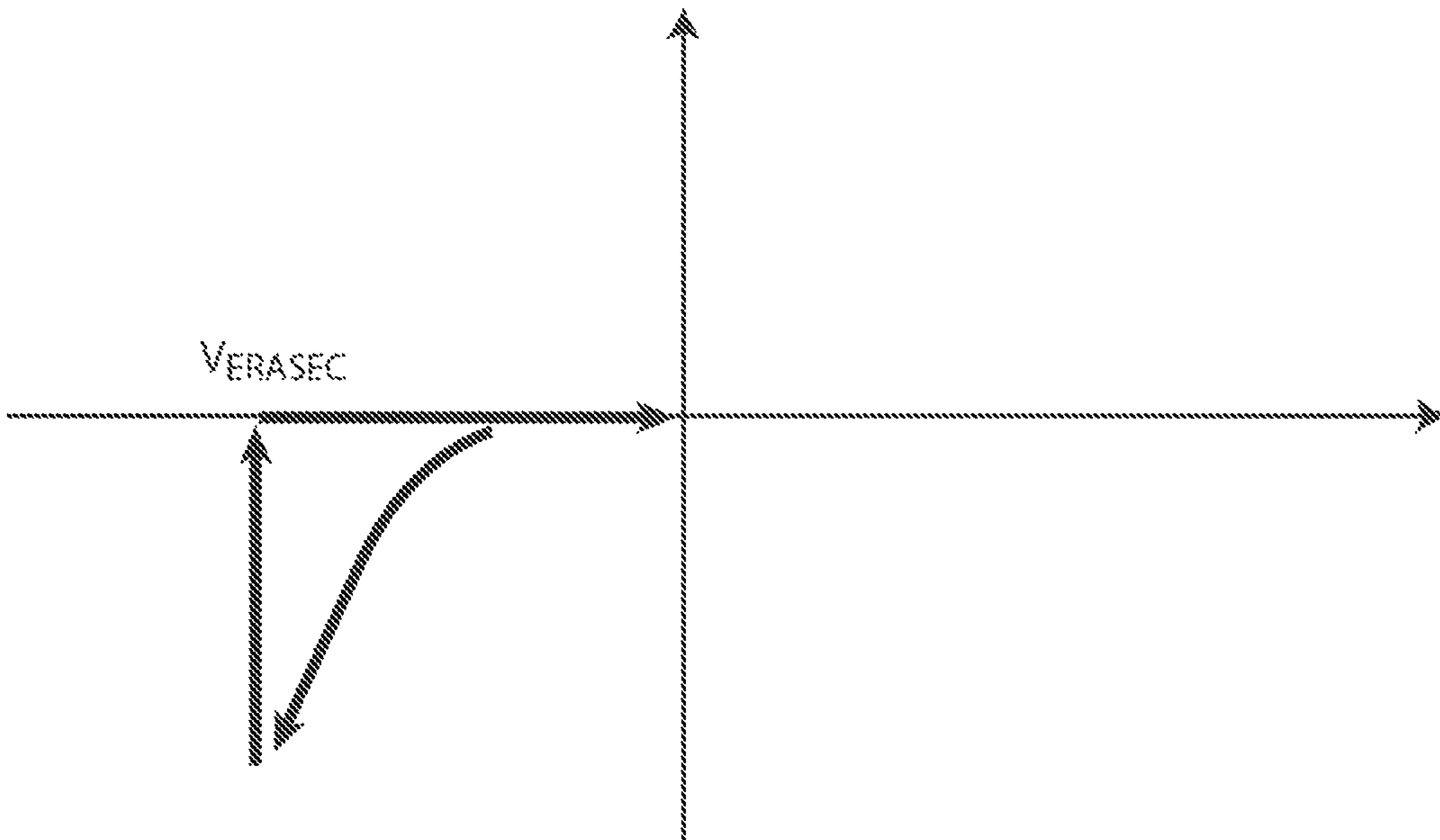

FIG. 7E

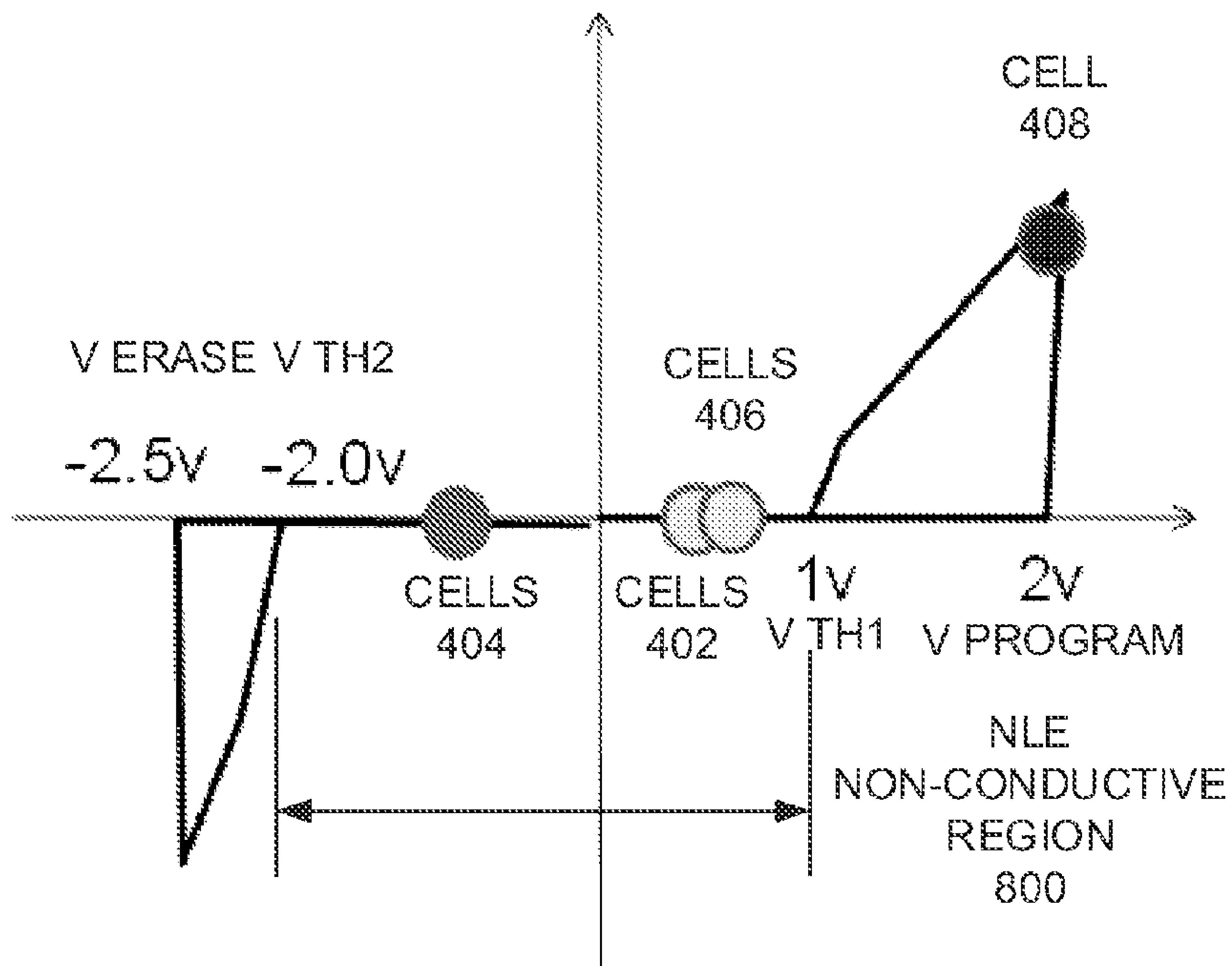

FIG. 8A

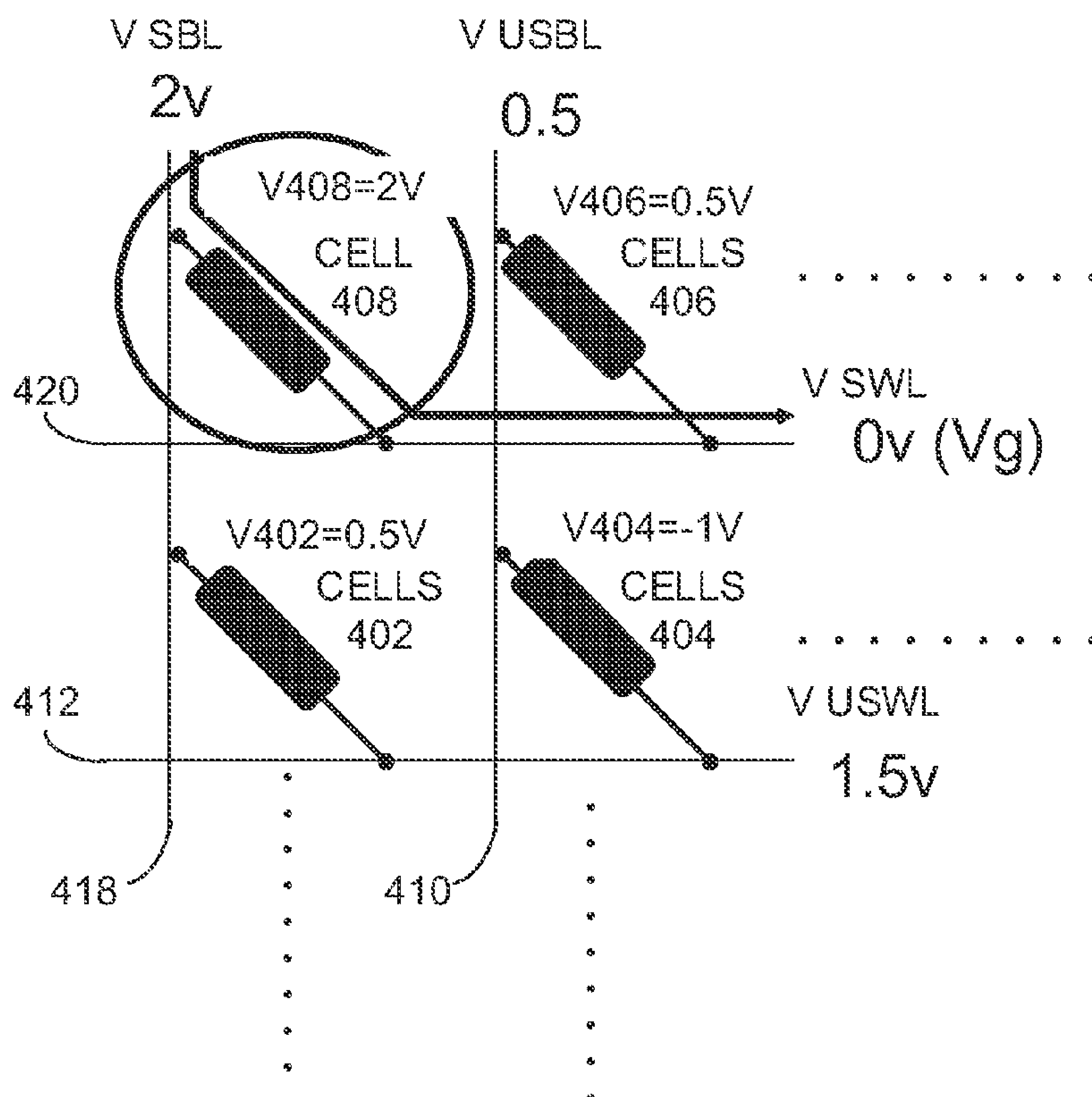

FIG. 8B

SWITCHING DEVICE HAVING A NON-LINEAR ELEMENT

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue; a claim printed with strikethrough indicates that the claim was canceled, disclaimed, or held invalid by a prior post-patent action or proceeding.

CROSS REFERENCE TO RELATED APPLICATIONS

This application *is a Reissue of U.S. Pat. No. 8,767,441 B2 issued Jul. 1, 2014 that* claims priority to and is a continuation-in-part of U.S. application Ser. No. 13/149,757, filed May 31, [2012. This application also] *2011, now issued as U.S. Pat. No. 8,502,185 on Aug. 6, 2013, and that* claims priority to U.S. application Ser. No. 13/290,024, filed Nov. 4, 2011, *now issued as U.S. Pat. No. 8,467,227 on Jun. 18, 2013,* which is a non-provisional of U.S. Application No. 61/410,035, filed Nov. 4, 2010, U.S. Application No. 61/712,171, filed Oct. 10, 2012, and U.S. application No. 61/786,100, filed Mar. 15, 2013. These cited documents are incorporated by reference herein, for all purposes.

JOINT RESEARCH AGREEMENT

The presently claimed invention was made by or on behalf of the below listed parties to a joint university-corporation research agreement. The joint research agreement was in effect on or before the date the claimed invention was made and the claimed invention was made as a result of activities undertaken within the scope of the joint research agreement. The parties to the joint research agreement are The University of Michigan and Crossbar, Incorporated.

BACKGROUND

The present invention is related to switching devices. More particularly, the present invention provides a structure and a method for forming non-volatile resistive switching memory devices characterized by a suppression of current at low bias and a high measured ON/OFF resistance ratio.

The success of semiconductor devices has been mainly driven by an intensive transistor down-scaling process. However, as field effect transistors (FET) approach sizes less than 100 nm, problems such as short channel effect start to prevent proper device operation. Moreover, such sub 100 nm device size can lead to sub-threshold slope non-scaling and increased power dissipation. It is generally believed that transistor based memories such as those commonly known as Flash memory may approach an end to scaling within a decade. Flash memory is one type of non-volatile memory device.

Other non-volatile random access memory (RAM) devices such as ferroelectric RAM (Fe RAM), magneto-resistive RAM (MRAM), organic RAM (ORAM), and phase change RAM (PCRAM), among others, have been explored as next generation memory devices. These devices often require new materials and device structures to couple with silicon based devices to form a memory cell, which lack one or more key attributes. For example, Fe-RAM and MRAM devices have fast switching characteristics and good programming endurance, but their fabrication is not CMOS compatible and size is usually large. Switching for a PCRAM device uses Joules heating, which inherently has high power consumption. Organic RAM or ORAM is incompatible with large volume silicon based fabrication and device reliability is usually poor.

As integration of memory devices increases, the size of elements is reduced while the density of elements in a given area is increased. As a result, dark current or leakage current becomes more of a problem, where leakage current can return a false result for a read operation or cause an unintentional state change in a cell. The problem of leakage current is particularly acute in two-terminal devices, in which multiple memory cells can form leakage paths through interconnecting top and bottom electrodes.

Conventional approaches to suppressing leakage current in switching devices include coupling a vertical diode to a memory element. However, the external diode approach has several disadvantages. In general, the diode fabrication process is a high temperature process, typically conducted above 500 degrees Celsius. Because most diodes rely on a P/N junction, it is difficult to scale the diode height to achieve a memory and diode structure with a desirable aspect ratio. And finally, a conventional diode is only compatible with a unipolar switching device, and not a two-way bipolar device. It is therefore desirable to have a robust and scalable method and structure for a highly integrated memory that is not adversely affected by leak currents.

BRIEF SUMMARY OF THE INVENTION

The present invention is generally related to switching devices. More particularly, the present invention provides a structure and a method for forming a non-volatile memory cell using resistive switching. It should be recognized that embodiments according the present invention have a much broader range of applicability.

In a specific embodiment, a switching device includes a substrate; a first electrode formed over the substrate; a second electrode formed over the first electrode; a switching medium disposed between the first and second electrode; and a nonlinear element disposed between the first and second electrodes and electrically coupled in series to the first electrode and the switching medium. The nonlinear element is configured to change from a first resistance state to a second resistance state on application of a voltage greater than a threshold.

The switching device includes a RRAM in an embodiment.

The switching device include a PCRAM in an embodiment.

The present invention has a number of advantages over conventional techniques. For example, embodiments of the present invention allow for a high density non-volatile memory characterized by high switching speed, low leakage current characteristic, and high device yield. Depending on the embodiment, one or more of these may be achieved. These and other advantages will be described below in more detail in the present specification.

BRIEF DESCRIPTION OF THE DRAWINGS

Exemplary embodiments will hereinafter be described in conjunction with the appended drawings, wherein like designations denote like elements, and wherein:

FIG. **1** illustrates a non-volatile memory device including a memory cell that has a bottom electrode, a switching medium, and a top electrode according to an embodiment of the present invention;

FIG. **2** illustrates I-V resistance switching characteristics of a resistive memory cell;

FIG. **3**A illustrates a two-terminal memory cell that is placed in an ON state by applying a program voltage $V_{PROGRAM}$ to the top electrode;

FIG. **3**B illustrates a two-terminal memory cell that is placed in an OFF state by applying an erase voltage V_{ERASE} to the top electrode;

FIG. **4** illustrates a memory array including a leakage current;

FIG. **5** illustrates a non-volatile memory cell including a nonlinear element according to an embodiment of the present invention;

FIG. **6**A illustrates I-V characteristics of a digital nonlinear element subjected to a voltage sweep;

FIG. **6**B illustrates I-V characteristics of a switch combined with a digital nonlinear element in an initially OFF state subjected to a positive voltage sweep;

FIG. **6**C illustrates I-V characteristics of a switch combined with a digital nonlinear element in an initially OFF state subjected to a negative voltage sweep;

FIG. **6**D illustrates I-V characteristics of a switch combined with a digital nonlinear element in an initially ON state subjected to a positive voltage sweep;

FIG. **6**E illustrates I-V characteristics of a switch combined with a digital nonlinear element in an initially ON state subjected to a negative voltage sweep;

FIG. **7**A illustrates I-V characteristics of an analog nonlinear element subjected to a positive voltage sweep;

FIG. **7**B illustrates I-V characteristics of a switch combined with an analog nonlinear element in an initially OFF state subjected to a positive voltage sweep;

FIG. **7**C illustrates I-V characteristics of a switch combined with an analog nonlinear element in an initially OFF state subjected to a negative voltage sweep;

FIG. **7**D illustrates I-V characteristics of a switch combined with an analog nonlinear element in an initially ON state subjected to a positive voltage sweep;

FIG. **7**E illustrates I-V characteristics of a switch combined with an analog nonlinear element in an initially ON state subjected to a negative voltage sweep; and

FIG. **8**A illustrates I-V characteristics of a non-volatile memory cell including a nonlinear element according to an embodiment of the present invention; and

FIG. **8**B illustrates a memory array including leakage currents.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

The present invention is generally directed to a memory device. More particularly, the present invention provides a structure and a method for a resistive switching cell having a nonlinear element. The switching cell may be used in a Resistive Random Access Memory (RRAM) or any highly integrated device. It should be recognized that embodiments of the present invention can have a broader range of applicability. Although the present invention is described with respect to specific embodiments, the embodiments are only used for illustrative purposes and should not be considered limiting.

RRAM is typically a two terminal device in which a switching element is sandwiched between a top electrode and a bottom electrode. The resistance of the switching element is varied by applying a voltage to the electrodes or a current through the switching element. Resistive switching can be bipolar or unipolar. In bipolar switching, the change in resistance of the switching element depends on polarity and a magnitude of a current or voltage based applied electrical signal. In the case of unipolar switching, the change in resistance of the switching element depends only on the magnitude of the applied voltage or current and typically is a result of Joule heating within the switching element. Embodiments of the present invention are explained with respect to a two-terminal RRAM device using bipolar switching, but are not limited thereto. As used herein, the terms "RRAM" or "resistive memory cell" refer to a memory cell or memory device that uses a switching medium whose resistance can be controlled by applying an electrical signal without ferroelectricity, magnetization, and phase change of the switching medium. The present invention is not limited to implementation in RRAM, e.g., the invention may be implemented using the phase change RAM.

FIG. **1** illustrates a resistive memory cell **100** in a non-volatile memory device, e.g., a semiconductor memory chip. The memory cell includes a bottom electrode **102**, a switching medium **104**, and a top electrode **106** according an embodiment of the present invention. The switching medium **104** exhibits a resistance that can be selectively set to various values and reset using appropriate control circuitry. The memory cell **100** is a two-terminal resistive memory device, e.g., RRAM, in the present embodiment. Terms such as "top" or "bottom" are used for illustrative purpose only and should not construe to be limiting.

In the present embodiment, the memory cell **100** is an amorphous-silicon-based resistive memory cell and uses amorphous silicon (a-Si) as the switching medium **104**. The resistance of the switching medium **104** changes according to formation or retrieval of a conductive filament inside the switching medium **104** according to a voltage applied to the electrodes. In an embodiment, the switching medium **104** is substantially free of dopants. In another embodiment, the switching medium **104** is a-Si doped with boron. In some embodiments, the resistive switching layer includes a silicon oxide, e.g. a silicon sub oxide, (e.g SixOy, where x $0<y<=1$, $0<x<2$,) or sub-oxide material such as Ge, SixGey, and SixGeyOz. It should be understood that any such sub-oxide refers to a non-stoichiometric oxide. An example of this is silicon oxide: stoichiometric silicon oxide is SiO_2, and non-stoichiometric oxide may be SiO_x where $0<x<2$. In various embodiments, other forms of non-stoichiometric oxide may be formed or grown using various fabrication techniques.

The top electrode **106** is a conductive layer containing silver (Ag) and acts as the source of filament-forming ions in the a-Si structure. Although silver is used in the present embodiment, it will be understood that the top electrode **106** can be formed from various other suitable metals, such as gold (Au), nickel (Ni), aluminum (Al), chromium (Cr), iron (Fe), manganese (Mn), tungsten (W), vanadium (V), and cobalt (Co). In certain embodiments, the bottom electrode **102** is pure metal, a boron-doped electrode, or other p-type polysilicon or silicon-germanium, which is in contact with a lower-end face of the a-Si structure. In an embodiment, the memory cell **100** is configured to store more than a single bit of information, e.g., by adjusting the external circuit resistance, as explained in application Ser. No. 12/575,921, filed on Oct. 9, 2009, which is entitled "Silicon-Based Nanoscale

Resistive Device with Adjustable Resistance" and is incorporated by reference in its entirety.

FIG. **2** illustrates resistance switching characteristics of the memory cell **100** according to an embodiment of the present invention. The switching medium **104** displays a bipolar switching effect. The resistance of the switching medium **104** changes depending on the polarity and magnitude of the voltage signal applied to the switching medium **104** via the top electrode **106** and the bottom electrodes **102**. The memory cell **100** is changed into an ON state (low resistance state) when a positive voltage equal to or greater than a threshold program voltage (also referred to as a "program voltage") $V_{PROGRAM}$ is applied. In an embodiment, the program voltage ranges between 1 volt to 5 volts depending on the materials used for the switching medium **104** and the top electrode **106**. In another embodiment, the program voltage ranges between 1 volt and 3 volts. The memory cell **100** is switched back to an OFF state (high resistance state) when a negative voltage equal to or greater than a threshold erase voltage (also referred to as "erase voltage") V_{ERASE} is applied. In an embodiment, the erase voltage ranges from −2 volts to −5 volts. The cell state is not affected if the voltage applied is between two threshold voltages $V_{PROGRAM}$ and V_{ERASE}, which enables a low-voltage read process. Once the memory cell **100** is set to a specific resistance state, the memory cell **100** retains the information for a certain period (or retention time) without electrical power.

FIG. **2** illustrates a current-voltage (I-V) relationship through a switching operation of a non-rectifying memory cell **100**. Electrical current flows from the top electrode **106** to the bottom electrode **102** when the potential applied to the top electrode **106** is positive potential with respect to the bottom electrode **102**. On the other hand, current flows in the reverse direction if the potential applied to the top electrode **106** is negative with respect to the bottom electrode **102**.

FIGS. **3**A and **39** illustrate a switching mechanism of the memory cell **100** during the ON and OFF states according to an embodiment of the present invention. The switching in the switching medium **104** is based on formation and retrieval of a conductive filament, or a plurality of filaments, in a filament region in the switching medium **104** according to the program and the erase voltages applied to the bottom electrode **102** and the top electrode **106** of the memory cell **100**.

FIG. **3**A illustrates the memory cell **100** that is placed in an ON state by applying the program voltage $V_{PROGRAM}$ to the top electrode **106**. The switching medium **104**, made of a-Si, is provided between the bottom electrode **102** and the top electrode **106**. An upper portion of the switching medium **104** includes a metallic region (or conductive path) **302** that extends from the top electrode **106** to approximately 10 nm above the bottom electrode **102**. The metallic region **302** is formed during an electroforming process when a slightly larger voltage than a subsequent switching voltage, e.g., 3~5 V, is applied to the top electrode **106**. This large voltage causes the electric field-induced diffusion of the metal ions from the top electrode **106** toward the bottom electrode **102**, thereby forming a continuous conductive path **312**. A lower portion of the switching medium **104** defines a filament region **304**, wherein the filament **310** is formed when the program voltage $V_{PROGRAM}$ is applied after the electroforming process. The continuous conductive path **312** and the filament **310** can also be formed together during the electroforming process. The filament **310** comprises a series of metal particles, which are trapped in defect sites in a lower portion of the switching medium **104** when the program voltage $V_{PROGRAM}$ applied provides sufficient activation energy to push a number of metal ions from the metallic region **302** toward the bottom electrode **102**.

The filament **310** is believed to be comprised of a collection of metal particles that are separated from each other by the non-conducting switching medium **104** and that do not define a continuous conductive path, unlike the continuous conductive path **312** in the metallic region **302**. The filament **310** extends about 2 to 10 nm depending on implementation. The conduction mechanism in an ON state is electrons tunneling through the metal particles in the filament **310**. The cell resistance is dominated by the tunneling resistance between the metal particle **306** and the bottom electrode **102**. The metal particle **306** is a metal particle in the filament region **304** that is closest to the bottom electrode **102** and that is the last metal particle in the filament region **304** in an ON state.

FIG. **3**B illustrates the memory cell **100** that is placed in an OFF state by applying an erase voltage V_{ERASE} to the top electrode **106**. The erase voltage exerts sufficient electromagnetic force to dislodge the metal particles trapped in the defects sites of the a-Si and retrieves at least part of the filament **310** from the filament region **304**. The metal particle **308** that is closest to the bottom electrode **102** in an OFF state is separated from the bottom electrode **102** by a distance greater than the metal particle **306** during an ON state. This increased distance between the metal particle **308** and the bottom electrode **102** places the memory cell **100** in a high resistance state compared to an ON state. In an embodiment, the resistance ratio between ON/OFF states ranges from 10E3 to 10E7. Memory cell **100** behaves like a resistor in an ON state and a capacitor in an OFF state (i.e., the switching medium **104** does not conduct a current in any meaningful amount and behaves as a dielectric in an OFF state). In an implementation, the resistance is 10E5 Ohm in an ON state and 10E10 Ohm in an OFF state. In another implementation, the resistance is 10E4 Ohm in an ON state and 10E9 Ohm in an OFF state. In yet another implementation, the resistance is at least 10E7 Ohm in an OFF state.

FIG. **4** illustrates a portion of an array **400** that is in a crossbar configuration in which the (common) top electrodes and the (common) bottom electrodes are arranged in an orthogonal manner according to an embodiment of the present invention. An array of such crossbar structures includes a plurality of parallel (common) top electrodes and a plurality of parallel (common) bottom electrodes with switching elements disposed between the intersection regions of the (common) top electrodes and the (common) bottom electrodes. Certain limitations may exist in such a configuration, as described below.

Four memory cells **402**, **404**, **406**, and **408** are shown. Memory cells **404** and **406** share a common first top electrode **410**, while cells **402** and **408** share a common second top electrode **418**. The first top electrode **410** and the second top electrode **418** are arranged parallel to each other. Memory cells **402** and **404** share a common first bottom electrode **412** and cells **406** and **408** share a common second bottom electrode **420**. The first bottom electrode **412** and the second bottom electrode **420** are spatially arranged parallel to each other. In addition, each of the top electrodes is configured to be non-parallel to each of the bottom electrodes.

To determine a state of a target cell which has a high resistance state, a voltage is applied and a current flowing through the target cell is measured. If some cells in the crossbar array are in low resistance states, the voltage applied to the target cell can cause a leakage current to flow

through the untargeted cells instead. In this case the cells causing the leakage, including the target cell, are interconnected through shared electrodes. The leakage current can form a current path, commonly known as a sneak current or a sneak current path, through these untargeted cells. Such a sneak current can cause undesirable behavior in a switching array.

For example, in an exemplary array, cells **402**, **404**, and **406** are at a low resistance ON state, and cell **408** is at a high resistance OFF state. Because the ON state is characterized by a low resistance, a sneak path **416** may be formed allowing current to flow through cells **402**, **404**, and **406**. Thus, when a read voltage is applied to target cell **408**, leakage current flowing along sneak path **416** may cause an erroneous reading of an ON state result.

In some embodiments, a sneak path can be very short, existing in as few as two forward biased cells and one reverse biased cell. In addition, once started, a sneak path can propagate throughout the array through cells in the ON state. The most common conductive path in a switching array is the shared top and bottom electrodes. Sneak path **416** is only one example of a sneak path passing leakage current through an array.

To mitigate problems caused by leakage current in a switching array, a nonlinear element (NLE) may be included in a resistive switching device. NLEs can be generally divided into two categories: an NLE that exhibits digital-like behavior, or "digital NLE," and an NLE that exhibits analog-like behavior, or an "analog NLE," both of which are described in detail separately below. The categories of digital and analog behavior are not strictly defined, so it is possible for a particular NLE to have properties that are characteristic of both digital and analog behavior, or somewhere in between. In its most basic form, an NLE is an element that has a nonlinear response with respect to voltage, for instance, with a nonlinear I-V relationship. In most embodiments, the relationship is characterized by a high resistance state at low amplitude voltages and a lower resistance state at higher amplitude voltages, with a nonlinear transition from the high resistance state to the low resistance state. Unlike a switching medium, an NLE does not have a memory characteristic; an NLE returns to an original state when a voltage is no longer applied. An NLE that is suitable for suppressing leak currents is characterized by a high resistance state at a low bias, a lower resistance state at a higher bias, and a threshold between the states.

In an embodiment, an NLE is a two terminal device which shows an apparent threshold effect such that the resistance measured below a first voltage is significantly higher than the resistance measured above a second voltage. In a typical embodiment, the resistance below the first voltage is more than 100 times greater than the resistance above the second voltage. In other embodiments, the ratio may be in the range of about 100 to about 500 times, in the range of about 500 times to about 1000 times, in the range of about 1000 times to about 10,000 times, or the like, depending upon specific engineering requirements of the NLE material. In some embodiments, the first and second voltages are different, and are typically referred to as a hold voltage V_{HOLD} and threshold voltage V_{TH}, respectively. In other embodiments, the first voltage and second voltage may be the same. In various embodiments, these relationships may exist in both polarities of voltage, or only in one polarity, and the NLE can be a single material or multiple layers of different materials.

As shown in FIG. **5**, to mitigate the effects of leakage current in a memory cell **500**, an NLE **504** is electrically coupled in series to the top electrode **508**, bottom electrode **502**, and switching medium **506**. An NLE **504** may be disposed between the bottom electrode **502** and switching medium **506**. In other embodiments, the NLE is disposed between the top electrode **508** and the switching medium **506**. Higher temperatures may be experienced by the lower portions of a semiconductor device during various semiconductor processes, so an NLE that is located lower in a stack structure may be designed to withstand higher temperatures than an NLE located further from the substrate.

The behavior of a digital NLE is characterized by abrupt changes in current at certain voltages, which may be referred to as threshold voltages. Such behavior is illustrated in FIG. **6**A, which shows the results of a voltage sweep in an embodiment with respect to current on an NLE that is not coupled to a resistive switching device. As positive bias voltage is applied to the NLE, the NLE is in a resistive state characterized by high resistance until it reaches the threshold voltage V_{TH1}. After this threshold has been reached, the NLE will retain its conductive state until the applied voltage drops below a hold voltage V_{HOLD1}. Thus a NLE that is in a conductive state by having a voltage applied above V_{TH1} will continue to have a low resistance so long as a voltage above V_{HOLD1} is supplied to the NLE, after which it reverts to the original high-resistance state. An NLE does not have a memory characteristic, so the same I-V relationship is experienced every time a voltage is applied from an original state.

Referring back to FIG. **6**A, when a negative bias voltage is applied that is more negative than a threshold voltage V_{TH2}, an abrupt transition is experienced, and the resistance in the NLE is significantly reduced. The NLE retains its low resistance state until the voltage becomes less negative than a value V_{HOLD2}, at which point the NLE reverts to an original high resistance state. Although FIG. **6**A shows an embodiment with symmetrical I-V behavior between positive and negative bias performance, in other embodiments the relationship is not symmetrical.

FIGS. **6**B to **6**E show I-V relationships of an embodiment where an NLE is coupled to a memory cell ("combined device"), in this case a digital NLE. Memory cell **500** is an example of such a combined device. If the memory cell depicted in those figures was not coupled to the NLE, it would have an I-V response according to FIG. **2**. Turning to FIG. **6**B, an I-V curve showing a program operation switching a cell from an initially OFF state to an ON state is shown. To establish a conductive ON state in a cell, a voltage above $V_{PROGRAMC}$ is applied. $V_{PROGRAMC}$ is the program voltage for the combined device, which switches the combined device from an OFF state to an ON state. V_{HOLDC1} is the hold voltage of a combined device, which performs in essentially the same way as V_{HOLDC1} described above. In a preferred embodiment, V_{HOLD1} is less than V_{TH1}, which is less than $V_{PROGRAM}$.

The relationships between I-V performance in a memory cell, an NLE, and a combined device can also be explained through equations. The equations assume that both the NLE and the switching medium switch instantly (e.g., a few nsa few hundreds of ns) when experiencing a threshold voltage. In addition to the definitions given above, the following variables are designated:

R_{MOFF}=The OFF state resistance of a memory element
R_{MON}=The ON state resistance of a memory element
R_{NOFF}=The OFF state resistance of an NLE
R_{NON}=The ON state resistance of an NLE

Using these variables, the relationship between the hold voltage of a combined device and the hold voltage of an NLE can be expressed as:

$$VHOLDC1=((RMON+RNON)/RNON)VHOLD1$$

The value for the program voltage of the combined device can be expressed as:

$$VPROGRAMC\approx small\{large((RMOFF+RNOFF)/RNOFF)VTH1,VPROGRAM),large(VTH1,((RMOFF+RNOFF)/RMOFF)VPROGRAM)\}$$

Where "small" indicates the smaller of two values in a set, and "large" indicates the larger of two values in a set. In most embodiments, the $V_{PROGRAM}$ is significantly higher than V_{TH1}, and $V_{PROGRAMC}$ is thus similar to $V_{PROGRAM}$.

FIG. **6**C shows the result of a negative voltage sweep of the same switch in an OFF state. Because it is already in the OFF state, a negative voltage does not cause an erase operation, and the cell remains in a high resistance OFF state.

FIGS. **6**D and **6**E show I-V relationships of a combined device (e.g. memory cell **500**) where the memory cell is initially in a low-resistance ON state. FIG. **6**D shows a read operation, where the read voltage must be greater than threshold voltage V_{THC1} to return an accurate read value. As the read voltage drops below the hold voltage V_{HOLDC1}, the resistance in the cell increases substantially. The threshold voltage of the combined device is related to the threshold voltage of the NLE through the following equation:

$$VTHC1=((RMON+RNOFF)/RNOFF)VTH1\approx VTH1$$

Thus, the read threshold voltage of the combined device is approximately the same as the threshold voltage of the NLE, or $V_{THC1}\cong V_{TH1}$.

Similarly, as seen in FIG. **6**E, an erase operation must overcome a second threshold value V_{THC2} to allow current to start flowing through the cell, and the switch is changed to a high-resistance OFF state at voltage V_{ERASEC} Like the positive threshold voltage, the negative threshold voltage of the combined device is about the same as the negative threshold voltage of the NILE. The value of the erase voltage V_{ERASEC} in a combined device can be expressed as:

$$VERASEC\approx large((RMON+RNON)/RMON)VERASE,VTH2)$$

The relationship between the negative threshold voltages of a discrete and combined device can be expressed as:

$$VTHC2=((RMON+RNOFF)/RNOFF)VTH2\approx VTH2.$$

So that in most embodiments, $V_{THC2}\cong V_{TH2}$.

Various embodiments of a digital NLE can be made of many different materials. For example, a digital NLE can be a threshold device such as a film that experiences a field-driven metal-insulating (Mott) transition. Such materials are known in the art, and include VO_2 and doped semiconductors. Other threshold devices include material that experiences resistance switching due to electronic mechanisms observed in metal oxides and other amorphous films, or other volatile resistive switching devices such as devices based on anion or cation motion in oxides, oxide heterostructures, or amorphous films. A digital NLE can also be in the form of a breakdown element exhibiting soft breakdown behavior such as SiO_2, HfO_2, and other dielectrics. Examples of such breakdown elements are described in further detail by application Ser. No. 12/826,653, filed on Jun. 29, 2010, which is entitled "Rectification Element for Resistive Switching for Non-volatile Memory Device and Method," and is incorporated by reference in its entirety. In other embodiments, the NLE may be a solid electrolyte material. The solid electrolyte material can include be chalcogenide based such as GexSy, GexSey, SbxTey, AgxSey, and CuxSy, or can be metal oxide based such as WOx, TiOx, AlOx, HfOx, CuOx, and TaOx, where 0<x<appropriate stoichiometric value (e.g. 2, 3, etc.) (e.g. GeS, GeSe, WO3, or SbTe, and the like).

As is known in the art, the precise values of threshold, hold, program and erase can be adjusted for different embodiments by changing the form of and materials used for the NLE and the memory cell. In various embodiments the threshold voltage for the NLE can be about the same as the hold voltage, the program voltage, or both. In other embodiments the threshold voltage for the NLE can exceed the program and erase voltages of a resistive switching device.

An analog NLE differs from a digital NLE in that its I-V relationship is characterized by a more gradual transition when current starts to flow through the element. As shown in FIG. **7**A, which illustrates the response of an analog NLE to a voltage sweep, the current transition follows an exponential-like curve. The transition or threshold is therefore less abrupt than a digital NLE. Threshold voltage values where substantial current starts to flow through an analog NLE are designated as V_A and V_B for positive and negative bias values, respectively. Another significant difference between an analog and digital NLE is that an analog NLE does not experience the hysteretic hold voltage characteristic of a digital NLE.

FIGS. **7**B to **7**E show I-V characteristics of a combined device with an analog NLE. As shown in FIG. **7**B, when a program voltage $V_{PROGRAMC}$ is applied to a combined device where the switch is initially in an OFF state, the switch changes to a low resistance ON state. The $V_{PROGRAMC}$ is approximately the sum of the V_A of the NLE and the $V_{PROGRAM}$ of the switch as shown in FIG. **2**, or $V_{PROGRAMC}\approx V_A+V_{PROGRAM}$. As a result, the programming voltage of a combined device with an analog NLE is typically higher than the programming voltage of a switching element alone.

Turning now to FIG. **7**C, a negative voltage sweep of a combined device in an OFF state is shown. Because the switch is already in an OFF state, the negative voltage does not induce a state change, and the switch remains in a high resistance state.

FIG. **7**D shows the result of a read operation in a combined switch that is in an ON state. In the present embodiment, $V_{AC}<V_{READ}<V_{PROGRAMC}$. Because the switch is already in a low-resistance ON state, current flow above the threshold voltage V_{AC} is characterized by low resistance. Circuitry can detect the current flow, resulting in a positive read result. The value tier V_A is not affected by the switching apparatus in most embodiments, so typically $V_{AC}\approx V_A$.

FIG. **7**E shows an I-V curve for an erase operation in a combined device. To change the switch from the ON state to the OFF state, a voltage of V_{ERASEC} is applied to the combined device, thereby increasing the resistance of the switch. The voltage required to complete an erase operation in a combined device is normally the sum of the erase value of the discrete switch and the threshold value of the analog NLE, or $V_{ERASEC}\approx V_{ERASE}+V_B$.

An analog NLE can be any element that exhibits the above described behavior. Examples of suitable materials include a punch-through diode, a Zener diode, an impact ionization (or avalanche) element, and a tunneling element such as a tunneling barrier layer. Such elements can be fabricated using standard fabrication techniques.

In most embodiments, $|V_A, V_B| < |V_{PROGRAM}, V_{ERASE}|$. As is known in the art, the precise threshold values of V_A, V_B, program, and erase can be adjusted for different embodiments by changing the form of and materials used for the NLE and the memory cell. In various embodiments the threshold voltage for the NLE can be about the same as the program voltage. In other embodiments the threshold voltage can exceed the program and erase voltages.

In other embodiments, a resistive switching cell may be configured to retain multiple resistive states. That is, rather than being configured to have binary states of ON and OFF, a cell can retain a plurality of resistance states. An array of such switches has the same limitations regarding leakage current, and would similarly benefit from the inclusion of an NLE.

FIGS. **8**A-B illustrate examples according to various embodiments of the present invention. In various embodiments of the present invention, as discussed in FIG. **4**, when a program (or read or erase) voltage is applied to a target cell **408**, e.g. across second top electrode **418** and second bottom electrode **420**, a sneak path **416** may allow a sneak path current to flow through cells **402**, **404** and **406**. To reduce this, a non-linear element, described above (e.g. NLE **504** in FIG. **5**), was incorporated in each memory cell. The characteristics of an example NLE was illustrated in FIG. **6**A. More particularly, when a voltage across the NLE exceeded VTH1 the resistance for the NLE switched from a relatively non-conductive state to a relatively conductive state. Accordingly, in an example, to program target cell **408**, a program voltage would be applied to target cell **408** that would exceed VTH1 and exceed the programming voltage of target cell **408** (VProgram, FIG. **8**A). In another example, to read target cell **408**, a read (or program) voltage would be applied to target cell **408** that would exceed VTH1, but would be less than the programming voltage of target cell **408** (VProgram, FIG. **8**A).

In an example described in co-pending application Ser. No. 13/290,024, filed Nov. 4, 2011, incorporated by reference above, the read voltage to the target cell was limited to be no greater than three times the threshold voltage of the nonlinear element. This three times number assumed that unselected top electrodes and unselected bottom electrodes in the memory array were allowed to float. By way of explanation, using the numbering of FIG. **4** above, in FIG. **8**B, the read voltage would not only be applied across target cell **408**, but also across sneak path **416** through cells **402**, **404** and **406**. In such a configuration, if the read (or program) voltage exceeded three times the voltage threshold (e.g. 3×VTH1) of the non-linear element, the voltage across non-linear element of **402**, for example, would also exceed VTH1. Accordingly, the NLE of **402** would switch to a relatively-conductive state, and significant current could flow through the sneak path **416**. It was recognized in the above incorporated patent application, that to reduce sneak path current, unselected cells, e.g. **402**, **404** and **406** had to have voltages applied that were lower than the threshold voltage (e.g. VTH1) of the non-linear elements. For example, when the read (or program) voltage (V**408**) is applied across target cell **408**, the resultant relationships should be met: voltage across cell(s) V**402**<VTH1, voltage across cell(s) V**404**<VTH1, and voltage across cell(s) **406**<VVTH1. Additionally, the voltages across these unselected cells should be greater than VTH2 (FIG. **8**A). By observing such conditions, it is understood that NLEs of unselected cells (along sneak paths) should have voltages across hem such that they remained non-conductive, see suppressed region **800** in FIG. **8**A.

In various embodiments of the present invention, in the example of FIG. **4**, during a read operation (for example), when the read voltage Vread is applied to target cell **408**, the voltage Vread (e.g. VTH1<Vread (V**408**)<Vprogram, e.g. Vread=2 volts) is applied to second top electrode **418** and ground (e.g. Vg, e.g. Vg=0 volts) is applied to the second bottom electrode **420**. In the case of a program operation V**408**>Vprogram. To reduce power consumption/requirements of the memory, the inventors have recognized that it is advantageous to set unselected bit lines (e.g. top electrodes/conductors) and unselected word lines (e.g. bottom conductors/electrodes) to voltages other than floating during a read operation. The specific voltages may vary, and are generally guided by the following concepts.

For a read (or program or erase) operation, for memory cells, e.g. memory cells **402**, that share second top electrode **418** (e.g. selected bit line), the difference (V**402**) between the voltage across second top electrode **418** (VSBL) and unselected word lines, (e.g. first bottom electrode **412**) (VUSWL) should be less than the voltage threshold of the NLE of memory cells such as memory cell **402**. In variable format: VSBL−VUSWL<VTH1 or V**402**<VTH1 (FIG. **8**A). This condition would inhibit the NLE memory cells such as memory cell **402** from entering into relatively non-conductive states. It should be noted that, depending upon the polarity of V**402**, to inhibit the NLE of memory cells, such as memory cell **402** from become relatively non-conductive in a reverse-bias condition, the relationship maybe VTH2<V**402**<VTH1. This was graphically illustrated by the flat region in FIG. **6**D (0 to VTHC1), and the flat region in FIG. **6**E (VTHC2 to 0), illustrated together in region **800** in FIG. **8**A. These restrictions are desirable also in program or erase operations upon memory cell **408**. In other memory configurations, these specific relationships and polarities may be changed.

For a read (or program or erase) operation, for memory cells, e.g. memory cells **406**, that share second bottom electrode **420** (e.g. selected word line), the difference V**406** between the voltage across unselected bit lines (e.g. first top electrode **410**) (VUSBL) and second bottom electrode **420** (e.g. selected word line) (VSWL) should be less than the voltage threshold of the NLE of memory cells such as memory cell **406**. In variable format: VUSBL−VSWL<VTH1 V**406**<VTH1. This condition would inhibit the NLE of memory cells such as memory cell **406** from entering into relatively non-conductive states. It should be noted that, depending upon the polarity of V**406**, to inhibit the NLE of memory cells, such as memory cell **406** from become relatively non-conductive in a reverse-bias, the relationship maybe VTH2<V**406**<VTH1. This was graphically illustrated by the flat region in FIG. **6**D (0 to VTHC1), and the flat region in FIG. **6**E (VTHC2 to 0), illustrated together in region **800** in FIG. **8**A. These restrictions are desirable also in program or erase operations upon memory cells **404**. In various embodiments, VTH1 and |VTH2| may be different, or similar. In other memory configurations, these specific relationships and polarities may be changed.

For a read (or program or erase) operation, for memory cells, e.g. memory cells **404**, that share unselected word lines (e.g. first bottom electrode **412**), the difference (V**404**) between the voltage across unselected bit lines (e.g. first top electrode **410**) (VUSBL) and unselected word lines (e.g. first bottom electrode **412**) (VUSWL) should be less than the voltage threshold of the NLE of memory cells such as memory cells **404**. In variable format: VUSBL−VUSWL<VTH1 or V**404**<VTH1. This condition would inhibit the NLE of memory cell **404** from entering into a

relatively non-conductive state. It should be noted that depending upon the polarity of V**404**, to inhibit the NLE of memory cells, such as memory cell **404** from become relatively non-conductive in a reverse-bias, the relationship maybe VTH2<V**404**<VTH1. This was graphically illustrated by the flat region in FIG. **6**D (0 to VTHC1), and the flat region in FIG. **6**E (VTHC2 to 0), illustrated together in region **800** in FIG. **8**A. These restrictions are desirable also in program or erase operations upon memory cells **404**. In other memory configurations, these specific relationships and polarities may be changed.

FIGS. **8**A-B illustrate an example according to various embodiments of the present invention. In one example of the above, the programming voltage Vprogram=2 volts, the positive threshold voltage (VTH1) of the NLE=1 volt, and the negative threshold voltage (VTH2) of the NLE=−2 volts. In such a configuration, to perform a program operation, the selected word line (e.g. second bottom electrode **420**) is grounded (VSWL=0 volts), and selected bit line (e.g. second top electrode **418**) (VSBL) is greater than the positive threshold voltage (e.g. VTH1 (1 volt)<VSBL, Vprogram (2 volts)). Thus, Vprogram=V**408**. Additionally, the unselected word lines (e.g. first bottom electrode **412**) are set to about 1.5 volts (VUSWL=1.5 volts), accordingly, the voltage across memory cells such as memory cells **402** are less than the NLE switching voltage (e.g. VTH2 (~2 volts)<V**402** (2 volts−1.5 volts=0.5 volts)<VTH1 (1 volts). Further, the unselected bit lines (e.g. first top electrode **410**) (VUSBL) are set to about 0.5 volts, accordingly, the voltage across memory cells such as memory cells **406** are thus less than the NLE switching voltage (e.g. VTH2 (−2 volts)<V**406** (0.5 volts−0 volts=0.5 volts)<VTH1 (1 volts). Still further, from above the unselected bit lines (e.g. first top electrode **410**) are set to about 0.5 volts (VUSBL=0.5 volts), and the unselected word lines (e.g. first bottom electrode **412**.) (VUSWL) are set to about 1.5 volts (VUSWL=1.5 volts). In such a configuration, because the bottom electrodes (e.g. **412**) have a higher voltage than the top electrodes (e.g. **410**), memory cells, such as memory cells **404** are in a reverse bias voltage region. Accordingly, the voltage across memory cells such as memory cell **404** are less than the NLE switching voltage VTH1, but also need to be greater than VTH2: (e.g. VTH2 (−2 volts)<V**404** (0.5 volts−1.5 volts=−1.0 volts)<VTH1 (1 volts). As mentioned above, these restrictions are also desirable in write and erase operations. For example in a read case VTH1<Vread (V**408**)<Vprogram; and in an erase case Verase (V**408**)<VTH2.

In various embodiments, based upon the voltages V**408**, V**402**, V**406**, V**404**, and the like, the current requirements of memory cells may be computed during read, program, or erase operations. For example, power consumption for memory cells such as memory cells **402** (along the selected bit line second top electrode **418**) is the number of cells times the current across memory cells (V**402** (e.g. 0.5 volts)/resistance of NLE in relatively non-conductive state); plus power consumption for memory cells such as memory cells **406** (along unselected bit lines, first top electrode **410**) is the number of cells times the current across memory cells (V**406** (e.g. 0.5 volts)/resistance of NLE in relatively non-conductive state); plus power consumption for memory cells such as memory cells **404** (along unselected bit lines, first top electrode **410**, and along unselected word lines, first bottom electrode **412**) is the number of cells times the current across the memory cells (V**404** (e.g. −1 volt)/resistance of NLE in relatively non-conductive state). In some embodiments, setting of the bias voltages of unselected bit lines **410** (VUSBL) and unselected word lines may **412** (VUSWL) be made considering the power consumption described above.

In one example, using a large array (e.g. 100×100) of memory cells, if the voltage of the unselected bit lines (e.g. first top electrode **410**) (VUSBL) and the unselected word lines (e.g. first bottom electrode **412**) (VUSWL) are substantially the same the voltages, V**404** is small (e.g. about 0). Accordingly, the power consumption of these memory cells (99 cells×99 cells=9801 cells) is small (e.g. about 0), and power consumed/required is computed, consumed, mainly from the memory cells along the selected bit line **418** (99 cells along the second top electrode **418**) and from the memory cells along the selected word line **420** (99 cells along the second bottom electrode **420**). In one example of this VSBL=4V, VSWL=0V, VUSBL=2V, VUSWL=2V.

Although certain of the above passages have been described with respect to a read operation, it should be understood that the above also apply to other operations, such as programming operations and erase operations. In each of these situations, embodiments of the present invention incorporating NLE elements within a memory cell help to reduce sneak paths/currents through unselected memory cells. More particularly, for memory cells **402**, **404** and **406** along sneak path **416**, the voltages across these cells should be within a NLE non-conductive (suppressed) region **800**, illustrated in FIG. **8**A, to reduce sneak path current. This is in comparison with the graph illustrated in FIG. **2**, for embodiments without NLE-type elements.

In other embodiments, NLEs with different threshold voltages may be used, resistive switching material having different program and erase voltages may be used, different voltages may be applied to bias unselected word lines and/or unselected bit lines, different polarity materials may be used, and the like. Still other embodiments may be applied to unipolar-type memory cells.

In light of the present patent disclosure, one of ordinary skill in the art will recognize that in other embodiments, the voltages for selected bit lines, unselected bit lines, selected word lines, unselected word lines, NLE threshold voltages, read voltages, and the like may vary from those illustrated above, depending upon specific engineering requirements, e.g. power consumption, performance, and the like

The examples and embodiments described herein are for illustrative purposes only and are not intended to be limiting. Various modifications or alternatives in light thereof will be suggested to persons skilled in the art and are to be included within the spirit and purview of this application and scope of the appended claims.

We claim:

1. Method for operating a memory comprising:

applying a read voltage to the memory, wherein the memory comprising a plurality of cells including at least a first cell, a second cell, a third cell, and a fourth cell,

wherein the first cell and the second cell are coupled to a first top electrode,

wherein the third cell and the fourth cell are coupled to a second top electrode,

wherein the first cell and the third cell are coupled to a first bottom electrode,

wherein the second cell and the fourth cell are coupled to a second bottom electrode,

wherein each cell of the plurality of cells comprises a resistive switching material stack comprising a resistive switching material overlying a non-linear switching element material,

wherein the resistive switching material is characterized by a first voltage associated with switching from a non-conductive state to a conductive state,

wherein the non-linear switching element material is characterized by a second voltage associated with switching from a non-conductive state to a conductive state,

wherein the second voltage is less than the first voltage,

wherein the read voltage is between the first voltage and the second voltage, and

wherein applying the read voltage to the memory comprises applying the read voltage to the first top electrode while grounding the first bottom electrode to thereby cause non-linear switching element material of the first cell to be in the conductive state, while maintaining non-linear switching element material of the second cell, the third cell, and the fourth cell to remain in the non-conductive state; **[**and**]**

detecting a read current across the first cell in response to the read voltage**[**.**]***;*

wherein the resistive switching material is characterized by a third voltage associated with switching from the conductive state to the non-conductive state;

wherein the non-linear switching element material is characterized by a fourth voltage associated with switching from the non-conductive state to the conductive state; and

wherein the third voltage is less than the fourth voltage.

2. The method of claim **1** wherein a resistance of the non-conductive state is related to a resistance of the conductive state in a range of ratios selected from a group consisting of: about 100 to about 500 times greater, about 500 to about 1000 times greater, about 1000 times to about 10,000 times greater.

3. The method of claim **1** wherein while applying the read voltage to the first top electrode while grounding the first bottom electrode, a voltage across the second cell is maintained at less than the second voltage.

[4. The method of claim **1**

wherein the resistive switching material is characterized by a third voltage associated with switching from the conductive state to the non-conductive state;

wherein the non-linear switching element material is characterized by a fourth voltage associated with switching from the non-conductive state to the conductive state; and

wherein the third voltage is less than the fourth voltage.**]**

5. The method of claim **[4]** *1* wherein while applying the read voltage to the first top electrode while grounding the first bottom electrode, a voltage across the fourth cell is maintained at greater than the fourth voltage to thereby maintain the non-linear switching element material of the third cell in the non-conductive state.

6. The method of claim **[4]** *1* wherein while applying the read voltage to the first top electrode while grounding the first bottom electrode, the method further comprises applying a fifth voltage between ground and the read voltage to the second bottom electrode.

7. The method of claim **6** wherein while applying the read voltage to the first top electrode while grounding the first bottom electrode, the method further comprises applying a sixth voltage between ground and the read voltage to the second top electrode.

8. The method of claim **7** wherein a difference between the sixth voltage and the fifth voltage is greater than the fourth voltage.

9. The method of claim **1** further comprising:

applying a write voltage to the memory, wherein the write voltage exceeds the first voltage, wherein applying the write voltage to the memory comprises applying the write voltage to the first top electrode while grounding the first bottom electrode to thereby cause the resistive switching material of the first cell to be in the conductive state.

10. The method of claim **9** wherein applying the write voltage to the first top electrode comprises applying the write voltage to the first top electrode while grounding the first bottom electrode to thereby cause the non-linear switching element material of the first cell to switch from the non-conductive state to the conductive state.

11. A memory operated according to the method described in claim **1**.

12. A memory comprising:

a plurality of cells including at least a first cell, a second cell, a third cell, and a fourth cell, wherein each cell of the plurality of cells comprises a resistive switching material stack comprising a resistive switching material overlying a non-linear switching element material, wherein the resistive switching material is characterized by a first voltage associated with switching from a non-conductive state to a conductive state, wherein the non-linear switching element material is characterized by a second voltage associated with switching from a non-conductive state to a conductive state, wherein a second voltage is less than the first voltage;

a plurality of top electrodes including a first top electrode and a second top electrode, wherein the first cell and the second cell are coupled to the first top electrode, and wherein the third cell and the fourth cell are coupled to the second top electrode;

a plurality of bottom electrodes including a first bottom electrode and a second bottom electrode, wherein the first cell and the third cell are coupled to the first bottom electrode, and wherein the second cell and the fourth cell are coupled to the second bottom electrode, wherein a read current path is associated with the first cell, wherein non-read current paths are associated with the second cell, the third cell, and the fourth cell, wherein the non-linear switching element material of the first cell is configured to reduce resistance of the read current path, and wherein the non-linear switching element material of the second cell, the third cell, and the fourth cell are configured to increase resistance of the non-read current; **[**and**]**

a voltage source coupled to the plurality of top electrodes and to the plurality of bottom electrodes, wherein the voltage source is configured to provide a plurality of voltages to the plurality of top electrodes and to the plurality of bottom electrodes**[**.**]***;*

wherein the resistive switching material is characterized by a third voltage associated with switching from the conductive state to the non-conductive state;

wherein the non-linear switching element material is characterized by a fourth voltage associated with switching from the non-conductive state to the conductive state; and

wherein the third voltage is less than the fourth voltage.

13. The memory of claim **12**

wherein the non-linear switching element material of the first cell is configured to be in the conductive state dependent upon a read voltage that is greater than the

second voltage but less than the first voltage, that is applied to the first top electrode while grounding the first bottom electrode; and

wherein the voltage source is configured to provide the read voltage.

14. The memory of claim **12**

wherein the non-linear switching element material of the second cell is configured to be in the non-conductive state dependent upon a read voltage that is greater than the second voltage but less than the first voltage, is applied to the first top electrode while grounding the first bottom electrode; and

wherein the voltage source is configured to provide the read voltage.

15. The memory of claim **14** wherein when the read voltage is applied to the first top electrode while grounding the first bottom electrode, a voltage greater than ground is applied to the second bottom electrode such that a voltage across the second cell is less than the second voltage.

16. The memory of claim **12** wherein the resistive switching material is selected from a group consisting of: an amorphous silicon material, a silicon sub-oxide, a silicon germanium sub-oxide.

17. The memory of claim **12** wherein each of the plurality of bottom electrodes comprises *a metal or* a conductive silicon material selected from a group consisting of: a doped polysilicon**[**,**]** *and* a doped silicon germanium material.

[18. The memory of claim **12**

wherein the resistive switching material is characterized by a third voltage associated with switching from the conductive state to the non-conductive state;

wherein the non-linear switching element material is characterized by a fourth voltage associated with switching from the non-conductive state to the conductive state; and

wherein the third voltage is less than the fourth voltage.**]**

19. The memory of claim **12**

wherein the non-linear switching element material of the fourth cell is configured to be in the non-conductive state dependent upon a read voltage that is greater than the second voltage but less than the first voltage, that is applied to the first top electrode while grounding the first bottom electrode; and

wherein a voltage difference greater than the fourth voltage is applied to the fourth cell.

20. The memory of claim **12**

wherein the voltage source is configured to provide a read voltage to the first top electrode, wherein the voltage source is configured to provide a fifth voltage to the second bottom electrode and a sixth voltage to the second top electrode, wherein a voltage difference between the second top electrode and the second bottom electrode is greater than the fourth voltage.

21. The memory of claim 12 wherein a ratio between the resistance of the first cell compared to a resistance of the second cell is greater than 1:1000.

22. The memory cell of claim 12 wherein the non-linear switching material is selected from a group consisting of: a solid electrolyte material and a metal sub-oxide.

23. The memory cell of claim 12 wherein the non-linear switching material is bi-polar.

24. The memory cell of claim 12 wherein the non-linear switching material consists of multiple layers of materials.

25. A method for operating a memory comprising:

applying a program voltage to the memory, wherein the memory comprising a plurality of cells including at least a first cell, a second cell, a third cell, and a fourth cell,

wherein the first cell and the second cell are coupled to a first top electrode,

wherein the third cell and the fourth cell are coupled to a second top electrode,

wherein the first cell and the third cell are coupled to a first bottom electrode,

wherein the second cell and the fourth cell are coupled to a second bottom electrode,

wherein each cell of the plurality of cells comprises a resistive switching material stack comprising a resistive switching material having crystal defect regions and a non-linear switching element material,

wherein each cell is characterized by a first first-polarity voltage associated with the resistive switching material switching from a non-conductive state to a conductive state and a first second-polarity voltage associated with the resistive switching material switching from the conductive state to the non-conductive state,

wherein each cell is characterized by a second first-polarity voltage and a second second-polarity voltage associated with the non-linear switching element material switching from a second non-conductive state to a second conductive state,

wherein the second first-polarity voltage is less than the first first-polarity voltage,

wherein the first second-polarity voltage is less than the second second-polarity voltage,

wherein the program voltage is greater than or equal to the first first-polarity voltage, and

wherein applying the program voltage to the memory comprises applying the program voltage to the second top electrode;

grounding the second bottom electrode;

applying a first bias to the first top electrode and applying a second bias to the first bottom electrode;

causing a non-linear switching element material of the fourth cell to enter the conductive state and causing a resistive switching material of the fourth cell to enter the conductive state,

maintaining non-linear switching element materials of the first cell, the second cell, and the third cell in the non-conductive state in response to the applying the program voltage, grounding the second bottom electrode, the applying the first bias and the applying the second bias; and

removing the program voltage from the second top electrode, whereby the non-linear switching element material of the fourth cell returns to the non-conductive state, and wherein the resistive switching material of the fourth cell remains in the conductive state.

26. The method of claim 25

wherein applying the program voltage to the second top electrode while grounding the second bottom electrode causes metal particles from the second top electrode to diffuse into crystal defect regions of the resistive switching material of the fourth cell; and

wherein after removing the program voltage from the second top electrode, the metal particles from the second top electrode remain trapped in the crystal defect regions of the resistive switching material of the fourth cell.

27. The method of claim 25 wherein while applying the program voltage to the second top electrode while grounding the second bottom electrode, a voltage across the second cell is maintained at less than the second first-polarity voltage.

28. The method of claim 25

wherein the first and second first-polarity voltages are positive; and

wherein the first and second second-polarity voltage are negative.

29. The method of claim 28 wherein

applying the first bias to the first top electrode comprises applying a first bias voltage less than the second first-polarity voltage to the first top electrode; and

wherein a voltage across the second cell in response to the applying the first bias voltage is less than the second first-polarity voltage.

30. The method of claim 29

wherein applying the second bias to the first bottom electrode comprises applying a second bias voltage to the first bottom electrode;

wherein a voltage difference between the program voltage and the second bias voltage is less than the second first-polarity voltage; and

wherein a voltage across the third cell is less than the second first-polarity voltage.

31. The method of claim 30

wherein a voltage across the first cell comprises a third second-polarity voltage; and

wherein the second second-polarity voltage is less than the third second-polarity voltage.

32. The method of claim 25 wherein a resistance ratio between the second conductive state to the second non-conductive state of the non-linear switching element material is within a range of about 1,000 to about 10,000.

33. The method of claim 25 further comprising:

applying an erase voltage to the second top electrode;

further grounding the second bottom electrode;

further biasing the first top electrode;

further biasing the first bottom electrode to thereby cause the non-linear switching element material of the fourth cell to enter the conductive state and cause the resistive switching material of the fourth cell to enter the non-conductive state, while maintaining non-linear switching element materials of the first cell, the second cell, and the third cell in the non-conductive state; and

removing the erase voltage from the second top electrode, whereby the non-linear switching element material of the fourth cell returns to the non-conductive state, and wherein the resistive switching material of the fourth cell remains in the non-conductive state.

34. The method of claim 33, wherein:

the further biasing the first top electrode comprises applying a first bias voltage less than the second first-polarity voltage to the first top electrode; and

a voltage across the second cell in response to the applying the first bias voltage is greater than the second second-polarity voltage and less than the second first-polarity voltage.

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