US00RE46100E

(19) **United States**

(12) **Reissued Patent**

Aburada et al.

(10) **Patent Number: US RE46,100 E**

(45) **Date of Reissued Patent: Aug. 9, 2016**

(54) **METHOD OF FABRICATING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE**

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(73) Assignee: **KABUSHIKI KAISHA TOSHIBA**, Tokyo (JP)

(21) Appl. No.: **14/284,709**

(22) Filed: **May 22, 2014**

Related U.S. Patent Documents

Reissue of:

(64) Patent No.: **8,183,148**
Issued: **May 22, 2012**
Appl. No.: **12/542,540**
Filed: **Aug. 17, 2009**

(30) **Foreign Application Priority Data**

Aug. 18, 2008 (JP) 2008-209849

(51) **Int. Cl.**
H01L 21/4763 (2006.01)
H01L 21/033 (2006.01)
H01L 21/3213 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 21/0337*** (2013.01); ***H01L 21/32139*** (2013.01)

(58) **Field of Classification Search**
CPC H01L 121/3205; H01L 121/3213; H01L 121/768; H01L 123/52; H01L 123/522
See application file for complete search history.

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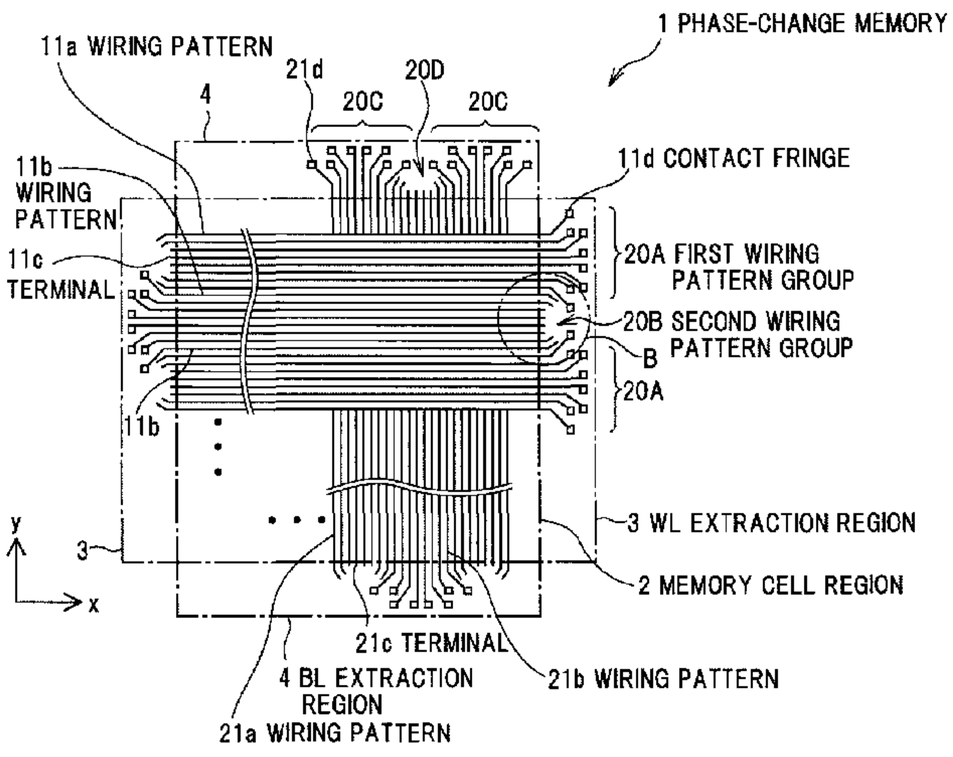
Primary Examiner — Leonardo Andujar

(74) *Attorney, Agent, or Firm* — Finnegan, Henderson, Farabow, Garrett & Dunner, LLP

(57) **ABSTRACT**

A method of fabricating a semiconductor device according to an embodiment includes forming a first pattern having linear parts of a constant line width and a second pattern on a foundation layer, the second pattern including parts close to the linear parts of the first pattern and parts away from the linear parts of the first pattern and constituting closed loop shapes independently of the first pattern or in a state of being connected to the first pattern and carrying out a closed loop cut at the parts of the second pattern away from the linear parts of the first pattern.

15 Claims, 28 Drawing Sheets



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			WO	WO 2008/027239 A2	3/2008

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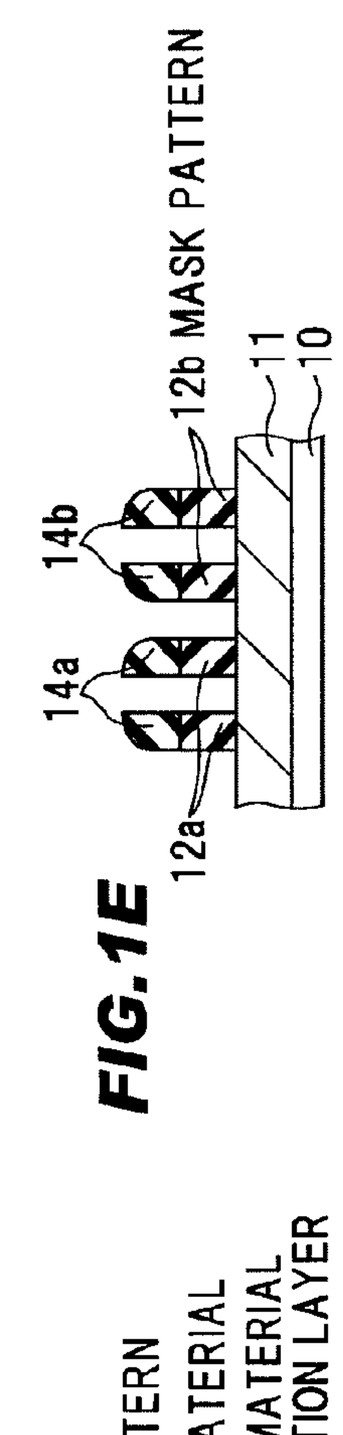


FIG.1A

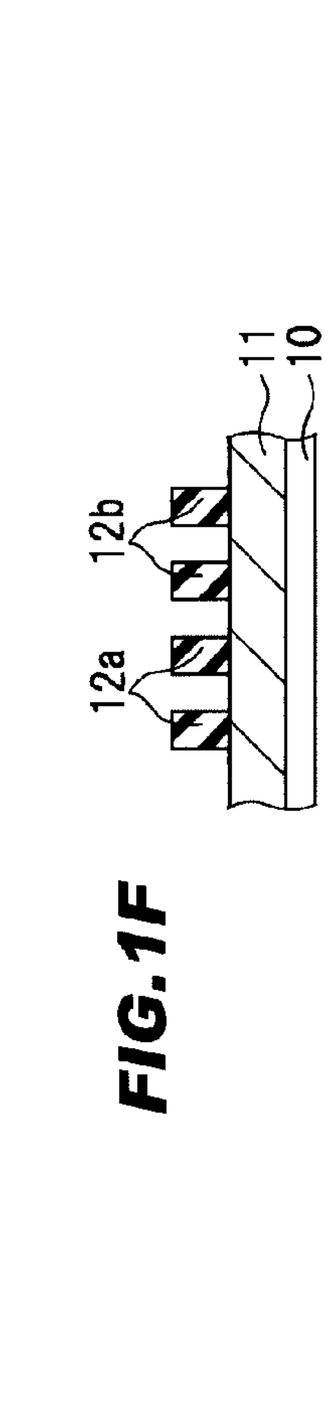


FIG.1B

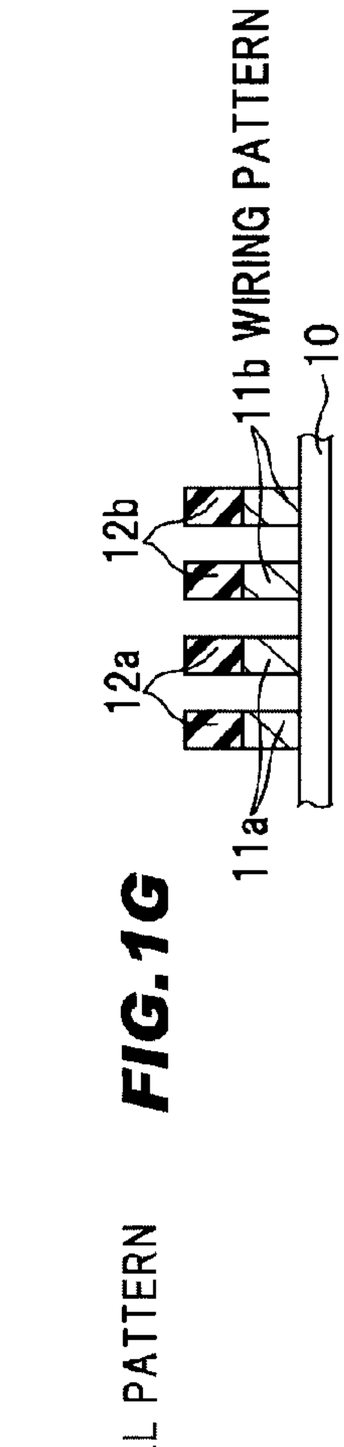


FIG.1C

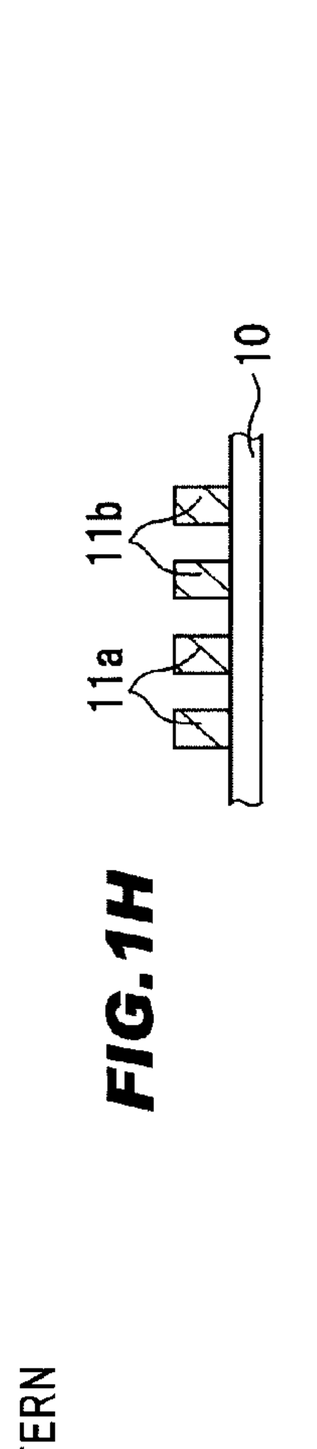


FIG.1D

FIG.1E

FIG.1F

FIG.1G

FIG.1H

FIG.2C

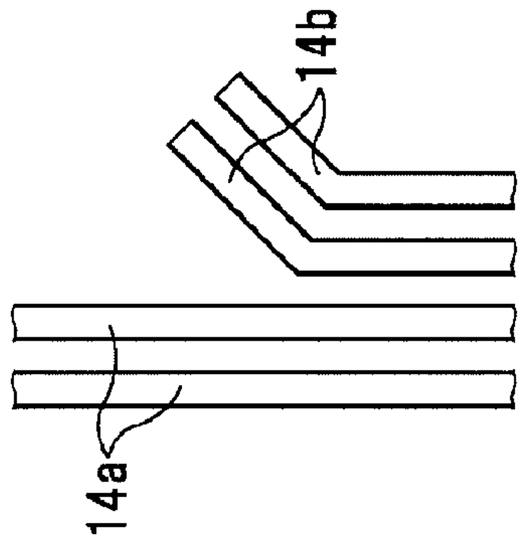


FIG.2B

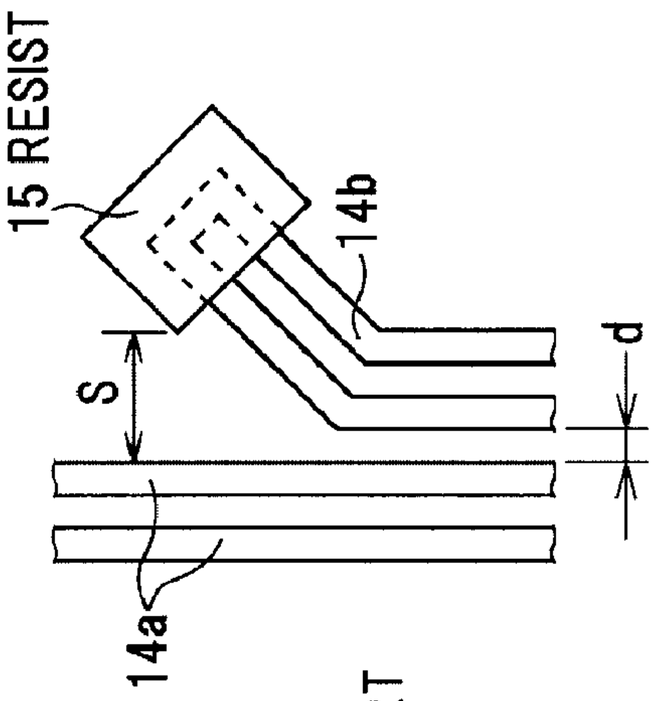
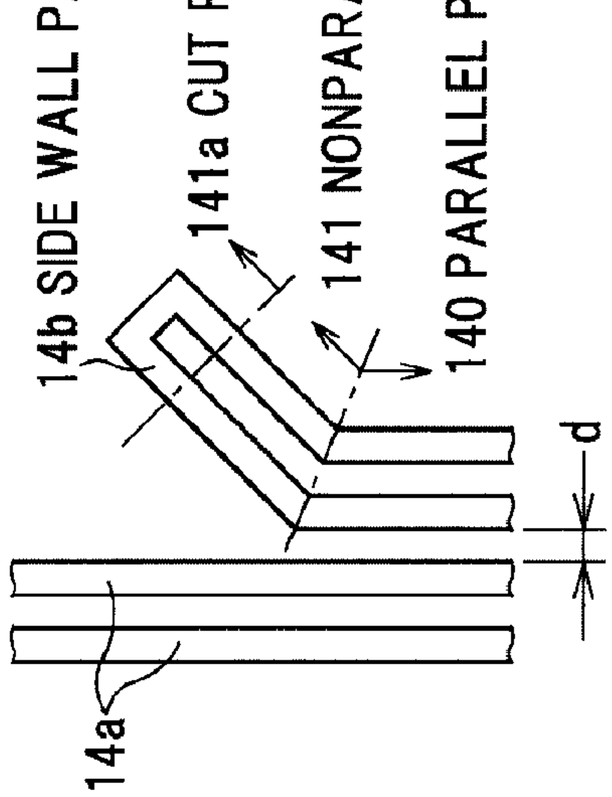


FIG.2A




13a
13b
10
FIG.3A
13a
13b
10
FIG.3B
13a
14a
13b
14b
10
FIG.3C
14a
14b
10
FIG.3D
14a
12a
12b MASK PATTERN
10
FIG.3E
12a
12b
10
FIG.3F
11a
12a
11 WIRING MATERIAL
12b
10
11b WIRING PATTERN
11b
FIG.3G
11a
11b
11e WIDE PATTERN
10
FIG.3H
10 FOUNDATION LAYER
12 MASK MATERIAL
12a CORE PATTERN
12b SIDE WALL PATTERN

FIG.4C

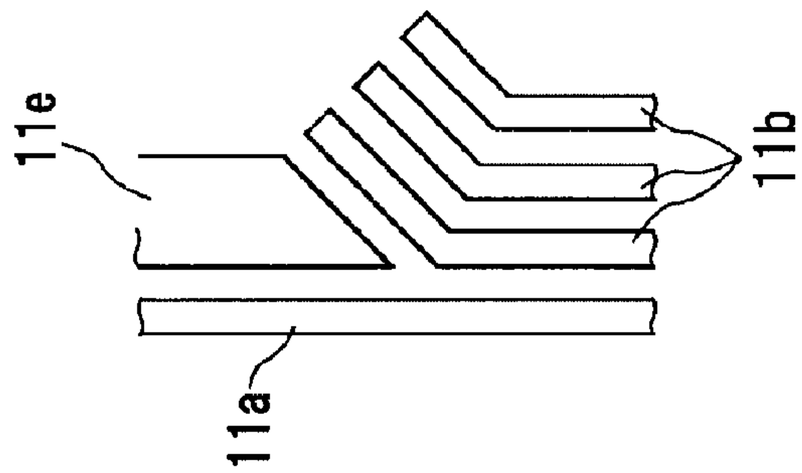


FIG.4B

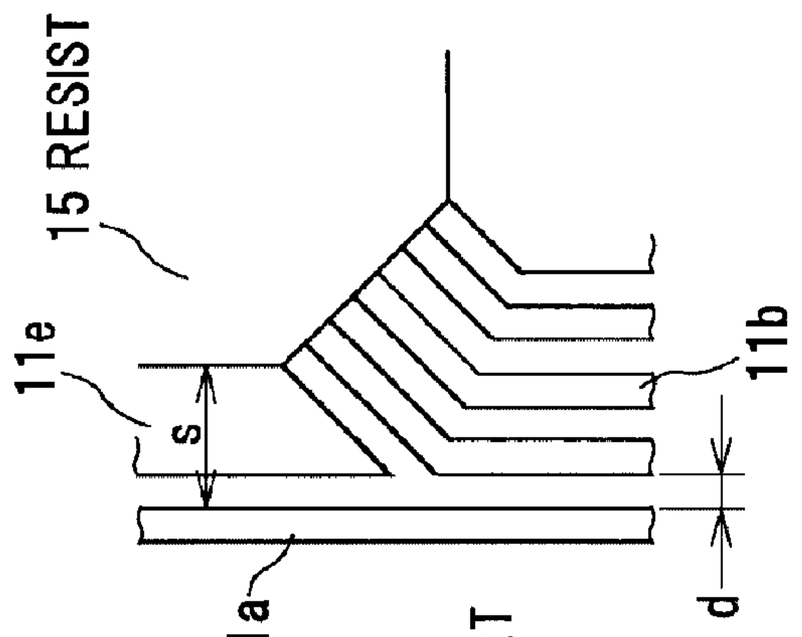


FIG.4A

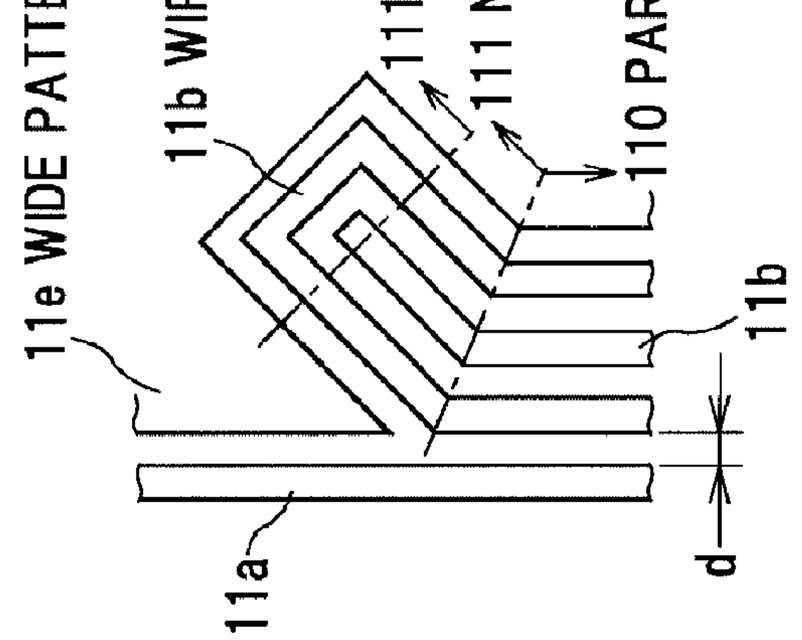


FIG.5A

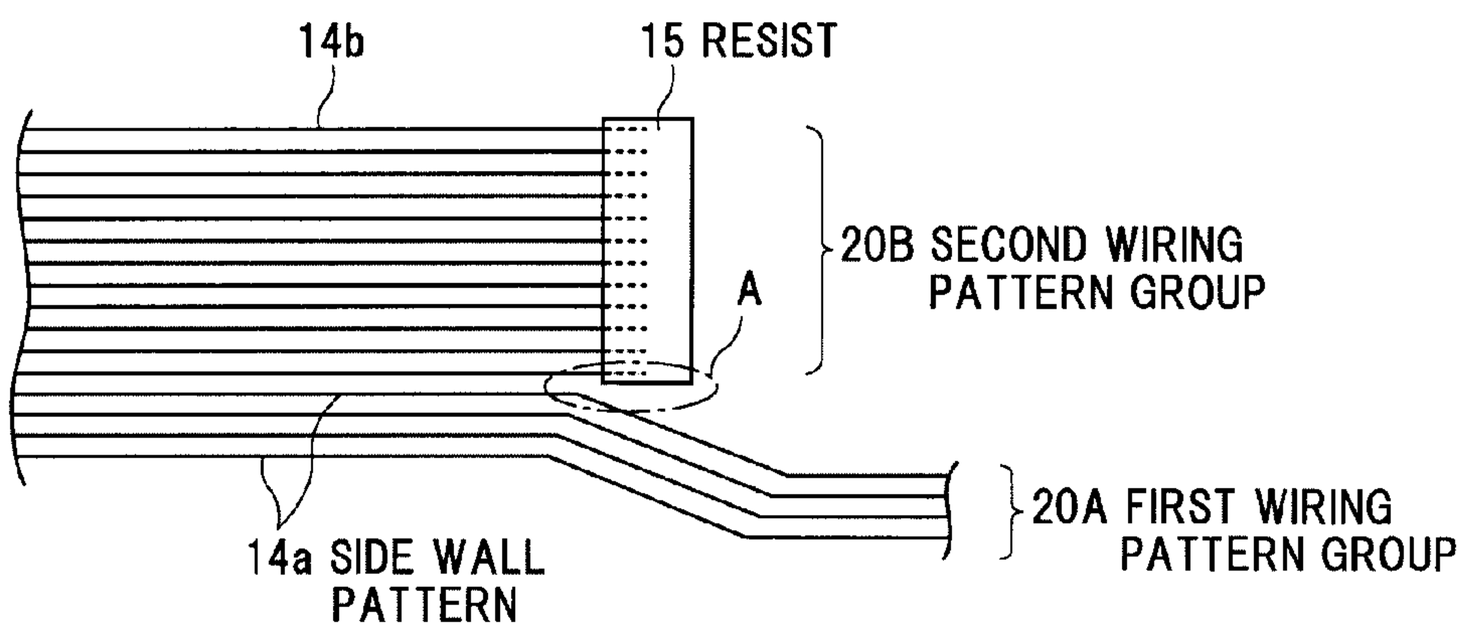

14b
15 RESIST
20B SECOND WIRING PATTERN GROUP
A
20A FIRST WIRING PATTERN GROUP
14a SIDE WALL PATTERN

FIG.5B

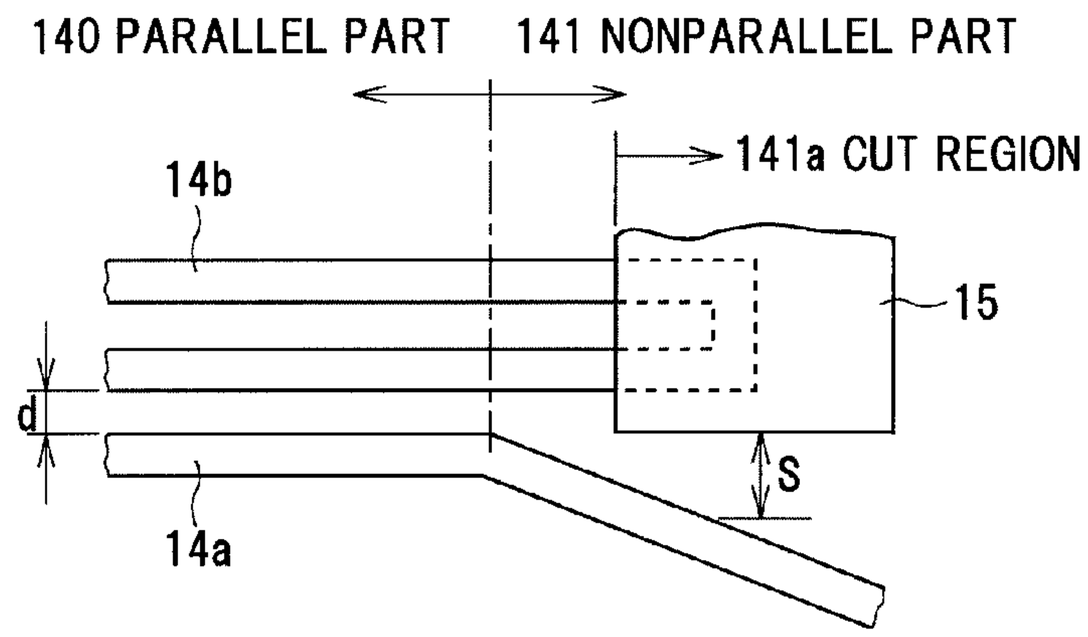

140 PARALLEL PART
141 NONPARALLEL PART
141a CUT REGION
14b
15
d
S
14a

FIG.6A

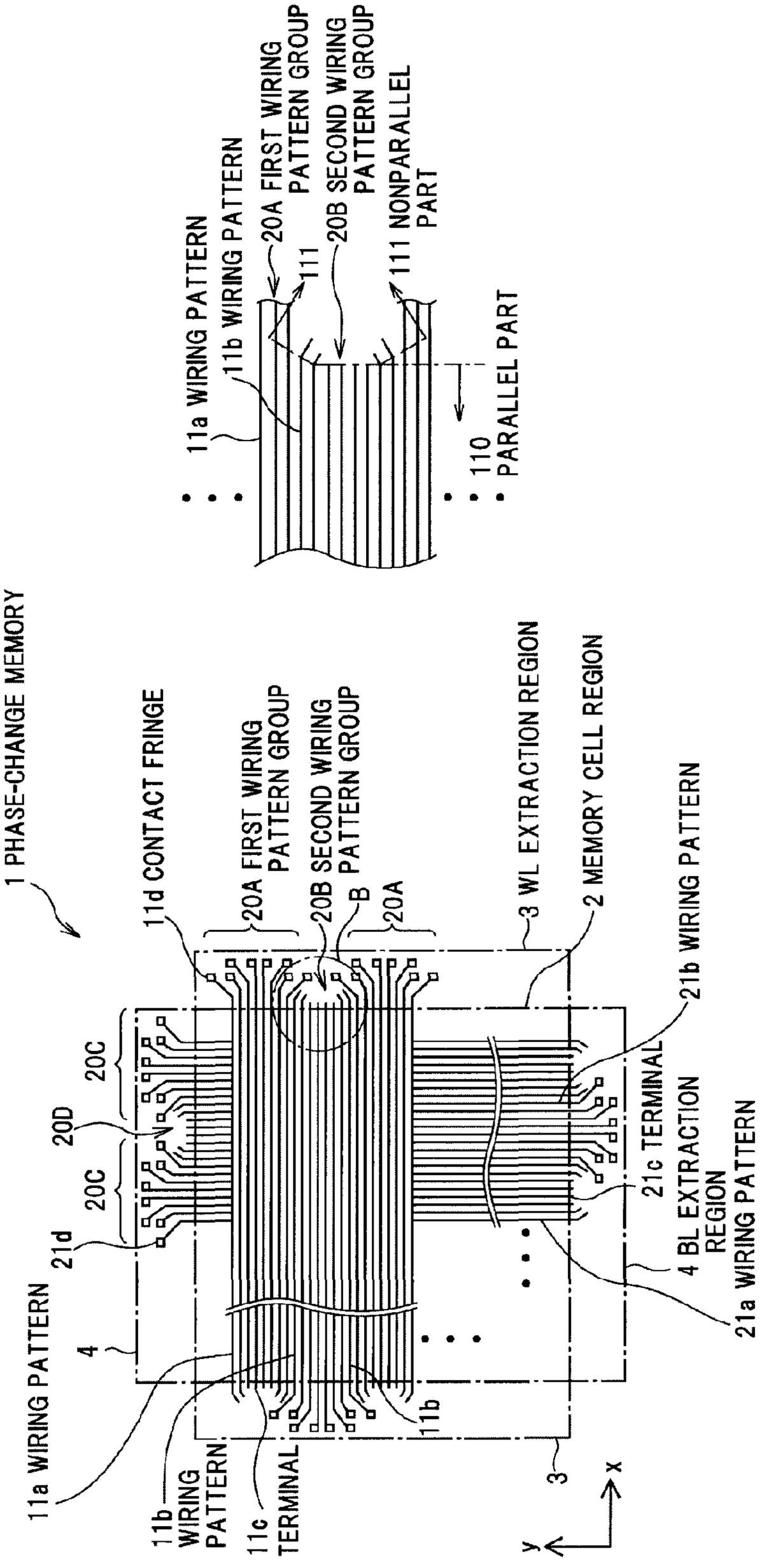

1 PHASE-CHANGE MEMORY
11d CONTACT FRINGE
20A FIRST WIRING PATTERN GROUP
20B SECOND WIRING PATTERN GROUP
B
20A
3 WL EXTRACTION REGION
2 MEMORY CELL REGION
20C
20D
20C
21d
4
11a WIRING PATTERN
11b WIRING PATTERN
11c TERMINAL
11b
3
y
x
21b WIRING PATTERN
21c TERMINAL
4 BL EXTRACTION REGION
21a WIRING PATTERN

FIG.6B

11a WIRING PATTERN
11b WIRING PATTERN
20A FIRST WIRING PATTERN GROUP
111
20B SECOND WIRING PATTERN GROUP
111 NONPARALLEL PART
110 PARALLEL PART

FIG.7A

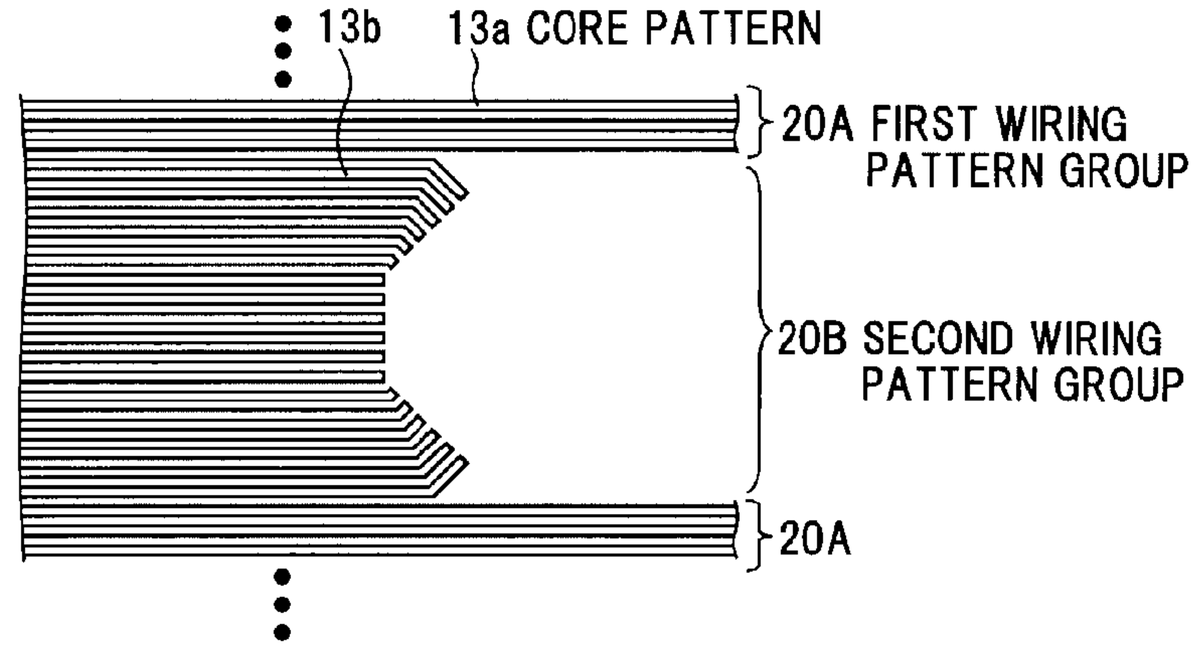


FIG.7B

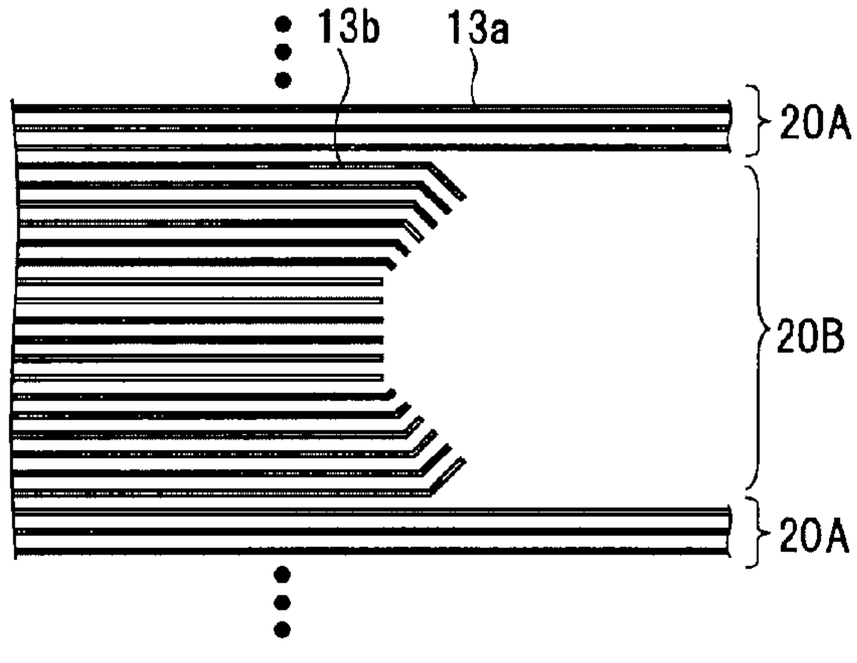


FIG.7C

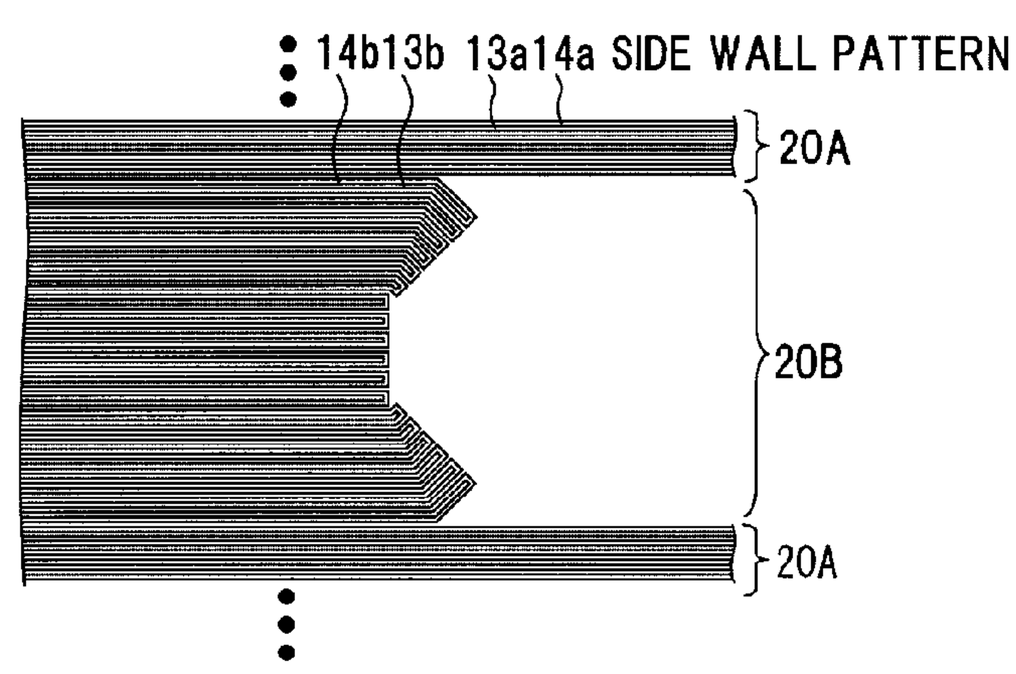


FIG.7D

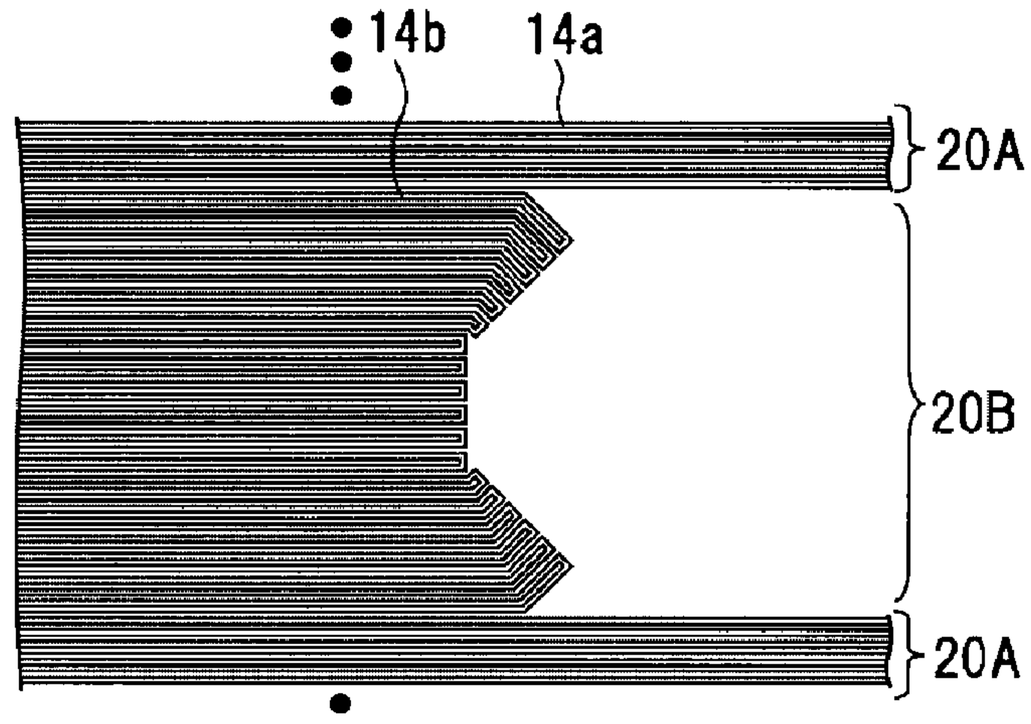


FIG.7E

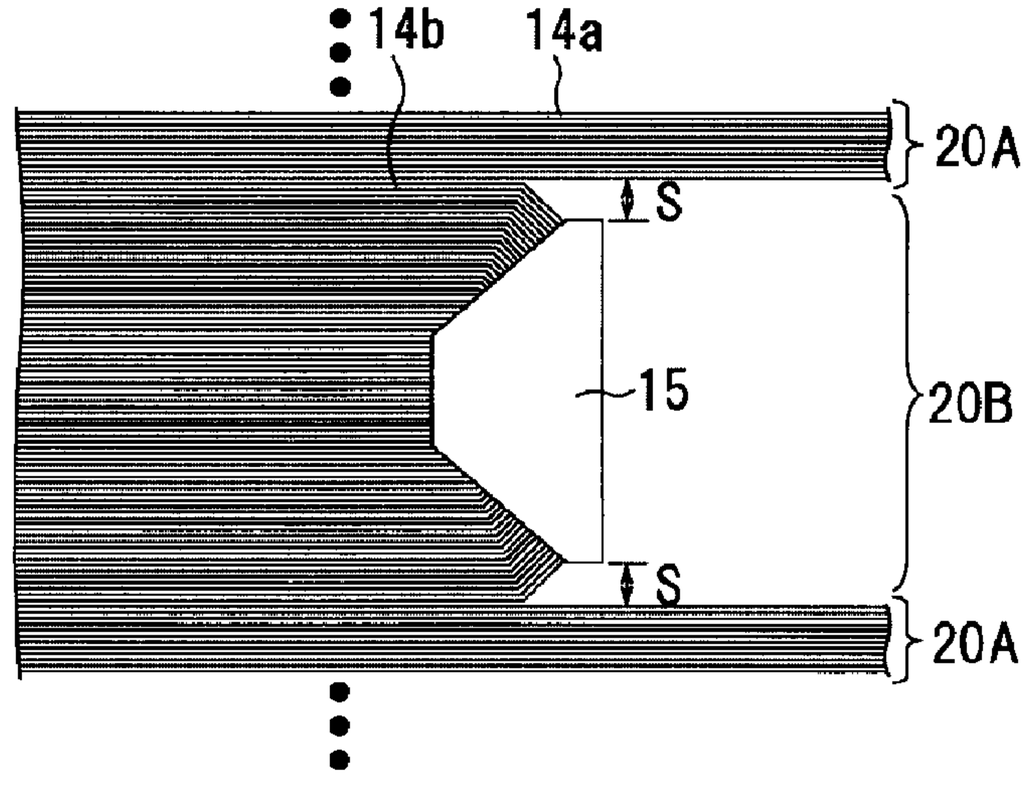


FIG.7F

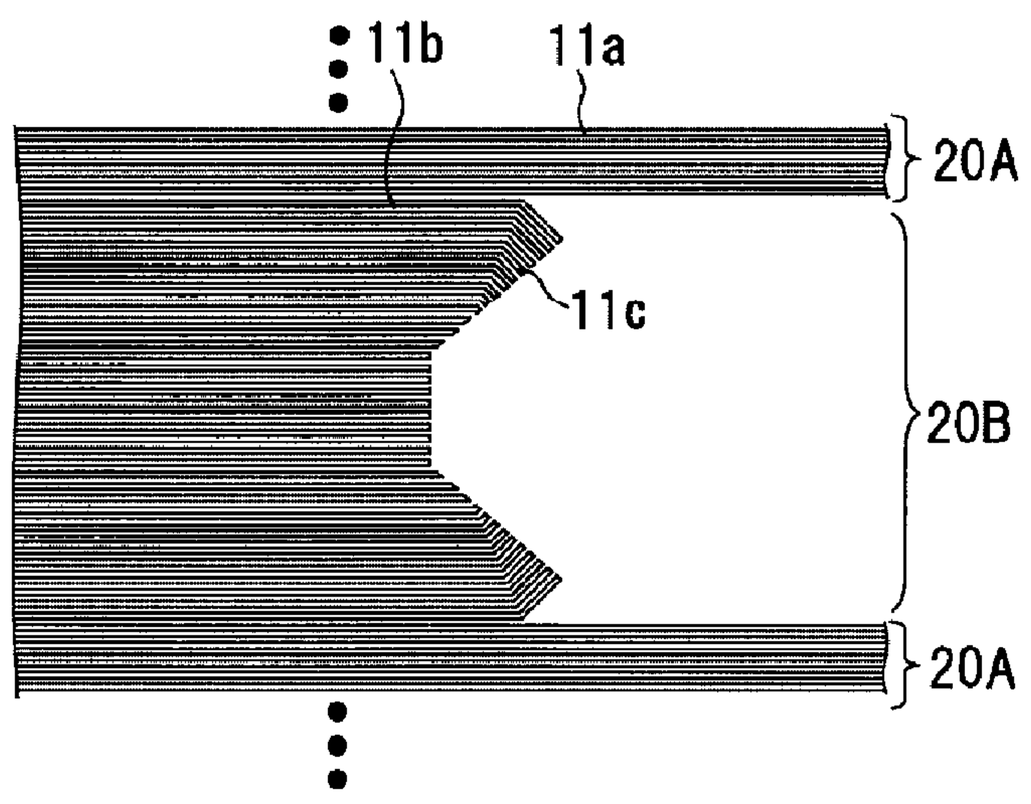


FIG.8A

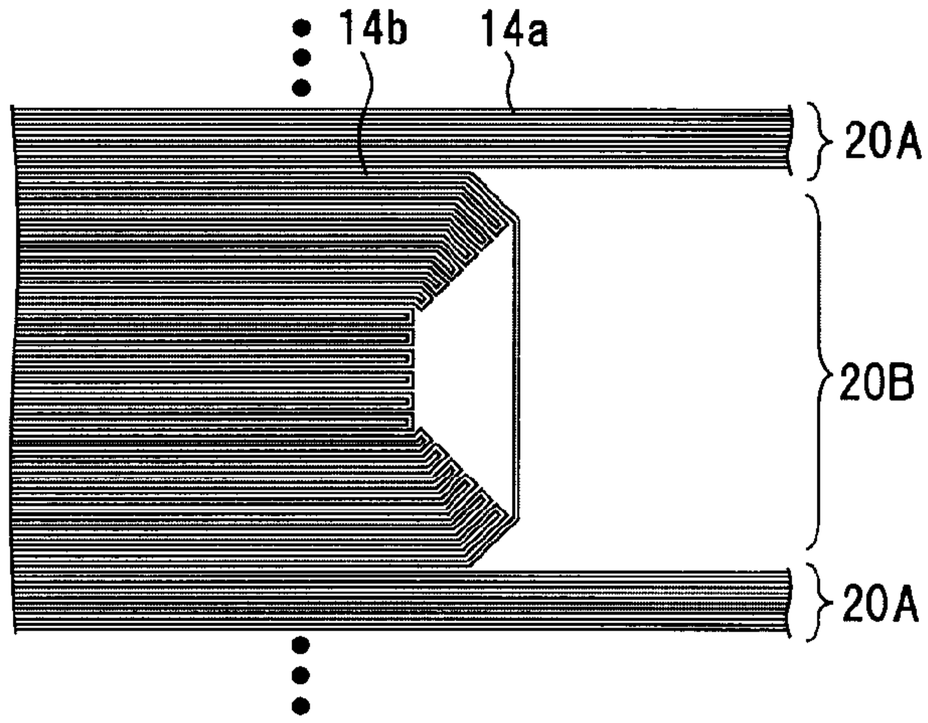


FIG.8B

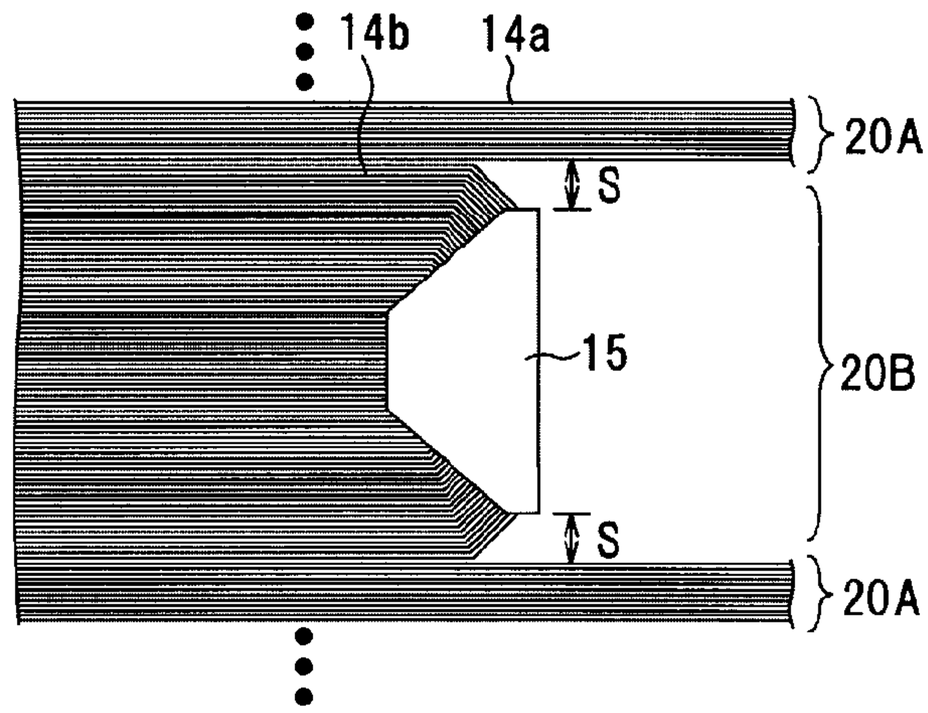


FIG.8C

FIG.9A

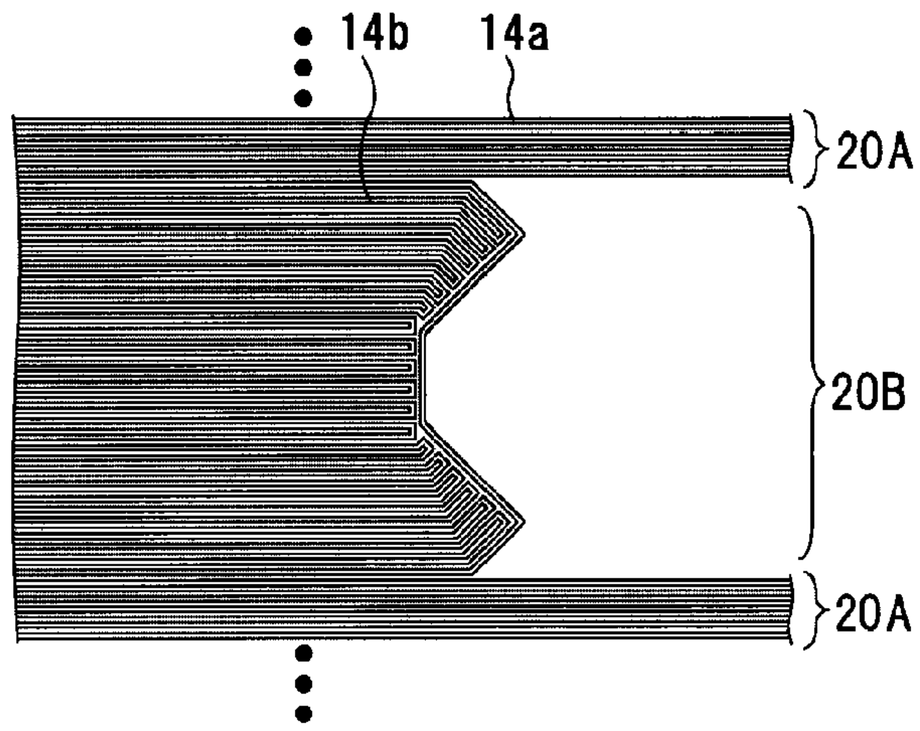


FIG.9B

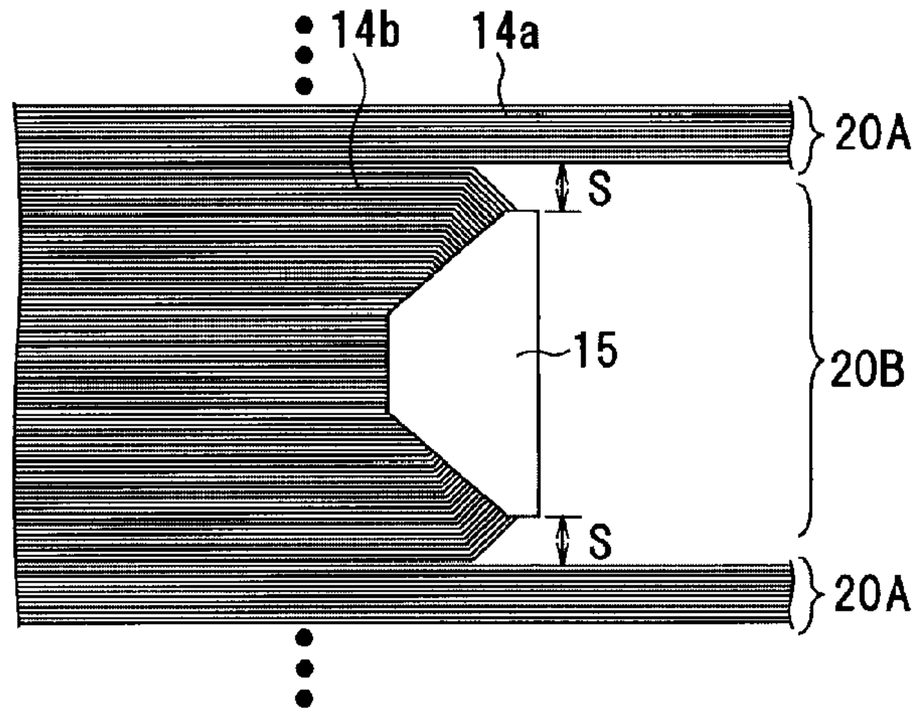


FIG.9C

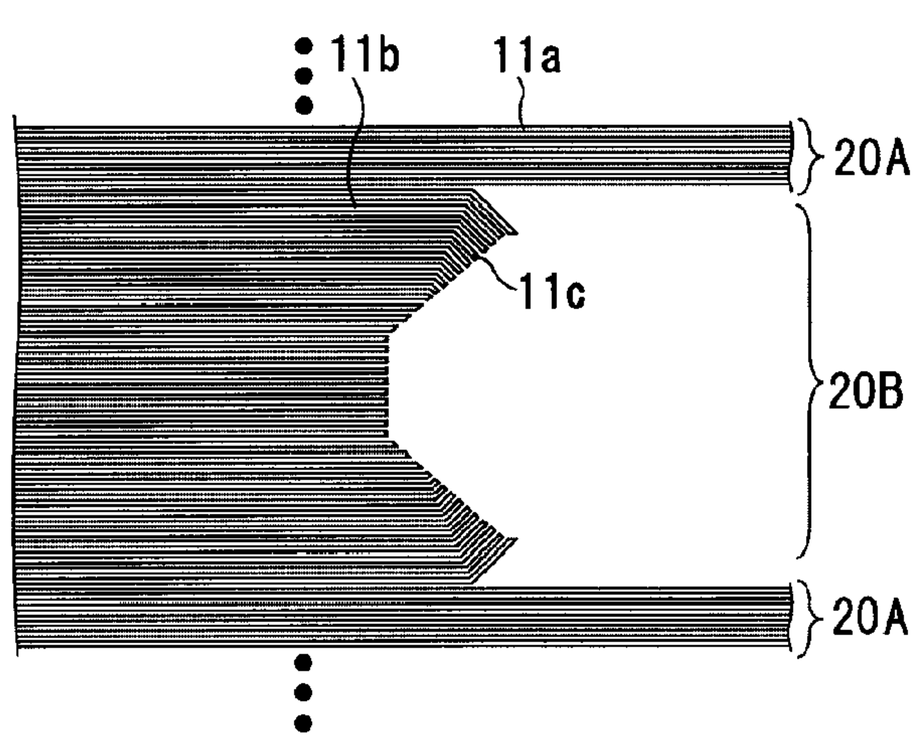


FIG.10A

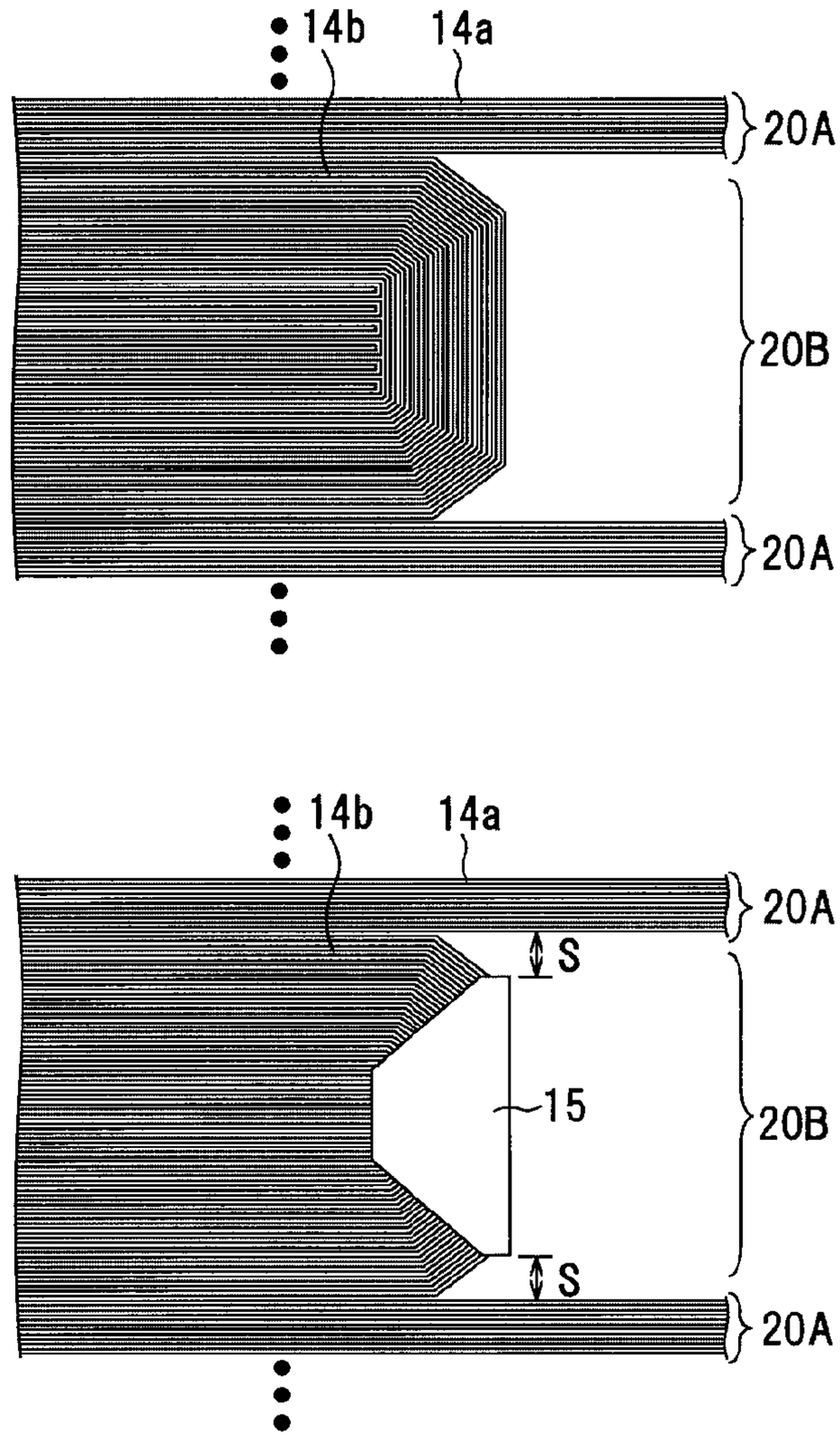


FIG.10B

FIG.10C

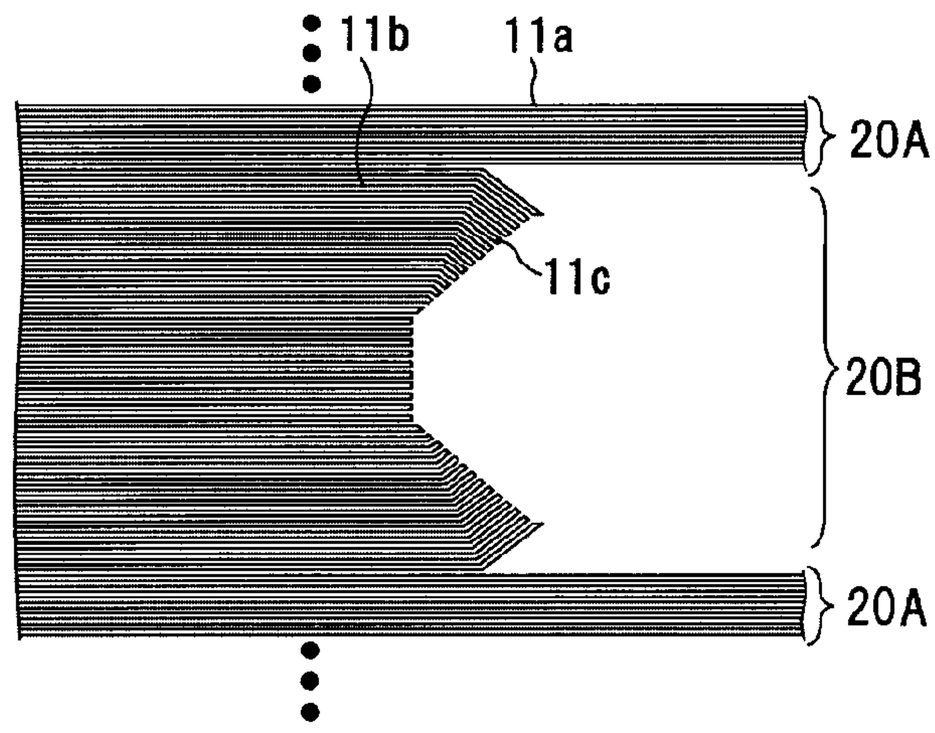


FIG.11A

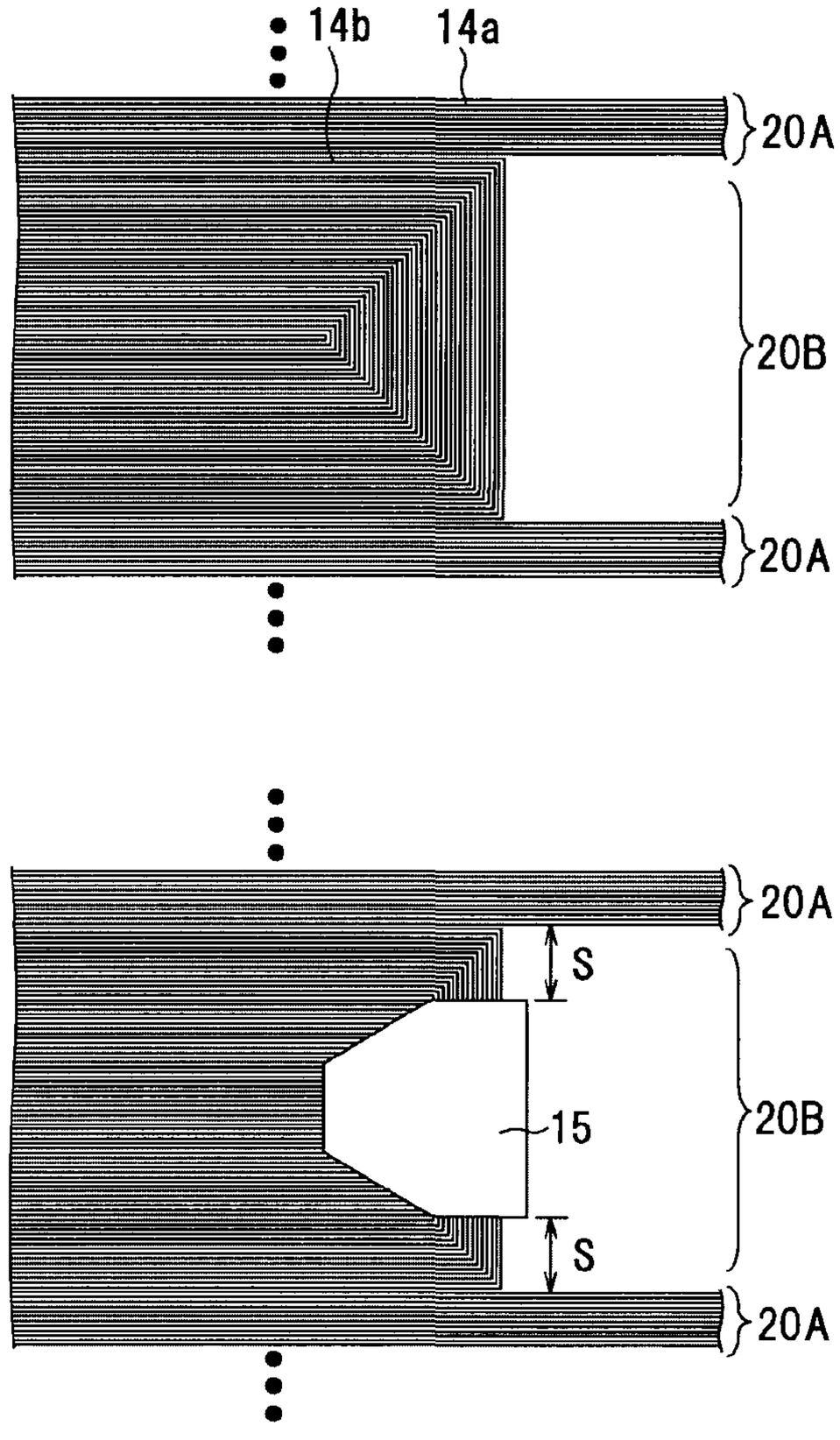


FIG.11B

FIG.11C

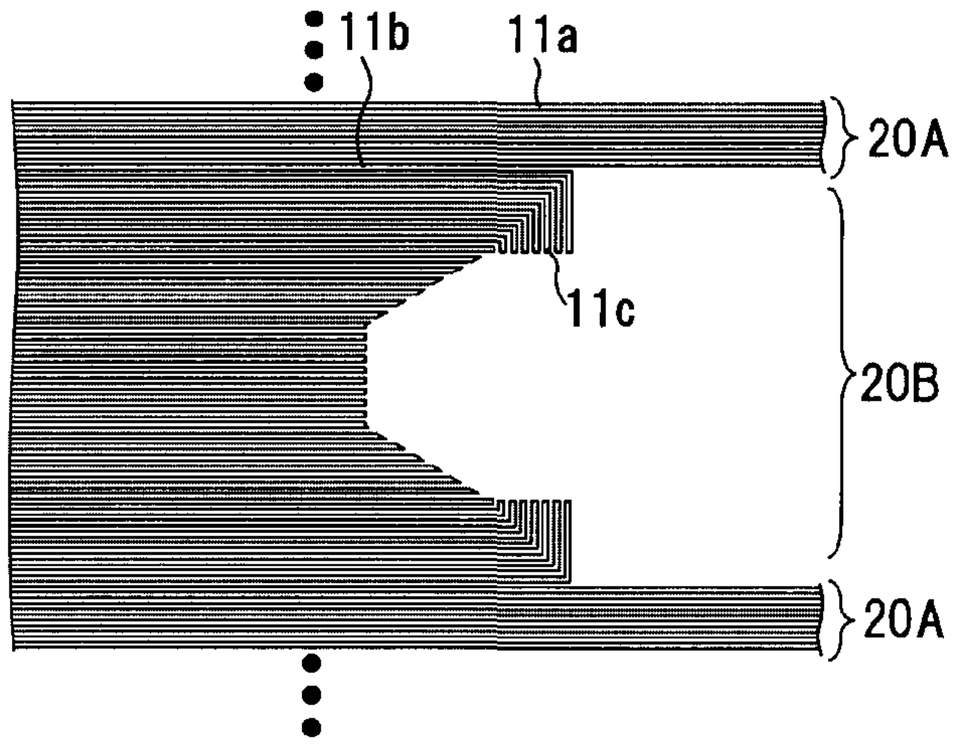


FIG.12A

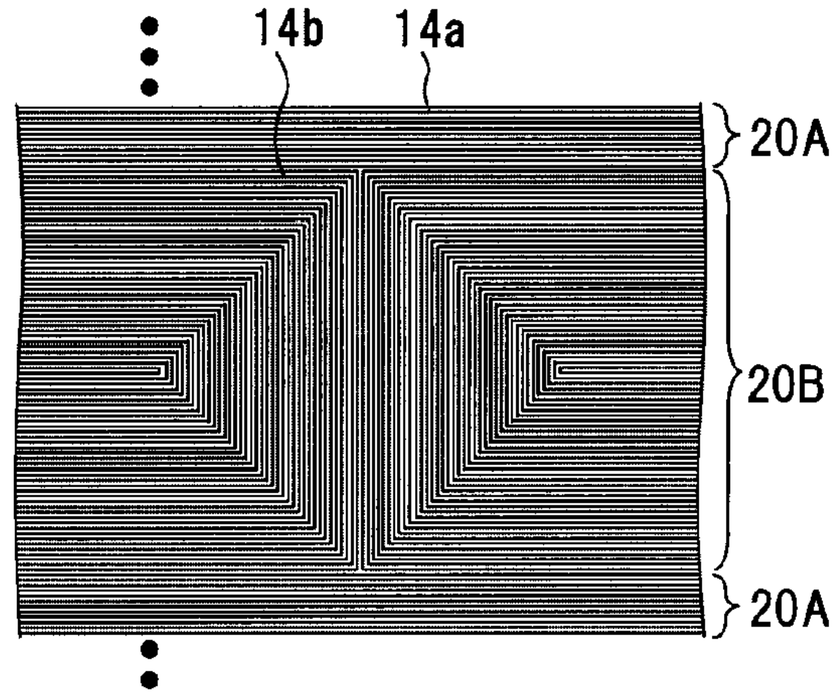


FIG.12B

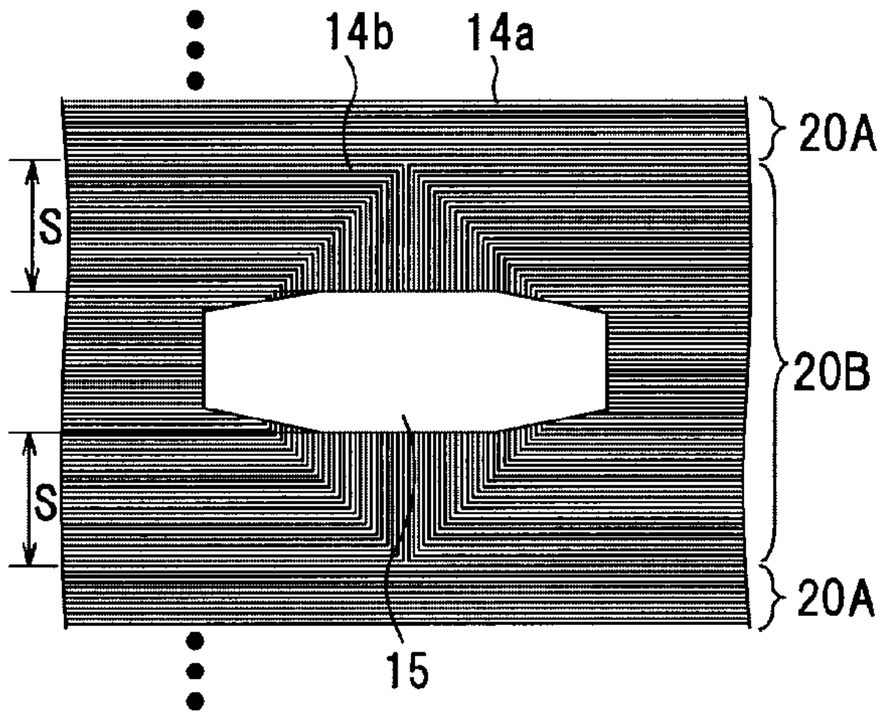


FIG.12C

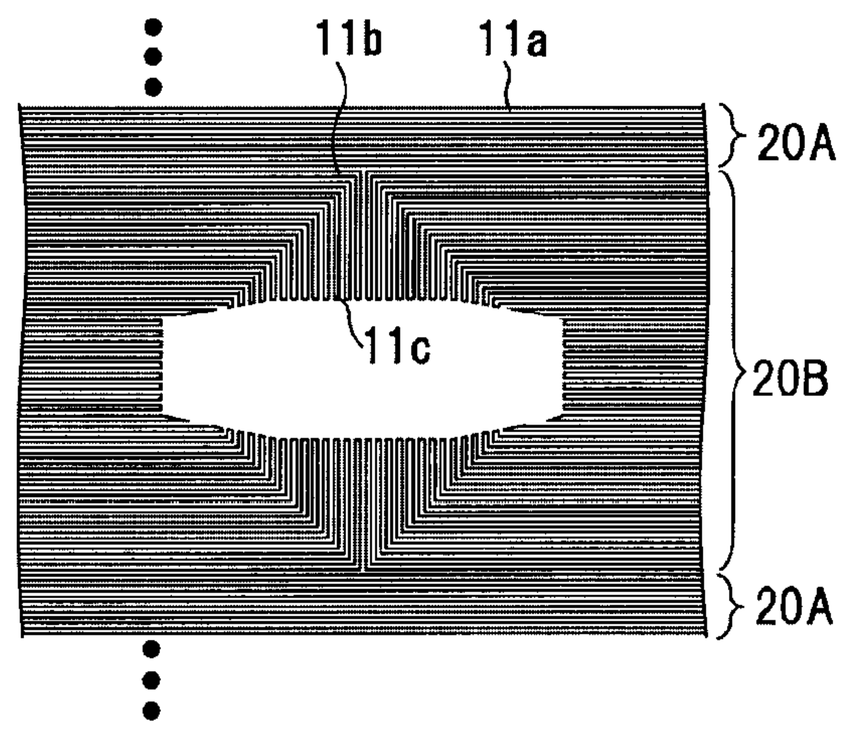


FIG.13A

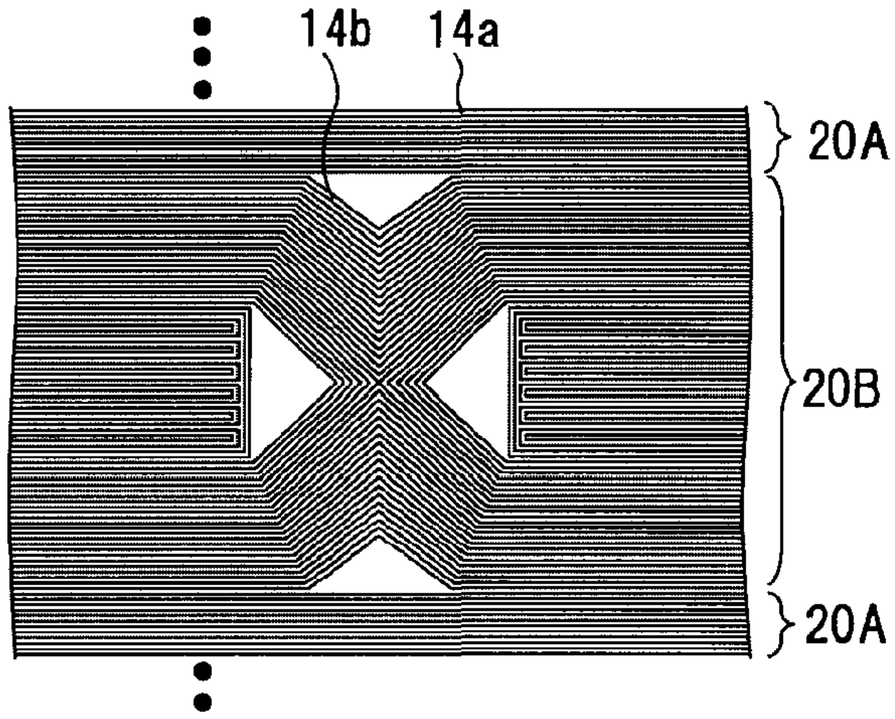
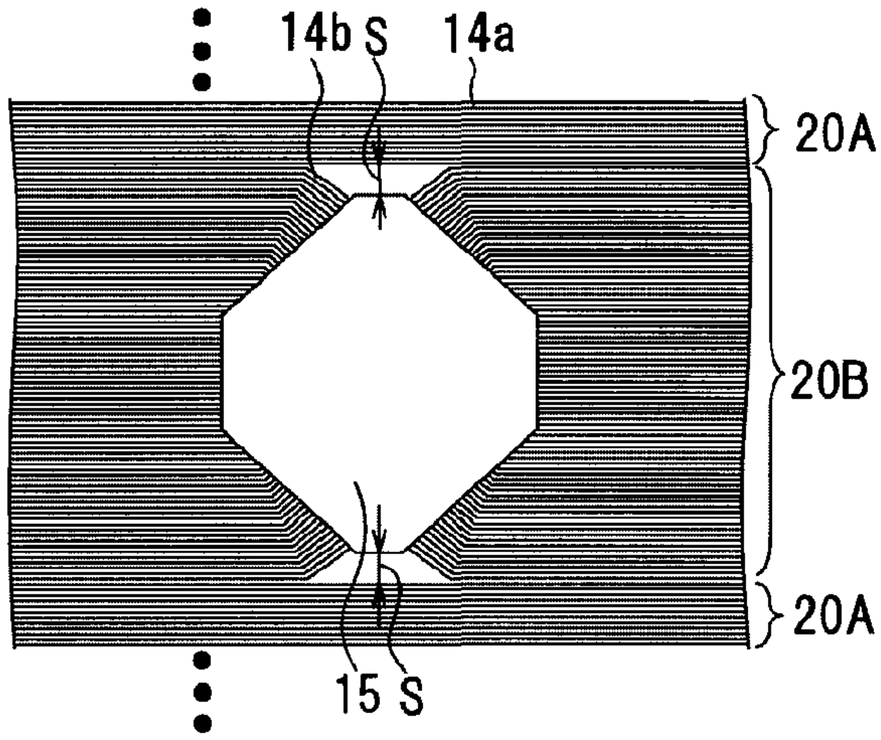


FIG.13B



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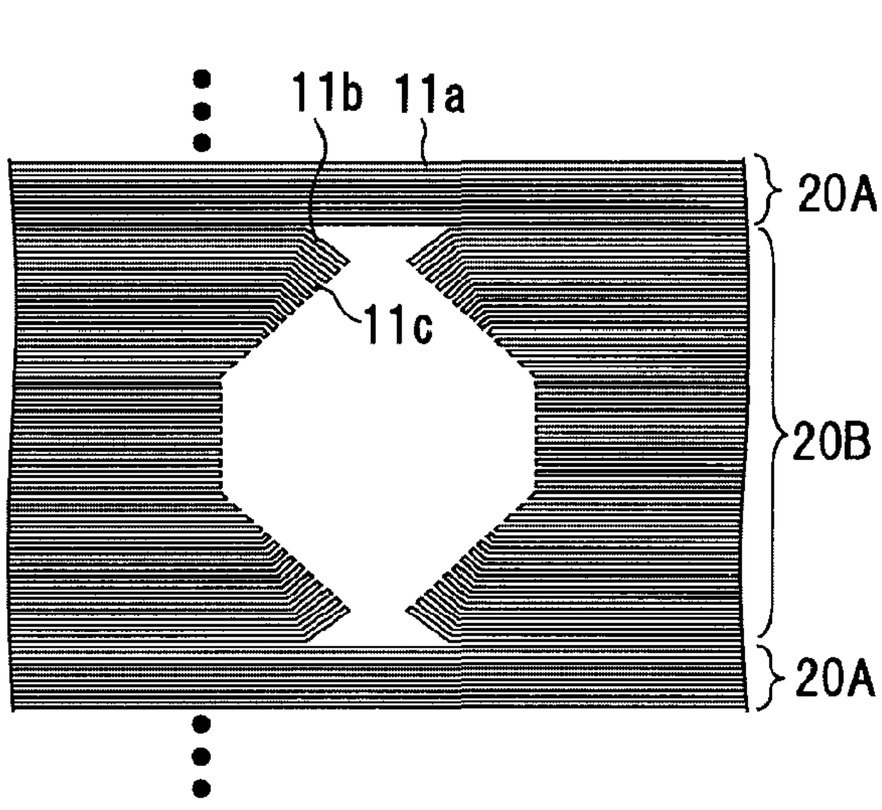


FIG.14A

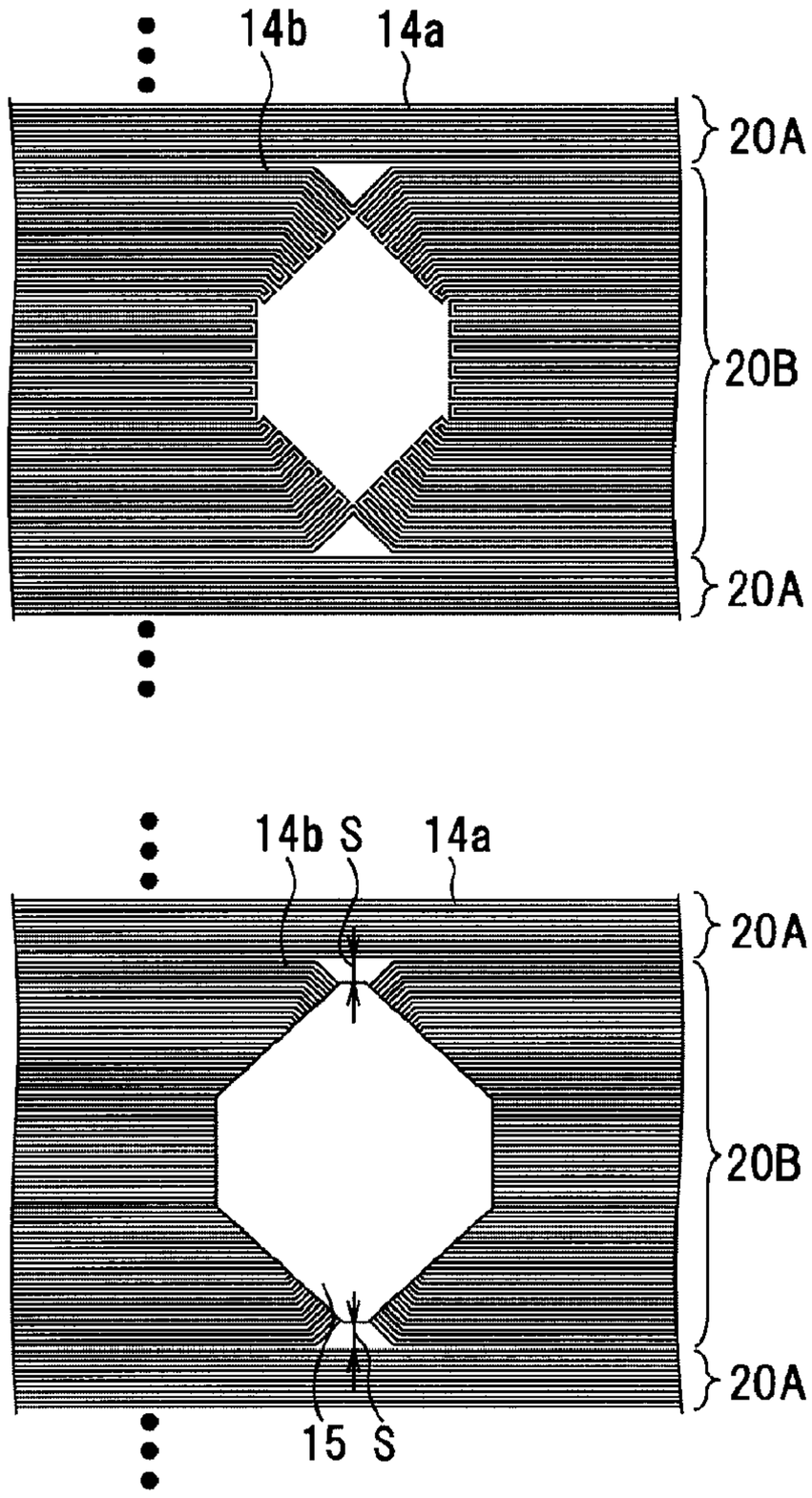


FIG.14B

FIG.14C

FIG.15A

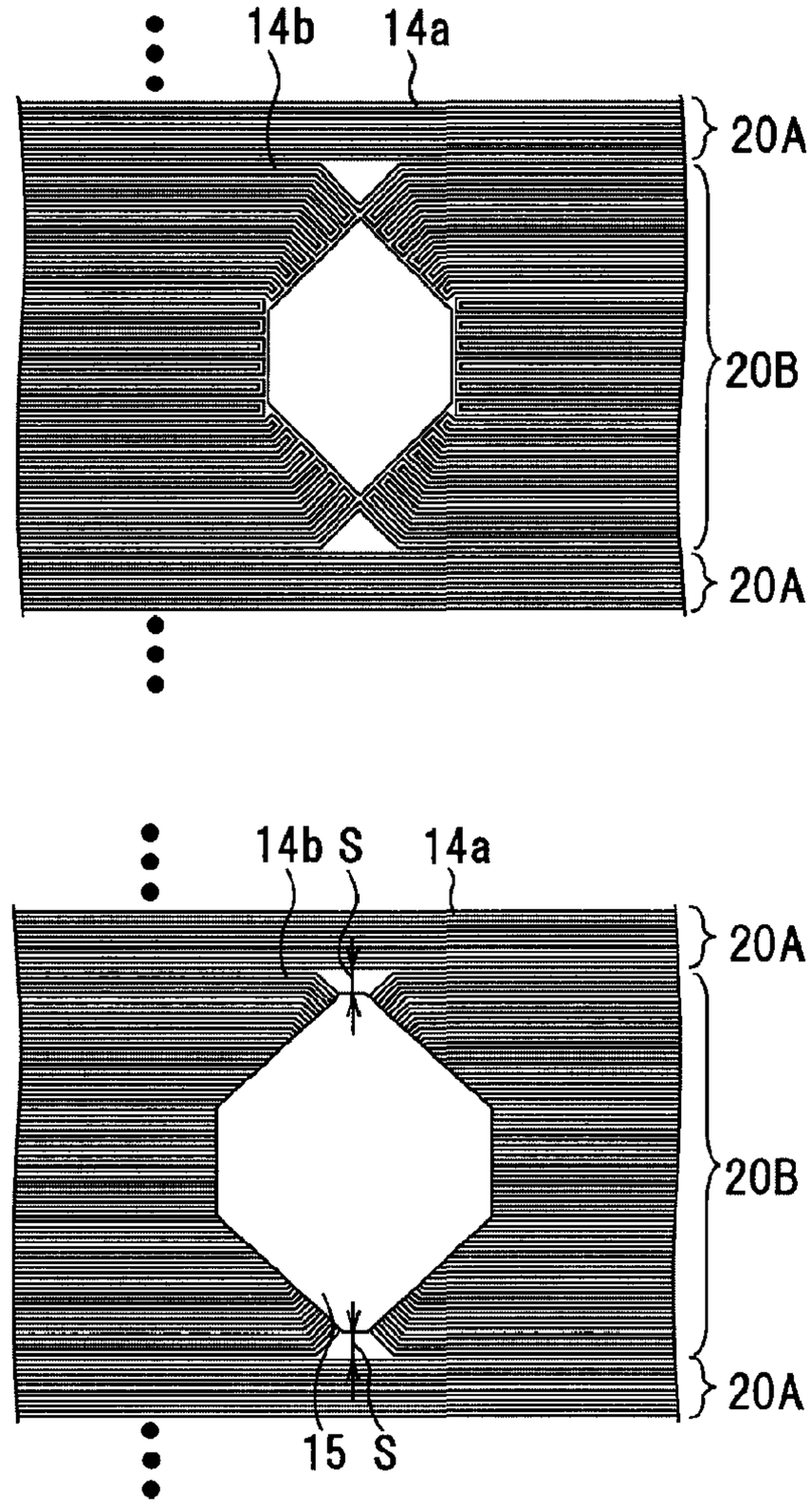


FIG.15B

FIG.15C

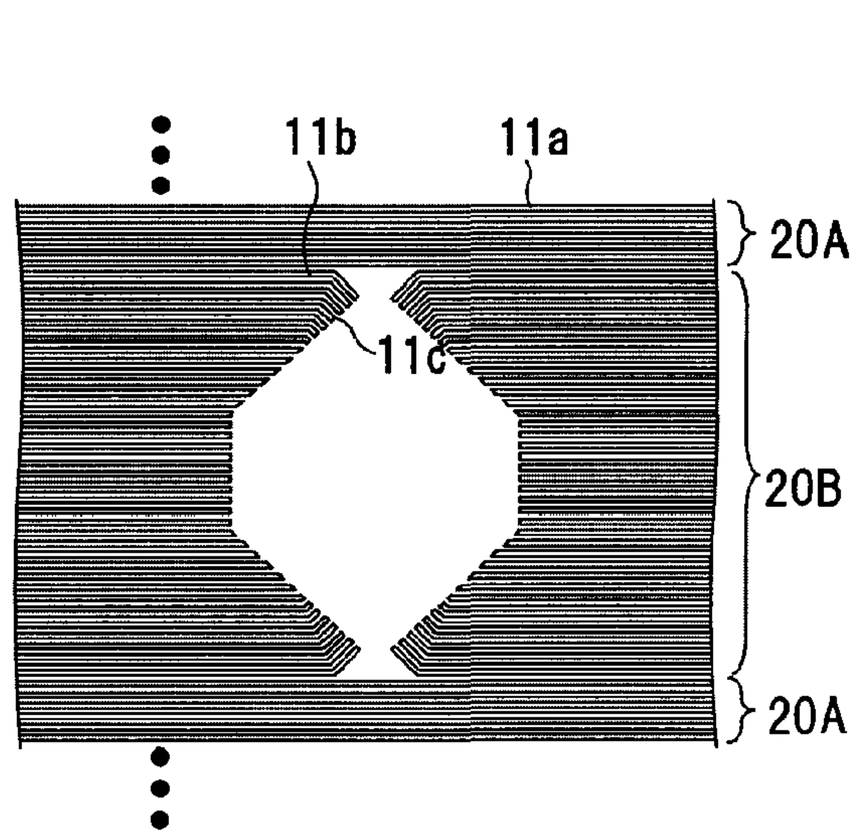
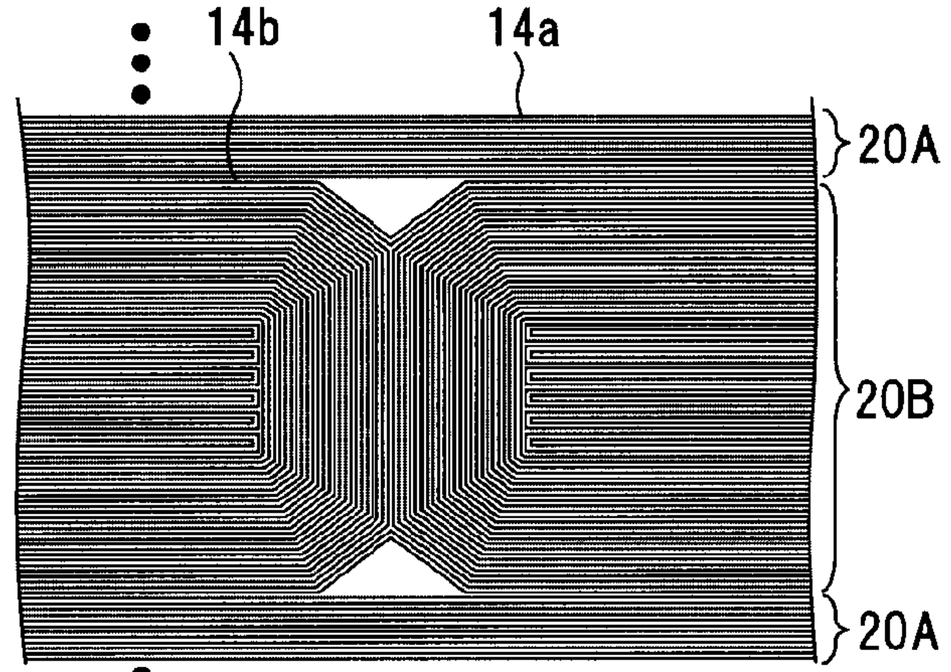


FIG.16A



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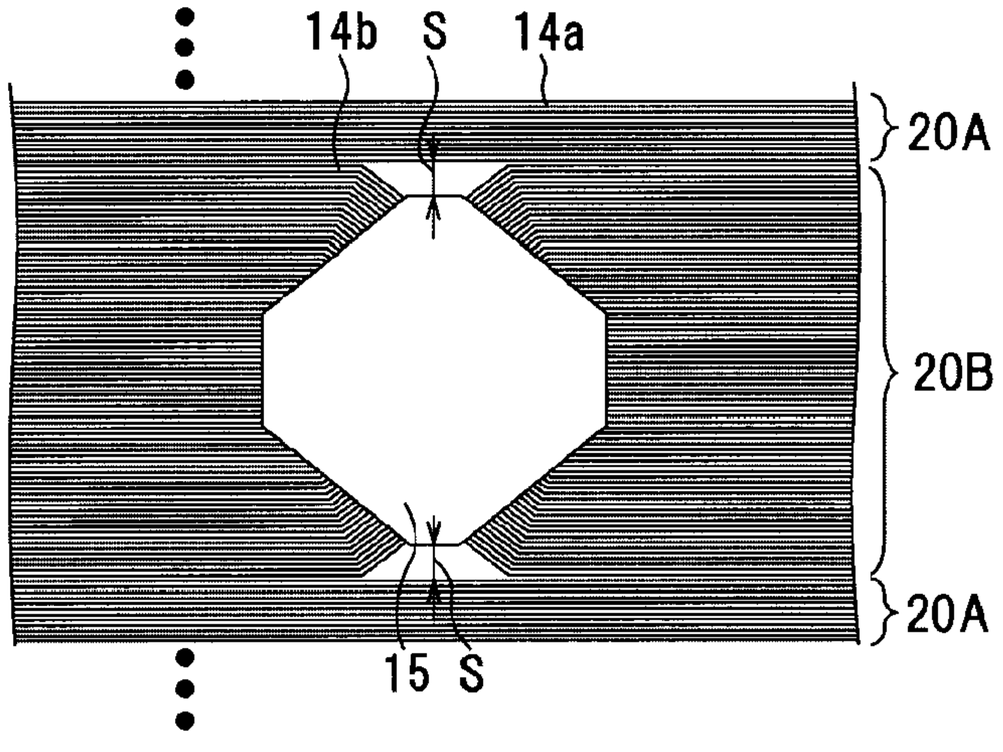


FIG.16C

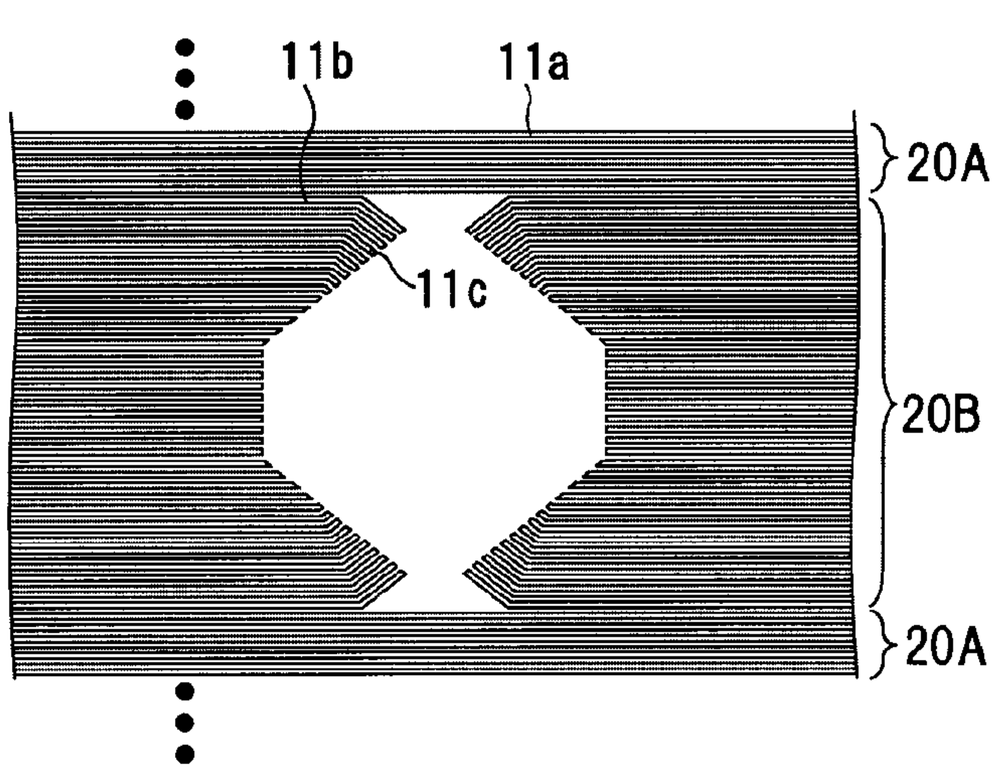


FIG.17A

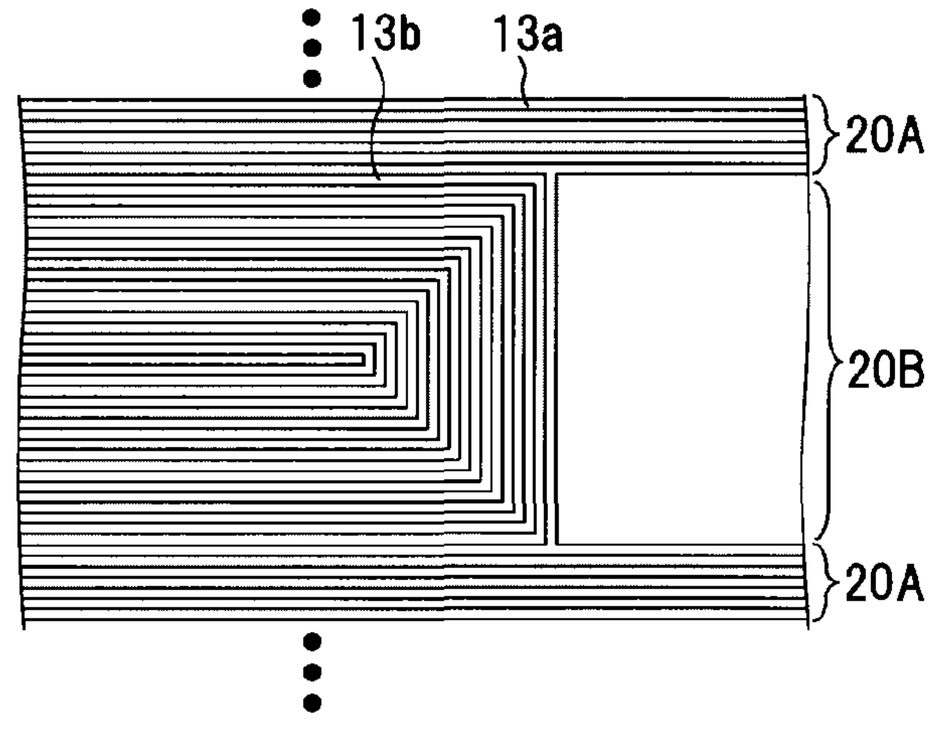


FIG.17B

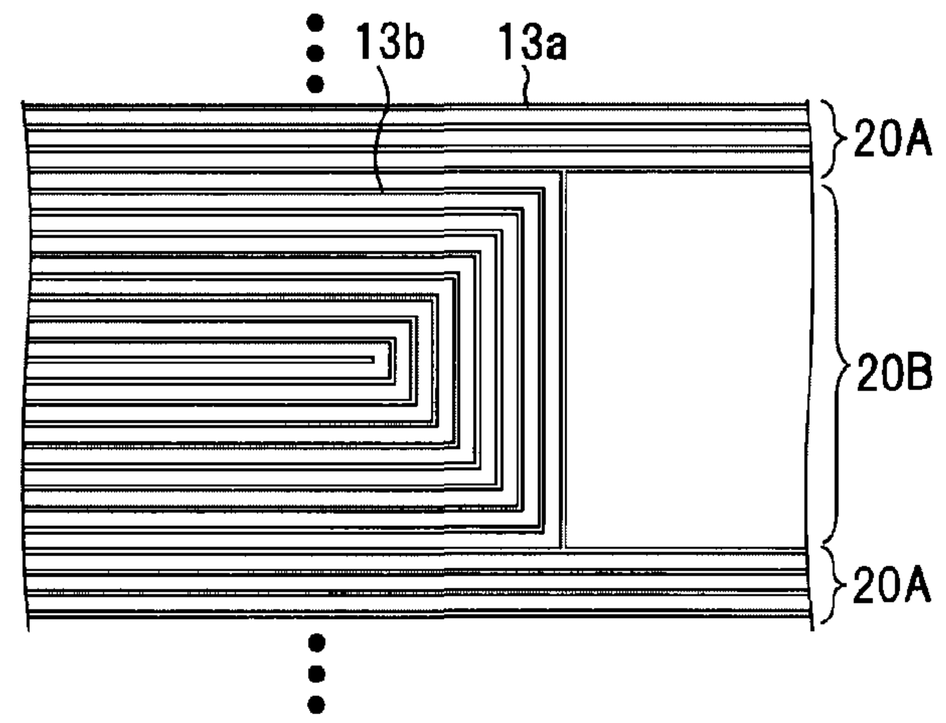


FIG.17C

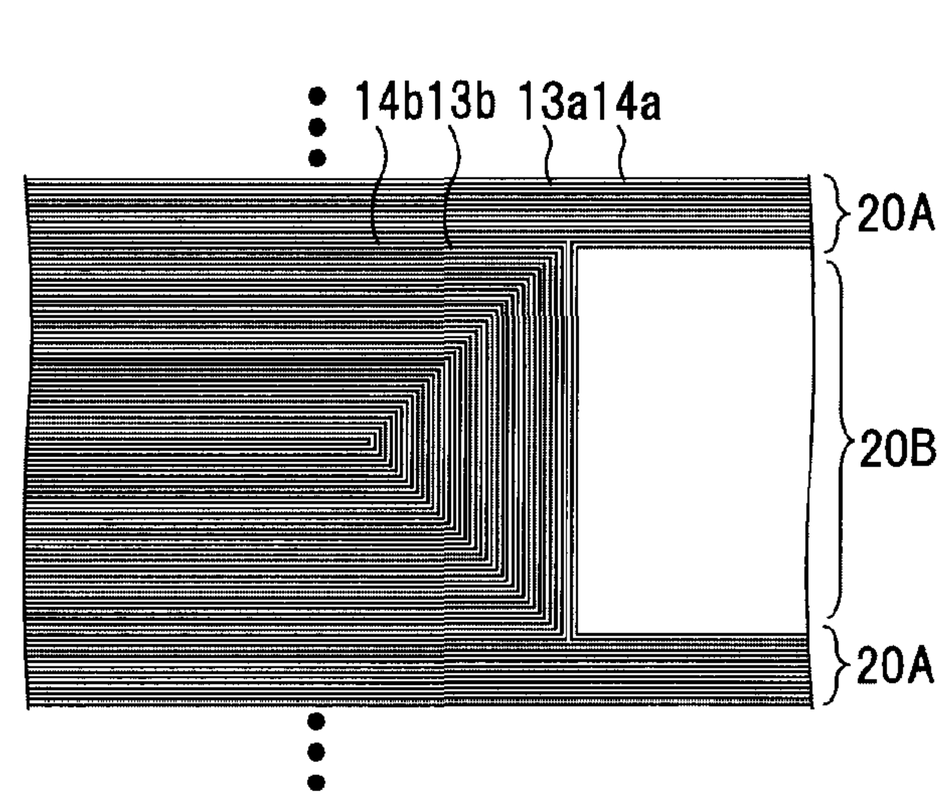


FIG.17D

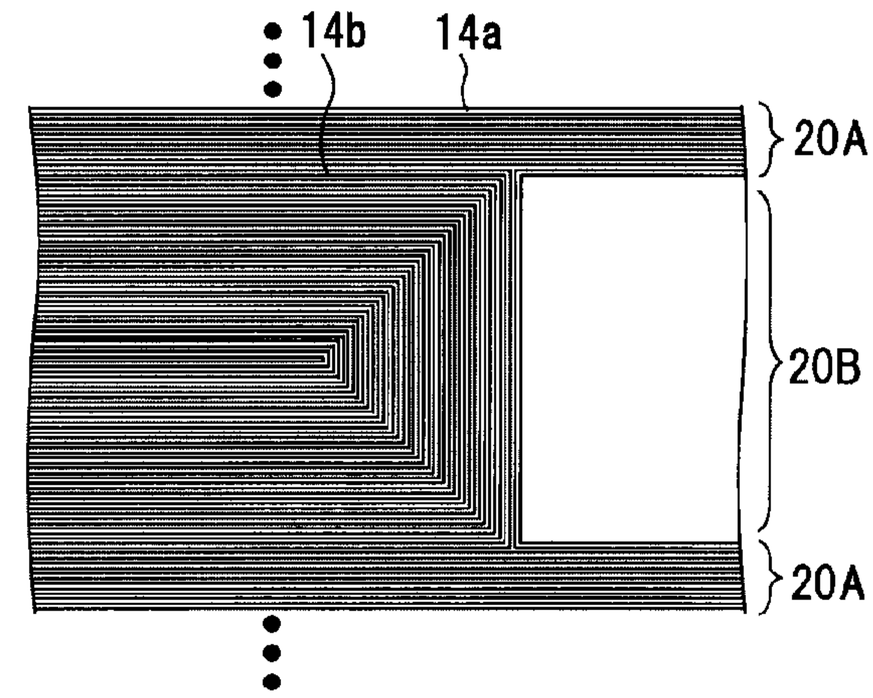


FIG.17E

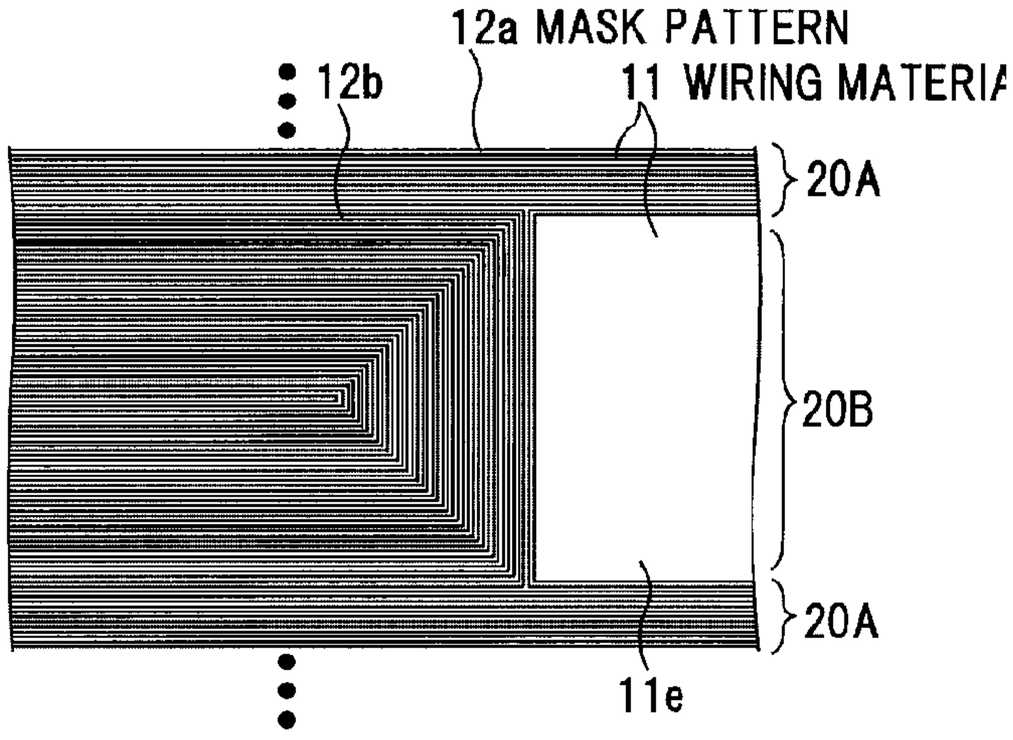


FIG.17F

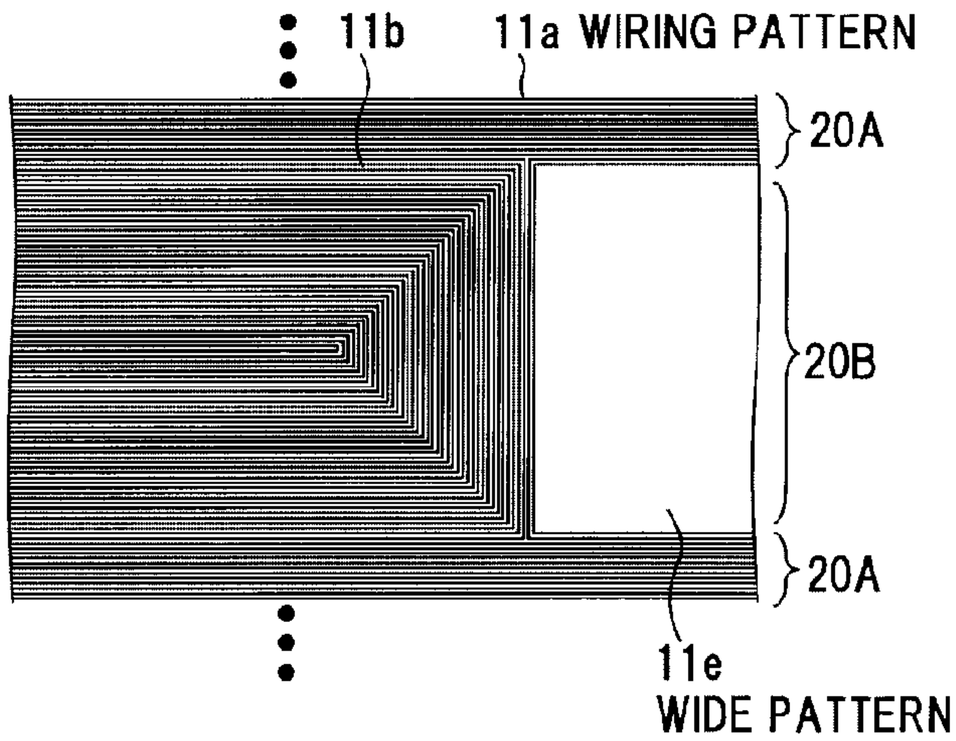


FIG.17G

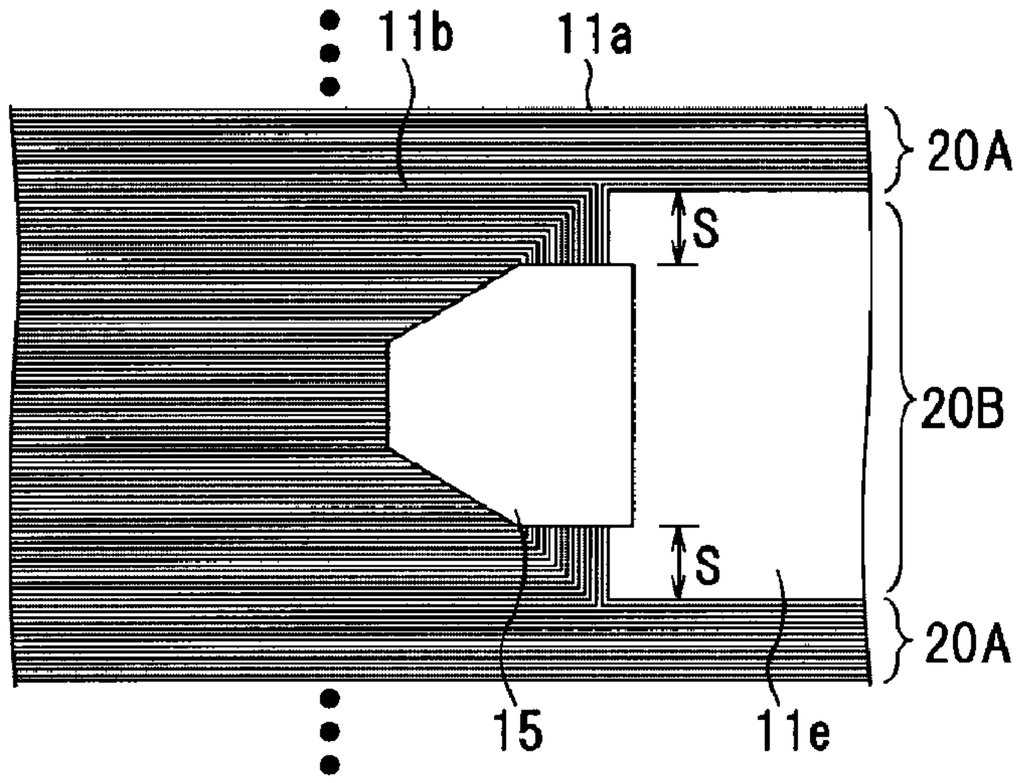


FIG.17H

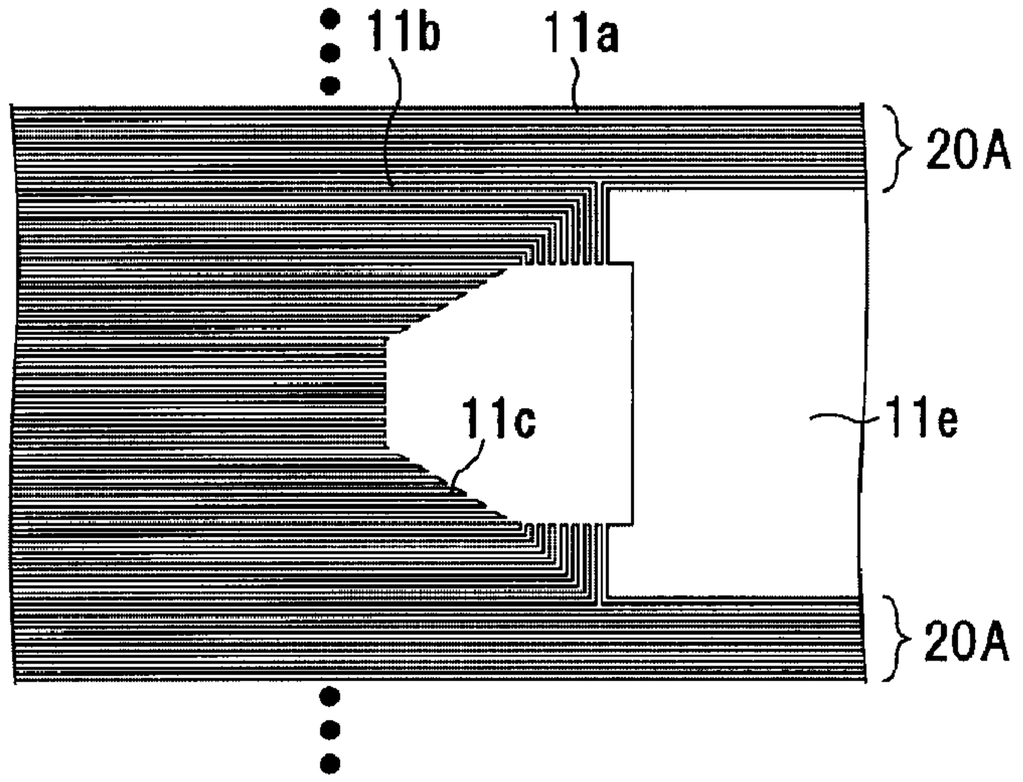


FIG.18A

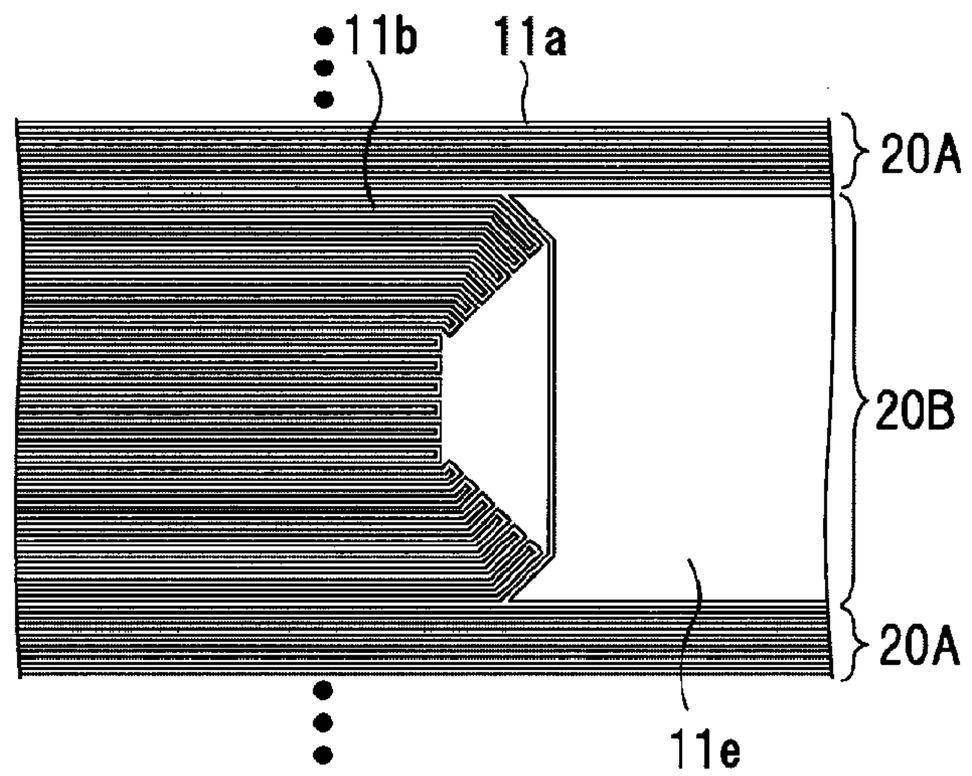


FIG.18B

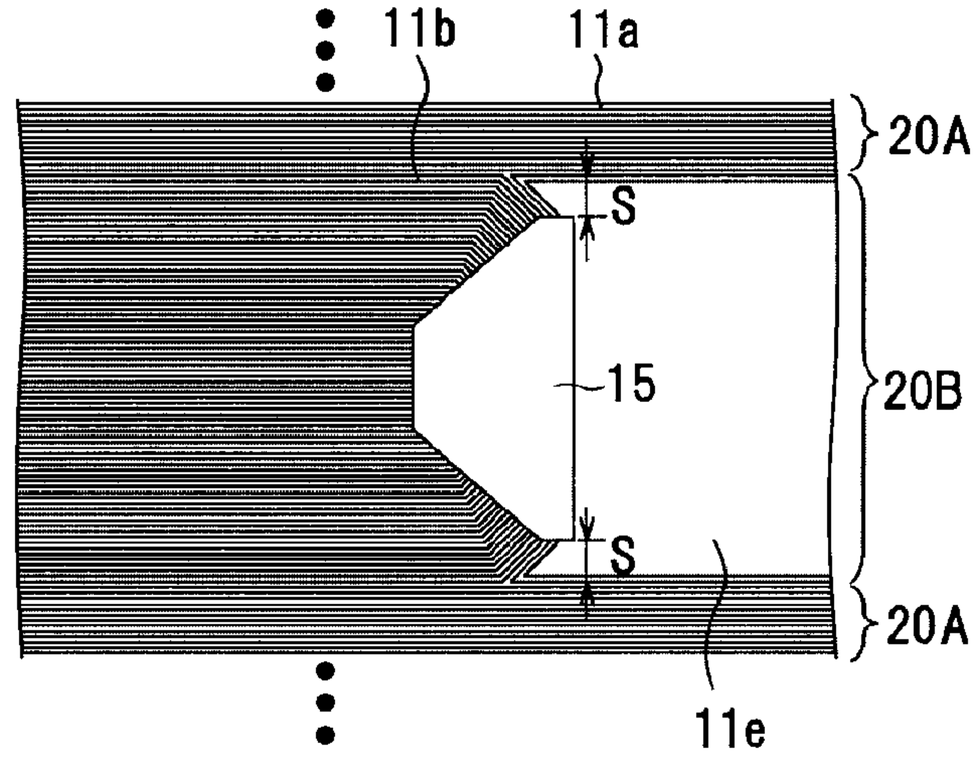


FIG.18C

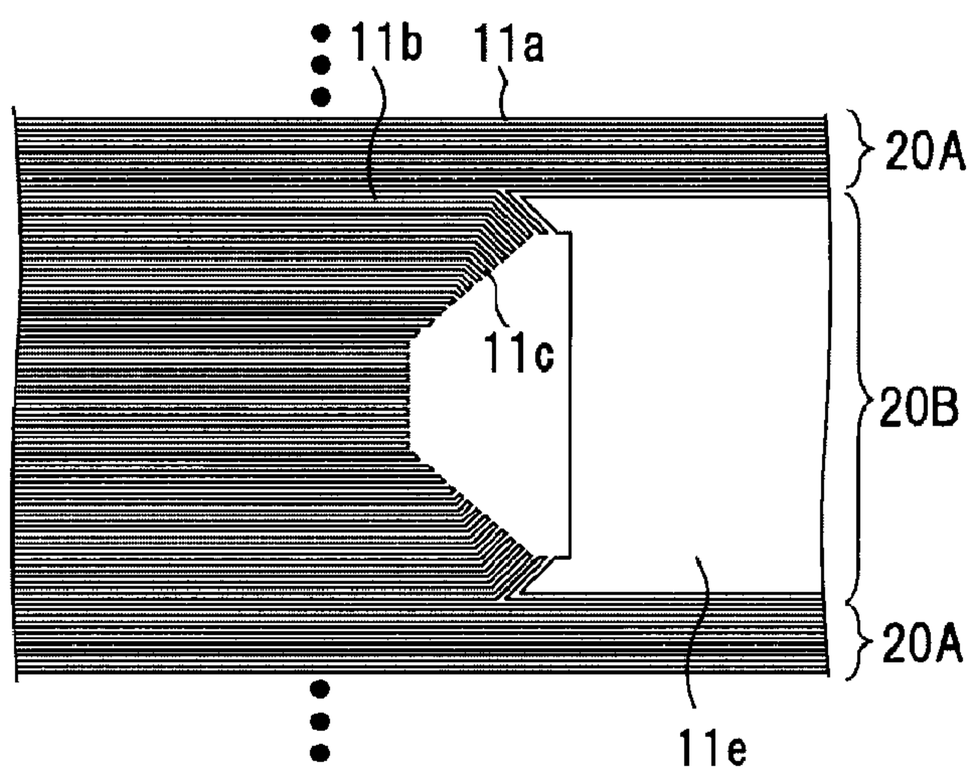


FIG.19A

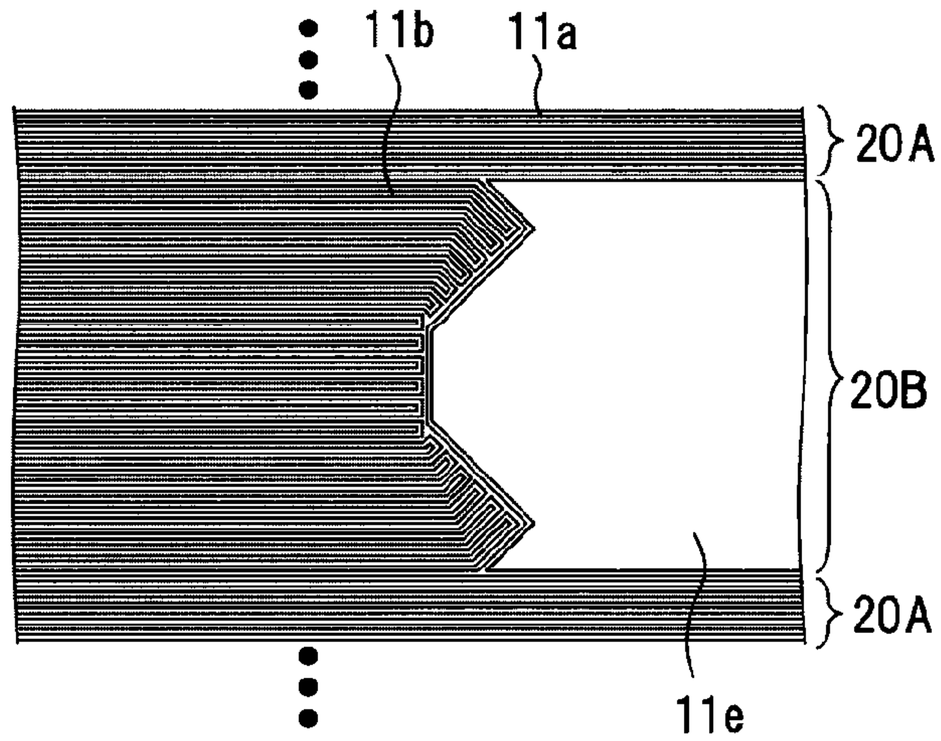


FIG.19B

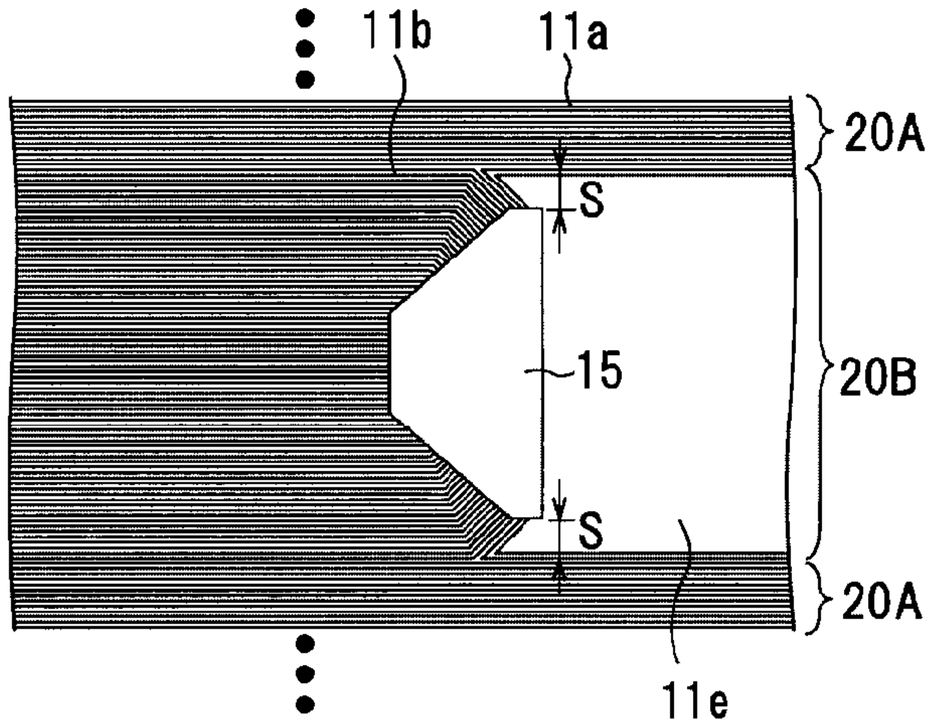


FIG.19C

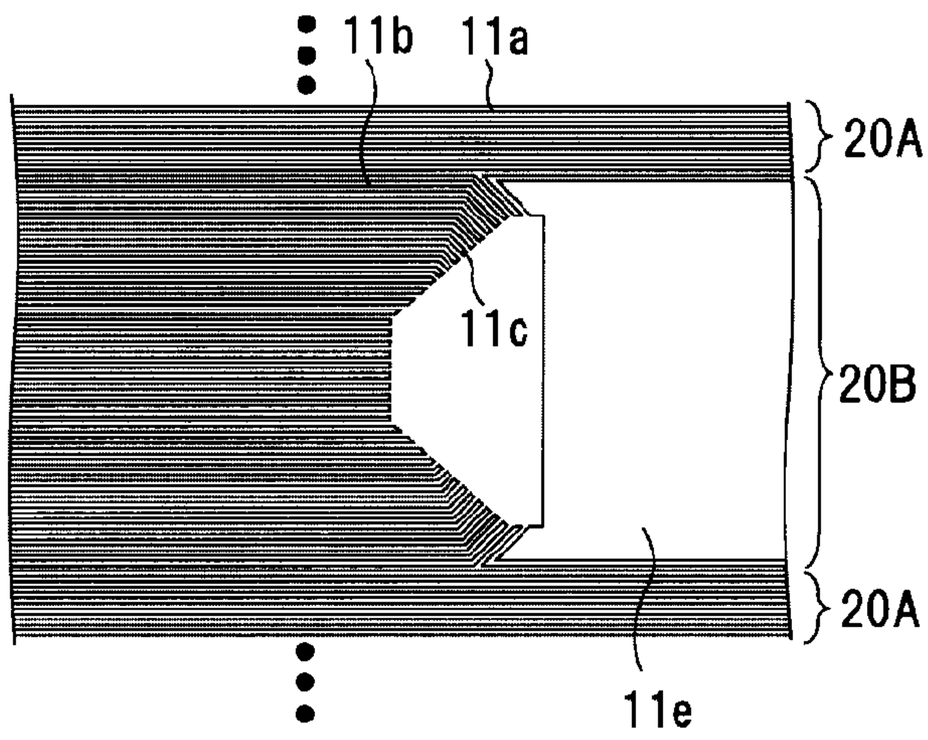


FIG.20A

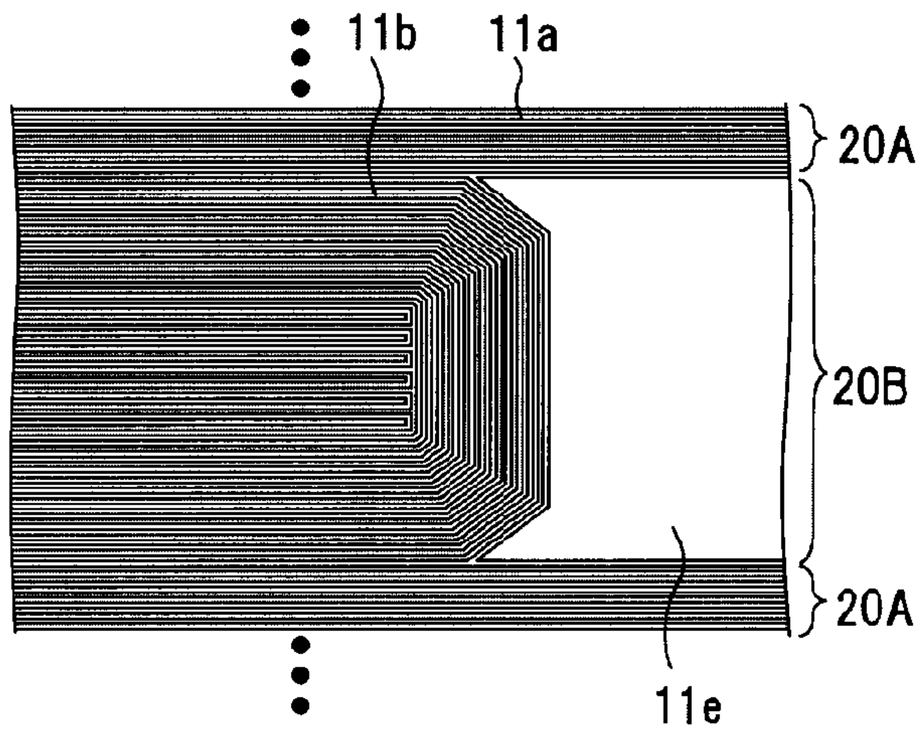


FIG.20B

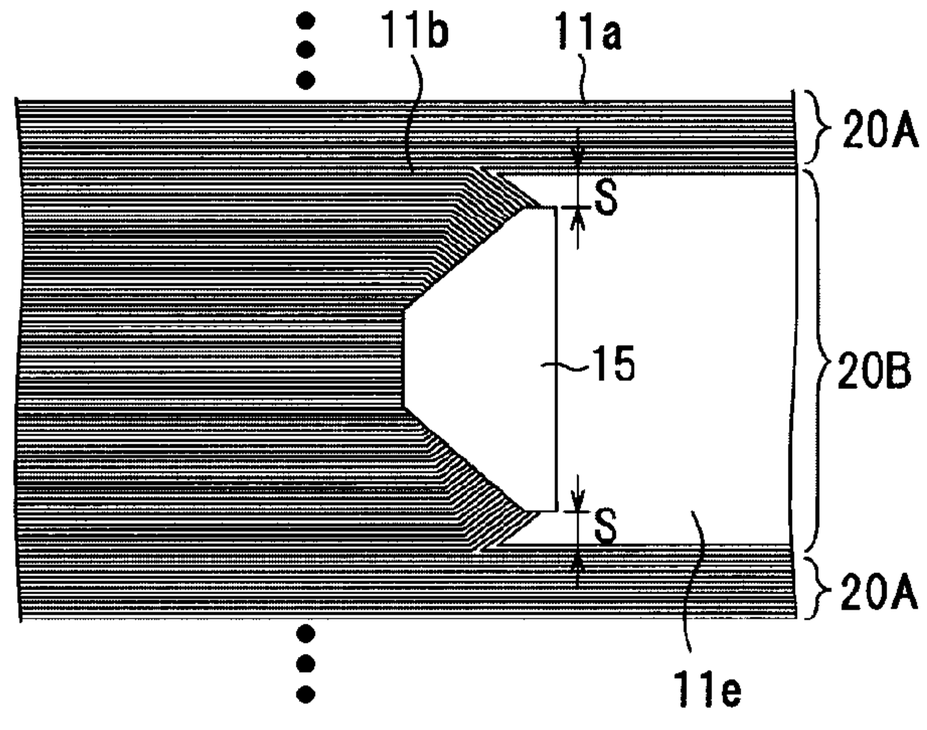


FIG.20C

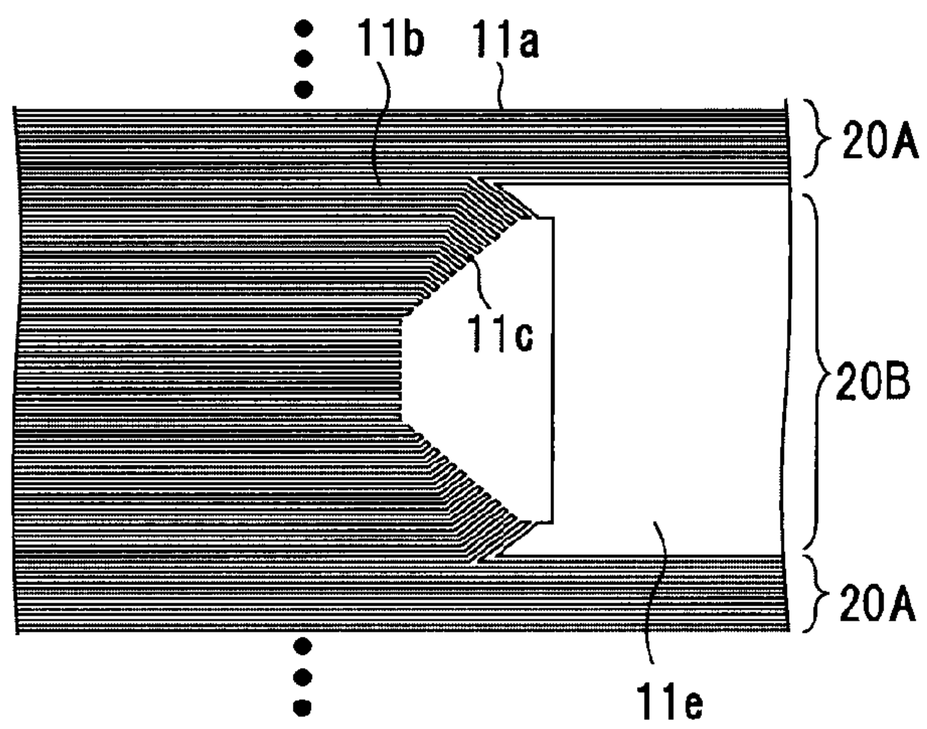


FIG.21A

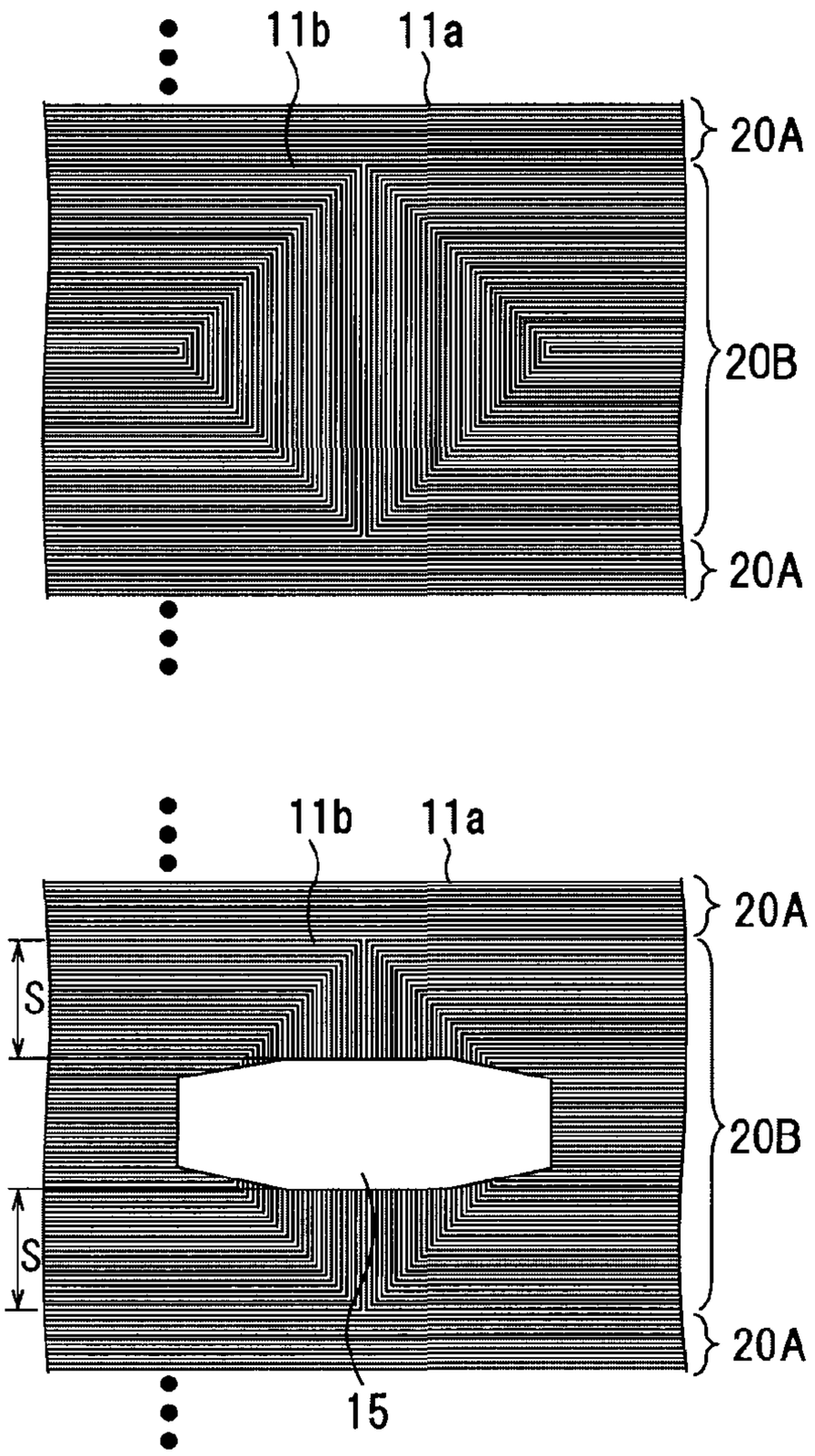


FIG.21B

FIG.21C

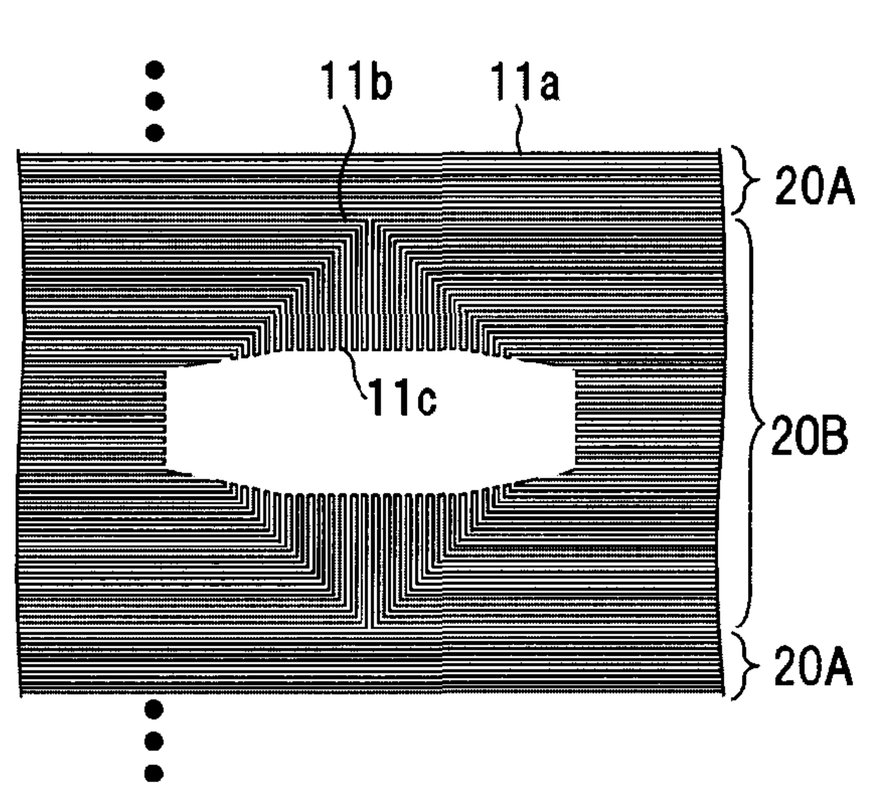


FIG.22A

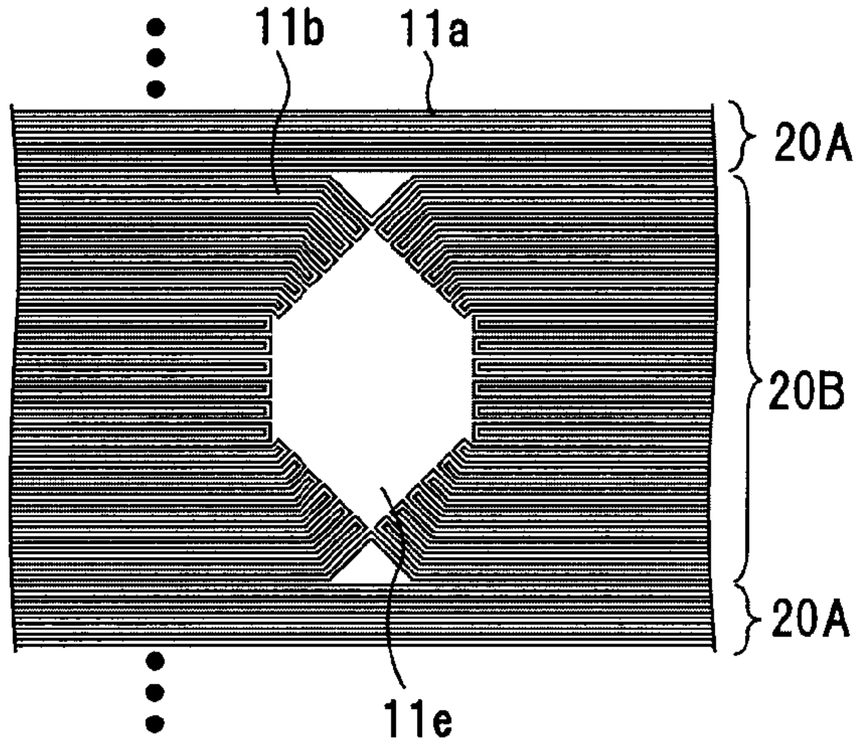


FIG.22B

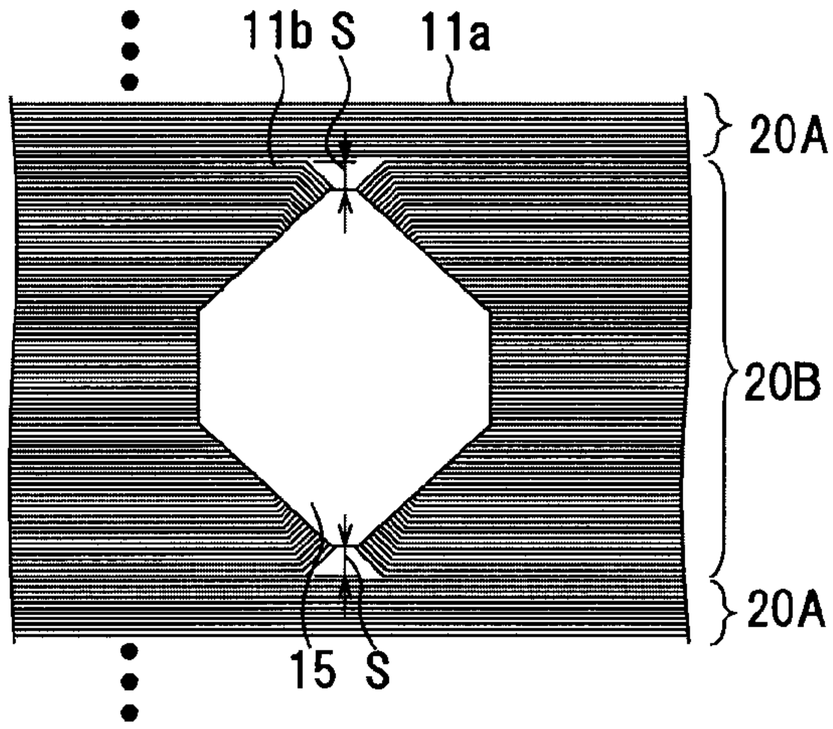


FIG.22C

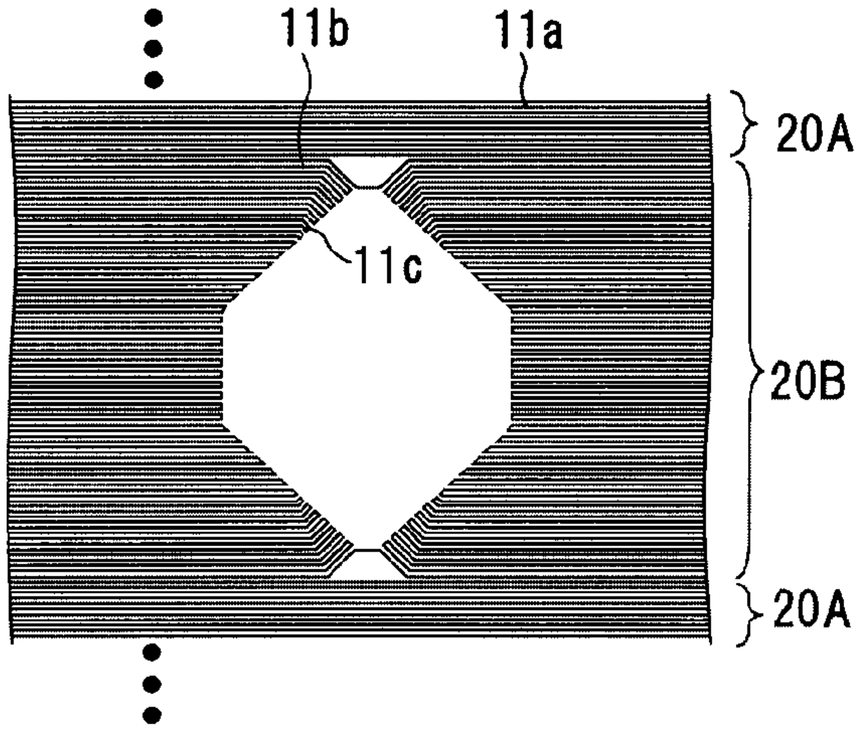


FIG.23A

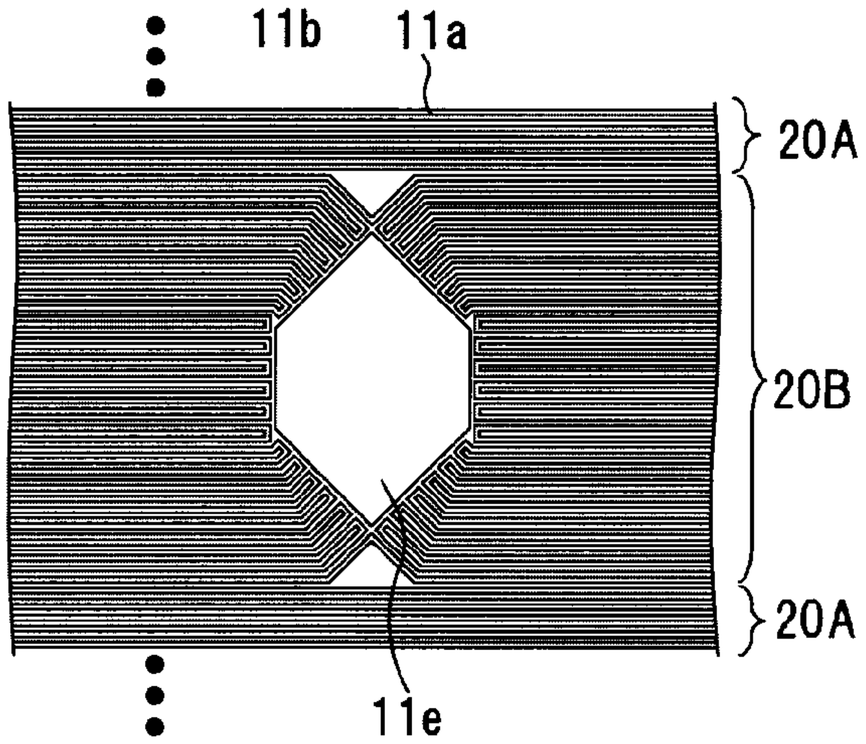


FIG.23B

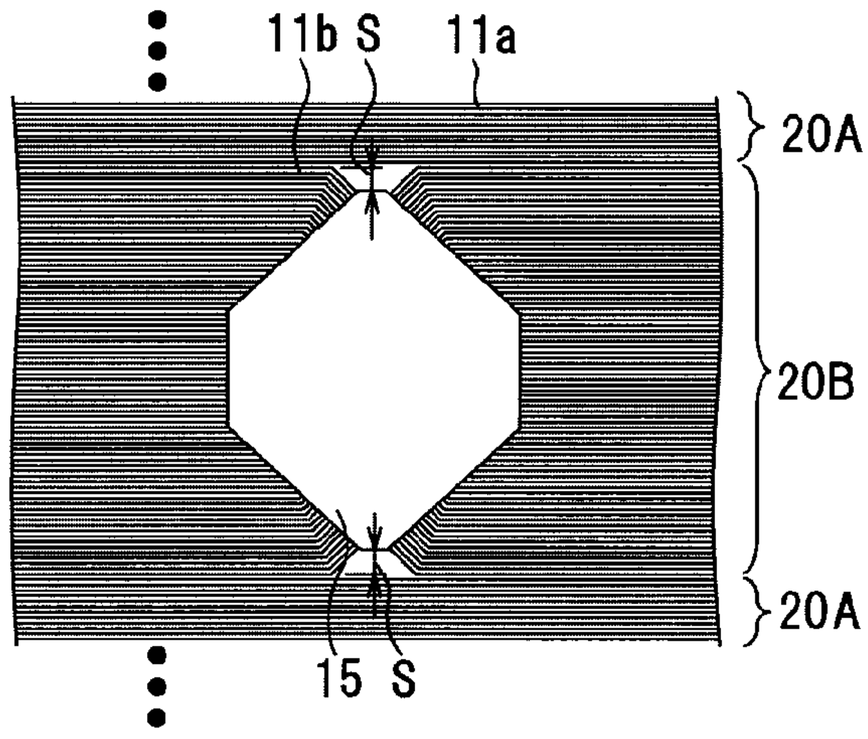


FIG.23C

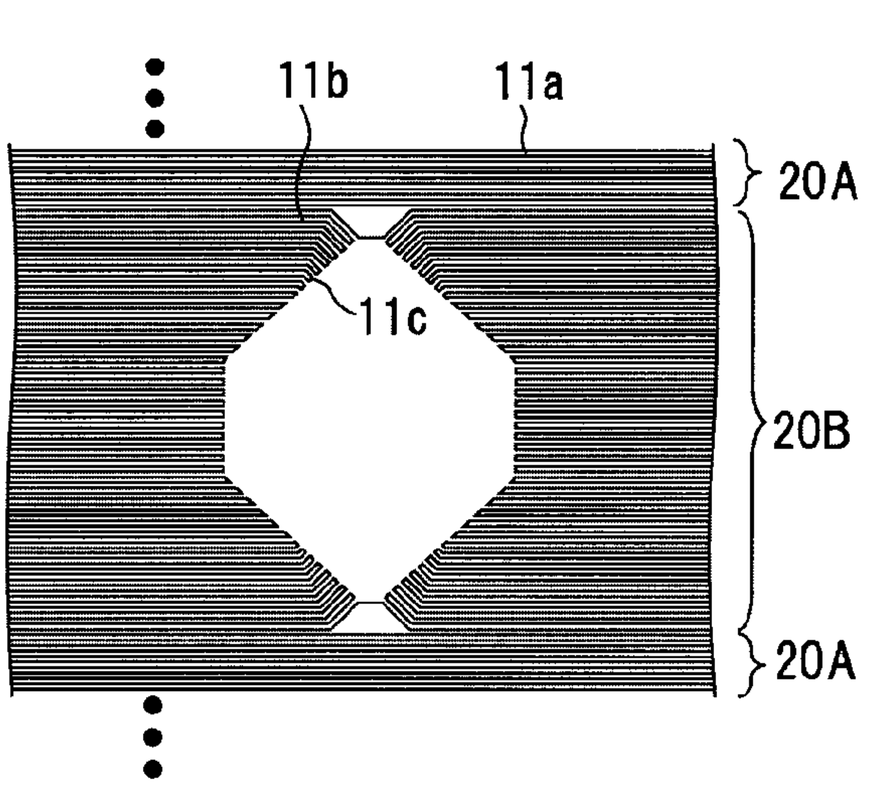


FIG.24A

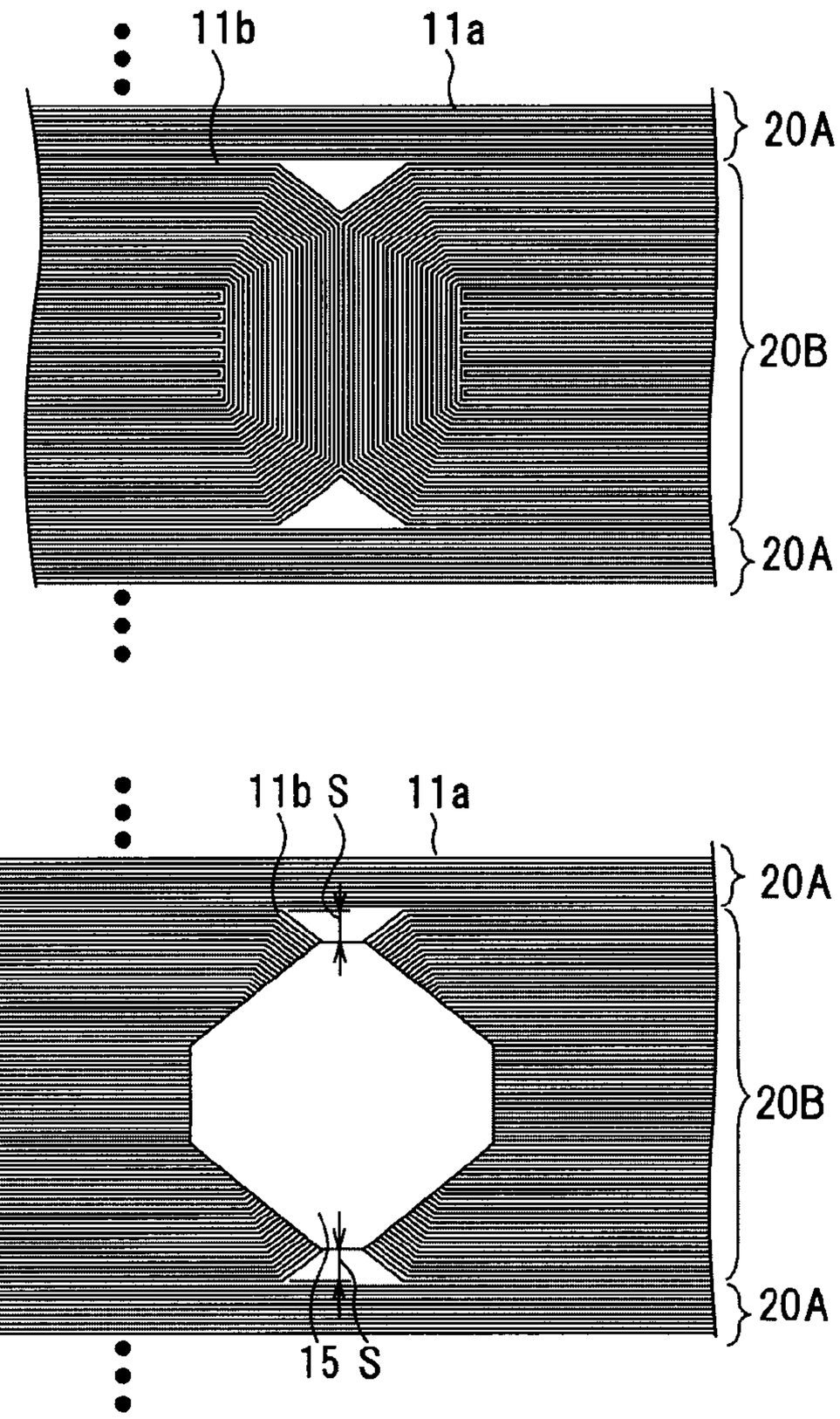


FIG.24B

FIG.24C

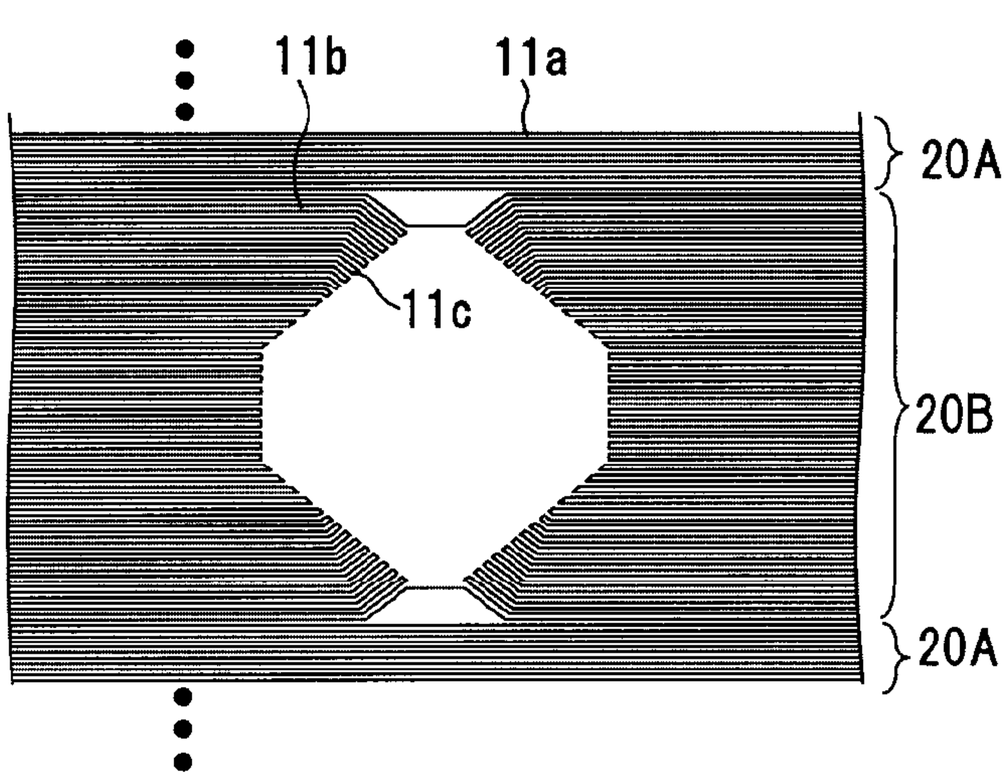


FIG.25A

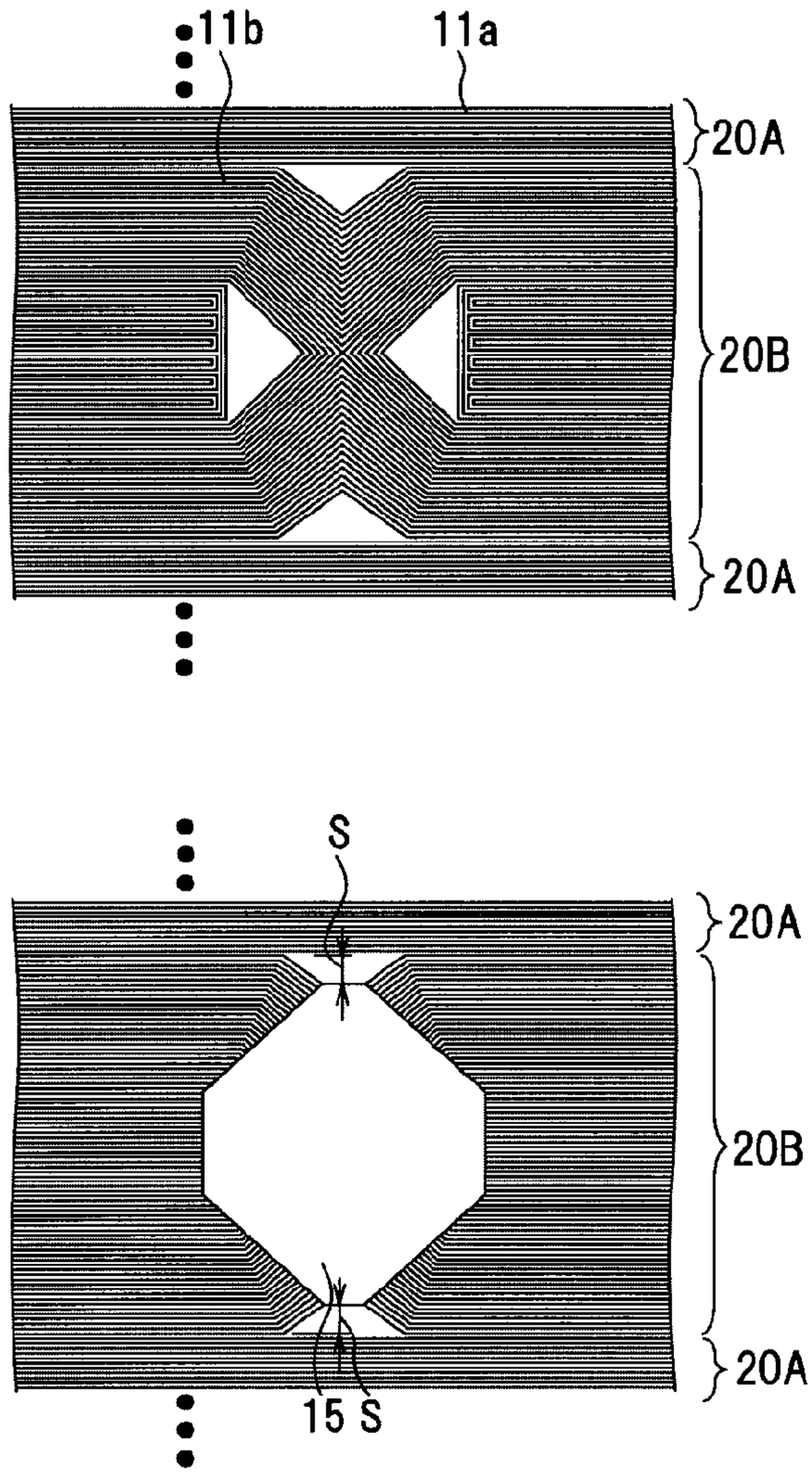
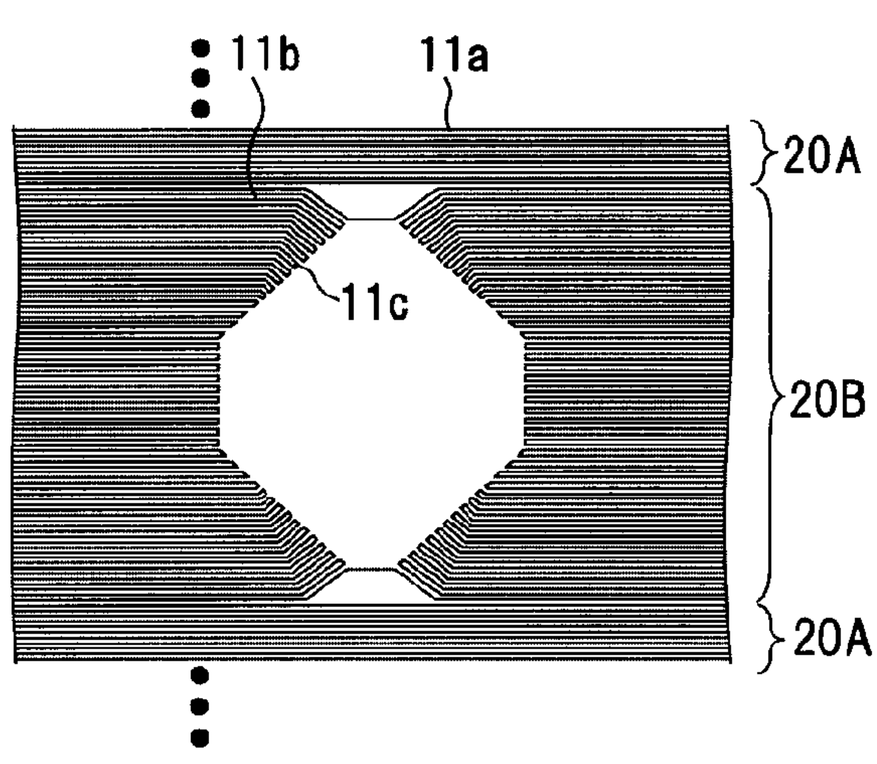


FIG.25B

FIG.25C



METHOD OF FABRICATING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue; a claim printed with strikethrough indicates that the claim was canceled, disclaimed, or held invalid by a prior post-patent action or proceeding.

CROSS-REFERENCE TO RELATED APPLICATIONS

This [application] *is a reissue of U.S. Pat. No. 8,183,148, issued on May 22, 2012 from U.S. patent application Ser. No. 12/542,540 filed Aug. 17, 2009, which* is based upon and claims the benefit of priority from prior Japanese Patent Application No. 2008-209849, filed on Aug. 18, 2008, the entire contents of *both of* which are incorporated herein by reference.

BACKGROUND

Recently, in accordance with miniaturization of a semiconductor element, a method capable of forming a pattern having a dimension beyond a resolution limit in lithography method is required.

As one sample of the method, a method is known, that includes steps of forming sidewall patterns on side surfaces of core materials, eliminating the core materials, and etching a workpiece film by using the sidewall patterns as a mask, for example, disclosed in JP-A-1996-55908.

Since the sidewall patterns and wiring patterns formed by using the sidewall patterns as a mask have closed loop shapes, a step of a closed loop cut for cutting a part of the closed loop shape is needed. In case that the other patterns exist close to the sites where the closed loop cut is carried out, generally, spaces are created between the other patterns in terms of a margin of displacement at the alignment in the lithography method.

BRIEF SUMMARY

A method of fabricating a semiconductor device according to an embodiment includes forming a first pattern having linear parts of a constant line width and a second pattern on a foundation layer, the second pattern including parts close to the linear parts of the first pattern and parts away from the linear parts of the first pattern and constituting closed loop shapes independently of the first pattern or in a state of being connected to the first pattern and carrying out a closed loop cut at the parts of the second pattern away from the linear parts of the first pattern.

A method of fabricating a semiconductor device according to another embodiment includes forming a first pattern having linear parts of a constant line width and a second pattern having parts parallel to the first pattern which have a first distance between the linear parts of the first pattern, and constituting closed loop shapes independently of the first pattern or in a state of being connected to the first pattern and forming a resist in the parts of the second pattern so as to have a second distance between the linear parts of the first pattern larger than the first distance, and carrying out a closed loop cut at the parts of the second pattern in which the resist is formed.

A method of fabricating a semiconductor device according to another embodiment includes forming a first pattern group including a plurality of first patterns arranged at a predetermined pitch, and second pattern group including a plurality of second patterns arranged at the predetermined pitch, the closest second patterns to at least the first pattern group of the plural second patterns having parallel parts parallel to the first pattern group and parts away from the second pattern group and constituting closed loop shapes independently of the first pattern group or in a state of being connected to the first pattern group and carrying out a closed loop cut at the parts of the second pattern away from the first pattern group.

A semiconductor device according to another embodiment includes a first pattern group including a plurality of first patterns arranged at a predetermined pitch and a second pattern group including a plurality of second patterns arranged at the predetermined pitch, wherein the closest second patterns to at least the first pattern group of the plural second patterns have parallel parts parallel to the first pattern group and non-parallel parts formed so as to be connected to the parallel parts, to be away from the first pattern group and to be not parallel to the first pattern group.

BRIEF DESCRIPTION OF THE DRAWING

FIGS. **1**A to **1**H are cross-sectional views schematically showing each feature in a fabrication process of a semiconductor device according to a first embodiment;

FIGS. **2**A to **2**C are plan views schematically showing processes of a closed loop cut carried out between the process shown in FIG. **1**D and the process shown in FIG. **1**E;

FIGS. **3**A to **3**H are cross-sectional views schematically showing each feature in a fabrication process of a semiconductor device according to a second embodiment;

FIGS. **4**A to **4**C are plan views schematically showing processes of a closed loop cut carried out after the process shown in FIG. **3**H;

FIG. **5**A is a plan view schematically showing an example of side wall patterns used in a third embodiment;

FIG. **5**B is a detail view of an "A" part of the side wall patterns shown in FIG. **5**A;

FIG. **6**A is a plan view schematically showing a structure of a wiring pattern in a wiring layer of a phase-change memory used in a fourth embodiment;

FIG. **6**B is a detail view of a "B" part of the side wall patterns shown in FIG. **6**A;

FIGS. **7**A to **7**F are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to a fourth embodiment;

FIGS. **8**A to **8**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to a fifth embodiment;

FIGS. **9**A to **9**C are main part plan views schematically showing each main part of upper wiring layers used in an example of a fabrication process according to a sixth embodiment;

FIGS. **10**A to **10**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to a seventh embodiment;

FIGS. **11**A to **11**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to an eighth embodiment;

FIGS. **12**A to **12**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to a ninth embodiment;

FIGS. **13**A to **13**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to a tenth embodiment;

FIGS. **14**A to **14**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to an eleventh embodiment;

FIGS. **15**A to **15**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to a twelfth embodiment;

FIGS. **16**A to **16**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to a thirteenth embodiment;

FIGS. **17**A to **17**H are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to a fourteenth embodiment;

FIGS. **18**A to **18**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to a fifteenth embodiment;

FIGS. **19**A to **19**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to a sixteenth embodiment;

FIGS. **20**A to **20**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to a seventeenth embodiment;

FIGS. **21**A to **21**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to an eighteenth embodiment;

FIGS. **22**A to **22**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to a nineteenth embodiment;

FIGS. **23**A to **24**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to a twentieth embodiment;

FIGS. **24**A to **24**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to a twenty-first embodiment; and

FIGS. **25**A to **25**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to a twenty-second embodiment.

DETAILED DESCRIPTION

A method of fabricating a semiconductor device according to the embodiment includes forming a first pattern having linear parts of a constant line width and a second pattern on a foundation layer, the second pattern including parts close to the linear parts of the first pattern and parts away from the linear parts of the first pattern and constituting closed loop shapes independently of the first pattern or in a state of being connected to the first pattern and carrying out a closed loop cut at the parts of the second pattern away from the linear parts of the first pattern.

As the foundation layer, a substrate such as a silicon substrate or a workpiece film to be processed by using the first and second patterns as a mask can be used. Further, the workpiece film can be formed between the foundation layer and the first and second patterns.

As the first and second patterns, a bit-line and a word line constituting a memory device, a wiring by a line and space, or a pattern used as a mask can be used.

As the first pattern, for example, a pattern having a closed loop shape or a line pattern can be used. Further, the first pattern can include a part having a line width wider than that of the linear part of the constant line width.

The part of the second pattern close to the linear part of the first pattern is, for example, a parallel part close to and parallel to the linear part of the first pattern. The parallel part of the second pattern can have a linear shape or a carved shape, if it is parallel to the linear part of the first pattern.

(First Embodiment)

FIGS. **1**A to **1**H are cross-sectional views schematically showing each feature in a fabrication process of a semiconductor device according to the first embodiment. FIGS. **2**A to **2**C are plan views schematically showing processes of a closed loop cut carried out between the process shown in FIG. **1**D and the process shown in FIG. **1**E.

As shown in FIG. **1**A, a wiring material (a workpiece film) **11** for forming a wiring layer via a foundation layer **10** is formed on a semiconductor substrate such as a silicon substrate, a mask material **12** is formed on the wiring material **11** and core patterns **13**a, **13**b are formed on the mask material **12** by a lithography method and an etching process which use a resist. The core patterns **13**a, **13**b have, for example, a line width (for example, 40 nm) near the resolution limit "W" of lithography method.

As the wiring material **11**, for example, Cu, W, Al or the like can be used. As the mask material **12**, for example, silicon oxide film or the like can be used. As the core patterns **13**a, **13**b, for example, amorphous silicon film or the like can be used.

Next, as shown in FIG. **1**B, a slimming treatment is carried out so as to make the width of the core patterns **13**a, **13**b thin up to a half size by an anisotropic etching or the like. By this, the core patterns **13**a, **13**b having a line width (for example, 20 nm) of almost a half size of the resolution limit "W" can be obtained.

Next, as shown in FIG. **1**C, a film to become a material of side wall patterns is deposited on the whole surfaces including the side surfaces of the core patterns **13**a, **13**b after the slimming treatment, parts of the film which are deposited on the upper surfaces of the core patterns **13**a, **13**b and the surface of the mask material **12** are eliminated by using the anisotropic etching or the like so as to form side wall patterns **14**a, **14**b on the side surfaces of the core patterns **13**a, **13**b. The side wall patterns **14**a, **14**b has, for example, a line width and an distance of almost a half size of the resolution limit "W".

The side wall patterns **14**a, **14**b are formed of a material having a high etching selectivity to the core patterns **13**a, **13**b, for example, if the core patterns **13**a, **13**b are formed of the amorphous silicon film, silicon nitride film or the like can be used as the material.

Next, as shown in FIG. **1**D, the core patterns **13**a, **13**b are eliminated by a dry etching such as a chemical dry etching (CDE), a reactive ion etching (RIE) or the like so as to leave the side wall patterns **14**a, **14**b having a high etching selectivity to the core patterns **13**a, **13**b. At this time, each of the both end portions of the side wall patterns **14**a, **14**b forms a closed loop shape.

In FIG. **2**A, the side wall patterns **14**b show an object pattern (the second pattern) which is an object of the closed loop cut, and the side wall patterns **14**a show an adjacency pattern (the first pattern) adjacent to the side wall patterns **14**b. In case of the embodiment, the side wall patterns **14**a, **14**b include linear parts of a constant line width. Further, the adjacency pattern can be an object of the closed loop cut. In order to carry out the closed loop cut of the side wall patterns **14**b, in terms of a margin of displacement at the alignment in the lithography method, it is needed for a region of the side wall patterns **14**b where the closed loop cut is carried out to be away from the side wall patterns **14**a so that the resist **15** does

not fall over the side wall patterns **14**a. Therefore, the side wall patterns **14**b are formed so as to have the following shape.

Namely, the side wall patterns **14**b are close to the side wall patterns **14**a so as to have a distance "d" (a first distance) between the side wall patterns **14**a, and has parallel parts **140** parallel to the side wall patterns **14**a and nonparallel parts **141** formed so as to be connected to the parallel parts **140** and to be not parallel to the side wall patterns **14**a, and cut regions **141**a where the closed loop cut is carried out is formed in the nonparallel parts **141**. The nonparallel parts **141** are formed in a shape bent in an oblique direction from the joining point of the parallel part **140** and the nonparallel part **141** so as to be apart from the side wall patterns **14**a, but it can have a shape bent in a rectangular direction.

As shown in FIG. **2**B, a space "S" (a second distance) is formed on the cut region **141**a located at the end portions of the side wall patterns **14**b, between the side wall patterns **14**a and a resist **15** is formed, and as shown in FIG. **2**C, the cut region **141**a of the side wall patterns **14**b is cut by the lithography method. The space "S" is formed so as to be larger than the distance "d" (the first distance) between the side wall patterns **14**a and the side wall patterns **14**b.

Next, as shown in FIG. **1**E, the mask material **12** is eliminated by using the side wall patterns **14**a, **14**b as a mask and by a dry etching or the like where a gas such as CF_4, CHF_3 is used so as to form mask patterns **12**a, **12**b, and as shown in FIG. **1**F, the side wall patterns **14**a, **14**b are eliminated by a wet etching or the like.

Next, as shown in FIG. **1**G, the wiring material **11** is etched by using the mask patterns **12**a, **12**b so as to form wiring patterns **11**a, **11**b, and as shown in FIG. **1**H, the mask patterns **12**a, **12**b are eliminated by the wet etching or the like.

According to the first embodiment, even if the side wall patterns have an arrangement pitch less than the resolution limit "W" in lithography method, the closed loop cut of the side wall patterns can be carried out.

(Second Embodiment)

FIGS. **3**A to **3**H are cross-sectional views schematically showing each feature in a fabrication process of a semiconductor device according to the second embodiment and FIGS. **4**A to **4**C are plan views schematically showing processes of a closed loop cut carried out after the process shown in FIG. **3**H. In the first embodiment, the wiring material is preliminarily formed, the closed loop cut of the end portions of the side wall patterns are carried out, and then the wiring pattern is formed from the wiring material, but in the second embodiment, the wiring pattern having a closed loop shape is formed, and then the closed loop cut of the end portions of the side wall patterns is carried out.

As shown in FIG. **3**A, the mask material **12** is formed on a semiconductor substrate such as a silicon substrate via the foundation layer **10**, and the core patterns **13**a, **13**b are formed on the mask material **12** by a lithography method and an etching process which use a resist. The core patterns **13**a, **13**b have, for example, a line width (for example, 40 nm) near the resolution limit "W" of lithography method.

As the mask material **12**, for example, silicon oxide film or the like can be used. As the core patterns **13**a, **13**b, for example, amorphous silicon film or the like can be used.

Next, as shown in FIG. **3**B, a slimming treatment is carried out so as to make the width of the core patterns **13**a, **13**b thin up to a half size by an anisotropic etching or the like. By this, the core patterns **13**a, **13**b having a line width (for example, 20 nm) of almost a half size of the resolution limit "W" can be obtained.

Next, as shown in FIG. **3**C, a film to become a material of side wall patterns is deposited on the whole surfaces including the side surfaces of the core patterns **13**a, **13**b after the slimming treatment, parts of the film which are deposited on the upper surfaces of the core patterns **13**a, **13**b and the surface of the mask material **12** are eliminated by using the anisotropic etching or the like so as to form side wall patterns **14**a, **14**b on the side surfaces of the core patterns **13**a, **13**b. The side wall patterns **14**a, **14**b has, for example, a line width and an distance of almost a half size of the resolution limit "W".

Next, as shown in FIG. **3**D, the core patterns **13**a, **13**b are eliminated by a dry etching such as CDE, RIE or the like so as to leave the side wall patterns **14**a, **14**b having a high etching selectivity to the core patterns **13**a, **13**b. Each of the both end portions of the side wall patterns **14**a, **14**b forms a closed loop shape similarly to the first embodiment.

Next, as shown in FIG. **3**E, the mask material **12** is eliminated by using the side wall patterns **14**a, **14**b as a mask and by a dry etching or the like where a gas such as CF_4, CHF_3 is used so as to form mask patterns **12**a, **12**b, and as shown in FIG. **3**F, the side wall patterns **14**a, **14**b are eliminated by a wet etching or the like.

Next, as shown in FIG. **3**G, the wiring material **11** is formed on the whole surfaces including grooves between the mask patterns **12**a, **12**b by a sputtering method, a plating method or the like, and then the wiring material **11** located outside the grooves is eliminated by a chemical mechanical polishing (CMP) so as to fill the wiring material **11** in the grooves between the mask patterns **12**a, **12**b. As the wiring material **11**, for example, Cu, W, Al or the like can be used.

Next, as shown in FIG. **3**H, the mask patterns **12**a, **12**b are eliminated so as to form the wiring patterns **11**a, **11**b and wide patterns **11**e having a width wider than that of the wiring patterns **11**a, **11**b. Both of the end portions of the wiring patterns **11**a, **11**b are formed in a closed loop shape.

In FIG. **4**A, the wiring pattern **11**b shows an object pattern (the second pattern) which is an object of the closed loop cut, and the wiring pattern **11**a shows an adjacency pattern (the first pattern) adjacent to the wiring pattern **11**b. In case of the embodiment, the wiring patterns **11**a, **11**b include linear parts of a constant line width. Further, the adjacency pattern can be an object of the closed loop cut. In order to carry out the closed loop cut of the wiring pattern **11**b, in terms of a margin of displacement at the alignment in the lithography method, it is needed for a region of the wiring pattern **11**b where the closed loop cut is carried out to be away from the wiring pattern **11**a so that the resist **15** does not fall over the wiring pattern **11**a. Therefore, the wiring pattern **11**b is formed so as to have the following shape.

Namely, the wiring pattern **11**b has parallel parts **110** parallel to the wiring pattern **11**a and nonparallel parts **111** formed so as to be connected to the parallel parts **110** and to be not parallel to the wiring pattern **11**a, and cut regions **111**a where the closed loop cut is carried out is formed in the nonparallel parts **111**. The nonparallel parts **111** are formed in a shape bent in an oblique direction from the joining point of the parallel part **110** and the nonparallel part **111** so as to be apart from the wiring pattern **11**a, but it can have a shape bent in a rectangular direction.

As shown in FIG. **4**B, a space "S" (the second distance) is formed on the cut region **111**a located at the end portion of the wiring pattern **11**b, between the wiring pattern **11**a and a resist **15** is formed, and as shown in FIG. **4**C, the cut region **111**a of the wiring pattern **11**b is cut by the lithography method. The space "S" is formed so as to be larger than the distance "d" (the first distance) between the wiring pattern **11**a and the wiring pattern **11**b.

According to the second embodiment, even if the wiring pattern has an arrangement pitch less than the resolution limit "W" in lithography method, the closed loop cut of the wiring pattern can be carried out. The side wall patterns **14**b as the second pattern are close to the side wall patterns **14**a so as to have a distance "d" (a first distance) between the side wall patterns **14**a, and has parallel parts **140** parallel to the side wall patterns **14**a and nonparallel parts **141** formed so as to be connected to the parallel parts **140** and to be not parallel to the side wall patterns **14**a, and cut regions **141**a where the closed loop cut is carried out is formed in the nonparallel parts **141**.

(Third Embodiment)

FIG. **5**A is a plan view schematically showing an example of side wall patterns used in a third embodiment and FIG. **5**B is a detail view of an "A" part of the side wall patterns shown in FIG. **5**A. In the first embodiment, the side wall patterns **14**a as the first pattern have a linear shape and the side wall patterns **14**b as the second pattern have a nonlinear and bent shape, but in the third embodiment, the side wall patterns **14**a as the first pattern have a bent shape, and the side wall patterns **14**b as the second pattern have a linear shape and have the cut regions **141**a in the end portions where the closed loop cut is carried out.

According to the third embodiment, similarly to the first embodiment, even if the side wall patterns have an arrangement pitch less than the resolution limit "W" in lithography method, the closed loop cut of the side wall patterns can be carried out.

Next, the fourth to the eighth embodiments where the semiconductor device of the first embodiment is applied to a phase-change memory will be explained. The fourth to the eighth embodiments show a case that the wiring patterns **11**a, **11**b constituting each of wiring pattern groups **20**A, **20**B include thirty-six (36) lines of 20 nm in line width respectively.

(Fourth Embodiment)

FIG. **6**A is a plan view schematically showing a structure of a wiring pattern in a wiring layer of a phase-change memory used in a fourth embodiment and FIG. **6**B is a detail view of a "B" part of the side wall patterns shown in FIG. **6**A.

As shown in FIG. **6**A, the phase-change memory **1** includes a memory cell region **2**, a WL extraction region **3** where word lines (WL) are extracted, formed on the right and left sides of memory cell region **2**, a BL extraction region **4** where bit lines (BL) are extracted, formed on the top and bottom sides of memory cell region **2**, and a peripheral circuit disposed under the memory cell region **2**.

The phase-change memory **1** includes a plurality of bit lines formed of the wiring patterns **11**a, **11**b extending in an "x" direction, a plurality of word lines formed of the wiring patterns **21**a, **21**b extending in an "y" direction, and a plurality of memory cells disposed in each of crossing parts of the bit lines and the word lines. The memory cell includes a series circuit having a variable resistive element formed of chalcogenide or the like and a diode such as a Schottky diode. In the phase-change memory **1**, signal lines for sell selection can be omitted so that high cell-integration can be achieved.

A three dimensional memory structure can be configured by that a cell array is configured so as to include a lower wiring layer where a plurality of word lines are formed, a memory layer having a plurality of memory cells and formed on the lower wiring layer, and an upper wiring layer formed on the memory cells, where a plurality of bit lines are formed, and a plurality of the cell arrays are disposed on a silicon substrate in a stacked state.

As shown in FIG. **6**A, the bit lines constituting the upper wiring layer include a first wiring pattern group **20**A formed at a location totally shifted in the right side and including the wiring pattern **11**a (the first pattern) of a predetermined lines, and a second wiring pattern group **20**B formed at a location totally shifted in the left side and including the wiring pattern **11**b (the second pattern) of a predetermined lines.

As shown in FIG. **6**A, the word lines constituting the lower wiring layer include a first wiring pattern group **20**C formed at a location totally shifted in the top side and including the wiring pattern **21**a (the first pattern) of a predetermined lines, and a second wiring pattern group **20**D formed at a location totally shifted in the bottom side and including the wiring pattern **21**b (the second pattern) of a predetermined lines.

The wiring patterns **11**a, **11**b include terminals **11**c to which the closed loop cut is carried out in one end portion, and contact fringes **11**d formed in another end portion by that the closed loop cut is carried out after a treatment of leaving the core materials is conducted. The terminals **11**c and the contact fringes **11**d are formed in the WL extraction region **3**. The wiring patterns **21**a, **21**b include terminals **21**c to which the closed loop cut is carried out in one end portion, and contact fringes **21**d formed in another end portion by that the closed loop cut is carried out after a treatment of leaving the core materials is conducted. The terminals **21**c and the contact fringes **21**d are formed in the BL extraction region **4**.

As shown in FIG. **6**B, in the wiring pattern **11**b constituting the second wiring pattern group **20**B of the upper wiring layer, a plurality of wiring patterns **11**b adjacent to the first wiring pattern group **20**A include a parallel part **110** and a nonparallel part **111**, and a plurality of wiring patterns **11**b located at a center portion do not have the nonparallel part **111**. The first wiring pattern group **20**A has also the same structure, and the first and second wiring pattern groups **20**C, **20**D on the lower wiring layer have also the same structure.

FIGS. **7**A to **7**F are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to the fourth embodiment. FIGS. **7**A to **7**D correspond to FIGS. **1**A to **1**D respectively, FIG. **7**E corresponds to FIG. **2**B and FIG. **7**F corresponds to FIG. **1**H.

Similarly to the first embodiment, after the wiring material and the mask material are formed on the foundation layer, as shown in FIG. **7**A, the core patterns **13**a, **13**b are formed on the mask material. A plurality of core patterns **13**b of the second wiring pattern group **20**B adjacent to the first wiring pattern group **20**A are bent in the end portions thereof in an oblique direction so as to be apart from the first wiring pattern group **20**A.

Next, as shown in FIG. **7**B, a slimming treatment of the core patterns **13**a, **13**b is carried out, and as shown in FIG. **7**C, the side wall patterns **14**a, **14**b are formed on the side surfaces of core patterns **13**a, **13**b after the slimming treatment, and as shown in FIG. **7**D, the core patterns **13**a, **13**b are eliminated by an etching so as to leave the side wall patterns **14**a, **14**b.

As shown in FIG. **7**E, a space "S" is formed on the cut region located at the end portion of the side wall patterns **14**b, between the first wiring pattern group **20**A, and the resist **15** having a hexagonal shape is formed, and the cut regions of the side wall patterns **14**b are cut by the lithography method. The space "S" between the first wiring pattern group **20**A and the resist **15** is, for example, set to 140 nm, in terms of a margin of displacement at the alignment in the lithography method.

Next, the mask material is eliminated by using the side wall patterns **14**a, **14**b as a mask and by an etching so as to form mask patterns, and the side wall patterns **14**a, **14**b are eliminated. Next, the wiring material is etched by using the mask patterns so as to form wiring patterns **11**a, **11**b, and the mask

patterns are eliminated. As shown in FIG. **7**F, the wiring patterns **11**a, **11**b having a line width and distance of 20 nm are obtained.

According to the fourth embodiment, even if the side wall patterns have an arrangement pitch less than the resolution limit "W" in lithography method, the closed loop cut of the side wall patterns can be carried out. Further, the first and second wiring pattern groups are alternately shifted in the right and left sides, and the top and bottom sides so that the areas of the extraction regions **3**, **4** can be reduced, and high cell-integration of the phase-change memory can be achieved.

(Fifth Embodiment)

FIGS. **8**A to **8**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to the fifth embodiment. FIG. **8**A corresponds to FIG. **1**D, FIG. **8**B corresponds to FIG. **2**B, and FIG. **8**C corresponds to FIG. **1**H. Further, drawings corresponding to FIGS. **1**A to **1**C are omitted.

As shown in FIG. **8**A, in the side wall patterns **14**b constituting the second wiring pattern group **20**B of the fifth embodiment, the side wall patterns **14**b closest to the first wiring pattern groups **20**A are connected each other so as to form a closed loop shape and the other thirty-four (34) lines of the side wall patterns **14**b form the closed loop shapes between the side wall patterns **14**b adjacent to each other.

After that, as shown in FIG. **8**B, a space "S" is formed on the cut region located at the end portions of the side wall patterns **14**b, between the first wiring pattern group **20**A, the resist **15** having a hexagonal shape is formed, the cut region of the side wall patterns **14**b is cut by the lithography method, and as shown in FIG. **8**C, the wiring patterns **11**a, **11**b similar to those of the fourth embodiment are formed.

(Sixth Embodiment)

FIGS. **9**A to **9**C are main part plan views schematically showing each main part of upper wiring layers used in an example of a fabrication process according to the sixth embodiment. FIG. **9**A corresponds to FIG. **1**D, FIG. **9**B corresponds to FIG. **2**B, and FIG. **9**C corresponds to FIG. **1**H. Further, drawings corresponding to FIGS. **1**A to **1**C are omitted.

As shown in FIG. **9**A, in the side wall patterns **14**b constituting the second wiring pattern group **20**B of the sixth embodiment, the side wall patterns **14**b closest to the first wiring pattern groups **20**A are connected each other along the end portions of the other side wall patterns **14**b so as to form a closed loop shape and the other thirty-four (34) lines of the side wall patterns **14**b form the closed loop shapes between the side wall patterns **14**b adjacent to each other.

After that, as shown in FIG. **9**B, a space "S" is formed on the cut region located at the end portions of the side wall patterns **14**b, between the first wiring pattern group **20**A, the resist **15** having a hexagonal shape is formed, the cut region of the side wall patterns **14**b is cut by the lithography method, and as shown in FIG. **9**C, the wiring patterns **11**a, **11**b similar to those of the fourth embodiment are formed.

(Seventh Embodiment)

FIGS. **10**A to **10**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to a seventh embodiment. FIG. **10**A corresponds to FIG. **1**D, FIG. **10**B corresponds to FIG. **2**B, and FIG. **10**C corresponds to FIG. **1**H. Further, drawings corresponding to FIGS. **1**A to **1**C are omitted.

As shown in FIG. **10**A, in the side wall patterns **14**b constituting the second wiring pattern group **20**B of the seventh embodiment, twenty-six (26) lines of the side wall patterns **14**b located at the side close to the first wiring pattern group **20**A are connected each other so as to form a closed loop shape between two side wall patterns **14**b, starting from the two side wall patterns **14**b closest to the first wiring pattern groups **20**A. Further, the ten (10) lines of the side wall patterns **14**b located interiorly form the closed loop shapes between the side wall patterns **14**b adjacent to each other.

After that, as shown in FIG. **10**B, a space "S" is formed on the cut region located at the end portion of the side wall patterns **14**b, between the first wiring pattern group **20**A, the resist **15** having a hexagonal shape is formed, the cut region of the side wall patterns **14**b is cut by the lithography method, and as shown in FIG. **10**C, the wiring patterns **11**a, **11**b similar to those of the fourth embodiment are formed.

(Eighth Embodiment)

FIGS. **11**A to **11**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to the eighth embodiment. FIG. **11**A corresponds to FIG. **1**D, FIG. **11**B corresponds to FIG. **2**B, and FIG. **11**C corresponds to FIG. **1**H. Further, drawings corresponding to FIGS. **1**A to **1**C are omitted.

As shown in FIG. **11**A, in the side wall patterns **14**b constituting the second wiring pattern group **20**B of the eighth embodiment, the side wall patterns **14**b are connected each other so as to form a closed loop shape between two side wall patterns **14**b, starting from the side wall patterns **14**b closest to the first wiring pattern groups **20**A.

After that, as shown in FIG. **11**B, a space "S" is formed on the cut region located at the end portions of the side wall patterns **14**b, between the first wiring pattern group **20**A, the resist **15** having a hexagonal shape is formed, the cut region of the side wall patterns **14**b is cut by the lithography method, and as shown in FIG. **11**C, the wiring patterns **11**a, **11**b are formed.

According to the fourth to eighth embodiments, even if the side wall patterns formed by a line and space have an arrangement pitch less than the resolution limit "W" in lithography method, the closed loop cut of the side wall patterns can be carried out.

Next, the ninth to the thirteenth embodiments where the semiconductor device of the first embodiment is applied to a wiring by a line and space will be explained. The ninth to the thirteenth embodiments show a case that the wiring patterns **11**a, **11**b constituting each of wiring pattern groups **20**A, **20**B include thirty-six (36) lines of 20 nm in line width respectively.

(Ninth Embodiment)

FIGS. **12**A to **12**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to the ninth embodiment. FIG. **12**A corresponds to FIG. **1**D, FIG. **12**B corresponds to FIG. **2**B, and FIG. **12**C corresponds to FIG. **1**H. Further, drawings corresponding to FIGS. **1**A to **1**C are omitted. Furthermore, the embodiment shows a case that the second wiring pattern groups **20**B exist in the right-and-left sides.

As shown in FIG. **11**A, in the side wall patterns **14**b constituting the second wiring pattern group **20**B of the ninth embodiment, the side wall patterns **14**b are connected each other so as to form a closed loop shape between the side wall patterns **14**b, starting from the side wall patterns **14**b closest to the first wiring pattern groups **20**A, and to provide a symmetrical appearance.

After that, as shown in FIG. **12**B, a space "S" is formed on the cut region located at the end portions of the side wall patterns **14**b, between the first wiring pattern group **20**A, the resist **15** having an octagon shape is formed, the cut region of

the side wall patterns **14**b is cut by the lithography method, and as shown in FIG. **12**C, the wiring patterns **11**a, **11**b are formed.

(Tenth Embodiment)

FIGS. **13**A to **13**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to the tenth embodiment. FIG. **13**A corresponds to FIG. **1**D, FIG. **13**B corresponds to FIG. **2**B, and FIG. **13**C corresponds to FIG. **1**H. Further, drawings corresponding to FIGS. **1**A to **1**C are omitted. Furthermore, the embodiment shows a case that the second wiring pattern groups **20**B exist in the right-and-left sides.

As shown in FIG. **13**A, in the side wall patterns **14**b constituting the second wiring pattern group **20**B of the tenth embodiment, sixteen (16) lines of the side wall patterns **14**b located at the sides close to the first wiring pattern groups **20**A are connected each other at the right-and-left end portions (not shown) so as to form the closed loop shapes between the side wall patterns **14**b close to the first wiring pattern groups **20**A. Further, ten (10) lines of the side wall patterns **14**b located interiorly are connected each other so as to form the closed loop shape between the side wall patterns **14**b, starting from the side wall patterns **14**b closest to the first wiring pattern groups **20**A, and so as to provide a symmetrical appearance. Further, ten (10) lines of the side wall patterns **14**b located further interiorly form the closed loop shapes between the side wall patterns **14**b adjacent to each other, and provide a symmetrical appearance.

After that, as shown in FIG. **13**B, a space "S" is formed on the cut region located at the end portions of the side wall patterns **14**b, between the first wiring pattern group **20**A, the resist **15** having an octagon shape is formed, the cut region of the side wall patterns **14**b is cut by the lithography method, and as shown in FIG. **13**C, the wiring patterns **11**a, **11**b are formed.

(Eleventh Embodiment)

FIGS. **14**A to **14**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to the eleventh embodiment. FIG. **14**A corresponds to FIG. **1**D, FIG. **14**B corresponds to FIG. **2**B, and FIG. **14**C corresponds to FIG. **1**H. Further, drawings corresponding to FIGS. **1**A to **1**C are omitted. Furthermore, the embodiment shows a case that the second wiring pattern groups **20**B exist in the right-and-left sides.

As shown in FIG. **14**A, in the side wall patterns **14**b constituting the second wiring pattern group **20**B of the eleventh embodiment, two (2) lines of the side wall patterns **14**b located at the sides closest to the first wiring pattern groups **20**A are connected each other at the right-and-left end portions (not shown) so as to form a loop shape between the two side wall patterns **14**b, and the other side wall patterns **14**b located interiorly form the loop shapes between the side wall patterns **14**b adjacent to each other, and provide a symmetrical appearance.

After that, as shown in FIG. **14**B, a space "S" is formed on the cut region located at the end portions of the side wall patterns **14**b, between the first wiring pattern group **20**A, the resist **15** having an octagon shape is formed, the cut region of the side wall patterns **14**b is cut by the lithography method, and as shown in FIG. **14**C, the wiring patterns **11**a, **11**b are formed.

(Twelfth Embodiment)

FIGS. **15**A to **15**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to the twelfth embodiment. FIG. **15**A corresponds to FIG. **1**D, FIG. **15**B corresponds to FIG. **2**B, and FIG. **15**C corresponds to FIG. **1**H. Further, drawings corresponding to FIGS. **1**A to **1**C are omitted. Furthermore, the embodiment shows a case that the second wiring pattern groups **20**B exist in the right-and-left sides.

As shown in FIG. **15**A, the side wall patterns **14**b constituting the second wiring pattern group **20**B of the twelfth embodiment have a structure that a side wall pattern **14**b having a hexagonal shape in the center portion is added to the side wall patterns **14**b of the eleventh embodiment, and the other parts are formed similarly to those of the eleventh embodiment.

After that, as shown in FIG. **15**B, a space "S" is formed on the cut region located at the end portions of the side wall patterns **14**b, between the first wiring pattern group **20**A, the resist **15** having an octagon shape is formed, the cut region of the side wall patterns **14**b is cut by the lithography method, and as shown in FIG. **15**C, the wiring patterns **11**a, **11**b similar to those of the eighth embodiment are formed.

(Thirteenth Embodiment)

FIGS. **16**A to **16**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to the thirteenth embodiment. FIG. **16**A corresponds to FIG. **1**D, FIG. **16**B corresponds to FIG. **2**B, and FIG. **16**C corresponds to FIG. **1**H. Further, drawings corresponding to FIGS. **1**A to **1**C are omitted. Furthermore, the embodiment shows a case that the second wiring pattern groups **20**B exist in the right-and-left sides.

As shown in FIG. **16**A, in the side wall patterns **14**b constituting the second wiring pattern group **20**B of the thirteenth embodiment, two (2) lines of the side wall patterns **14**b located at the sides closest to the first wiring pattern groups **20**A are connected each other at the right-and-left end portions (not shown) so as to form a loop shape between the two side wall patterns **14**b. Further, twenty-four (24) lines of the side wall patterns **14**b located interiorly form the loop shapes between the side wall patterns **14**b, from the parts located externally to the parts located internally in order, and provide a symmetrical appearance. Ten (10) lines of the side wall patterns **14**b located further interiorly form the loop shapes between the side wall patterns **14**b adjacent to each other, and provide a symmetrical appearance.

After that, as shown in FIG. **16**B, a space "S" is formed on the cut region located at the end portions of the side wall patterns **14**b, between the first wiring pattern group **20**A, the resist **15** having an octagon shape is formed, the cut region of the side wall patterns **14**b is cut by the lithography method, and as shown in FIG. **16**C, the wiring patterns **11**a, **11**b similar to those of the seventh embodiment are formed.

Next, the fourteenth to the seventeenth embodiments where the semiconductor device of the second embodiment is applied to a phase-change memory will be explained. The fourteenth to the seventeenth embodiments show a case that the wiring patterns **11**a, **11**b constituting each of wiring pattern groups **20**A, **20**B include thirty-three (33) lines of 20 nm in line width respectively.

FIGS. **17**A to **17**H are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to the fourteenth embodiment. FIGS. **17**A to **17**D correspond to FIGS. **3**A to **3**D, FIG. **17**E corresponds to FIG. **3**G, and FIG. **17**F corresponds to FIG. **3**H. FIG. **17**G corresponds to FIG. **4**B, and FIG. **17**H corresponds to FIG. **4**C.

Similarly to the second embodiment, as shown in FIG. **17**A, after a mask material is formed on a foundation layer, core patterns **13**a, **13**b are formed on the mask material. The core patterns **13**b constituting the second wiring pattern group **20**B are connected each other so as to form a closed

loop shape between two core patterns **13**b, starting from the two side wall patterns **14**b closest to the first wiring pattern groups **20**A.

Next, as shown in FIG. **17**B, a slimming treatment of the core patterns **13**a, **13**b is carried out, and as shown in FIG. **17**C, side wall patterns **14**a, **14**b are formed on the side surfaces of the core patterns **13**a, **13**b after the slimming treatment, and as shown in FIG. **17**D, the core patterns **13**a, **13**b are eliminate by an etching so as to leave the side wall patterns **14**a, **14**b.

Next, as shown in FIG. **17**E, the mask material is eliminated by an etching and by using the side wall patterns **14**a, **14**b as a mask so as to form mask patterns, and the side wall patterns **14**a, **14**b are eliminated.

Next, as shown in FIG. **17**E, the wiring material **11** is filled in the peripheral of the mask patterns **12**a, **12**b.

Next, as shown in FIG. **17**F, the mask patterns **12**a, **12**b are eliminated so as to form wiring patterns **11**a, **11**b. The wiring patterns **11**a, **11**b form closed loop shapes. Wide patterns **11**e are formed between the wiring pattern groups **20**A.

Next, as shown in FIG. **17**G, a space "S" is formed on the cut region located at the end portions of the wiring patterns **11**b, between the first wiring pattern group **20**A, the resist **15** having a hexagonal shape is formed, the cut region of the wiring patterns **11**b is cut by the lithography method, and as shown in FIG. **17**H, the wiring patterns **11**a, **11**b are formed.

(Fifteenth Embodiment)

FIGS. **18**A to **18**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to a fifteenth embodiment. FIG. **18**A corresponds to FIG. **3**H. FIG. **18**B corresponds to FIG. **4**B, and FIG. **18**C corresponds to FIG. **4**C. Further, drawings corresponding to FIGS. **3**A to **3**G are omitted.

As shown in FIG. **18**A, the wiring patterns **11**b constituting the second wiring pattern group **20**B of the fifteenth embodiment are connected each other on alternate lines so as to form closed loop shapes between the wiring patterns **11**b, further, the wiring patterns **11**a of the wiring pattern groups **20**A closest to the first wiring pattern group **20**B are also connected each other so as to form a closed loop shape between the wiring patterns **11**a.

After that, as shown in FIG. **18**B, a space "S" is formed on the cut region located at the end portions of the wiring patterns **11**b, between the first wiring pattern group **20**A, the resist **15** having a hexagonal shape is formed, the cut region of the wiring patterns **11**b is cut by the lithography method, and as shown in FIG. **18**C, the wiring patterns **11**a, **11**b are formed.

(Sixteenth Embodiment)

FIGS. **19**A to **19**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to the sixteenth embodiment. FIG. **19**A corresponds to FIG. **3**H. FIG. **19**B corresponds to FIG. **4**B, and FIG. **19**C corresponds to FIG. **4**C. Further, drawings corresponding to FIGS. **3**A to **3**G are omitted.

As shown in FIG. **19**A, the wiring patterns **11**b constituting the second wiring pattern group **20**B of the sixteenth embodiment are connected each other on alternate lines so as to form closed loop shapes between the wiring patterns **11**b, further, the wiring patterns **11**a of the wiring pattern groups **20**A closest to the first wiring pattern group **20**B are also connected each other so as to form a closed loop shape between the wiring patterns **11**a.

After that, as shown in FIG. **19**B, a space "S" is formed on the cut region located at the end portions of the wiring patterns **11**b, between the first wiring pattern group **20**A, the resist **15** having a hexagonal shape is formed, the cut region of the wiring patterns **11**b is cut by the lithography method, and as shown in FIG. **19**C, the wiring patterns **11**a, **11**b similar to those of the twelfth embodiment are formed.

FIGS. **20**A to **20**C are main part plan views schematically showing an example of a fabrication process according to a seventeenth embodiment

(Seventeenth Embodiment)

FIGS. **20**A to **20**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to the seventeenth embodiment. FIG. **20**A corresponds to FIG. **3**H. FIG. **20**B corresponds to FIG. **4**B, and FIG. **20**C corresponds to FIG. **4**C. Further, drawings corresponding to FIGS. **3**A to **3**G are omitted.

As shown in FIG. **20**A, in the wiring patterns **11**b constituting the second wiring pattern group **20**B of the seventeenth embodiment, twenty-four (24) lines of the wiring patterns **11**b located at the side close to the first wiring pattern group **20**A are connected each other so as to form a closed loop shape between two wiring patterns **11**b, starting from the two wiring patterns **11**b closest to the first wiring pattern groups **20**A. Further, nine (9) lines of the wiring patterns **11**b located interiorly are connected alternatively to the wiring patterns **11**b having a closed loop shape and located most interiorly. Furthermore, the wiring patterns **11**a of the wiring pattern groups **20**A closest to the first wiring pattern group **20**B are also connected each other so as to form a closed loop shape between the wiring patterns **11**a.

After that, as shown in FIG. **20**B, a space "S" is formed on the cut region located at the end portions of the wiring patterns **11**b, between the first wiring pattern group **20**A, the resist **15** having a hexagonal shape is formed, the cut region of the wiring patterns **11**b is cut by the lithography method, and as shown in FIG. **20**C, the wiring patterns **11**a, **11**b are formed.

Next, the eighteenth to twenty-second the embodiments where the semiconductor device of the second embodiment is applied to a wiring by a line and space will be explained. The eighteenth to twenty-second embodiments show a case that the wiring patterns **11**a, **11**b constituting each of wiring pattern groups **20**A, **20**B include thirty-six (36) lines of 20 nm in line width respectively.

(Eighteenth Embodiment)

FIGS. **21**A to **21**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to the eighteenth embodiment. FIG. **21**A corresponds to FIG. **4**A, FIG. **21**B corresponds to FIG. **4**B, and FIG. **21**C corresponds to FIG. **4**C. Further, drawings corresponding to FIGS. **3**A to **3**G are omitted. Furthermore, the embodiment shows a case that the second wiring pattern groups **20**B exist in the right-and-left sides.

As shown in FIG. **21**A, in the wiring patterns **11**b constituting the second wiring pattern group **20**B of the eighteenth embodiment, thirty-two (32) lines of the wiring patterns **11**b except for the lines centrally located are connected each other so as to form a closed loop shape between the wiring patterns **11**b, starting from the wiring patterns **11**b closest to the first wiring pattern groups **20**A, and to provide a symmetrical appearance.

After that, as shown in FIG. **21**B, a space "S" is formed on the cut region located at the end portions of the wiring patterns **11**b, between the first wiring pattern group **20**A, the resist **15** having an octagon shape is formed, the cut region of the wiring patterns **11**b is cut by the lithography method, and as shown in FIG. **21**C, the wiring patterns **11**a, **11**b are formed.

(Nineteenth Embodiment)

FIGS. **22**A to **22**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to the nineteenth embodiment. FIG. **22**A corresponds to FIG. **4**A, FIG. **22**B corresponds to FIG. **4**B, and FIG. **22**C corresponds to FIG. **4**C. Further, drawings corresponding to FIGS. **3**A to **3**G are omitted. Furthermore, the embodiment shows a case that the second wiring pattern groups **20**B exist in the right-and-left sides.

As shown in FIG. **22**A, the wiring patterns **11**b constituting the second wiring pattern group **20**B of the nineteenth embodiment are alternatively connected to the wide patterns **11**e formed in the center portion so as to form the closed loop shapes and to provide a symmetrical appearance. Further, the wiring patterns **11**a of the first wiring pattern groups **20**A closest to the second wiring pattern group **20**B include a part (a triangular shape) having a wide line width formed in the vicinity of the cut region where the closed loop cut is carried out.

After that, as shown in FIG. **22**B, a space "S" is formed on the cut region located at the end portions of the wiring patterns **11**b, between the first wiring pattern group **20**A, the resist **15** having a hexagonal shape is formed, the cut region of the wiring patterns **11**b is cut by the lithography method, and as shown in FIG. **22**C, the wiring patterns **11**a, **11**b similar to those of the twelfth embodiment are formed.

(Twentieth Embodiment)

FIGS. **23**A to **24**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to the twentieth embodiment. FIG. **23**A corresponds to FIG. **4**A, FIG. **23**B corresponds to FIG. **4**B, and FIG. **23**C corresponds to FIG. **4**C. Further, drawings corresponding to FIGS. **3**A to **3**G are omitted. Furthermore, the embodiment shows a case that the second wiring pattern groups **20**B exist in the right-and-left sides.

As shown in FIG. **23**A, the wiring patterns **11**b constituting the second wiring pattern group **20**B of the twentieth embodiment are alternatively connected to circular patterns formed in the periphery of the wide patterns **11**e centrally located so as to form the closed loop shapes and to provide a symmetrical appearance. Further, the wiring patterns **11**a of the first wiring pattern groups **20**A closest to the second wiring pattern group **20**B include a part (a triangular shape) having a wide line width formed in the vicinity of the cut region where the closed loop cut is carried out.

After that, as shown in FIG. **23**B, a space "S" is formed on the cut region located at the end portions of the wiring patterns **11**b, between the first wiring pattern group **20**A, the resist **15** having a hexagonal shape is formed, the cut region of the wiring patterns **11**b is cut by the lithography method, and as shown in FIG. **23**C, the wiring patterns **11**a, **11**b are formed.

(Twenty-First Embodiment)

FIGS. **24**A to **24**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to a twenty-first embodiment. FIG. **24**A corresponds to FIG. **4**A, FIG. **24**B corresponds to FIG. **4**B, and FIG. **24**C corresponds to FIG. **4**C. Further, drawings corresponding to FIGS. **3**A to **3**G are omitted. Furthermore, the embodiment shows a case that the second wiring pattern groups **20**B exist in the right-and-left sides.

As shown in FIG. **21**A, in the wiring patterns **11**b constituting the second wiring pattern group **20**B of the twenty-first embodiment, twenty-six (26) lines of the wiring patterns **11**b located at the side close to the first wiring pattern group **20**A are connected each other so as to form a closed loop shape between two wiring patterns **11**b, starting from the two wiring patterns **11**b closest to the first wiring pattern groups **20**A, and so as to provide a symmetrical appearance. Further, the ten (10) lines of the wiring patterns **11**b located interiorly are alternatively connected to the wiring patterns **11**b having a closed loop shape and located interiorly, and provide a symmetrical appearance. Further, the wiring patterns **11**a of the first wiring pattern groups **20**A closest to the second wiring pattern group **20**B include a part (a triangular shape) having a wide line width formed in the vicinity of the cut region where the closed loop cut is carried out.

After that, as shown in FIG. **24**B, a space "S" is formed on the cut region located at the end portions of the wiring patterns **11**b, between the first wiring pattern group **20**A, the resist **15** having an octagon shape is formed, the cut region of the wiring patterns **11**b is cut by the lithography method, and as shown in FIG. **24**C, the wiring patterns **11**a, **11**b are formed.

(Twenty-Second Embodiment)

FIGS. **25**A to **25**C are main part plan views schematically showing each of upper wiring layers used in an example of a fabrication process according to the twenty-second embodiment. FIG. **25**A corresponds to FIG. **4**A, FIG. **25**B corresponds to FIG. **4**B, and FIG. **25**C corresponds to FIG. **4**C. Further, drawings corresponding to FIGS. **3**A to **3**G are omitted. Furthermore, the embodiment shows a case that the second wiring pattern groups **20**B exist in the right-and-left sides.

As shown in FIG. **25**A, in the wiring patterns **11**b constituting the second wiring pattern group **20**B of the twenty-second embodiment, twenty-two (22) lines of the wiring patterns **11**b located at the side close to the first wiring pattern group **20**A form the closed loop shapes between the wiring patterns **11**b in the right-and-left end portions (not shown) Further, the four (4) lines of the wiring patterns **11**b located interiorly are connected each other so as to form a closed loop shape between the wiring patterns **11**b, starting from the wiring patterns **11**b closest to the first wiring pattern groups **20**A, and so as to provide a symmetrical appearance. Further, nine (9) lines of the wiring patterns **11**b located further interiorly are alternatively connected to the closed loop shapes located interiorly so as to provide a symmetrical appearance. Further, the wiring patterns **11**a of the first wiring pattern groups **20**A closest to the second wiring pattern group **20**B include a part (a triangular shape) having a wide line width formed in the vicinity of the cut region where the closed loop cut is carried out.

After that, as shown in FIG. **25**B, a space "S" is formed on the cut region located at the end portions of the wiring patterns **11**b, between the first wiring pattern group **20**A, the resist **15** having an octagon shape is formed, the cut region of the wiring patterns **11**b is cut by the lithography method, and as shown in FIG. **25**C, the wiring patterns **11**a, **11**b are formed.

Further, it should be noted that the present invention is not intended to be limited to the above-mentioned embodiments, and the various kinds of changes thereof can be implemented by those skilled in the art without departing from the gist of the invention.

What is claimed is:

1. A method of fabricating a semiconductor device, comprising:

forming a first pattern and a second pattern, the first pattern having linear parts of a constant line width, and the second pattern having parallel parts parallel to the linear parts and nonlinear parts not parallel to the linear parts, wherein:

the parallel parts are at a first distance away from the linear parts,

the parallel parts and the nonparallel parts are connected to each other at joining points,

the nonparallel parts bend from the joining points in a direction away from the linear parts, and

the second pattern is formed in a closed loop shape; and

forming a resist over the nonparallel parts, a point on the resist, which is closest to the linear parts, being at a second distance away from the linear parts, the second distance being larger than the first distance; and

carrying out a closed loop cut at a region covered by the resist.

2. The method of fabricating a semiconductor device according to claim **1**, wherein:

the second pattern is formed such that the nonparallel parts are connected to form the closed loop shape.

3. The method of fabricating a semiconductor device according to claim **1**, wherein:

the first pattern is formed in a closed loop shape, and

forming the first pattern and the second pattern comprises:

forming core patterns on a foundation layer,

forming side wall patterns on side surfaces of the core patterns, and

removing the core patterns, leaving the side wall patterns on the foundation layer,

wherein the first pattern includes a first one of the side wall patterns and the second pattern includes a second one of the side wall patterns.

4. The method of fabricating a semiconductor device according to claim **3**, wherein:

the closed loop cut is carried out to the second pattern including the second one of the side wall patterns.

5. The method of fabricating a semiconductor device according to claim **3**, wherein:

the closed loop cut is carried out to a wiring material filled in grooves having a closed loop shape, the grooves being formed by etching a processed film formed in the foundation layer or formed between the foundation layer and the second pattern by using the second pattern including the side wall patterns as a mask.

6. A method of fabricating a semiconductor device, comprising:

forming a first pattern group including a plurality of first patterns arranged at a predetermined pitch and a second pattern group including a plurality of second patterns arranged at the predetermined pitch, one of the second patterns closest to the first pattern group having parallel parts parallel to the first patterns and nonparallel parts not parallel to the first patterns, wherein:

the parallel parts are at a first distance away from a one of the first patterns which is closest to the second pattern group,

the parallel parts and the nonparallel parts are connected to each other at joining points,

the nonparallel parts bend from the joining points in a direction away from the first patterns, and

the second pattern is formed in a closed loop shape;

forming a resist over the nonparallel parts, a point on the resist, which is closest to the first pattern group, being at a second distance away from the one of the first patterns closest to the second pattern group, the second distance being larger than the first distance; and

carrying out a closed loop cut at a region covered by the resist.

7. The method of fabricating a semiconductor device according to claim **6**, wherein:

the first patterns have linear parts of a constant line width and are formed in closed loop shapes, and

forming the first pattern group and the second pattern group comprises:

forming core patterns on a foundation layer,

forming side wall patterns on side surfaces of the core patterns, and

removing the core patterns, leaving the side wall patterns on the foundation layer,

wherein the first patterns include first ones of the side wall patterns and the second patterns include second ones of the side wall patterns.

8. The method of fabricating a semiconductor device according to claim **7**, wherein:

the closed loop cut is carried out to a wiring material filled in grooves having a closed loop shape, the grooves being formed by etching a processed film formed in the foundation layer or formed between the foundation layer and the second pattern by using the second pattern including the side wall patterns as a mask.

9. The method of fabricating a semiconductor device according to claim **6**, wherein:

the first pattern group and second pattern group are shifted in opposite directions along a line parallel to a direction in which the first patterns and the second patterns extend.

10. The method of fabricating a semiconductor device according to claim **6**, wherein the first pattern group and the second pattern group constitute a lower wiring layer, and the method further comprises:

repeating the steps of claim **6** to form a third pattern group including a plurality of third patterns and a fourth pattern group including a plurality of fourth patterns, the third and fourth pattern groups being formed over the first and the second pattern groups, wherein:

the third pattern group is formed similar to the first pattern group,

the fourth pattern group is formed similar to the second pattern group,

the third patterns and the fourth patterns extend in a direction perpendicular to the first patterns and the second patterns, and

the third pattern group and the fourth pattern group constitute an upper wiring layer.

11. The method of fabricating a semiconductor device according to claim **6**, wherein:

after the closed loop cut is carried out, forming contact fringes.

12. A method of fabricating a semiconductor device including a wiring pattern, comprising:

forming an insulating layer above a semiconductor substrate;

forming a first pattern part, a second pattern part, and a third pattern part on the insulating layer, wherein:

the first pattern part linearly extends in an extension direction on the insulating layer,

the second pattern part:

is adjacent and parallel to the first pattern part, and

is at a first distance away from the first pattern part, and

the third pattern part:

is connected to the second pattern part continuously, and

is adjacent and nonparallel to the first pattern part, and

a distance between the first pattern part and the third pattern part gradually increases with a distance from the second pattern part along the extension direction;

forming a masking layer above the third pattern part, a point on an edge of the masking layer, which is closest to the first pattern part, being at a second distance away from the first pattern part, the second distance being larger than the first distance; and

etching the insulating layer using the first, second, and third pattern parts as a mask.

13. The method according to claim 12, wherein the semiconductor device is a semiconductor memory device.

14. The method according to claim 12, further comprising:

forming, after etching the insulating layer, the wiring pattern in a same layer as the insulating layer.

15. The method according to claim 14, wherein the wiring pattern includes at least one of Cu, Al, or W.

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