US00RE45579E

(19) **United States**
(12) **Reissued Patent**
Ahn et al.

(10) **Patent Number: US RE45,579 E**
(45) **Date of Reissued Patent: Jun. 23, 2015**

(54) **THIN-FILM TRANSISTOR AND METHOD OF MAKING SAME**

(71) Applicant: **LG Display Co., Ltd.**, Seoul (KR)

(72) Inventors: **Byung-Chul Ahn**, Seoul (KR); **Hyun-Sik Seo**, Goyang (KR)

(73) Assignee: **LG Display Co., Ltd.**, Seoul (KR)

(21) Appl. No.: **13/646,594**

(22) Filed: **Oct. 5, 2012**

Related U.S. Patent Documents

Reissue of:

(64) Patent No.: **6,815,321**
Issued: **Nov. 9, 2004**
Appl. No.: **10/377,732**
Filed: **Mar. 4, 2003**

U.S. Applications:

(60) Division of application No. 10/154,955, filed on May 28, 2002, now Pat. No. 6,548,829, which is a continuation of application No. 09/940,504, filed on Aug. 29, 2001,

(Continued)

(30) **Foreign Application Priority Data**

Mar. 4, 1997 (KR) 1997-7010

(51) **Int. Cl.**
H01L 21/3205 (2006.01)
H01L 29/423 (2006.01)
H01L 29/49 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 29/42384*** (2013.01); ***H01L 29/4908*** (2013.01)

(58) **Field of Classification Search**
USPC 438/149, 151, 154, 155, 158–160, 481, 438/482, 483, 588, 592
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,220,706	A	9/1980	Spak
5,036,370	A	7/1991	Miyago et al.

(Continued)

FOREIGN PATENT DOCUMENTS

EP	0301571	2/1989
EP	9206497	4/1992

(Continued)

OTHER PUBLICATIONS

LG Philips LCD Co., Ltd, Office Action, JP H10-37670, Dec. 3, 2007, 8 pgs.

(Continued)

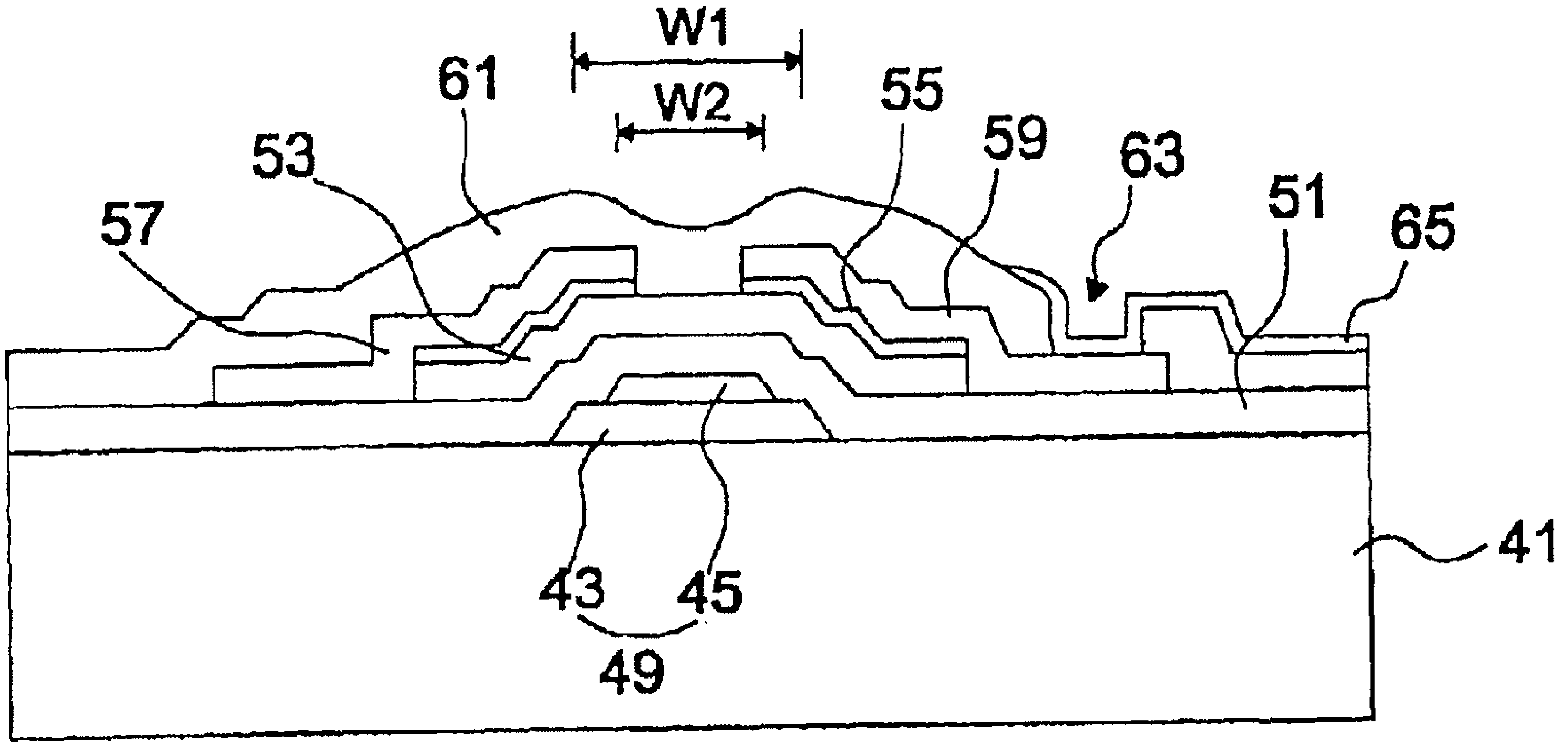
Primary Examiner — Marcos D Pizarro Crespo

(74) *Attorney, Agent, or Firm* — Morgan, Lewis & Bockius LLP

(57) **ABSTRACT**

A thin-film transistor includes a substrate, and a gate including a double-layered structure having first and second metal layers provided on the substrate, the first metal layer being wider than the second metal layer by 1 to 4 μm. A method of making such a thin-film transistor includes the steps of: depositing a first metal layer on a substrate, depositing a second metal layers directly on the first metal layer; forming a photoresist having a designated width on the second metal layer; patterning the second metal layer via isotropic etching using the photoresist as a mask; patterning the first metal layer by means of an anisotropic etching using the photoresist as a mask, the first metal layer being etched to have the designated width, thus forming a gate having a laminated structure of the first and second metal layers; and removing the photoresist.

33 Claims, 6 Drawing Sheets



Related U.S. Application Data

now abandoned, which is a division of application No. 09/243,556, filed on Feb. 2, 1999, now Pat. No. 6,340,610, which is a division of application No. 08/918,119, filed on Aug. 27, 1997, now Pat. No. 5,905,274.

(56) References Cited

U.S. PATENT DOCUMENTS

5,132,745	A	*	7/1992	Kwasnick et al.	257/412
5,156,986	A		10/1992	Wei et al.	
5,162,933	A		11/1992	Kakuda et al.	
5,191,453	A		3/1993	Okumura	
5,349,205	A		9/1994	Kobayashi et al.	
5,428,250	A		6/1995	Ikeda et al.	
5,464,500	A		11/1995	Tsujimura et al.	
5,644,146	A		7/1997	Arai et al.	
5,686,749	A		11/1997	Matsuo	
5,721,164	A		2/1998	Wu	
5,731,216	A		3/1998	Holmberg et al.	
5,808,336	A		9/1998	Miyawaki	
5,808,595	A		9/1998	Kubota et al.	
5,811,835	A	*	9/1998	Seiki et al.	257/57
5,821,159	A	*	10/1998	Ukita	438/592
5,889,573	A		3/1999	Yamamoto et al.	
5,903,326	A		5/1999	Lee	
5,982,004	A		11/1999	Sin et al.	
6,063,686	A		5/2000	Masuda et al.	
6,201,281	B1		3/2001	Miyazaki et al.	
6,333,518	B1		12/2001	Seo	
6,340,610	B1	*	1/2002	Ahn et al.	438/158
6,815,321	B2		11/2004	Ahn et al.	
2002/0048861	A1		4/2002	Seo	

FOREIGN PATENT DOCUMENTS

EP	0602315	7/1993
EP	0602315	6/1994
EP	0301571	6/1996
EP	0812012	12/1997
GB	2253742	9/1992
GB	2254187	9/1992
GB	2307597	5/1997
JP	56-118370	9/1981
JP	4097531	3/1982
JP	60-149173	8/1985
JP	61-044468	3/1986
JP	64-084668	3/1989
JP	1120068	5/1989
JP	1222448	9/1989
JP	03-114028	5/1991
JP	03-227022	10/1991
JP	04-188770	7/1992
JP	05-029282	2/1993
JP	05-066421	3/1993
JP	5315615	11/1993
JP	05-343683	12/1993
JP	6-37311	2/1994
JP	6104241	4/1994
JP	06-230428	8/1994
JP	06281954	10/1994
JP	7077695	3/1995
JP	08-106107	4/1996
JP	08-136951	5/1996
JP	08-264790	10/1996
JP	8254680	10/1996
JP	09-005786	1/1997
JP	09-171197	6/1997
JP	1-120068	5/2001
JP	1-222448	8/2001
JP	4-097531	4/2004
JP	5-315615	11/2005
JP	6-104241	4/2006
JP	6-281954	10/2006
JP	7-077695	3/2007
JP	08-095083	4/2008
JP	8-254680	10/2008
KR	954593	2/1995
KR	95-4593	7/2001
WO	9206504	4/1992
WO	WO 92/06497	4/1992
WO	WO 92/06504	4/1992

OTHER PUBLICATIONS

LG Display Co., Ltd, Office Action, JP H10-37670, Jun. 23, 2008, 10 pgs.

LG Display Co., Ltd, Office Action, JP H10-37670, Jan. 26, 2009, 6 pgs.

LG Display Co., Ltd, Office Action, JP H10-37670, Jan. 18, 2012, 20 pgs.

LG Display Co., Ltd, Office Action, JP 2009-173049, May 14, 2012, 4 pgs.

Hillock-Free Al-Gate Materials Using Stress-Absorbing Buffer Layer for Large Area AMLCDs, Soc. For Information Display 96 Digest, 1996, pp. 341-344.

Kim, Pure Al and Al-Alloy Gate-Line Processes in TFT-LCDs, Samsugn Electronics Co, Kiheung, Korea, SID 96 Digest, pp. 337-340.

Low Cost, High Display Quality TFT-LCD Process, Society for Information Display, EuroDisplay 96, Proc. 16th Int'l Display Research Conference, Oct. 1, 1996, pp. 591-594.

Wet-Etchant for Molybdenum Having High Selectivity Against Aluminum, IBM Technical Disclosure Bulletin, vol. 35, No. 3, Aug. 1, 1992, pp. 205-206.

AT Patent Abstracts of Japan, vol. 9, No. 315 [E-365] and Japan 60-149173 (Hitachi).

AU Patent Abstracts of Japan, vol. 5, No. 197 [E-86] and Japan 56-118370 (Cho Lsi Gijutsu).

"Pure Al and Al-Alloy Gate-Line Processes in TFT-LCDs", Samsung Electronics Co., Ltd., Kiheung, Korea, C.W. Kim et al., SID 96 Digest, pp. 337-340.

* cited by examiner

FIG.1A

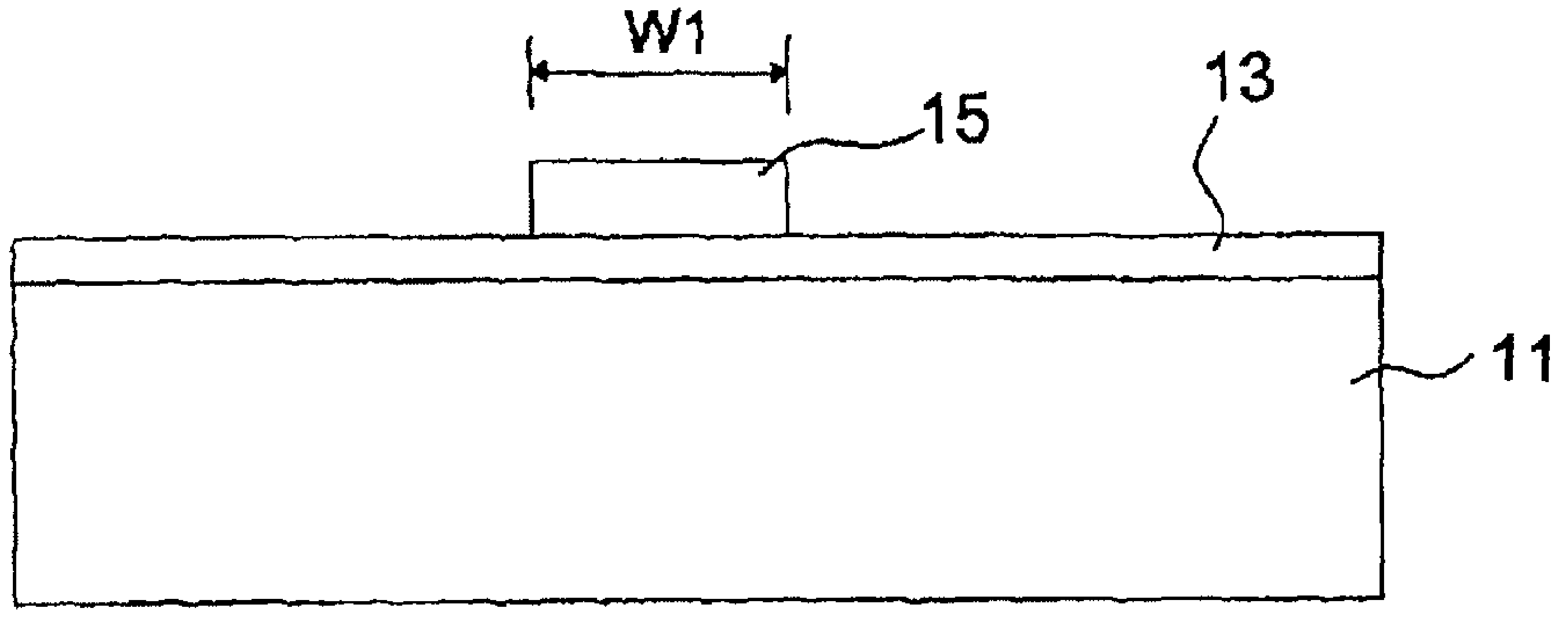


FIG.1B

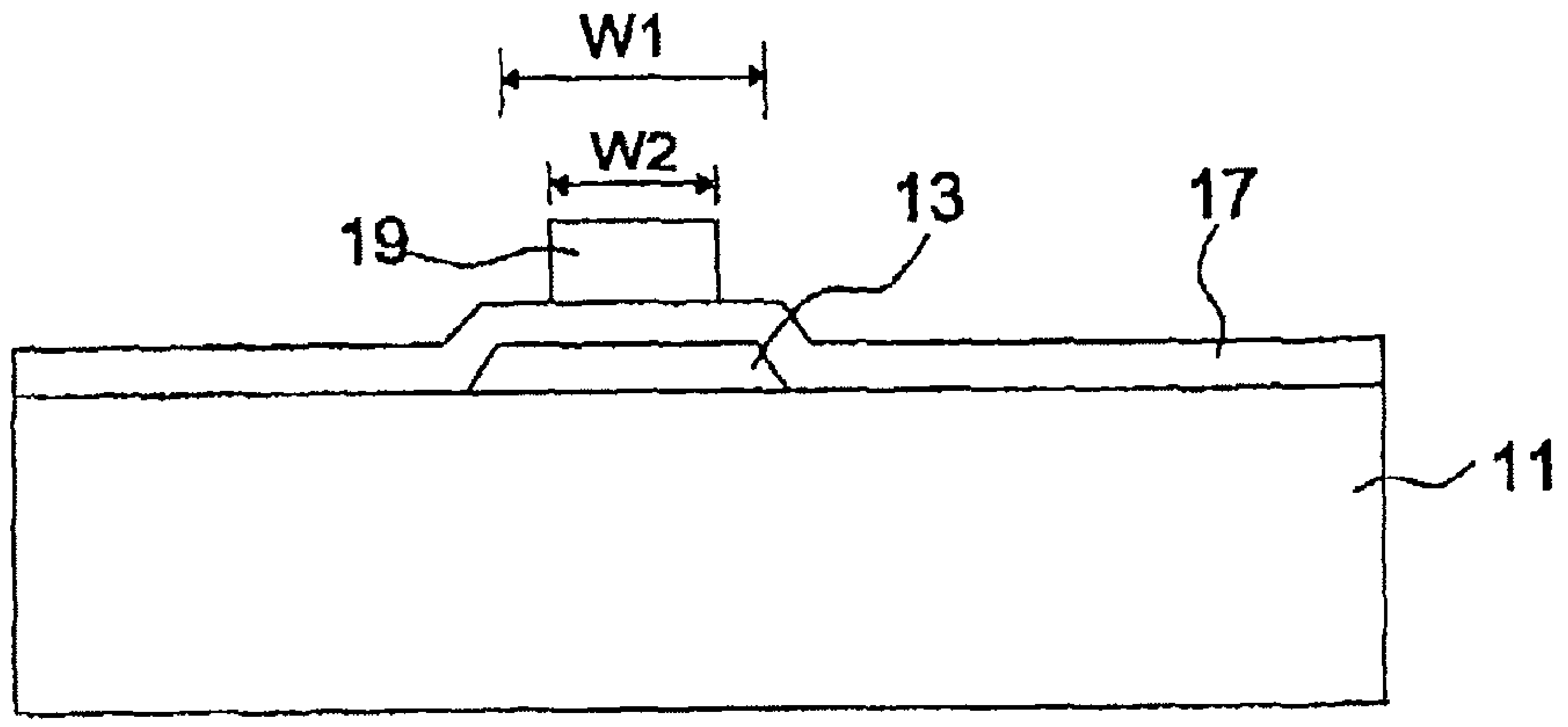


FIG.1C

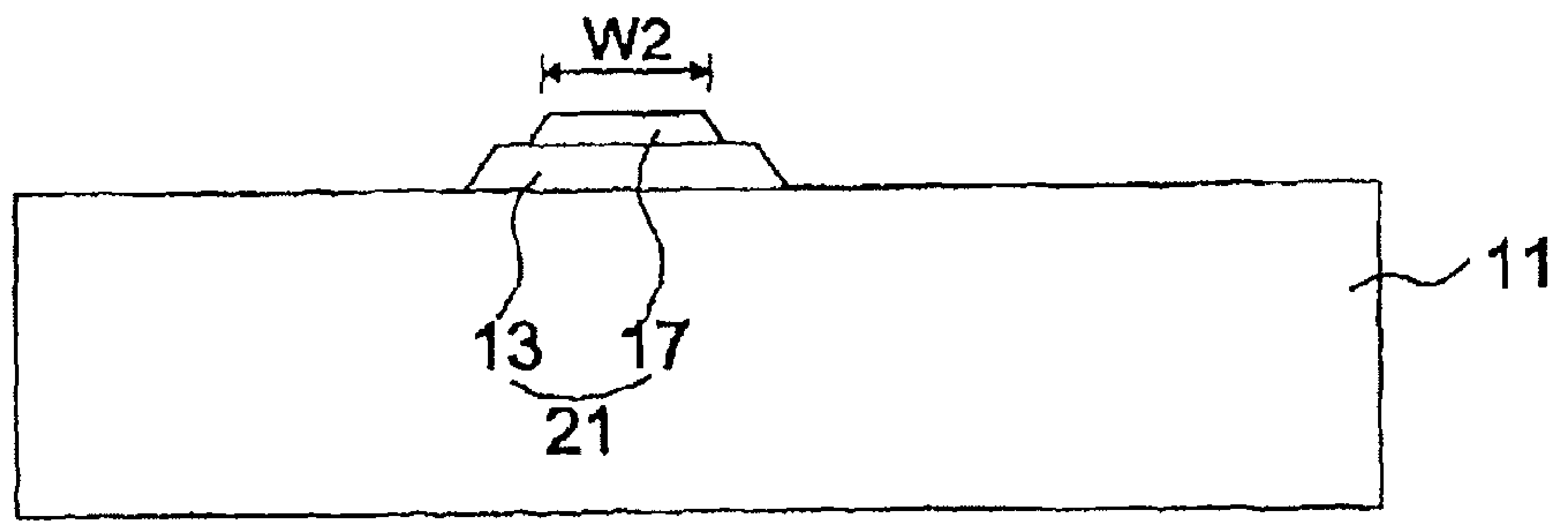


FIG.1D

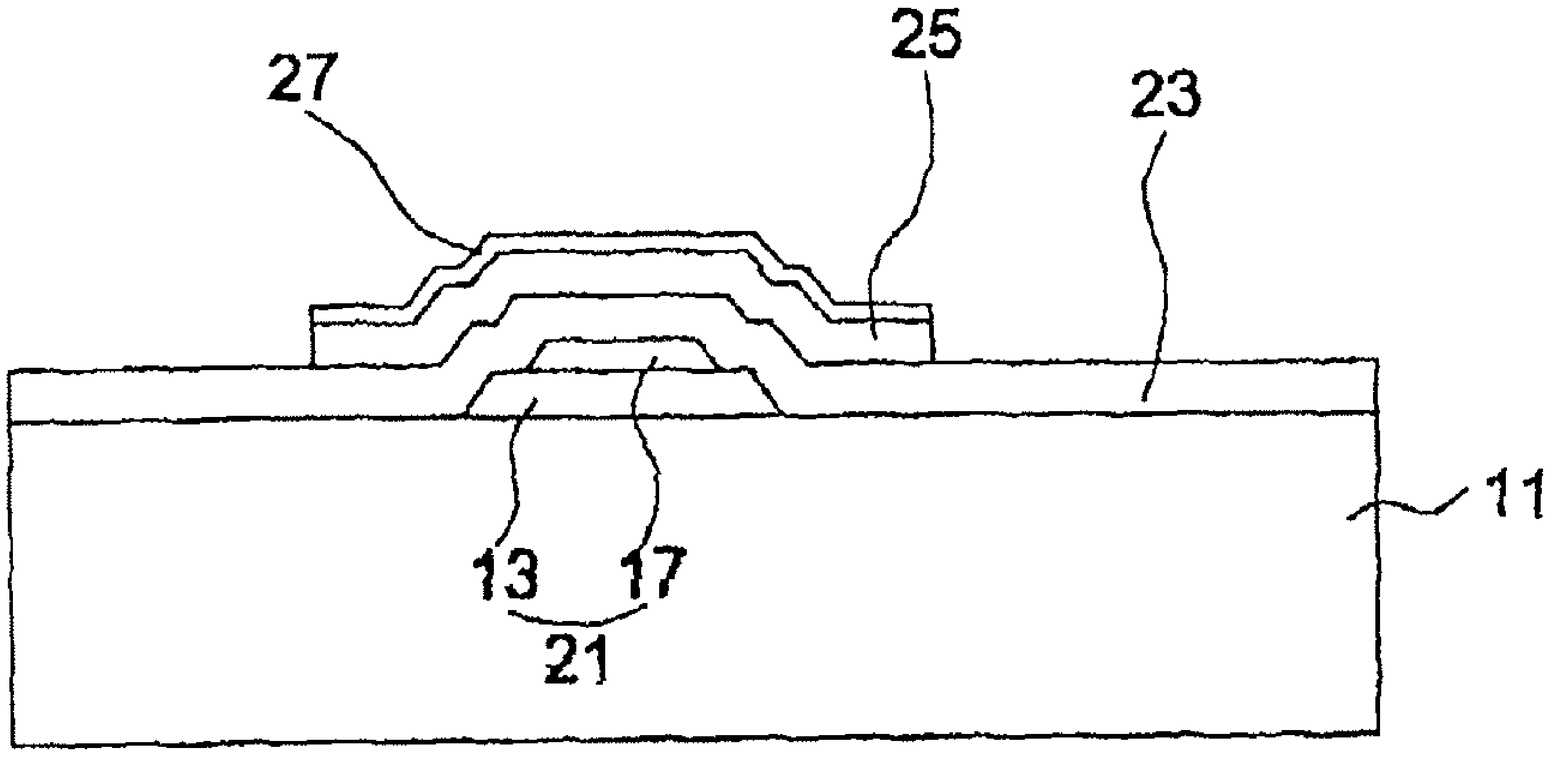


FIG.1E

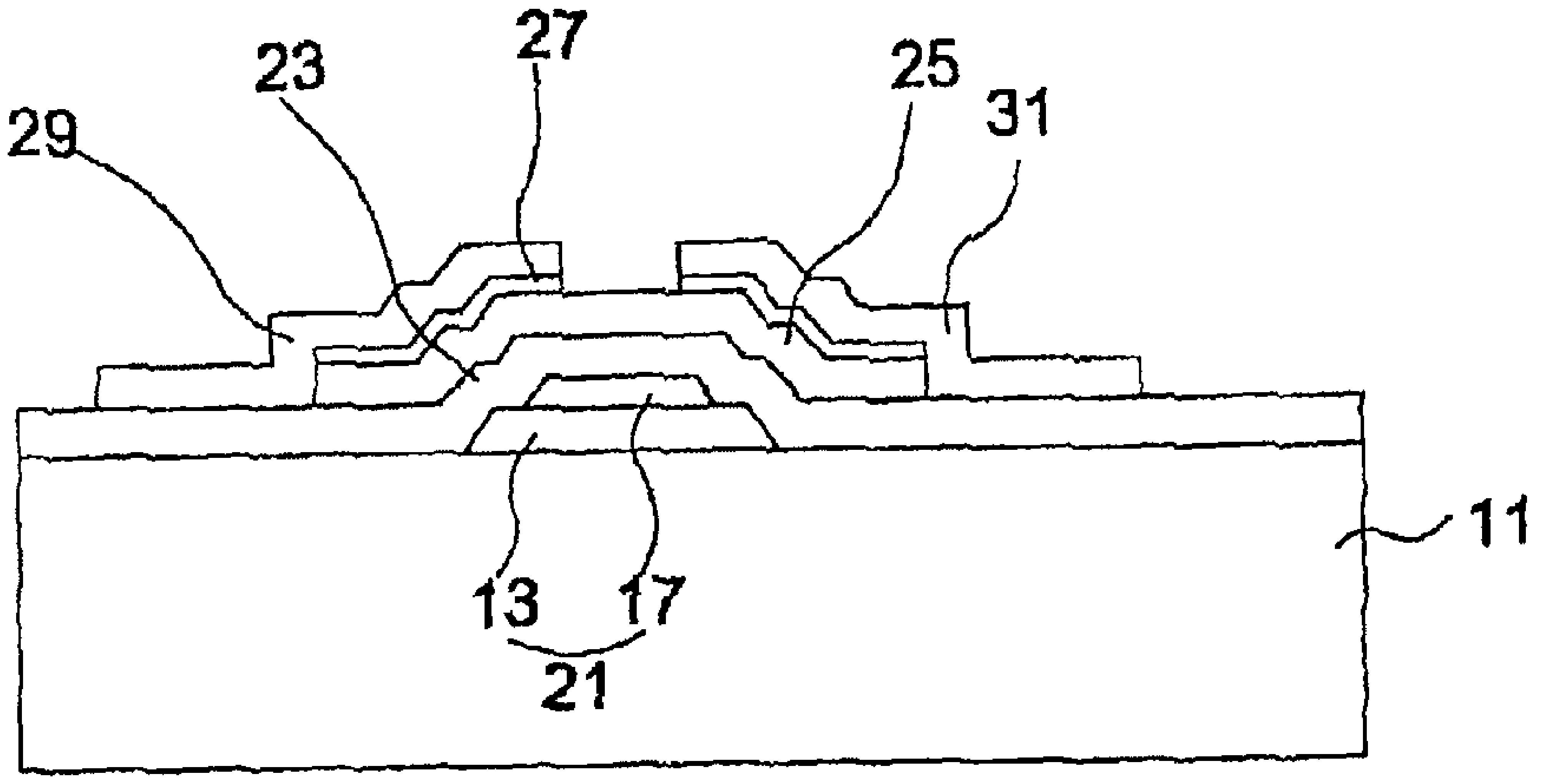


FIG.1F

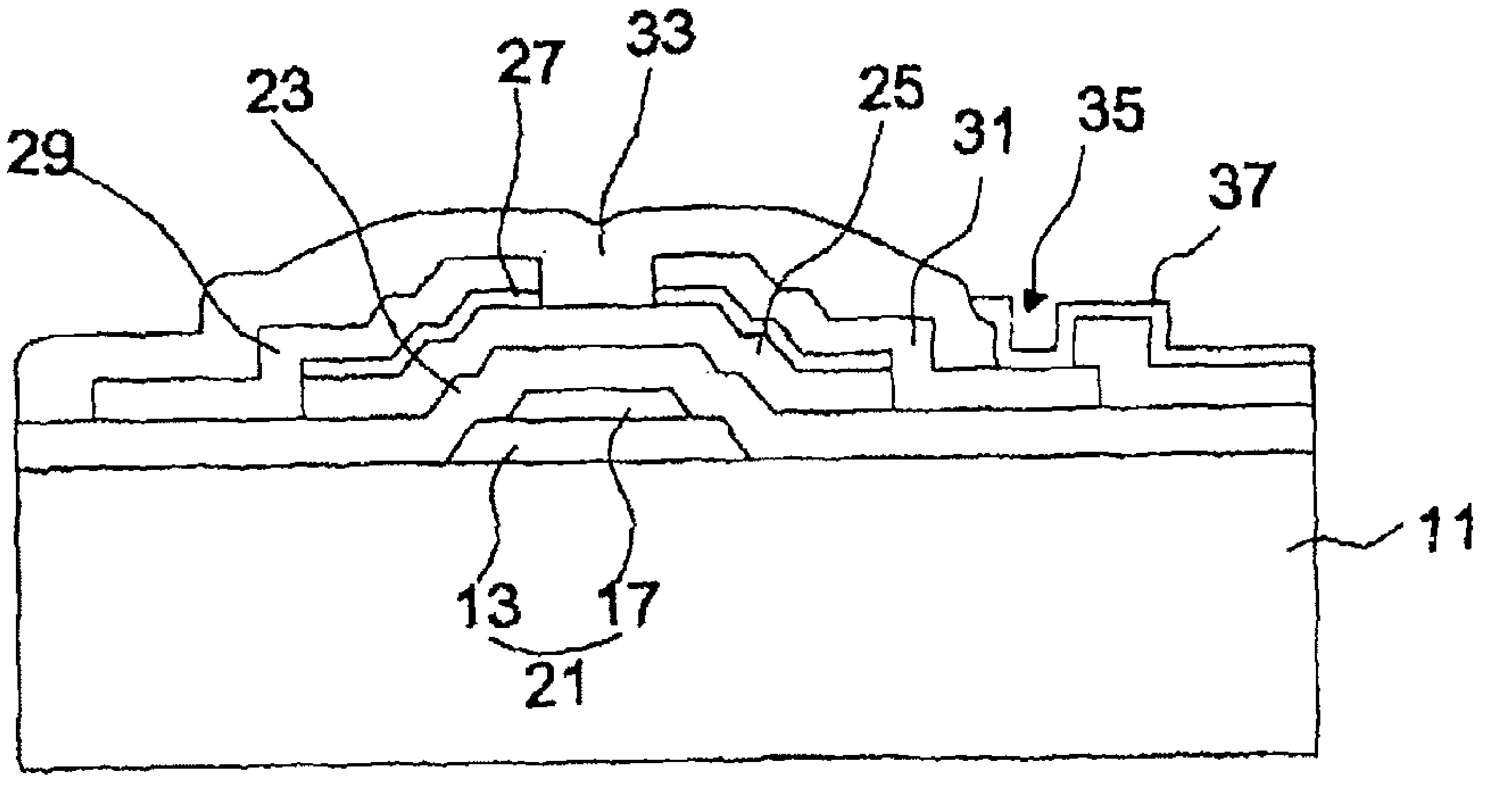


FIG.2

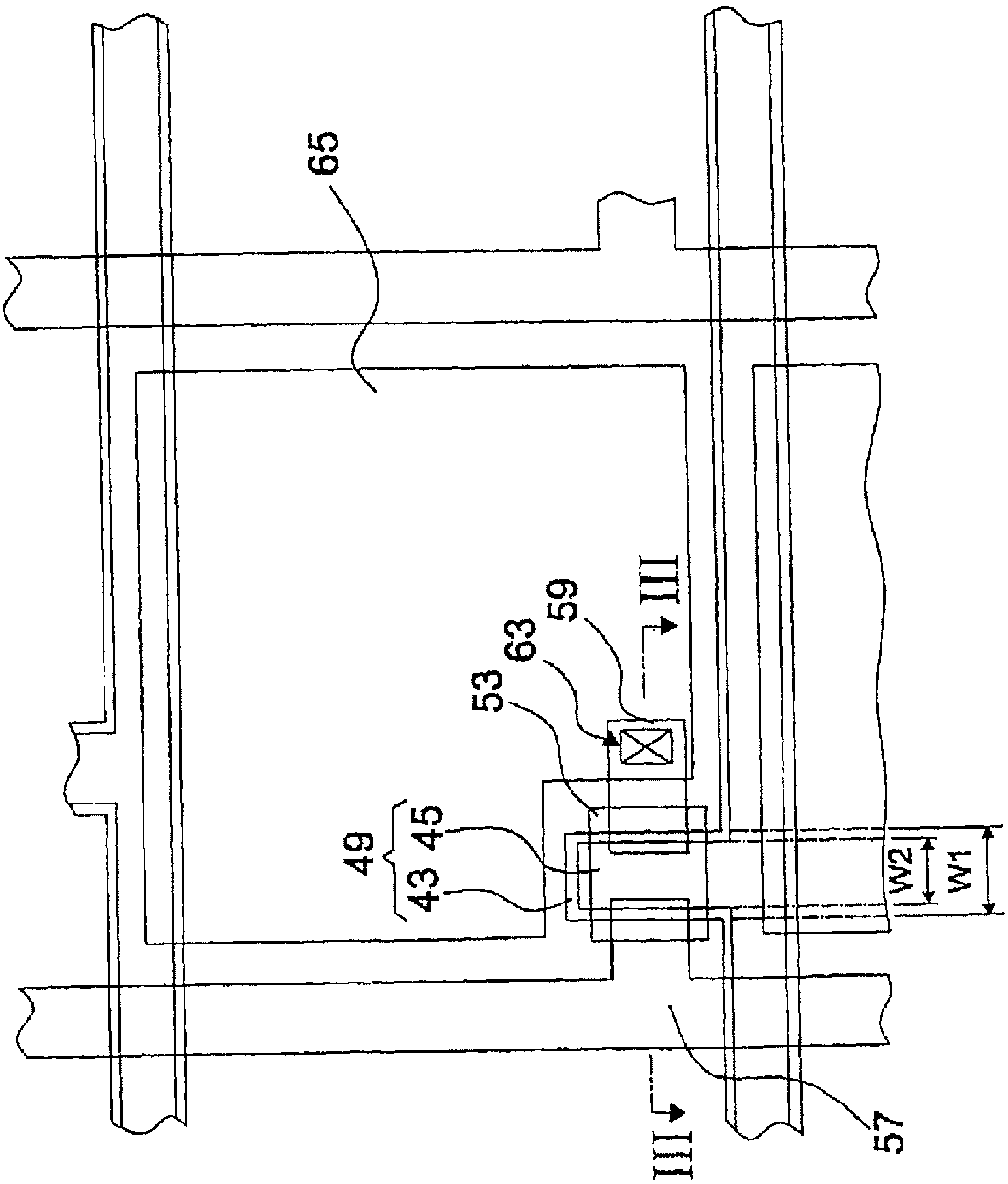


FIG.3

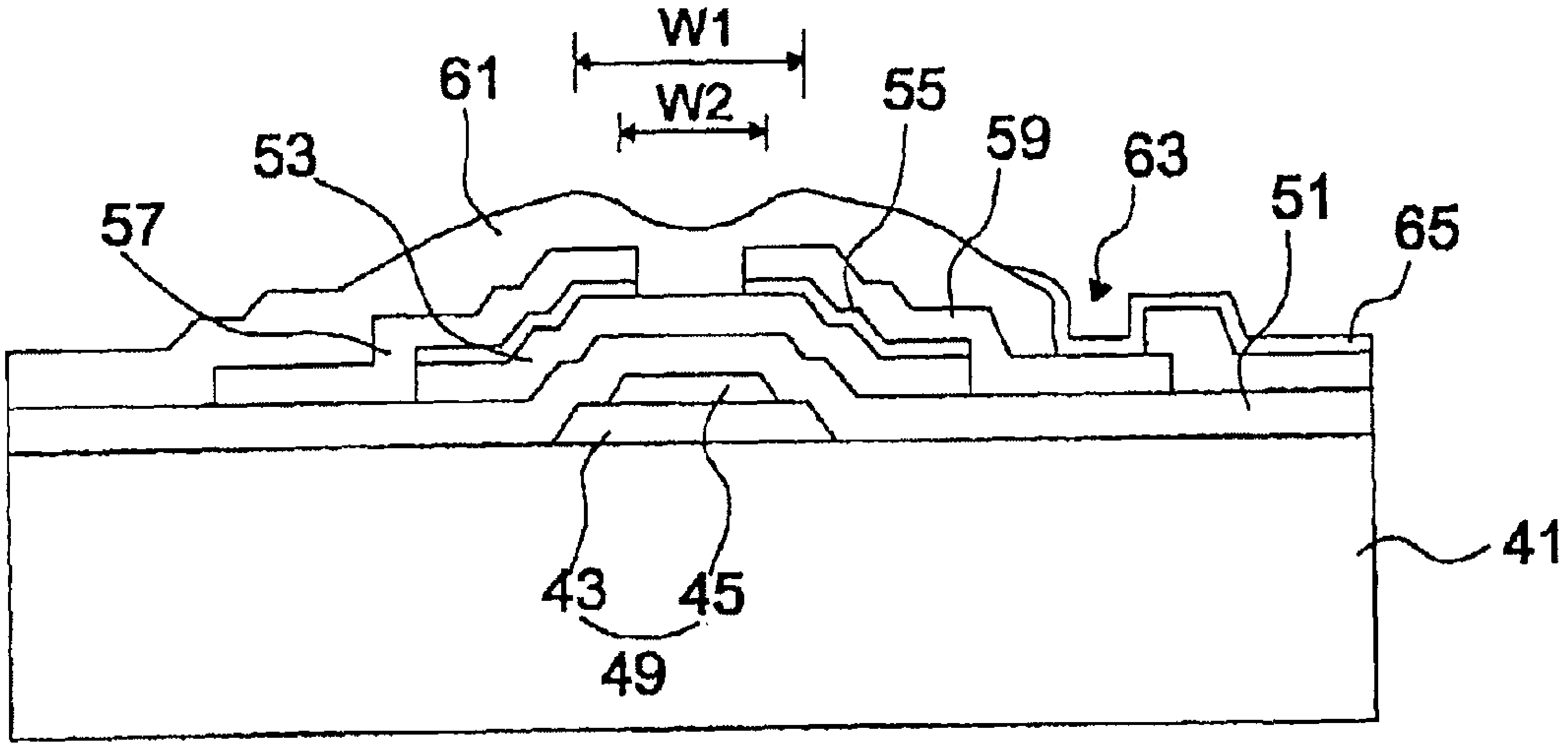


FIG.4A

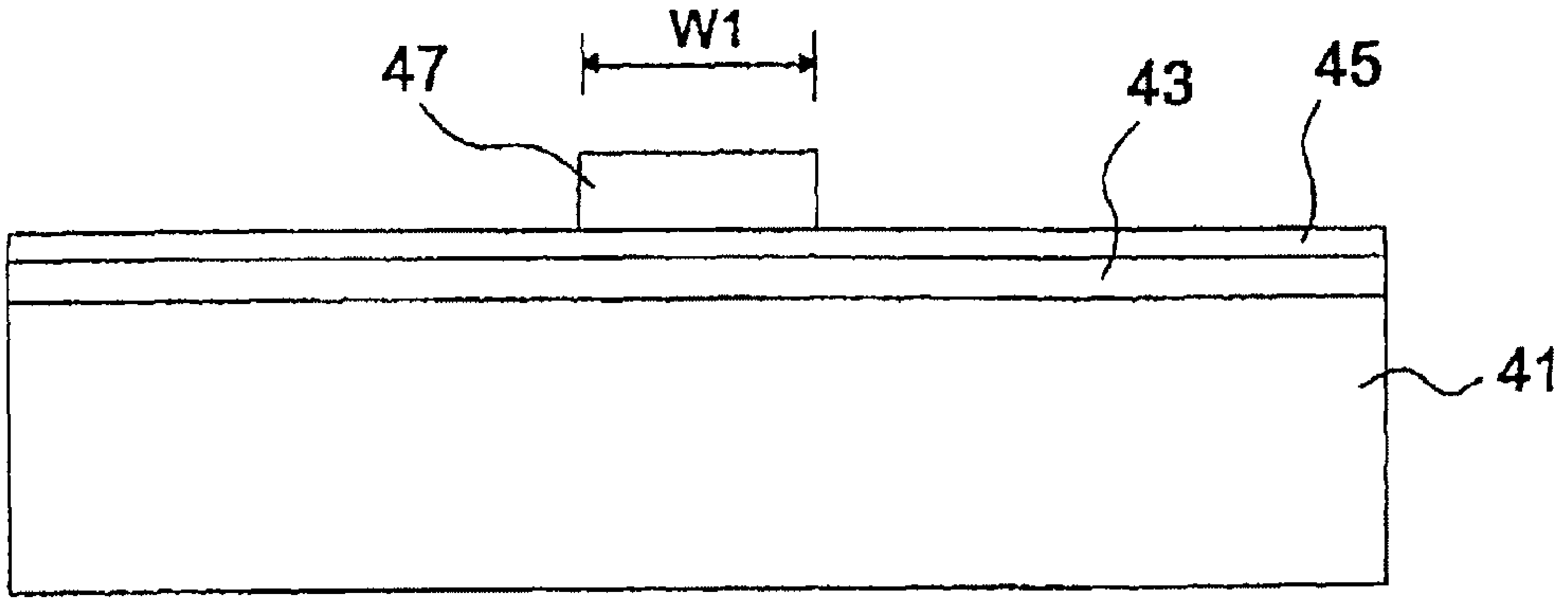


FIG.4B

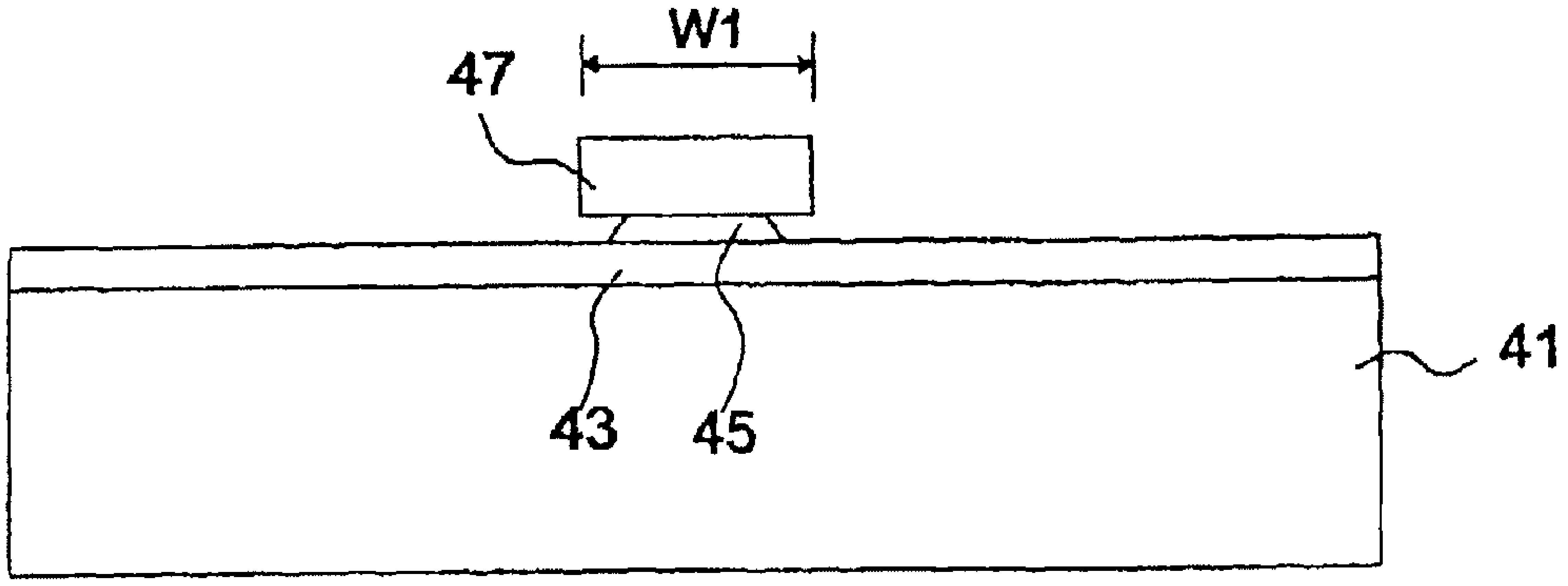


FIG.4C

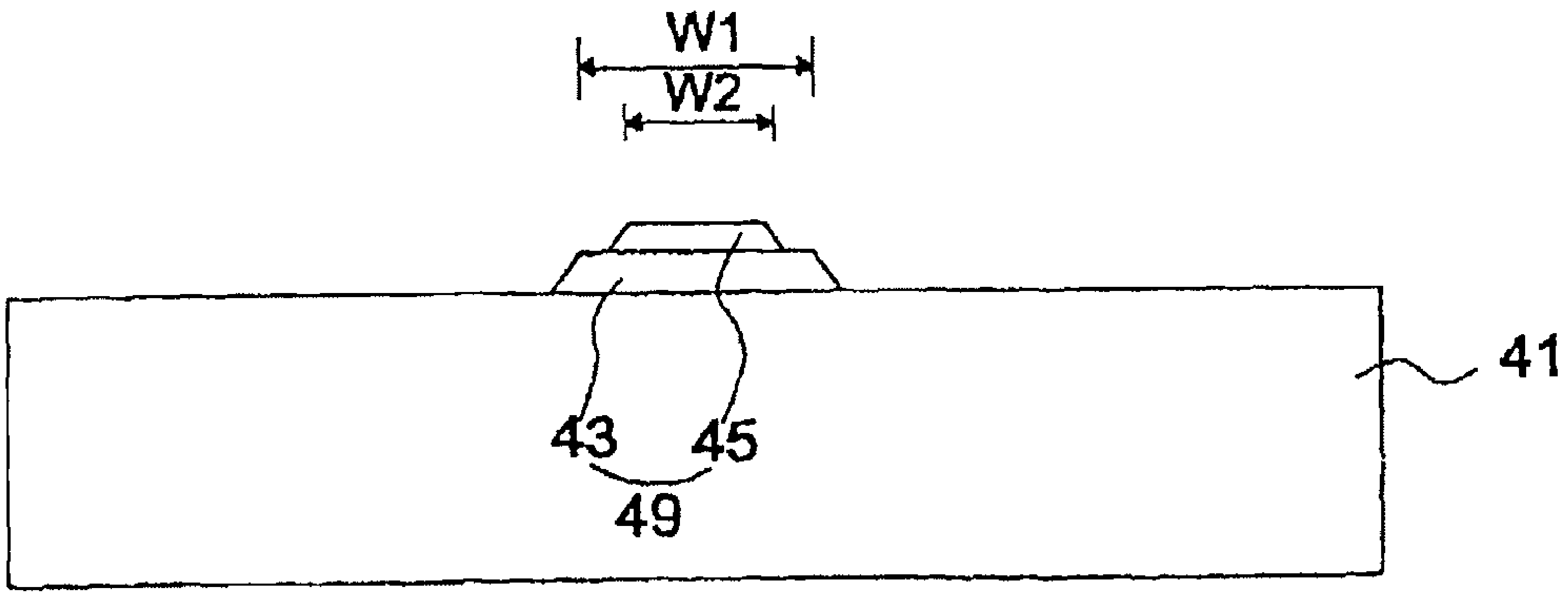


FIG.4D

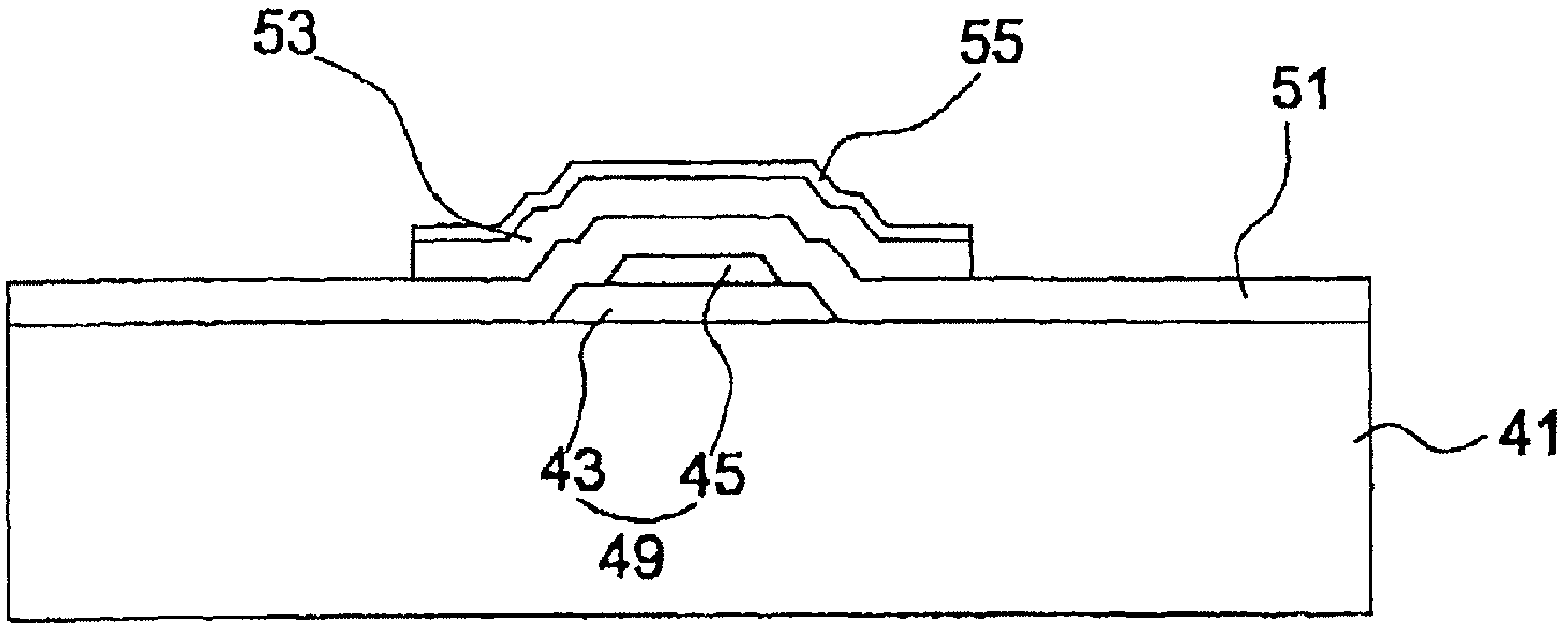


FIG.4E

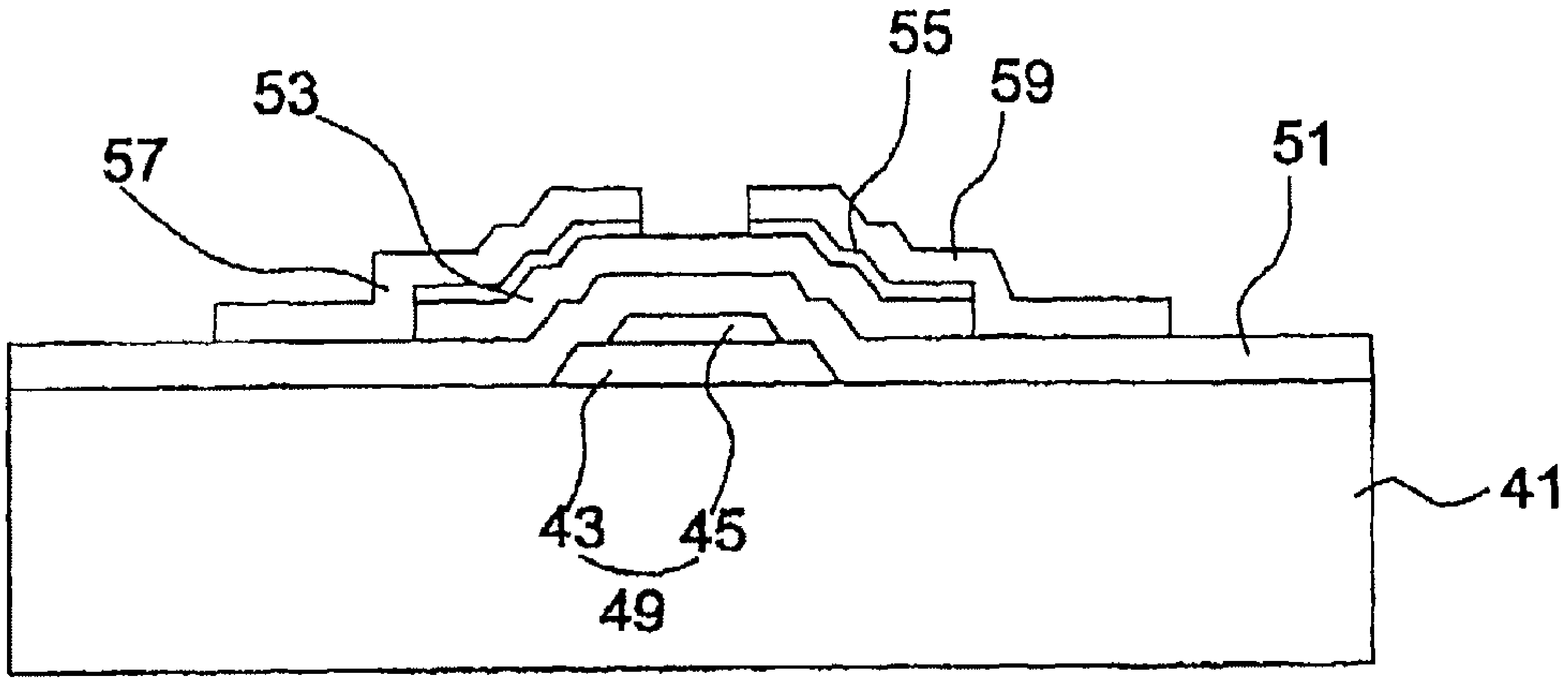
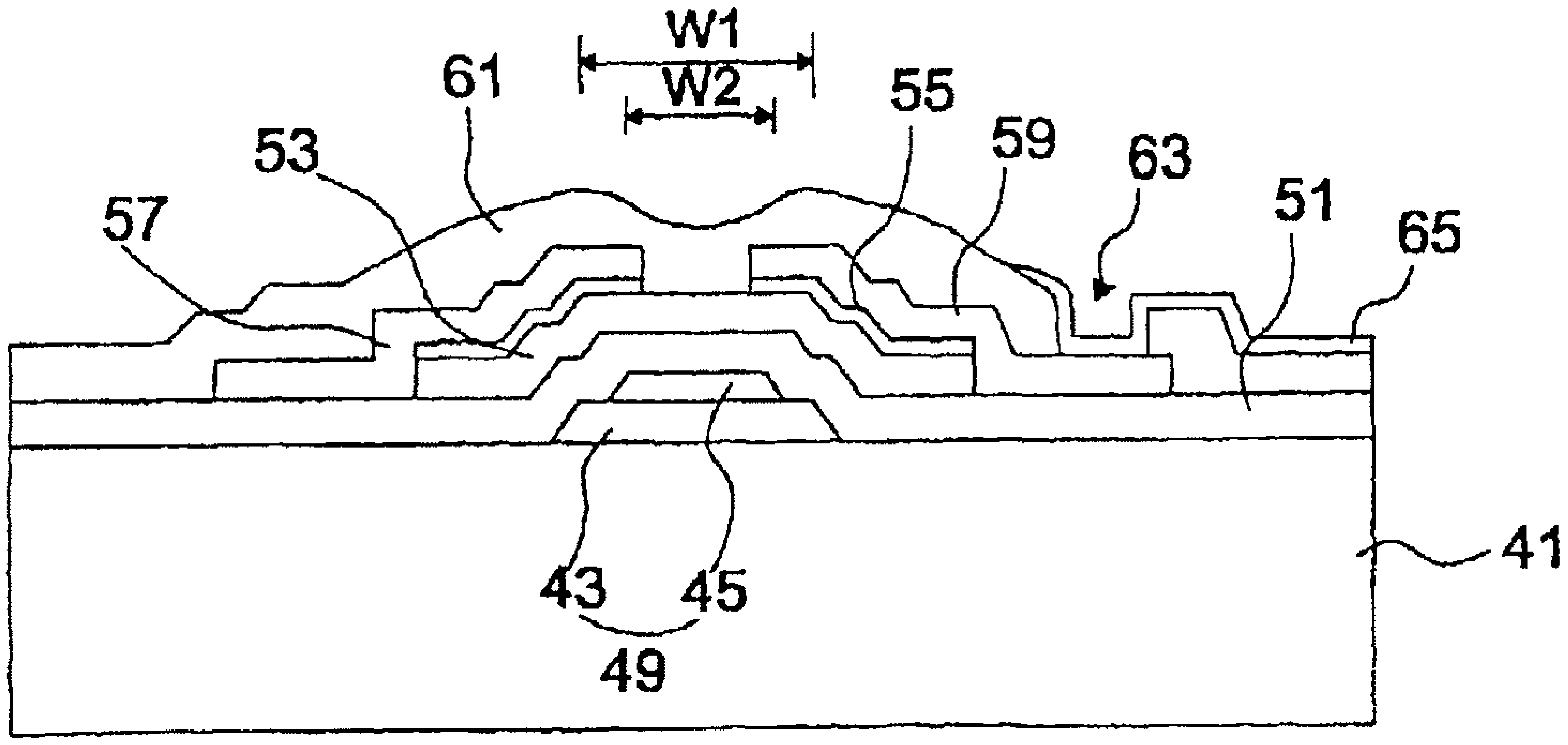


FIG.4F



THIN-FILM TRANSISTOR AND METHOD OF MAKING SAME

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue; a claim printed with strikethrough indicates that the claim was canceled, disclaimed, or held invalid by a prior post-patent action or proceeding.

This application is a divisional of application Ser. No. 10/154,955, filed on May 28, 2002, now U.S. Pat. No. 6,548,829 which is a continuation of abandoned application Ser. No. 09/940,504, filed on Aug. 29, 2001, which is a divisional application under 37 C.F.R. §1.53(b) of patented prior application Ser. No. 09/243,556 (U.S. Pat. No. 6,340,610 B1) filed on Feb. 2, 1999 (Issued on Jan. 22, 2002):, which is divisional application under 37 C.F.R. §1.53(b) of patented prior application Ser. No. 08/918,119 (U.S. Pat. No. 5,905,274) filed on Aug. 27, 1997 (Issued on May 18, 1999) the entire contents of which are hereby incorporated by reference and for which priority is claimed under 35 U.S.C. §120; and this application claims priority of Application No. 97-07010 filed in Korea on Mar. 4, 1997 under 35 U.S.C. §119.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a thin-film transistor of a liquid crystal display and, more particularly, to a thin-film transistor having a gate including a double-layered metal structure and a method of making such a double-layered metal gate.

2. Discussion of Related Art

An LCD (Liquid Crystal Display) includes a switching device as a driving element, and a pixel-arranged matrix structure having transparent or light-reflecting pixel electrodes as its basic units. The switching device is a thin-film transistor having gate, source and drain regions.

The gate of the thin-film transistor is made of aluminum to reduce its wiring resistance, but an aluminum gate may cause defects such as hillock.

A double-layered metal gate, i.e., molybdenum-coated aluminum gate is considered as a substitute for the aluminum gate to overcome the problem of the hillock.

To fabricate a double-layered gate, metals such as aluminum and molybdenum are sequentially deposited, followed by a patterning process carried out via photolithography to form resulting metal films which have the same width. Although the double-layered gate is desirable to overcome the problem of hillock, the resulting deposited metal films forming the double-layered gate are so thick that a severe single step is created by a thickness difference between the metal films and a substrate, thereby causing a single step difference between the substrate and the double-layered gate which deteriorates the step coverage of a later formed gate oxide layer. The source and drain regions formed on the gate oxide layer may have disconnections between areas of the source and drain regions which are overlapped and non-overlapped with the gate, or electrically exhibit short circuits as a result of contact with the gate.

According to another method of forming the gate, each of the metal layers of Al and Mo form a double step difference with the substrate so as to improve the step coverage of the gate oxide layer.

FIGS. **1**A through **1**F are diagrams illustrating the process for fabricating a thin-film transistor of a method which is related to the invention described and claimed in the present application. The method shown in FIGS. **1**A-**1**F is not believed to be published prior art but is merely a recently discovered method related to the invention described and claimed in the present application.

Referring to FIG. **1**A, aluminum is deposited on a substrate **11** to form a first metal layer **13**. A first photoresist **15** is deposited on the first metal layer **13**. The first photoresist **15** is exposed and developed so as to have a certain width w1 extending along the first metal layer **13**.

Referring to FIG. **1**B, the first metal layer **13** is patterned via wet etching using the first photoresist **15** as a mask so that the first metal layer **13** has a certain width w1. After the first photoresist **15** is removed, a second metal layer **17** is formed by depositing Mo, Ta, or Co on the substrate **11** so as to cover the first metal layer **13**. A second photoresist **19** is then deposited on the second metal layer **17**. The second photoresist **19** is exposed and developed so as to have a certain width w2 extending along the second metal layer **17** and located above the first metal layer **13**.

Referring to FIG. **1**C, the second metal layer **17** is patterned via a wet etching process using the second photoresist **19** as a mask such that the second metal layer **17** has a certain width w2 which is narrower than the width w1 of the first metal layer **13**. After formation of the gate **21**, the second photoresist **19** is removed.

Thus, the patterned first and second metal layers **13** and **17** form a gate **21** having a double-layered metal structure that provides double step difference between the double-layered metal gate structure **21** and the substrate **11**. The formation of the gate **21** as described above and shown in FIGS. **1**A-**1**F requires the use of two photoresists **15**, **19** and two photoresist steps.

In the gate **21**, shown in FIG. **1**C, the second metal layer **17** is preferably centrally located on the first metal layer **13**. Although there is no specific information available regarding a relationship of w1 to w2 of this related art method, based on their understanding of this related method resulting in the structure shown in FIG. **1**C, the inventors of the invention described and claimed in the present application assume that the width difference $w1-w2$ between the first and second metal layers **13** and **17** is larger than or equal to 4 μm, that is, $w1-w2 \geq 4$ μm.

Referring to FIG. **1**D, a first insulating layer **23** is formed by depositing silicon oxide SiO_2 or silicon nitride Si_3N_4 as a single-layered or double-layered structure on the gate **21** and substrate **11**. Semiconductor and ohmic contact layers **25** and **27** are formed by sequentially depositing undoped polycrystalline silicon and heavily doped silicon on the first insulating layer **23**. The semiconductor and ohmic contact layers **25** and **27** are patterned to expose the first insulating layer **23** by photolithography.

Referring to FIG. **1**E, conductive metal such as aluminum is laminated on the insulating and ohmic contact layers **23** and **27**. The conductive metal is patterned by photolithography so as to form source electrode **29** and a drain electrode **31**. A portion of the ohmic contact layer **27** exposed between the source and drain electrodes **29** and **31** is etched by using the source and drain electrodes **29** and **31** as masks.

Referring to FIG. **1**F, silicon oxide or silicon nitride is deposited on the entire surface of the structure to form a second insulating layer **33**. The second insulating layer **33** is etched to expose a designated portion of the drain electrode **31**, thus forming a contact hole **35**. By depositing transparent and conductive material on the second insulating layer **33** and patterning it via photolithography, a pixel electrode **37** is formed so as to be electrically connected to the drain electrode **31** through the contact hole **35**.

According to the method of fabricating a thin-film transistor as described above and shown in FIGS. **1**A-**1**F, respective first and second metal layers are formed through photolithography using different masks so as to form the gate with a double-layered metal structure, resulting in double step differences between the gate and substrate.

As a result of the double step difference between the gate **21** and the substrate **11** shown in FIG. **1**C, a hillock often occurs on both side portions of the first metal layer **13** which have no portion of the second metal layer **17** deposited thereon when the first metal layer **13** is wider than the second metal layer **17** as in FIG. **1**C. Another problem with this related art method is that the process for forming a gate is complex and requires two photoresists **15**, **19** and two steps of deposition and photolithography. As a result, the contact resistance between the first and second metal layers may be increased.

Another related art method of forming a double metal layer gate structure is described in "Low Cost, High Quality TFT-LCD Process", SOCIETY FOR INFORMATION DISPLAY EURO DISPLAY 96, Proceedings of the 16th International Display Research Conference, Birmingham, England, Oct. 1, 1996, pages 591-594. One page 592 of this publication, a method of forming a double metal gate structure includes the process of depositing two metal layers first and then patterning the two metal layer to thereby eliminate an additional photoresist step. However, with this method, process difficulties during the one step photoresist process for forming the double metal layer gate resulted in the top layer being wider than the bottom layer causing an overhang condition in which the top layer overhangs the bottom layer. This difficulty may result in poor step coverage and disconnection. This problem was solved by using a three-step etching process in which the photoresist had to be baked before each of the three etching steps to avoid lift-off or removal of the photoresist during etching. This three-step etching process and required baking of the photoresist significantly increases the complexity and steps of the gate forming method.

SUMMARY OF THE INVENTION

To overcome the problems discussed above, the preferred embodiments of the present invention provide a thin-film transistor which prevents a hillock and deterioration of step coverage of a later formed gate oxide layer on a double metal layer gate.

The preferred embodiments of the present invention also provide a method of fabricating a thin-film transistor that simplifies the process for forming a double metal layer gate.

The preferred embodiments of the present invention further provide a method of fabricating a thin-film transistor that reduces the contact resistance between the first and second metal layers constituting a gate.

Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof, as well as, the appended drawings.

To achieve these and other advantages and in accordance with the purpose of the preferred embodiments of the present invention, as embodied and broadly described, a thin-film transistor preferably comprises a substrate, and a gate including a double-layered structure of first and second metal layers disposed on the substrate, the first metal layer being wider than the second metal layer by about 1 to 4 μm, and a method of making such a thin-film transistor preferably comprises the steps of: depositing a first metal layer on a substrate, depositing a second metal layer directly on the first metal layer; forming a photoresist having a desired width on the second metal layer; patterning the second metal layer via an isotropic etching using the photoresist as a mask; patterning the first metal layer via an anisotropic etching using the photoresist as a mask, the first metal layer being etched to have a desired width, thus forming a gate having a laminated structure of the first and second layers; and removing the photoresist.

These and other elements, features, and advantages of the preferred embodiments of the present invention will be apparent from the following detailed description of the preferred embodiments of the present invention, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate preferred embodiments of the invention and together with the description serve to explain the principles of the invention, in which:

FIGS. **1**A through **1**F are diagrams illustrating a process for fabricating a thin-film transistor according to a method of the related art;

FIG. **2** is a top view of a thin-film transistor according to a preferred embodiment of the present invention;

FIG. **3** is a cross-sectional view taken along line III-III of FIG. **2**; and

FIGS. **4**A through **4**F are diagrams illustrating a process for fabricating a thin-film transistor of preferred embodiments of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Reference will now be made in detail to preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

FIG. **2** is a top view of a thin-film transistor according to a preferred embodiment of the present invention. FIG. **3** is a cross-sectional view taken along line III-III of FIG. **2**.

The thin-film transistor comprises a gate **49** having a double-layered structure of a first metal layer **43**, a second metal layer **45** disposed on a substrate **41**, a first insulating layer **51**, a second insulating layers **61**, a semiconductor layer **53**, an ohmic contact layer **55**, a source electrode **57**, a drain electrode **59**, and a pixel electrode **65**.

The gate **49** has a double-layered structure including the first and second metal layers **43** and **45** disposed on the substrate **41**. The first metal layer **43** is preferably formed from a conductive metal such as Al, Cu, or Au deposited to have a certain width w1. The second metal layer **45** is preferably formed from a refractory metal such as Mo, Ta, or Co deposited to have a certain width w2.

The present inventors have discovered that a relationship between the width of the first metal layer and the width of the second metal layer of a double metal layer gate electrode is critical to preventing deterioration of step coverage of a later formed gate oxide layer in such a structure having a double step difference between the substrate and the gate. More specifically, the present inventors determined that a structure wherein the first metal layer **43** is wider than the second metal layer **45** by about 1 to 4 μm, for example, 1 μm<w1−w2<4 μm, provides maximum prevention of deterioration of step coverage of a later formed gate oxide layer in such a structure having a double step difference between the substrate and the gate.

To achieve the best results, the second metal layer **45** is preferably positioned substantially in the middle of the first metal layer **45**, so that both side portions of the first metal layer **43** which have no portion of the second metal layer **45** disposed thereon have substantially the same width as each other. The width of each of the side portions is preferably larger than about 0.5 μm but less than about 2 μm.

The first insulating layer **51** is preferably formed by depositing single layer of silicon oxide SiO_2 or silicon nitride Si_3N_4 on the substrate including the gate **49**.

The semiconductor and ohmic contact layers **53** and **55** are formed on the portion of the first insulating layer **51** corresponding to the gate **49** by sequentially depositing undoped amorphous silicon and heavily doped amorphous silicon and patterning the two silicon layers. The semiconductor layer **53** is used as the active region of an element, thus forming a channel by means of a voltage applied to the gate **49**. The ohmic contact layer **55** provides an ohmic contact between the semiconductor layer **53** and the source and drain electrodes **57** and **59**. The ohmic contact layer **55** is not formed in the portion that becomes the channel of the semiconductor layer **53**.

The source and drain electrodes **57** and **59** are in contact with the ohmic contact layer **55**, and each electrode **57**, **59** extends to a designated portion on the first insulating layer **51**.

The second insulating layer **61** is formed by depositing insulating material such as silicon oxide SiO_2 silicon nitride Si_3N_4 to cover the source and drain electrodes **57** and **59** and the first insulating layer **51**. The second insulating layer **61** on the drain electrode **59** is removed to form a contact hole **63**. The pixel electrode **65** is formed from transparent and conductive material such as ITO (Indium Tin Oxide) or Tin oxide SnO_2, so that it is connected to the drain electrode **59** through the contact hole **63**.

In the first and second metal layers **43** and **45** constituting the gate **49**, each side portion of the first metal layer **43** having no portion of the second metal layer **45** thereon has a width that is preferably larger than about 0.5 μm and less than about 2 μm. Because the first metal layer **43** is wider than the second metal layer **45** by about 1.0 μm to 4.0 μm, double step differences determined according to the relationship between the width of the first metal layer and the width of the second metal layer are formed between the gate **49** and substrate **41**. The double step differences determined according to the novel features of the preferred embodiments of the present invention prevent deterioration of the coverage of the first insulating layer **51** which deterioration occurs in prior art devices. The hillock in the first metal layer **43** is also avoidable because the width difference between the first and second metal layers **43** and **45** is between about 1 μm to 4 μm.

FIGS. **4**A through **4**F are diagrams illustrating the process for fabricating the thin-film transistor of the preferred embodiments of the present invention.

Referring to FIG. **4**A, metal such as Al, Cu, or Au is deposited on a substrate so as to form a first metal layer **43**. A second metal layer **45** is formed from Mo, Ta, or Co and deposited on the first metal layer **43** without performing a masking step between the step of depositing the first metal layer and the step of depositing the second metal layer. The first and second metal layers **43** and **45** are sequentially deposited so as to preferably have a thickness as large as about 500-4000 Angstroms and 500-2000 Angstroms, respectively, by means of sputtering or chemical vapor deposition (hereinafter, referred to as CVD) without breaking a vacuum state. As a result, the contact resistance between the first and second metal layers **43** and **45** is reduced.

According to the preferred embodiments of the present invention, a single photoresist step is used to pattern both the first metal layer **43** and the second metal layer **45** simultaneously. In the single photoresist step, a photoresist **47** is deposited on the second metal layer **45** and then the photoresist **47** is patterned through exposure and development to have the width w1 on a designated portion of the second metal layer **45**.

Referring to FIG. **4**B, the second metal layer **45** is patterned with an etching solution preferably prepared with a mixture of phosphoric acid H_3PO_4, acetic acid CH_3COOH and nitric acid HNO_3, by means of a wet etching using the photoresist **47** as a mask. Because the portion of the second metal layer **45** covered with the photoresist **47**, as well as, exposed side portions of the second metal layer **45** are isotropically etched, the second metal layer **45** is preferably patterned to have the width w2 which is narrower than the width w1 of the photoresist **47** which is the same as the width w1 of the first metal layer **43**, that is, about 1 μm<w1−w2<4 μm. Each side portion of the second metal layer **45** preferably has a width larger than about 0.5 μm and less than about 2 μm. That is, the two side portions of the second metal layer **45** covered with the photoresist **47** are preferably etched to have substantially the same width as each other. The lateral surfaces of the second metal layer **45** are preferably etched to have a substantially rectangular or inclined shape.

Referring to FIG. **4**C, the first metal layer **43** is patterned via dry etching having anisotropic etching characteristic such as reactive ion etching (hereinafter, referred to as RIE) by using the photoresist **47** as a mask. When etching the first metal layer **43** other than the portion of the layer **43** covered with the photoresist **47**, the first metal layer **43** preferably has the same width w1 of the photoresist **47**. Thus, patterning of the first and second metal layers **43**, **45**, respectively, only requires two etching steps and does not require baking of the photoresist before each step of etching. Also, the relation between the first and second metal layers **43** and **45** also may be represented by about 1 μm<w1−w2<4 μm.

The first and second metal layers **43** and **45** resulting form the single photoresist step process described above form a gate **49** having a double-layered metal structure. The gate **49** has the second metal layer **45** positioned substantially in the middle of the first metal layer **43** so that the each side portion of the first metal layer **43** having no second metal layer **45** thereon is wider than about 0.5 μm but narrower than about 2 μm. The photoresist **47** remaining on the second metal layer **45** is removed after the two etching steps are completed.

Referring to FIG. **4**D, a first insulating layer **51** is formed by depositing a single layer or double layers of silicon oxide SiO_2 or silicon nitride Si_3N_4 on the gate **49** and substrate **41** by CVD. Because each side portion of the first metal layer **43** having no second metal layer **45** thereon is wider than 0.5 μm, double step differences formed between the substrate and gate can prevent the coverage of the first insulating layer **51** from being deteriorated as in prior art devices. The hillock in the first metal layer **43** is also avoidable because a width of a portion of the first metal layer **43** which is exposed is less than about 2 μm.

Amorphous silicon which is undoped and heavily doped amorphous silicon are sequentially deposited on the first insulating layer **41** by CVD, thus forming semiconductor and ohmic contact layers **53** and **55**. The ohmic contact and semiconductor layers **55** and **53** are patterned by means of photolithography to expose the first insulating layer **51**.

Referring to FIG. **4**E, conductive metal such as Al or Cr is laminated on the insulating and ohmic contact layers **51** and **55** and patterned by photolithography to form source and drain electrodes **57** and **59**. The ohmic contact layer **55** exposed between the source and drain electrodes **57** and **59** is etched by using the source drain electrodes **57** and **59** as masks.

Referring to FIG. **4**F, a second insulating layer **61** is formed by depositing insulating material such as silicon oxide or silicon nitride by CVD on the entire surface of the above structure. The second insulating layer is removed by photolithography to expose a designated portion of the drain electrode **59** and thus form a contact hole **63**. Once transparent and conductive material such as ITO (Indium Tin Oxide) or Tin oxide SnO_2 is deposited on the second insulating layer **61** via sputtering and patterned by photolithography, a pixel electrode **65** is formed so that it is electrically connected to the drain electrode **59** through the contact hole **63**.

In another preferred embodiment of the present invention, the first and second metal layers **43** and **45** are first etched by means of a dry etching having anisotropic etching characteristic such as RIE by using the photoresist **47** as a mask. The gate **49** is formed by etching the second metal layer **45** under the photoresist **47** with an etching solution prepared with a mixture of phosphoric acid H_3PO_4, acetic acid CH_3COOH and nitric acid HNO_3.

In still another preferred embodiment of the present invention, the gate **49** is formed through a single etching step process for etching the first and second metal layers **43** and **45** simultaneously and via a single etching step, where the second metal layer **45** is etched more quickly than the first metal layer **43** with an etching solution prepared with a mixture of phosphoric acid H_3PO_4, acetic acid CH_3COOH and nitric acid HNO_3. Because of the etching material and metals used for the first and second metal layers of the gate, only a single etching step is required. Despite the fact that a single etching step is used, it is still possible to obtain the relationship between the widths w1 and w2 of the first and second metal layers described above. In this process, the first and second metal layers forming the gate **49** are formed and patterned with a single photo resist step as described above and a single etching step.

As described above, in the preferred embodiments of the present invention, the first and second metal layers are sequentially deposited on the substrate without performing a masking step between the step of depositing the first metal layer and the second metal layer, followed by forming a photoresist that covers a designated portion of the second metal layer. In one preferred embodiment, the second metal layer is wet etched by using the photoresist as a mask but the first metal layer is dry etched. As a result, the double-metal gate is formed. In another preferred embodiment, a single etching step is used to form the double-metal gate wherein both the first metal layer and the second metal layer are wet etched, but the difference in etching rates of the first and second metal layers produces different etching affects which result in the desired double-step structure.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. A method of making a thin-film transistor, comprising the steps of:

depositing a first metal layer on a substrate;

depositing a second metal layer on the first metal layer without forming a photoresist on the first metal layer beforehand;

forming a photoresist having a predetermined width on the second metal layer;

anisotropically etching the first and second metal layers so such that the first metal layer and the second metal layer have the same width of the photoresist by using the photoresist as a mask,

isotropically etching the second metal layer such that the second metal layer is narrower than the first metal layer by about 1 μm to about 4 μm by using the photoresist as a mask, thus forming a gate having a double-layered structure including the first and second metal layers; and

removing the photoresist.

2. The method of making a thin-film transistor as claimed in claim **1**, further comprising the steps of:

forming a first insulating layer on the substrate including the gate;

forming a semiconductor layer and an ohmic contact layer on a portion of the first insulating layer at a location corresponding to the gate;

forming a source electrode and drain electrode extending onto the first insulating layer on two sides of the ohmic contact layer, and removing a portion of the ohmic contact layer exposed between the source and drain electrodes; and

forming a second insulating layer covering the semiconductor layer, the source electrode, the drain electrode and the first insulating layer.

3. The method of making a thin-film transistor as claimed in claim **1**, wherein the first metal layer includes Al, Cu, or Au.

4. The method of making a thin-film transistor as claimed in claim **1**, wherein the second metal layer includes Mo, Ta, or Co.

5. The method of making a thin-film transistor as claimed in claim **1**, wherein the first and second metal layers are removed via a dry etching method.

6. The method of making a thin-film transistor as claimed in claim **1**, wherein the second metal layer is etched with an etching solution prepared with a mixture of phosphoric acid, acetic acid and nitric acid.

[7. A method of forming a thin film transistor comprising:

forming a first metal layer on a substrate,

forming a second metal layer on the first metal layer;

simultaneously patterning the first and second metal layers to form a double-layered metal gate, so that a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 μm.**]**

[8. The method of claim **7**, wherein the first and second metal layers are patterned so that the first metal layer has a first and a second side portion being exposed from the second metal layer, each side portion being at least about 0.5 μm in width.**]**

[9. The method of claim **8**, wherein each side portion of the first metal layer is exposed so that each side portion is less than about 2 μm in width.**]**

[10. The method of claim **7**, wherein the patterning step is such that the second metal layer is etched faster than the first etching layer.**]**

11. [The method of claim **10**,] *A method of forming a thin film transistor comprising:*

forming a first metal layer on a substrate,

forming a second metal layer on the first metal layer;

simultaneously patterning the first and second metal layers to form a double-layered metal gate, so that a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 μm, wherein:

the patterning step is such that the second metal layer is etched faster than the first etching layer; and

the second metal layer is wet etched, and the first metal layer is dry etched.

[**12**. The method of claim **10**, wherein both the first and second metal layers are wet etched.]

13. [The method of claim **7**,] *A method of forming a thin film transistor comprising:*

forming a first metal layer on a substrate;

forming a second metal layer on the first metal layer;

simultaneously patterning the first and second metal layers to form a double-layered metal gate, so that a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 μm, wherein the patterning step comprises:

isotropically etching the second metal layer; and

anisotropically etching the first metal layer.

[**14**. The method of claim **7**, wherein no masking step is required between the formation of the first and second metal layers.]

15. [The method of claim **7**,] *A method of forming a thin film transistor comprising:*

forming a first metal layer on a substrate,

forming a second metal layer on the first metal layer;

simultaneously patterning the first and second metal layers to form a double-layered metal gate, so that a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 μm, wherein the patterning step does not require processing of a photoresist before etching.

[**16**. A method of waking a thin-film transistor, comprising the steps of:

depositing a first metal layer on a substrate, the first metal layer including aluminum;

depositing a second metal layer on the first metal layer without forming a photoresist on the first metal layer beforehand;

forming a single photoresist having predetermined width on the second metal layer;

patterning the first and second metal layers simultaneously in a single etching step using the single photoresist as a mask, the first metal layer being etched to have a width greater than a width of the second metal layer by about 1 to 4 μm; and

removing the photoresist.]

[**17**. The method of making a thin film transistor as claimed in claim **16**, further comprising the steps of:

forming a first insulating layer on the substrate including the gate;

forming a semiconductor layer and an ohmic contact layer on a portion of the first insulating layer at a location corresponding to the gate;

forming a source electrode and a drain electrode extending onto the first insulating layer on two sides of the ohmic contact layer, and removing a portion of the ohmic contact layer exposed between the source and the drain electrodes; and

forming a second insulating layer covering the semiconductor layer, the source electrode, the drain electrode and the first insulating layer.]

[**18**. The method of making a thin film transistor as claimed in claim **16**, wherein the first and second metal layers are sequentially deposited via sputtering or a chemical vapor deposition method without breaking a vacuum state.]

[**19**. The method of making a thin film transistor as claimed in claim **16**, wherein the first metal layer has thickness of about 500 Å to about 4000 Å.]

[**20**. The method of making a thin film transistor as claimed in claim **16**, wherein the second metal layer includes Mo, Ta or Co.]

21. [The method of making a thin film transistor as claimed in claim **16**,] *A method of making a thin-film transistor, comprising the steps of:*

depositing a first metal layer on a substrate, the first metal layer including aluminum, wherein the first metal layer has a thickness of about 500 Å to about 2000 Å*;*

depositing a second metal layer on the first metal layer without forming a photoresist on the first metal layer beforehand;

forming a single photoresist having predetermined width on the second metal layer;

patterning the first and second metal layers simultaneously in a single etching step using the single photoresist as a mask, the first metal layer being etched to have a width greater than a width of the second metal layer by about 1 to 4 μm; and

removing the photoresist.

[**22**. The method of making a thin film transistor as claimed in claim **16**, wherein two side portions of the first metal layer having no second metal layer deposited thereon have substantially the same width as each other.]

23. A method of forming a thin film transistor comprising:

forming a first metal layer on a substrate,

forming a second metal layer on the first metal layer, wherein no masking step is required between the formation of the first and second metal layers; and

simultaneously patterning the first and second metal layers to form a double-layered metal gate, so that the first metal layer has a substantially trapezoidal cross-sectional area with a top edge that is substantially parallel to the substrate, wherein:

the patterning step is such that the second metal layer is etched faster than the first metal layer;

the second metal layer is wet etched, and the first metal layer is dry etched;

a first portion of the top edge is in contact with the second metal layer;

a second portion of the top edge is not in contact with the second metal layer; and

a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 μm.

24. A method of forming a thin film transistor comprising:

forming a first metal layer on a substrate,

forming a second metal layer on the first metal layer, wherein no masking step is required between the formation of the first and second metal layers; and

simultaneously patterning the first and second metal layers to form a double-layered metal gate, so that the first metal layer has a substantially trapezoidal cross-sectional area with a top edge that is substantially parallel to the substrate, wherein:

the patterning step comprises:

isotropically etching the second metal layer; and

anisotropically etching the first metal layer;

a first portion of the top edge is in contact with the second metal layer;

a second portion of the top edge is not in contact with the second metal layer; and

a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 μm.

25. A method of forming a thin film transistor comprising:

forming a first metal layer on a substrate,

forming a second metal layer on the first metal layer, wherein no masking step is required between the formation of the first and second metal layers; and

simultaneously patterning the first and second metal layers to form a double-layered metal gate, so that the first metal layer has a substantially trapezoidal cross-sectional area with a top edge that is substantially parallel to the substrate, wherein:

the patterning step does not require processing of a photoresist before etching;

a first portion of the top edge is in contact with the second metal layer;

a second portion of the top edge is not in contact with the second metal layer; and

a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 μm.

26. A method of forming a thin film transistor comprising:

forming a first metal layer on a substrate,

forming a second metal layer on the first metal layer, wherein no masking step is required between the formation of the first and second metal layers; and

simultaneously patterning the first and second metal layers to form a double-layered metal gate, so that the first metal layer has a substantially trapezoidal cross-sectional area with a top edge that is substantially parallel to the substrate, wherein:

a first portion of the top edge is in contact with the second metal layer;

a second portion of the top edge is not in contact with the second metal layer;

lateral surfaces of the second metal layer have a substantially rectangular shape; and

a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 μm.

27. A method of forming a thin film transistor comprising:

forming a first metal layer on a substrate,

forming a second metal layer on the first metal layer, wherein no masking step is required between the formation of the first and second metal layers; and

simultaneously patterning the first and second metal layers to form a double-layered metal gate, so that the first metal layer has a substantially trapezoidal cross-sectional area with a top edge that is substantially parallel to the substrate, wherein:

a first portion of the top edge is in contact with the second metal layer;

a second portion of the top edge is not in contact with the second metal layer;

lateral surfaces of the second metal layer are flat so that the second metal layer has a substantially rectangular cross-sectional area; and

a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 μm.

28. A method of forming a thin film transistor comprising:

forming a first metal layer on a substrate,

forming a second metal layer on the first metal layer, wherein no masking step is required between the formation of the first and second metal layers; and

simultaneously patterning the first and second metal layers to form a double-layered metal gate, so that the first metal layer has a substantially trapezoidal cross-sectional area with a top edge that is substantially parallel to the substrate, wherein:

a first portion of the top edge is in contact with the second metal layer;

a second portion of the top edge is not in contact with the second metal layer;

lateral surfaces of the second metal layer are inclined so that the second metal layer has a substantially trapezoidal cross-sectional area; and

a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 μm.

29. A method of forming a thin film transistor comprising:

forming a first metal layer on a substrate,

forming a second metal layer on the first metal layer, wherein no masking step is required between the formation of the first and second metal layers; and

simultaneously patterning the first and second metal layers to form a double-layered metal gate, so that the first metal layer has a substantially trapezoidal cross-sectional area with a top edge that is substantially parallel to the substrate, wherein:

a first portion of the top edge is in contact with the second metal layer;

a second portion of the top edge is not in contact with the second metal layer;

a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 μm; and

the width of the first metal layer is measured along the top edge of the first metal layer that is substantially parallel to the substrate.

30. A method of forming a thin film transistor comprising:

forming a first metal layer on a substrate,

forming a second metal layer on the first metal layer, wherein no masking step is required between the formation of the first and second metal layers; and

simultaneously patterning the first and second metal layers to form a double-layered metal gate, so that the first metal layer has a substantially trapezoidal cross-sectional area with a top edge that is substantially parallel to the substrate, wherein:

a first portion of the top edge is in contact with the second metal layer;

a second portion of the top edge is not in contact with the second metal layer;

a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 μm; and

the width of the second metal layer is measured along a top edge of the second metal layer that is substantially parallel to the substrate.

31. A method of making a thin-film transistor, comprising the steps of:

depositing a first metal layer on a substrate, the first metal layer including aluminum;

depositing a second metal layer on the first metal layer without forming a photoresist on the first metal layer beforehand, wherein the first and second metal layers are sequentially deposited via sputtering or a chemical vapor deposition method without breaking a vacuum state;

forming a single photoresist having predetermined width on the second metal layer; and *patterning the first and second metal layers simultaneously in a single etching step using the single photoresist as a mask, so that the first metal layer has a substantially trapezoidal cross-sectional area with a top edge that is substantially parallel to the substrate, wherein:*

a first portion of the top edge is in contact with the second metal layer;

a second portion of the top edge is not in contact with the second metal layer; and

the first metal layer is etched to have a width greater than a width of the second metal layer by about 1 to 4 μm; and

removing the photoresist.

32. The method of making a thin film transistor as claimed in claim 31, further comprising the steps of:

forming a first insulating layer on the substrate including the gate;

forming a semiconductor layer and an ohmic contact layer on a portion of the first insulating layer at a location corresponding to the gate;

forming a source electrode and a drain electrode extending onto the first insulating layer on two sides of the ohmic contact layer, and removing a portion of the ohmic contact layer exposed between the source and the drain electrodes; and

forming a second insulating layer covering the semiconductor layer, the source electrode, the drain electrode and the first insulating layer.

33. The method of making a thin film transistor as claimed in claim 31, wherein the first metal layer has thickness of about 500 Å to about 4000 Å.

34. The method of making a thin film transistor as claimed in claim 31, wherein the second metal layer includes Mo, Ta or Co.

35. The method of making a thin film transistor as claimed in claim 31, wherein the first metal layer has a thickness of about 500 Å to about 2000 Å.

36. The method of making a thin film transistor as claimed in claim 31, wherein two side portions of the first metal layer having no second metal layer deposited thereon have substantially the same width as each other.

37. The method of making a thin film transistor as claimed in claim 31, wherein lateral surfaces of the second metal layer have a substantially rectangular shape.

38. The method of making a thin film transistor as claimed in claim 31, wherein lateral surfaces of the second metal layer are flat so that the second metal layer has a substantially rectangular cross-sectional area.

39. The method of making a thin film transistor as claimed in claim 31, wherein lateral surfaces of the second metal layer are inclined so that the second metal layer has a substantially trapezoidal cross-sectional area.

40. The method of making a thin film transistor as claimed in claim 31, wherein the width of the first metal layer is measured along the top edge of the first metal layer that is substantially parallel to the substrate.

41. The method of making a thin film transistor as claimed in claim 31, wherein the width of the second metal layer is measured along a top edge of the second metal layer that is substantially parallel to the substrate.

42. A method of making a thin-film transistor, comprising the steps of:

depositing a first metal layer on a substrate, the first metal layer including aluminum;

depositing a second metal layer on the first metal layer without forming a photoresist on the first metal layer beforehand;

forming a single photoresist having predetermined width on the second metal layer;

patterning the first and second metal layers simultaneously in a single etching step using the single photoresist as a mask, so that the first metal layer has a substantially trapezoidal cross-sectional area with a top edge that is substantially parallel to the substrate, wherein:

a first portion of the top edge is in contact with the second metal layer;

a second portion of the top edge is not in contact with the second metal layer; and

the first metal layer is etched to have a width greater than a width of the second metal layer by about 1 to 4 μm;

removing the photoresist;

forming a first insulating layer on the substrate including the gate;

forming a semiconductor layer and an ohmic contact layer on a portion of the first insulating layer at a location corresponding to the gate;

forming a source electrode and a drain electrode extending onto the first insulating layer on two sides of the ohmic contact layer, and removing a portion of the ohmic contact layer exposed between the source and the drain electrodes; and

forming a second insulating layer covering the semiconductor layer, the source electrode, the drain electrode and the first insulating layer.

43. A method of making a thin-film transistor, comprising the steps of:

depositing a first metal layer on a substrate, the first metal layer including aluminum, wherein the first metal layer has thickness of about 500 Å to about 4000 Å;

depositing a second metal layer on the first metal layer without forming a photoresist on the first metal layer beforehand;

forming a single photoresist having predetermined width on the second metal layer;

patterning the first and second metal layers simultaneously in a single etching step using the single photoresist as a mask, so that the first metal layer has a substantially trapezoidal cross-sectional area with a top edge that is substantially parallel to the substrate, wherein:

a first portion of the top edge is in contact with the second metal layer;

a second portion of the top edge is not in contact with the second metal layer; and

the first metal layer is etched to have a width greater than a width of the second metal layer by about 1 to 4 μm; and

removing the photoresist.

44. A method of making a thin-film transistor, comprising the steps of:

depositing a first metal layer on a substrate, the first metal layer including aluminum;

depositing a second metal layer on the first metal layer without forming a photoresist on the first metal layer beforehand, wherein the second metal layer includes Mo, Ta or Co;

forming a single photoresist having predetermined width on the second metal layer;

patterning the first and second metal layers simultaneously in a single etching step using the single photoresist as a mask, so that the first metal layer has a substantially trapezoidal cross-sectional area with a top edge that is substantially parallel to the substrate, wherein:

a first portion of the top edge is in contact with the second metal layer;

a second portion of the top edge is not in contact with the second metal layer; and

the first metal layer is etched to have a width greater than a width of the second metal layer by about 1 to 4 μm; and

removing the photoresist.

45. A method of making a thin-film transistor, comprising the steps of:

depositing a first metal layer on a substrate, the first metal layer including aluminum;

depositing a second metal layer on the first metal layer without forming a photoresist on the first metal layer beforehand;

forming a single photoresist having predetermined width on the second metal layer;

patterning the first and second metal layers simultaneously in a single etching step using the single photoresist as a mask, so that the first metal layer has a substantially trapezoidal cross-sectional area with a top edge that is substantially parallel to the substrate, two side portions of the first metal layer having no second metal layer deposited thereon have substantially the same width as each other, wherein:

a first portion of the top edge is in contact with the second metal layer;

a second portion of the top edge is not in contact with the second metal layer; and

the first metal layer is etched to have a width greater than a width of the second metal layer by about 1 to 4 μm; and

removing the photoresist.

* * * * *