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(54) **APPARATUS AND METHODS FOR DETERMINING OVERLAY OF STRUCTURES HAVING ROTATIONAL OR MIRROR SYMMETRY**

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USPC **257/48**; 257/797; 257/E23.179

(58) **Field of Classification Search**
USPC 257/48, 797, E23.179
See application file for complete search history.

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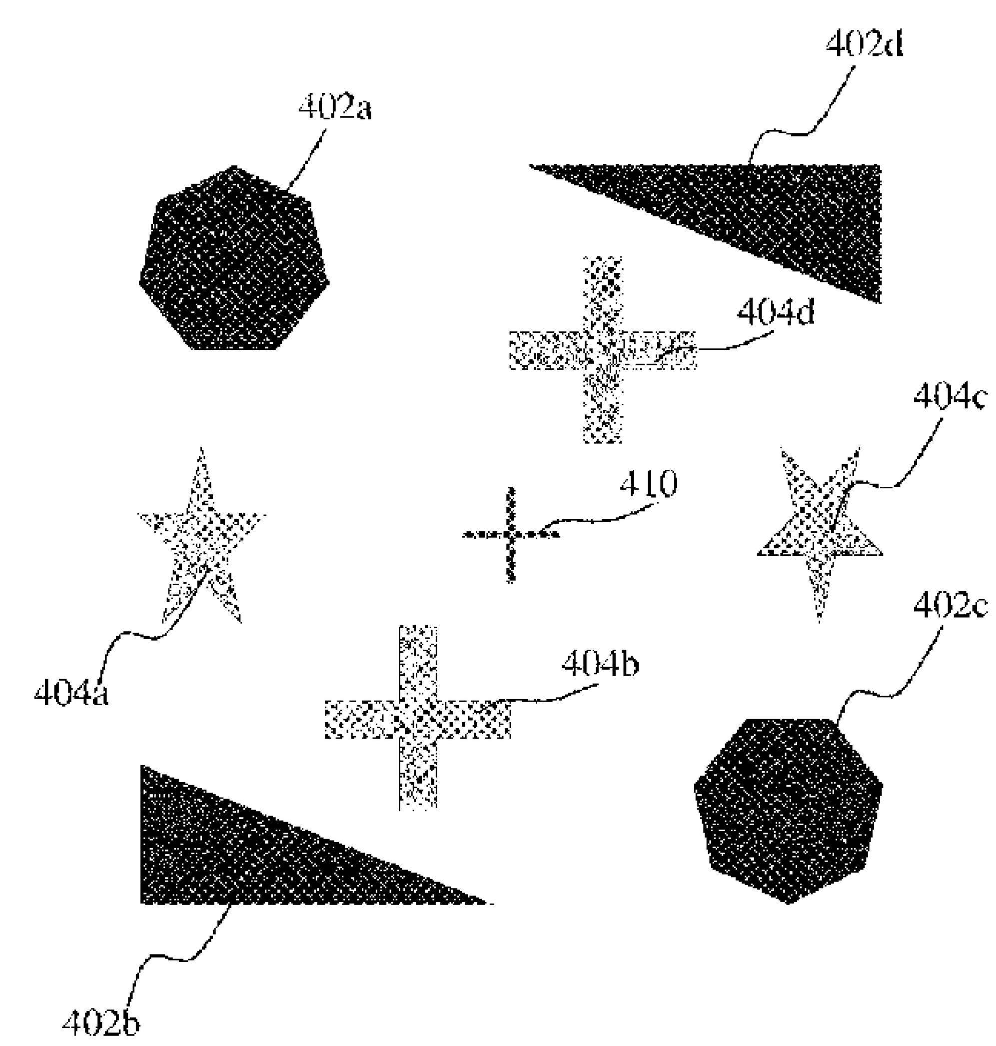
(57) **ABSTRACT**

Disclosed are overlay targets having flexible symmetry characteristics and metrology techniques for measuring the overlay error between two or more successive layers of such targets. Techniques for imaging targets with flexible symmetry characteristics and analyzing the acquired images to determine overlay or alignment error are disclosed.

11 Claims, 7 Drawing Sheets



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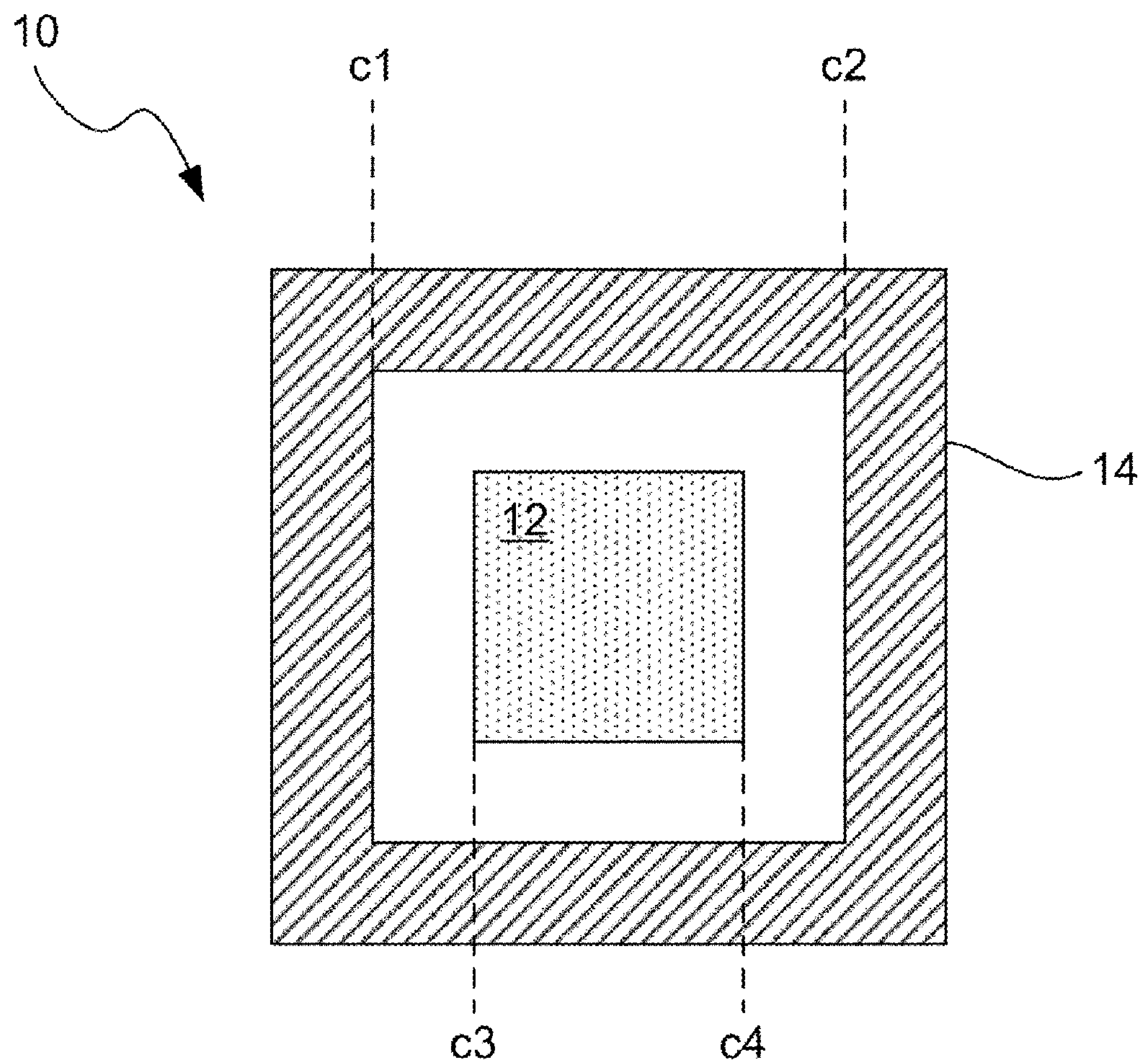

FIGURE 1

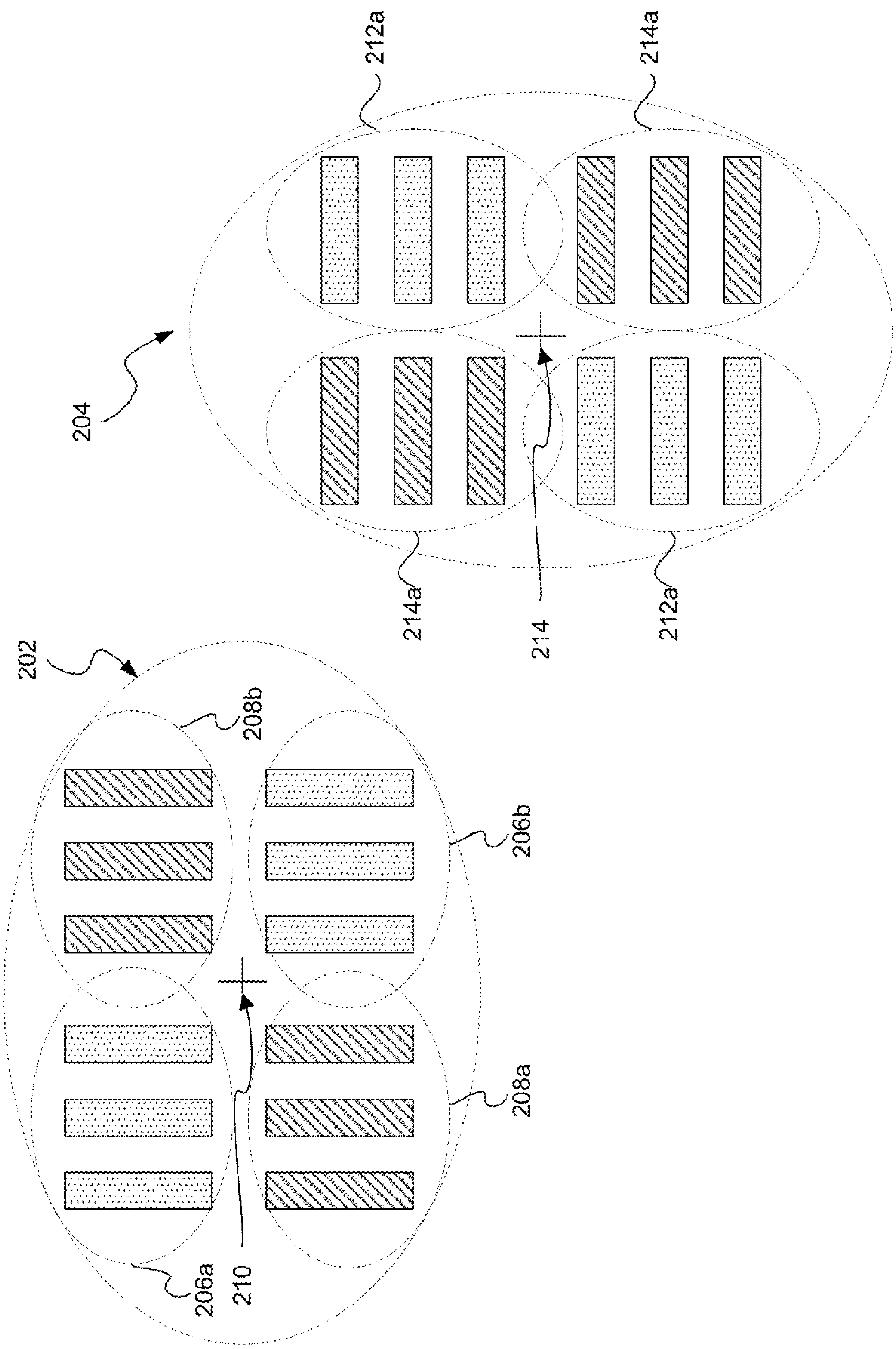

FIGURE 2

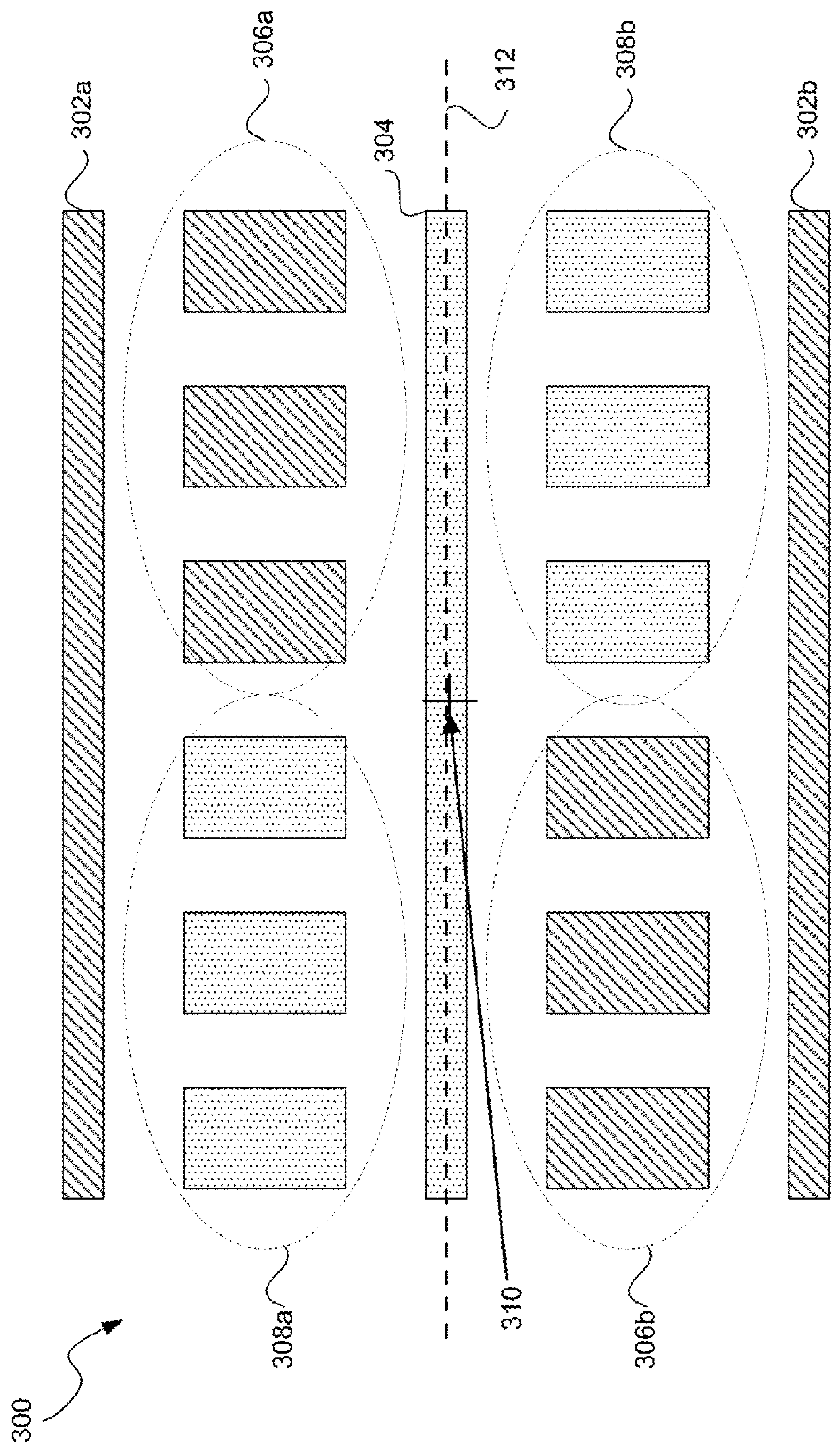

FIGURE 3

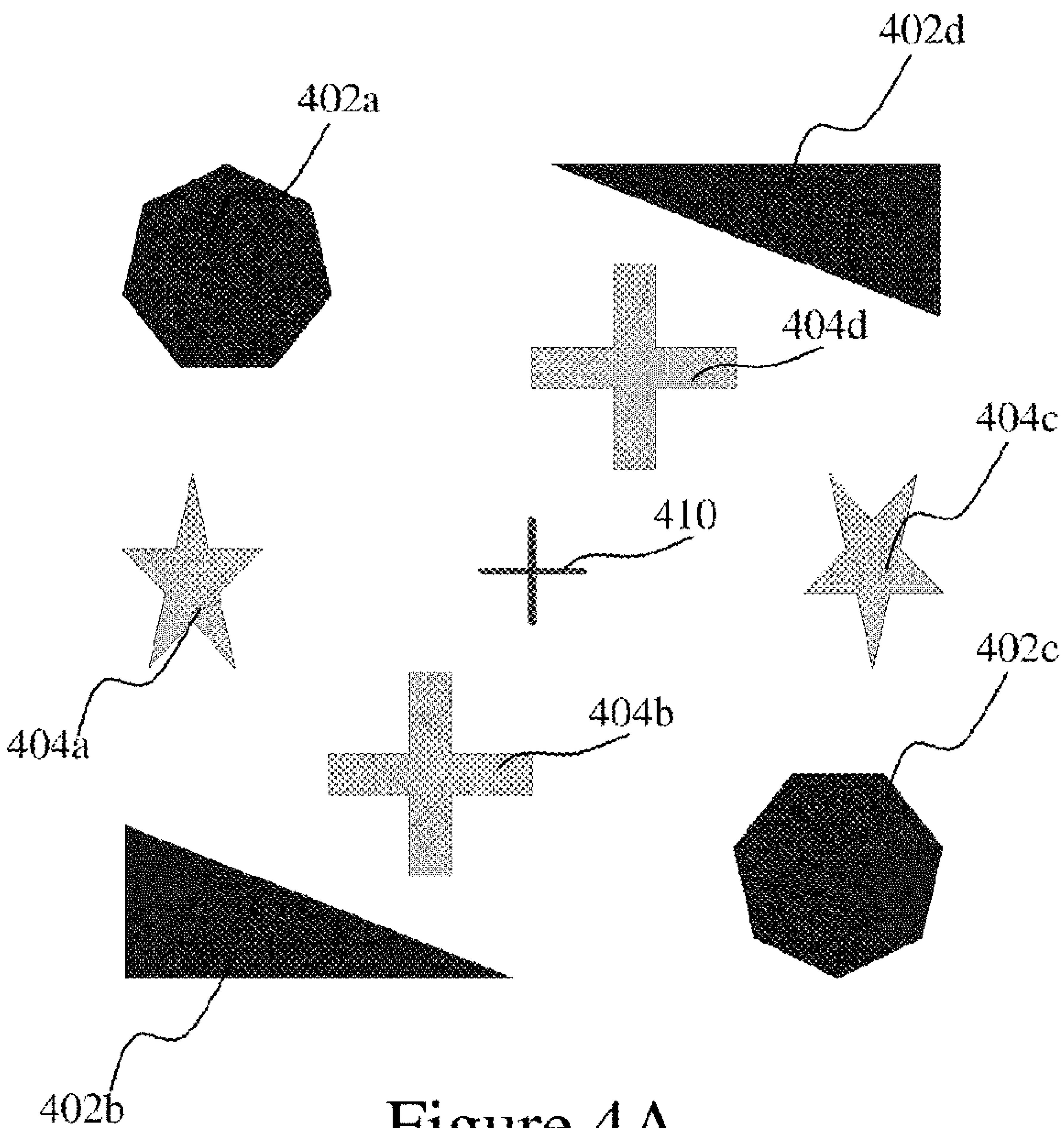

Figure 4A

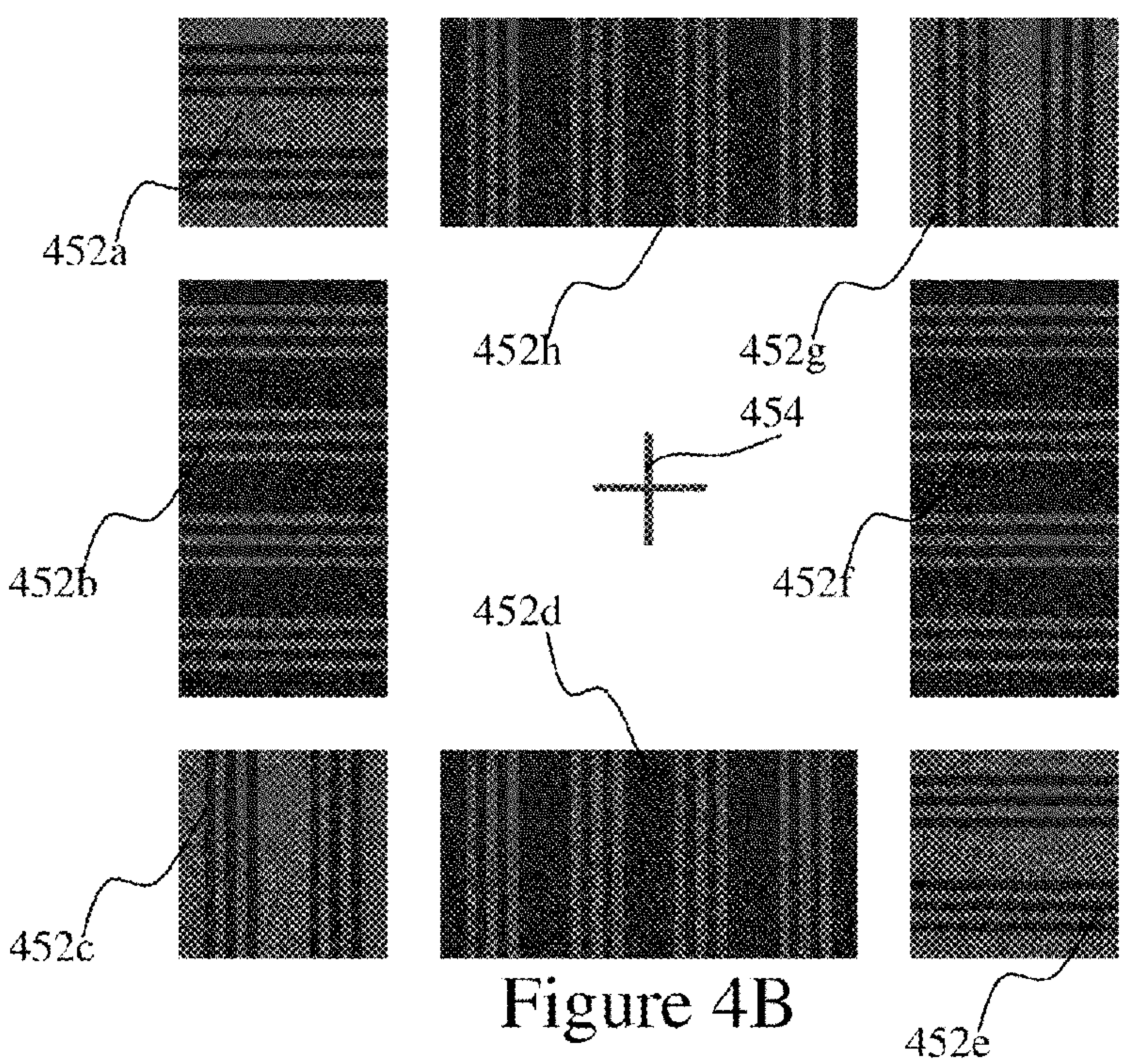

Figure 4B

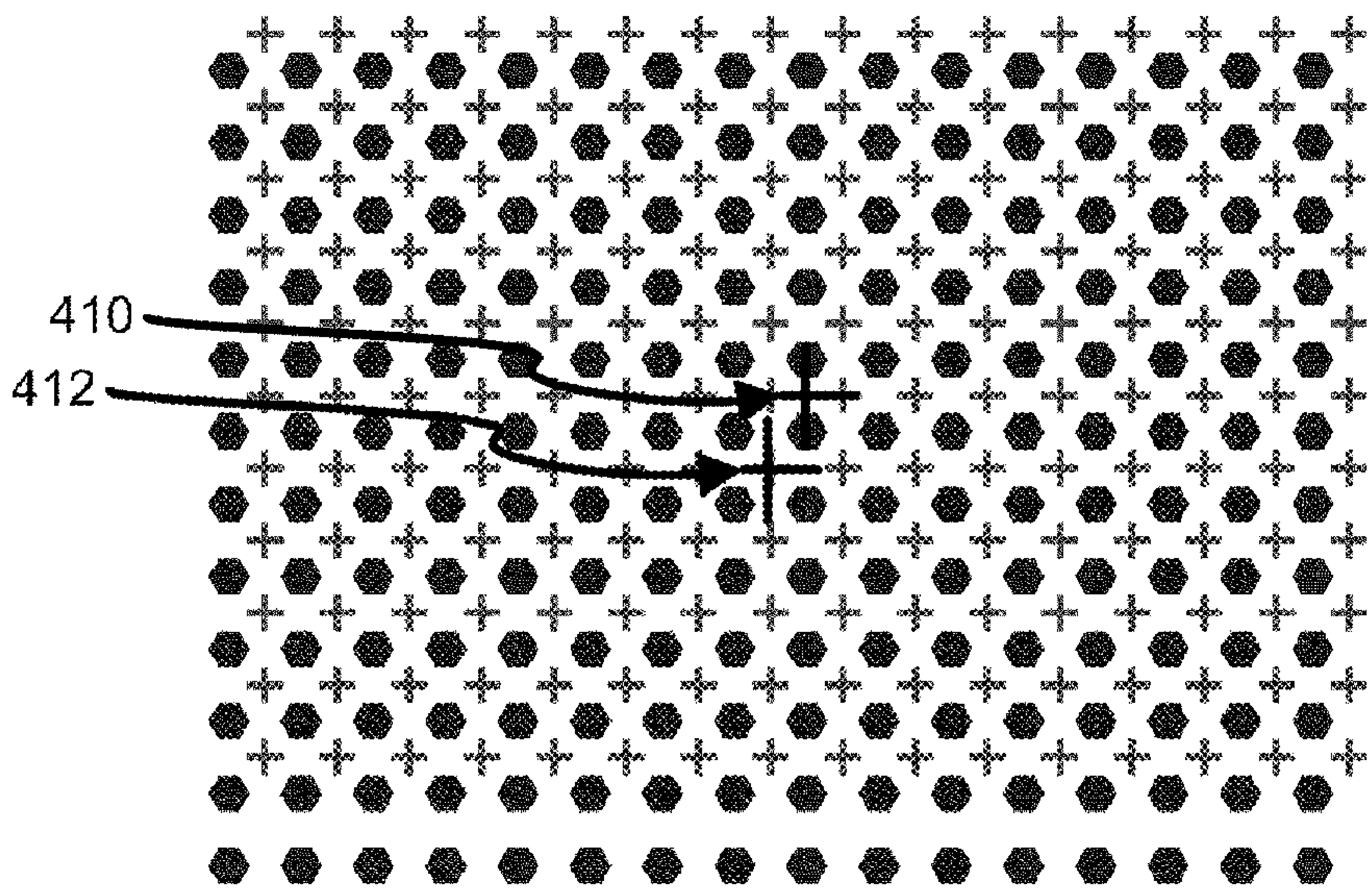

FIGURE 4C

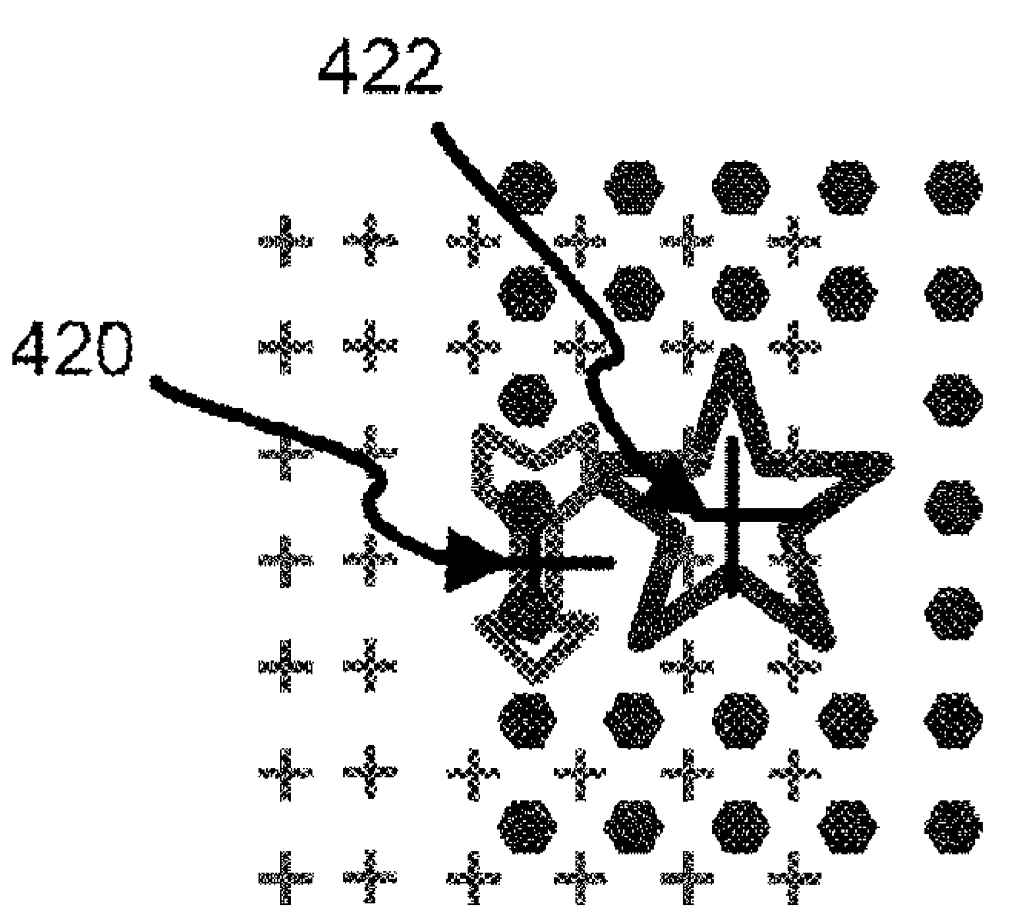

FIGURE 4D

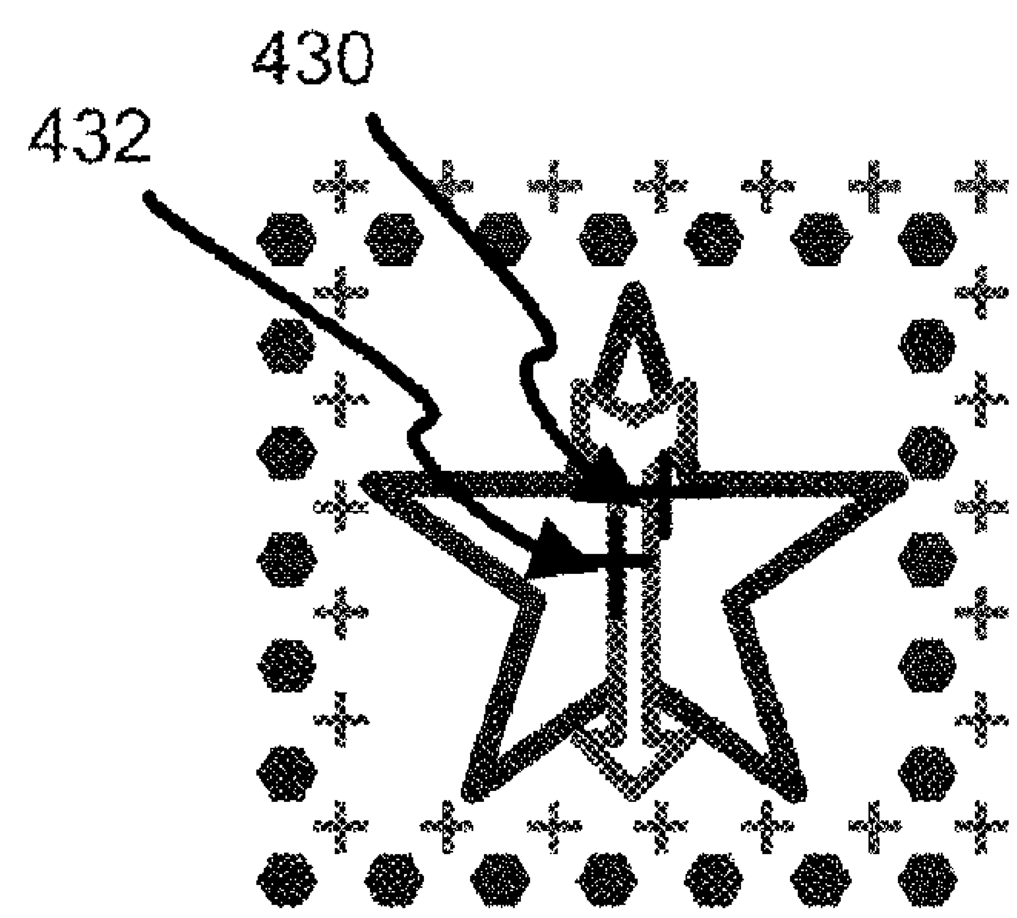

FIGURE 4E

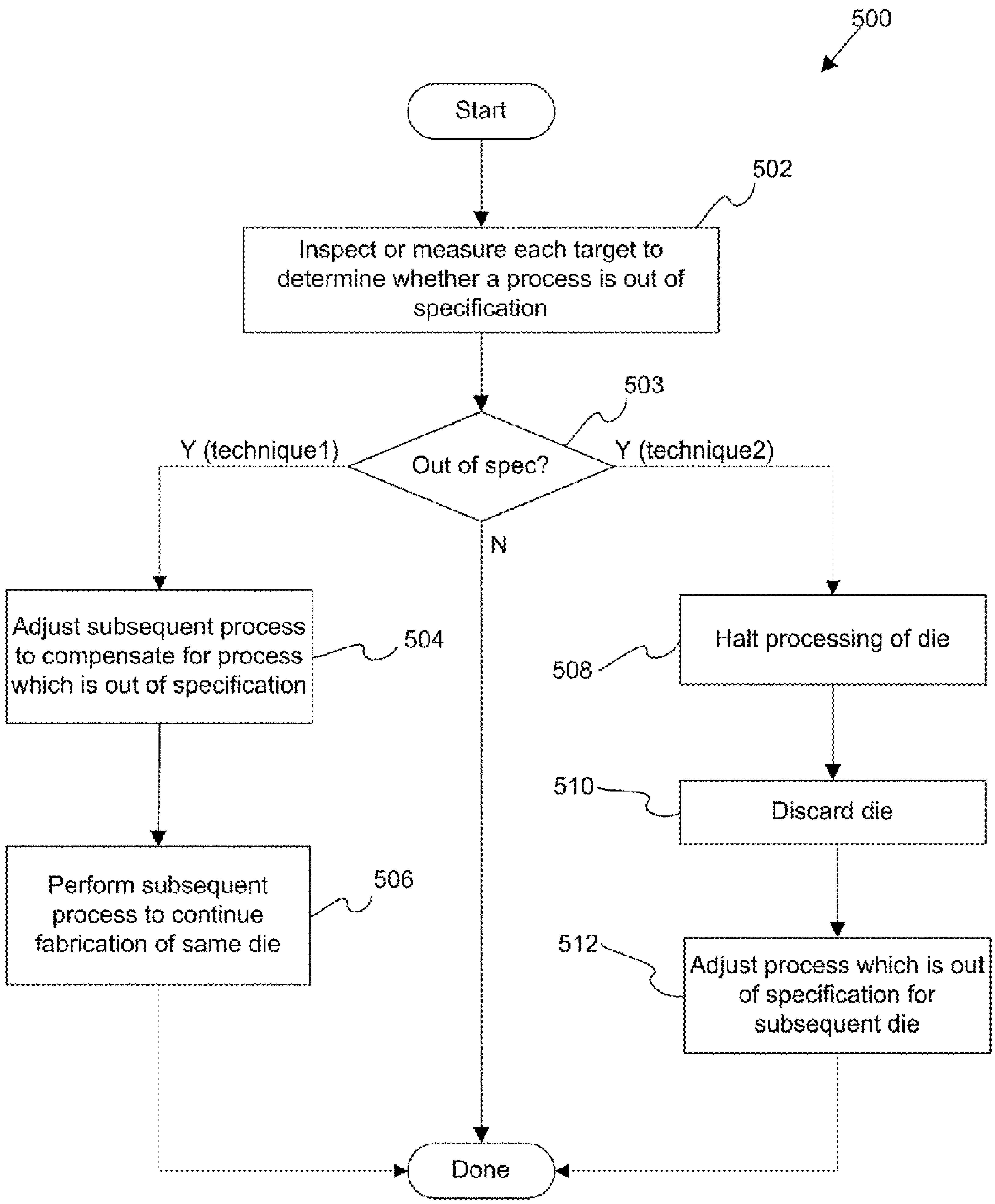
500
Start
502
Inspect or measure each target to determine whether a process is out of specification
503
Y (technique1)
Out of spec?
Y (technique2)
N
Adjust subsequent process to compensate for process which is out of specification
504
508
Halt processing of die
510
Discard die
Perform subsequent process to continue fabrication of same die
506
512
Adjust process which is out of specification for subsequent die
Done

Figure 5

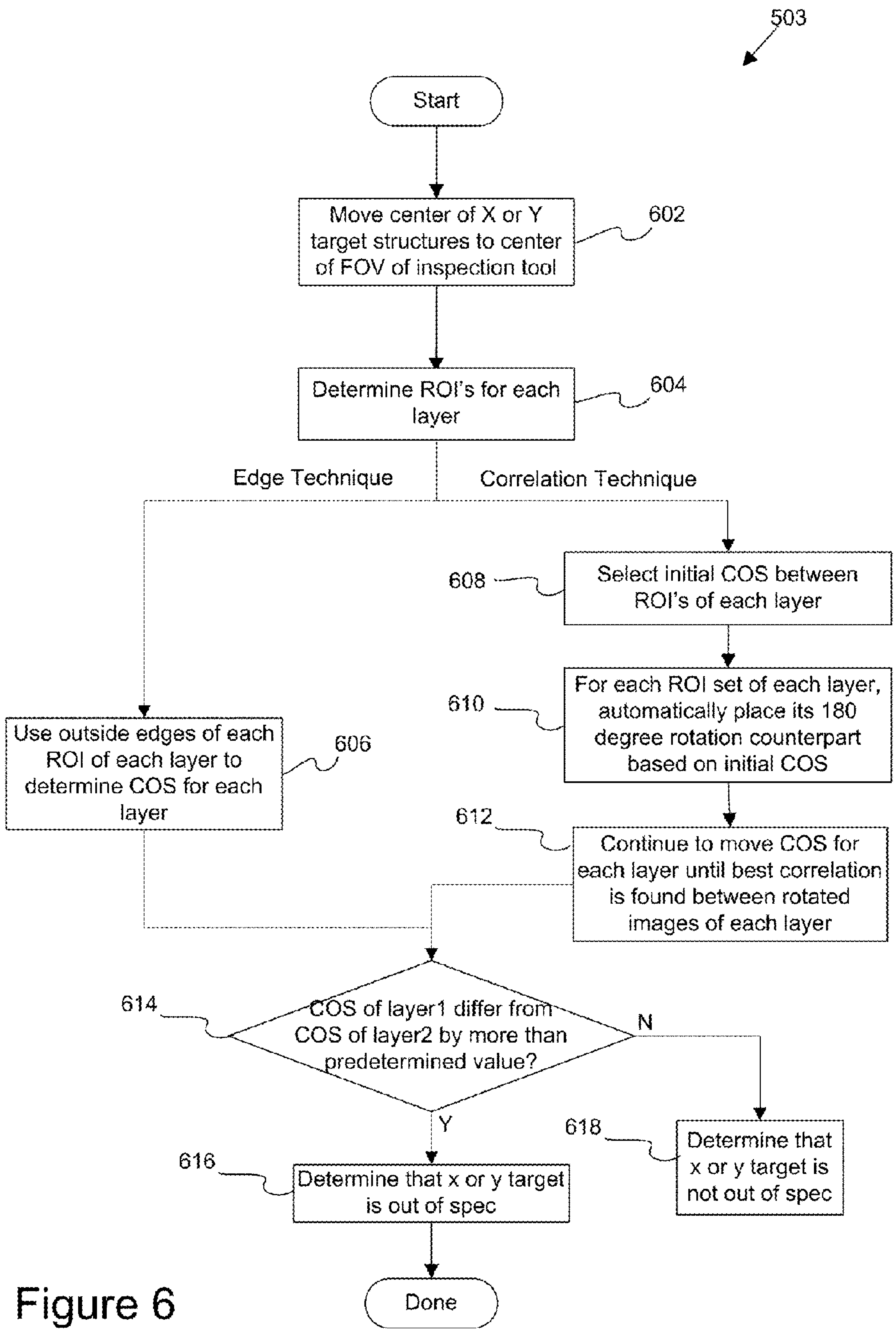
503
Start
Move center of X or Y target structures to center of FOV of inspection tool
602
Determine ROI's for each layer
604
Edge Technique
Correlation Technique
608
Select initial COS between ROI's of each layer
610
For each ROI set of each layer, automatically place its 180 degree rotation counterpart based on initial COS
Use outside edges of each ROI of each layer to determine COS for each layer
606
612
Continue to move COS for each layer until best correlation is found between rotated images of each layer
614
COS of layer1 differ from COS of layer2 by more than predetermined value?
N
Y
618
Determine that x or y target is not out of spec
616
Determine that x or y target is out of spec
Done

Figure 6

APPARATUS AND METHODS FOR DETERMINING OVERLAY OF STRUCTURES HAVING ROTATIONAL OR MIRROR SYMMETRY

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

CROSS REFERENCE TO RELATED PATENT APPLICATION

This application *is a reissue of application Ser. No. 12/410,317, which* claims priority and is a Divisional application of [copending] application Ser. No. 11/227,764, [entitled "APPARATUS AND METHODS FOR DETERMINING OVERLAY OF STRUCTURES HAVING ROTATIONAL OR MIRROR SYMMETRY",] filed 14 Sep. 2005 [by Mark Ghinovker], *now U.S. Pat. No. 7,541,201, issued on 2 Jun. 2009*, which application claims priority of (a) and is a Continuation-in-part application of application Ser. No. 09/894,987, filed on Jun. 27, 2001, now U.S. Pat. No. 7,068,833, issued on 27 Jun. 2006, which claims priority of Application No. 60/229,256, filed 30 Aug. 2000 and (b) U.S. Provisional Patent Application No. 60/698,535, [entitled "APPARATUS AND METHODS FOR DETERMINING OVERLAY STRUCTURES HAVING ROTATIONAL OR MIRROR SYMMETRY",] filed 11 Jul. 2005 [by Mark Ghinovker], and (c) is a Continuation-in-part application of application Ser. No. 10/729,838, filed on Dec. 5, 2003, now U.S. Pat. No. 7,317,531, issued on 8 Jan. 2008, which application claims priority of (i) Application No. 60/440,970, filed 17 Jan. 2003, (ii) Application No. 60/449,496, filed 22 Feb. 2003, (iii) Application No. 60/431,314, filed 5 Dec. 2002, (iv) Application No. 60/504,093, filed 19 Sep. 2003, and (v) Application No. 60/498,524, filed 27 Aug. 2003. These applications and patents are incorporated herein by reference in their entirety for all purposes. *Application Ser. No. 12/410,317 also is a Continuation-In-Part application and claims priority of application Ser. No. 11,926,603, filed on 29 Oct. 2007, now U.S. Pat. No. 7,564,557, issued on 21 Jul. 2009, which is a Divisional application and claims priority of application Ser. No. 10/785,732, filed on 23 Feb. 2004, now U.S. Pat. No. 7,289,213, issued on 30 Oct. 2007, which is a Continuation-In-Part application and claims priority of application Ser. No. 10/729,838, filed on 5 Dec. 2003, now U.S. Pat. No. 7,317,531, issued on 8 Jan. 2008, which claims priority of application Ser. No. 60/431,314, filed on 5 Dec. 2002, application Ser. No. 60/440,970, filed on 17 Jan. 2003, application Ser. No. 60/504,093, filed on 19 Sep. 2003, application Ser. No. 60/449,496, filed 22 Feb. 2003, and application Ser. No. 60/498,524, filed on 27 Aug. 2003.*

BACKGROUND OF THE INVENTION

The present invention relates generally to overlay measurement techniques, which are used in semiconductor manufacturing processes. More specifically, the present invention relates to techniques for measuring alignment error between different layers or different patterns on the same layer of a semiconductor wafer stack.

The measurement of overlay error between successive patterned layers on a wafer is one of the most critical process control techniques used in the manufacturing of integrated circuits and devices. Overlay accuracy generally pertains to

the determination of how accurately a first patterned layer aligns with respect to a second patterned layer disposed above or below it and to the determination of how accurately a first pattern aligns with respect to a second pattern disposed on the same layer. Presently, overlay measurements are performed via test patterns that are printed together with layers of the wafer. The images of these test patterns are captured via an imaging tool and an analysis algorithm is used to calculate the relative displacement of the patterns from the captured images.

The most commonly used overlay target pattern is the "Box-in-Box" target, which includes a pair of concentric squares (or boxes) that are formed on successive layers of the wafer. The overlay error is generally determined by comparing the position of one square relative to another square.

To facilitate discussion, FIG. **1** is a top view of a typical "Box-in-Box" target **10**. As shown, the target **10** includes an inner box **12** disposed within an open-centered outer box **14**. The inner box **12** is printed on the top layer of the wafer while the outer box **14** is printed on the layer directly below the top layer of the wafer. As is generally well known, the overlay error between the two boxes, along the x-axis for example, is determined by calculating the locations of the edges of lines **c1** and **c2** of the outer box **14**, and the edge locations of the lines **c3** and **c4** of the inner box **12**, and then comparing the average separation between lines **c1** and **c3** with the average separation between lines **c2** and **c4**. Half of the difference between the average separations **c1**&**c3** and **c2**&**c4** is the overlay error (along the x-axis). Thus, if the average spacing between lines **c1** and **c3** is the same as the average spacing between lines **c2** and **c4**, the corresponding overlay error tends to be zero. Although not described, the overlay error between the two boxes along the y-axis may also be determined using the above technique.

This type of target has a same center of symmetry (COS) for both the x and y structures, as well as for the first and second layer structures. When the target structures are rotated 180° about their COS, they maintain a same appearance. Conventionally, it has been a requirement that both the x and y structures and both the first and second layer structures have a same COS. However, these requirements may be too restrictive under certain conditions. For example, space may be limited on the wafer and a target having x and y structures (or first and second layer structures) with the same COS may not fit into the available space. Additionally, it may be desirable to use device structures for determining overlay, and device structures are not likely to meet this strict requirement.

Although this conventional overlay design has worked well, there are continuing efforts to provide improved techniques for determining or predicting overlay in device structures. For example, targets or device structures that have more flexible symmetry characteristics, as well as techniques for determining overlay with such structures, are needed.

SUMMARY OF THE INVENTION

In general, overlay targets having flexible symmetry characteristics and metrology techniques for measuring the overlay error between two or more successive layers of such targets or a shift between two sets of structures on the same layer are provided. In one embodiment, a target includes structures for measuring overlay error (or a shift) in both the x and y direction, wherein the x structures have a different center of symmetry (COS) than the y structures. In another embodiment, one of the x and y structures is invariant with a 180° rotation and the other one of the x and y structures has a mirror symmetry. In one aspect, the x and y structures together are variant with a 180° rotation. In yet another example, a target for measuring overlay in the x and/or y direction includes structures on a first layer having a 180 symmetry and structures on a second layer having mirror symmetry. In another embodiment, a target for determining overlay in the x and/or y direction includes structures on a first layer and structures on a second layer, wherein the structures on the first layer have a COS that is offset by a known amount from the COS of the structures on the second layer. In a specific implementation, any of the disclosed target embodiments may take the form of device structures. In a use case, device structures that have an inherent 180° rotational symmetry or a mirror symmetry in each of the first and second layers are used to measure overlay in a first layer and a second layer. Techniques for imaging targets with flexible symmetry characteristics and analyzing the acquired images to determine overlay or alignment error are disclosed.

In one embodiment, a semiconductor target for determining a relative shift between two or more successive layers of a substrate or between two or more separately generated patterns on a single layer of a substrate is disclosed. This target includes a plurality of first structures having a first center of symmetry (COS) or first line of symmetry (LOS) and being arranged to determine the relative shift in an x direction by analyzing an image of the first structures. This target further includes a plurality of second structures having a second COS or second LOS and being arranged to determine the relative shift in an x direction by analyzing an image of the second structures. The first COS or LOS has a different location than the second COS or LOS.

In a further aspect, the first structures have a first LOS about which the first structures have a mirror symmetry or the first structures have a 180° rotational symmetry with respect to the first COS, and the second structures have a first LOS about which the second structures have a mirror symmetry or the second structures have a 180° rotational symmetry with respect to the second COS. In another aspect, the first and second structures are in the form of device structures. In a further embodiment, a one of the first or second structures has a 180° rotational symmetry with respect to its COS and the other one of the first or second structures' has a mirror symmetry with respect to its LOS. In yet a further implementation, the first structures and the second structures together are variant with a 180° rotational asymmetry or together have a mirror asymmetry.

In an alternative embodiment, a semiconductor target for determining an overlay error between two or more successive layers of a substrate is disclosed. This target comprises a plurality of first structures formed in a first semiconductor layer and having a first center of symmetry or first line of symmetry (LOS) and a plurality of second structures formed in a second semiconductor layer and having a second COS OR LOS. The first COS OR LOS is designed to have a known offset from the second COS or LOS so that the overlay error can be determined by acquiring an image of the first and second structures and then analyzing a shift between the first and second COS's or LOS's in the image and comparing the shift to the known offset.

In a specific implementation, the first structures have a first LOS about which the first structures have a mirror symmetry or the first structures have a 180° rotational symmetry with respect to the first COS, and the second structures have a first LOS about which the second structures have a mirror symmetry or the second structures have a 180° rotational symmetry with respect to the second COS. In yet a further aspect, the first and second structures are in the form of device structures. In another implantation, a one of the first or second structures has a 180° rotational symmetry with respect to its COS and the other one of the first or second structures' has a mirror symmetry with respect to its LOS. In a further implementation, the first structures and the second structures together are variant with a 180° rotational asymmetry or together have a mirror asymmetry.

In another embodiment, the invention pertains to a method for determining the relative shift between two or more successive layers of a substrate or between two or more separately generated patterns on a single layer of a substrate. A first image is acquired of a plurality of first structures having a first center of symmetry (COS) or first line of symmetry (LOS) and being arranged to determine the relative shift in an x direction by analyzing an image of the first structures. A first image is acquired of a plurality of second structures having a second COS or second LOS and being arranged to determine the relative shift in an x direction by analyzing an image of the second structures. The first COS or LOS has a different location than the second COS or LOS. The first image of the first structures' COS is analyzed to determine whether the first structures have a shift in the x direction that is out of specification, and the second image of the second structures' COS is analyzed determine whether the second structures have a shift in the y direction that is out of specification.

In a specific aspect, the first and second images are acquired together in a same field of view. In another aspect, analyzing the first image comprises (i) when it is determined that the first structures fail to have a 180 rotational or mirror symmetry, determining that the first structures are out of specification; and (ii) when it is determined that the second structures fail to have a 180 rotational or mirror symmetry, determining that the second structures are out of specification. In another feature, analyzing the first image and analyzing the second image each includes (i) using outside edges of each region of interest of the first or second image to determine a COS or LOS for a first set of substructures and a COS or LOS for a second set of substructures, and (ii) when the COS or LOS of the first set of substructures differs from the COS or LOS of the second set of substructures by more than a predetermined amount, determining that the corresponding structures are out of specification. In a further aspect, the first set of substructures are formed from a first layer and the second set of substructures are formed from a second layer.

In yet another implementation, analyzing the first image and analyzing the second image each includes (i) for a first set of substructures, selecting an initial COS or LOS between a plurality of regions of interest, (ii) for the first set of substructures, automatically placing its 180 degree or mirror counterpart based on the initial COS or LOS, respectively, for each of the first and second images, (iii), for the first set of substructures, continuing to move the initial COS or LOS until a best correlation is found between the first substructures and their counterpart, (iv) repeating operations (i) through (iii) for a second set of substructures, (v) when a best correlation is found for both the first and second substructures and when the COS or LOS of the first set of substructures differs from the COS or LOS of the second set of substructures by more than a predetermined amount, determining that the corresponding first structures are out of specification. In a further aspect, the first set of substructures are formed from a first layer and the second set of substructures are formed from a second layer.

In a further method embodiment, the overlay error between two or more successive layers of a substrate is determined. An image is acquired of a plurality of first structures formed in a first semiconductor layer and having a first center of symmetry (COS) or line of symmetry (LOS) and a plurality of second structures formed in a second semiconductor layer and having a second COS or LOS. The first COS or LOS is designed to have a known offset from the second COS or LOS so that the overlay error can be determined by acquiring an image of the first and second structures and then analyzing a shift between the first and second COS's or LOS's in the image and comparing the shift to the known offset. The image of the first and second structures' COS or LOS is analyzed to determine whether there is an overlay error between the first and second structures that is out of specification.

In a specific implementation, the first structures have a first LOS about which the first structures have a mirror symmetry or the first structures have a 180° rotational symmetry with respect to the first COS, and the second structures have a first LOS about which the second structures have a mirror symmetry or the second structures have a 180° rotational symmetry with respect to the second COS. In another implementation, the first and second structures are in the form of device structures. In another embodiment, a one of the first or second structures has a 180° rotational symmetry with respect to its COS and the other one of the first or second structures' has a mirror symmetry with respect to its LOS. In another aspect, the first structures and the second structures together are variant with a 180° rotational asymmetry or together have a mirror asymmetry.

These and other features and advantages of the present invention will be presented in more detail in the following specification of the invention and the accompanying figures which illustrate by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not by way of limitation.

FIG. **1** is a top plan view of a box-in-box type overlay mark.

FIG. **2** is a top plan view of overlay targets for measuring overlay error between two different process layers in both an x and y direction in accordance with one embodiment of the present invention.

FIG. **3** is a diagrammatic top view an overlay target, wherein one of its x and y direction structures has a 180° rotational symmetry while the other of its x and y direction structures has a mirror symmetry, in accordance with an alternative embodiment of the present invention.

FIG. **4**A is a diagrammatic top view of an overlay target in accordance with a specific implementation of the present invention.

FIG. **4**B is a diagrammatic top view of an overlay target in accordance with an alternative implementation of the present invention.

FIGS. **4**C through **4**E together illustrate a technique for forming combination dummy and overlay structures, as well as example structures, in accordance with specific implementations of the present invention.

FIG. **5** is a flowchart illustrating a procedure for inspecting targets in accordance with techniques of the present invention.

FIG. **6** is a flowchart illustrating the operation of FIG. **5** for determining whether a target is out of specification in accordance with a specific implementation of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to a specific embodiment of the invention. An example of this embodiment is illustrated in the accompanying drawings. While the invention will be described in conjunction with this specific embodiment, it will be understood that it is not intended to limit the invention to one embodiment. On the contrary, it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. The present invention may be practiced without some or all of these specific details. In other instances, well known process operations have not been described in detail in order not to unnecessarily obscure the present invention.

In general, the present invention provides semiconductor targets for determining an overlay error between two process layers or a shift between two sets of structures on the same layer, where the target structures are designed with a known relationship between their symmetry characteristics. Although the following target examples are shown to have structures on two layers for measuring overlay, it is readily apparent that each target may include two sets of structures on the same layer for determining a shift error between such set of structures.

FIG. **2** is a top plan view of overlay targets for measuring overlay error between two different process layers in both an x and y direction in accordance with one embodiment of the present invention. As shown, a first target **202** is arranged for measuring an overlay error between a set of first structures **206** in a first layer and a set of second structures **208** in a second layer with respect to an x direction. A second target **204** is arranged for measuring an overlay error between a set of first structures **212** in a first layer and a set of second structures **214** in a second layer with respect to a y direction.

In this embodiment, each of the x and y targets are designed so that its first structures have a same 180° rotational center of symmetry as its second structures although the x direction target **202** is designed to have a center of symmetry (COS) **210** that has a different location than the y direction target **204** COS **214**. For example, the x direction target **202** has first structures that are divided into two groups **206**a and **206**b that are positioned with respect to each other so that if they were rotated 180° about a center of symmetry **210**, the first structures would have a same appearance before and after such rotation. The x direction target **204** also includes second structures **208** that are divided into two groups **208**a and **208**b that are positioned with respect to each other so that if they were rotated 180° about a center of symmetry **210**, the first structures would have a same appearance before and after such rotation. In this illustration, the COS of the first structures is at the same position as the COS of the second structures. When a overlay error is present within a target, the COS of the first structures of such target is shifted from the COS of the second structures. This shift is called the overlay error.

The overlay error in separate x and y targets may be determined based on a priori knowledge that each target is designed to have structures in each layer that have a 180° rotational symmetry about a same COS. Any shift between the COS's of the first and second layer structures may be imaged and measured as an overlay error. In alternative embodiments, the x and/or y targets of FIG. **2** may be arranged so that the first and second structures have a COS with a known offset. In this case, if the shift does not match the known offset, the amount of variance corresponds to the overlay error.

FIG. **3** is a diagrammatic top view an overlay target **300**, wherein one of its x and y direction structures has a 180° rotational symmetry while the other of its x and y direction structures has a mirror symmetry, in accordance with an alternative embodiment of the present invention. As shown, the target **300** includes x direction structures **306** and **308** and y direction structures **302** and **304**. The x direction structures include a first set of structures **306**a and **306**b on a first layer and a second set of structures **308**a and **308**b on a second layer. The y direction structures include a first set of structures **302**a and **302**b on a first layer and a single structure **304** on a second layer. The first and second structures of the x direction target are designed to have a 180° rotational symmetry with respect to a same center of symmetry (COS) **310**, while the first and second structures of the y direction target are designed to have a mirror symmetry with respect to a same line of symmetry (LOS) **312**. A shift between either the COS's or LOS's of the first and second layer structures can be imaged and measured to determine an overlay error in the x or y direction, respectively. In alternative embodiments, the x and/or y targets of FIG. **3** may be arranged so that the first and second structures have COS's or LOS's with a known offset. In this case, if the shift does not match the known offset, the amount of variance corresponds to the overlay error.

Targets having flexible symmetry characteristics may be in the form of device structures. In other words, device structures which have inherent symmetrical properties, such as a 180 rotational symmetry and/or a mirror symmetry for structures in a first and second layer may be used. These structures may also have a known offset between their COS's or LOS's. Such devices may be identified by the designer and identified by tags in the design layout. Alternatively, such "target" devices may be located manually or automatically after fabrication.

The target structures of the present invention may have any suitable shape and arrangement so as to provide flexible symmetry characteristics. FIGS. **4**A and **4**B illustrate various examples of target shapes and arrangements. Although the targets are shown as having structures on a first layer with a same COS as structures on a second layer, the first and second layer structures may easily be designed to have different COS's. These FIGS. **4**A and **4**B are merely meant to illustrate the different shapes that the targets of the present invention may take.

FIG. **4**A is a diagrammatic top view of an overlay target in accordance with a specific implementation of the present invention. Each set of target structures in each layer may include any number and shape of structures. A first set of structures in a first layer (shaded black) includes structure **402**a through **402**d which have a center of symmetry **410**. Structures **402**a and **402**c are **7** sided polygons, while structures **402**b and **402**d are triangles. A second set of structures in a second layer (shaded gray) includes structure **404**a through **404**d which have the same center of symmetry **410** as the first set of structures in the first layer. Structures **404**a and **404**c are star shaped polygons, while structures **404**b and **404**d are cross shaped polygons. In one embodiment of the present invention, the center of symmetry of the first layer structures is offset from the center of symmetry of the second layer structures by a known distance (not shown).

FIG. **4**B is a diagrammatic top view of an overlay target in accordance with an alternative implementation of the present invention. In this embodiment, each structure includes a plurality of horizontal or vertical lines in two different layers. A first layer is shaded black, while a second layer is shaded gray. Each horizontal and vertical line may also be formed from a plurality of segments (not shown). As shown, horizontal structures **452**a, **452**b, **452**e and **452**f and vertical structures **452**b, **452**c, **452**d, **452**g, and **452**h have a same center of symmetry **454**. Additionally, the different layers of each set of vertical and horizontal structures are shown as having a same center of symmetry. In a specific implementation of the present invention, the center of symmetry of the horizontal structures is offset from the center of symmetry vertical structures by a known distance (not shown). In another specific implementation of the present invention, the center of symmetry of the first layer structures (from the horizontal and/or vertical structures) is offset from the center of symmetry of the second layer structures (from the horizontal and/or vertical structures) by a known distance (not shown).

The target rules preferably include a requirement that the target be placed in a layer which is measurable or inspectable by a particular type of tool. For example, the target may have to be on a top layer or be covered with only optically transparent layers so that the target may be inspected by an optical tool. In other applications, the target may be required to be underneath an opaque layer so that the opaque layer's conformance to the underlying target may be inspected and/or measured. Additionally, each inspection, review, or metrology tool typically has a size constraint as to the measured or inspected structure. That is, structures below a particular size cannot be seen. Therefore, the targets must be sized so that they can be measured or inspected by the relevant tool.

The targets of the present invention described herein may be placed in any suitable space on the wafer. By way of examples, the targets may be placed in the scribe line or within the dies themselves. When targets are placed in a die, the die layout may also be analyzed to determine whether particular portions or areas have a characteristic which negatively or positively affects metrology or inspection results, as compared with other areas of the die layout. For example, particular layout characteristics may result in more reliable or accurate metrology or inspection results. In one specific case, targets may be placed in areas which have characteristics that positively affect the metrology or inspection. In an example of such a feature characteristic, a chemical mechanical polishing (CMP) procedure is typically tuned to achieve superior accuracy with a particular feature density range. Thus, targets, such as overlay targets, may be placed in layout regions which are within the particular feature density range for an optimal CMP process.

The circuit designer may be aware of feature locations in the die layout which are most susceptible to error or defects. The designer may communicate the position of such features to the target placement software or layout engineer so that targets may be placed proximate to such problem features. This placement technique would likely result in a higher incidence of defect capture and more reliable resulting products.

The targets may also be placed within a dummy layer. It is common practice in semiconductor manufacturing today to include dummy structures in open areas of the circuit layout to ensure uniform pattern density. Dummy structures are generally used for optimal results in chemical mechanical polishing and other semiconductor manufacturing processes.

In order to enable targets inside the chip area, there are significant advantages in combining the functionality of the particular metrology (or inspection) target with the purpose of the dummy structures. That is, a structure which has two components that serve both purposes of a dummy structure and a metrology (or inspection) target would efficiently utilize the open spaces of the die area to increase CMP uniformity (and other dummy requirements where applicable), as well as to provide a metrology or inspection target. Additionally, a new type of metrology or inspection may be used with such combination marks. For example, a particular design pattern's fidelity may be monitored via such combination target. That is, a designer's intent regarding a particular pattern's function or structure may be verified with respect to the pattern being combined and measured or inspected in a dummy structure.

A combination target and dummy structure can be achieved in a number of different ways. In one example of a combination dummy and overlay structure, the structures can be designed on two masks such that they form interlaced periodic structures. Any suitable types of overlay structures may be altered to have flexible COS's or LOS's as described herein. Suitably modifiable overlay targets and techniques for determining overlay with same are described in the following U.S. patents and applications: (1) U.S. Pat. No. 6,462,818, issued 8 Oct. 2002, entitled "OVERLAY ALIGNMENT MARK DESIGN", by Bareket, (2) U.S. Pat. No. 6,023,338, issued 8 Feb. 2000, entitled "OVERLAY ALIGNMENT MEASUREMENT OF WAFER", by Bareket, (3) application Ser. No. 09/894,987, filed 27 Jun. 2001, entitled "OVERLAY MARKS, METHODS OF OVERLAY MARK DESIGN AND METHODS OF OVERLAY MEASUREMENTS", by Ghinovker et al., (4) U.S. Pat. No. 6,486,954, issued 26 Nov. 2002, entitled "OVERLAY ALIGNMENT MEASUREMENT MARK" by Levy et al., (5) application Ser. No. 10/367,124, filed 13 Feb. 2004, entitled OVERLAY METROLOGY AND CONTROL METHOD, by Mike Adel et al, (6) application Ser. No. 10/785,396 filed 23 Feb. 2004, entitled APPARATUS AND METHODS FOR DETECTING OVERLAY ERRORS USING SCATTEROMETRY, by Walter D. Mieher, et al., (7) application Ser. No. 10/729,838 filed 5 Dec. 2003, entitled APPARATUS AND METHODS FOR DETECTING OVERLAY ERRORS USING SCATTEROMETRY, by Walter D. Mieher, et al., and (8) application Ser. No. 10/858,836 filed 1 Jun. 2004, entitled APPARATUS AND METHODS FOR PROVIDING IN-CHIP MICROTARGETS FOR METROLOGY OR INSPECTION, by Avi Cohen et al. These patents and applications are all incorporated herein by reference in their entirety.

An overlay type combination and dummy structure includes two components one on a first layer or mask and one on a second layer or mask. Each component preferably complies with the requirements for a dummy structure of the process step associated with that layer or mask. A further example may be a case where these periodic structures are aligned such that the component on a first mask is symmetrically positioned with respect to the component on a second mask when the masks are correctly aligned. Also, the component on a first mask may be designed to fit into the open spaces within the component on a second mask and visa versa. As a further particular example, the periodic component on the two masks could be identical but offset by half a unit cell of the periodic structure along both x and y axes. Alternatively the component on a first mask may have a different structure than the component on a second mask but is still offset by half a unit cell of the component as above. Example overlay type combination targets are shown in FIG. **4**C through **4**E.

Each component may also contain an additional coarse segmentation which is periodic and is designed to improve the contrast and information content for the metrology tool as further described in the above referenced U.S. application Ser. No. 10/367,124 by Mike Adel et al.

FIGS. **4**C through **4**E together illustrate a technique for forming combination dummy and overlay structures, as well as example structures, in accordance with specific implementations of the present invention. An open space may be filled with any suitably sized and shaped combination dummy and target structures (referred to herein as targets). As shown in FIG. **4**C, an array of targets are formed within an open area. The targets include a first set of structures on a first layer (e.g., the "+" shaped structures) and a second set of structures on a second layer (e.g., the hexagon shaped structures). Note that the first set of structures has a COS **410**, while the second set of structures have a second COS **412** that is offset from the first COS **410**.

In another technique, an array of targets may be conceptually used to fill in around actual device structures. As shown in FIG. **4**D, an array of hexagon shaped and "+" shaped structures are overlaid onto two device structures. For illustration purposes, one device structure is shaped like a star and is on a same layer as the hexagon target structures, while another device structure is shaped like an arrow and is on the same layer as the "+" shaped target structures. After the target array is overlaid with the device structures, some of the target structures are removed to accommodate the device structures. That is, target structures on one layer are removed from an area encompassing the device structure on the same layer. As shown, the "+" shaped structures are removed from an area encompassing the arrow shaped device structure, and the hexagon shaped structures are removed from an area encompassing the star shaped device structure. The target structures are removed such that a COS of each layer is maintained. For example, the first layer structures have a first COS **420** that differs from the second COS **422** of the second layer structures.

If the device structures on two different layers are overlapping, however, both layers of targets are removed from an area encompassing the two overlapping device structures as illustrated in FIG. **4**E. In this example, the target structures are also removed such that a COS of each layer is maintained. For example, the first layer structures have a first COS **430** that differs from the second COS **432** of the second layer structures.

In these combination dummy and target examples, a signal is detected from the field of views (FOV's) as represented in FIGS. **4**C-**4**E. The center of symmetries of the first and second layers are determined. In embodiments of the present invention, the center of symmetries are designed to be located at a known offset from each other so that a discrepancy can be translated into an overlay value. In alternative embodiments, a first set of structures are used to measure overlay in an x direction and a set of second structures are used to measure overlay in a y direction. The x direction structures have a center of symmetry or line of symmetry that differs from the y direction structures.

When the FOV includes both targets and devices as in FIGS. **4**D and **4**E, it is first determined which parts of the signal are noise (or device structures) and which parts correspond to the target structures. This determination may be determined in suitable manner. In one embodiment, the signal (or image generated from such signal) is compared to a design file which identifies device structures and the device structures' contribution to the signal (or image) is subtracted from the signal (or image). The resulting signal (or image) corresponds to the target which may then be assessed as previously described. Alternatively, one may manually train the metrology tool to locate targets by manually moving the tool to known target locations and identifying the targets. These identified targets can then be used by the metrology tool to search for other targets with a similar appearance using standard pattern recognition techniques. Alternatively, a representative target in the design file may be used to train the metrology tool. The representative target may also be located in a easily found position, such as the scribe line.

In general, rules for both dummy structures and the particular target type are followed when forming combination dummy and target structures. For instance, the dummy structure rules may require a particular pattern density or maximum open space size for ensuring a particular level of CMP uniformity. Additionally, the particular metrology or inspection procedure rules for the targets are followed. In one type of overlay metrology technique, the structures on two different layers are assessed to determine whether their centers of symmetry are where they should be (e.g., aligned or offset by a known distance) to thereby determine overlay. In this example, the structures are designed on two different layers and have a same center of symmetry or known offset centers of symmetry.

After a die and targets are fabricated, the targets may be inspected, reviewed, or measured in any suitable manner. FIG. **5** is a flowchart illustrating a procedure **500** for inspecting targets fabricated from a layout pattern generated in accordance with techniques of the present invention. Initially, each target is inspected or measured to determine whether a process is out of specification in operation **502**. It is then determined whether a process is out of specification in operation **503**. If a process is not out of specification, the inspection, review, or measurement procedure ends.

If a process is out of specification, a number of techniques may be implemented to alleviate the problem. In a first technique, a subsequent process may be adjusted to compensate for the process which is out of specification in operation **504**. For example, if it is determined that the photoresist pattern is misaligned in any portion, the photoresist may then be stripped and reapplied in a corrected pattern to eliminate the misalignment. The subsequent process is then performed so as to continue fabrication of the same die in operation **506**. For example, the wafer may be patterned. In a second technique, processing of the die may be halted in operation **508**. The die may then be discarded in operation **510**. The process which is out of specification may then be adjusted for subsequent die(s) in operation **512**.

One may determine whether the targets with flexible COS's and/or LOS's of the present invention are within specification in any suitable manner. FIG. **6** is a flow chart illustrating the operation **503** of FIG. **5** for determining whether a target is out of specification in accordance with a specific implementation of the present invention. Although this procedure is described with respect to a target having structures with a 180° rotational COS, of course, this procedure may be easily modified for structures with mirror symmetry. This procedure may also be applied to determining an alignment error between two sets of structures on the same layer, rather than an overlay error on two different layers as illustrated.

In the illustrated example of FIG. **6**, the center of either X or Y target structures are initially moved to the center of the FOV of the inspection tool in operation **602**. The region of interests (ROI's) of each layer are then determined in operation **604**. The x target structures of FIG. **2** will be used to illustrate the procedure of FIG. **6**. For example, four ROI's may be formed for the x direction target structures **206**a, **206**b, **208**a and **208**b of FIG. **2**, as represented by the dotted lines. The dotted line **202** may represent the FOV of the inspection tool, while the cross **210** represents the center of the x target structures.

The COS for each set of structures **206** and **208** from the first and second layers, respectively, may be determined using any suitable technique. For example, an edge technique may be utilized to determine COS for the structures in each layer. In the illustrated embodiment, the outside edges of each ROI of each layer are used to determine the COS for each layer in operation **606**. For the structures **206** and **208**, the outside edges of each ROI may be determined and then the edges are then used to find a center position between the outside edges of each set of structures (e.g., between structures **206**a and structures **206**b). For structures having subresolution features (e.g., target of FIG. **4**B), the edge of each set of subresolution lines (e.g., the first layer lines of set **452**a) would be measured as a single edge.

Another COS determination technique is referred to as the correlation technique. In this technique, an initial COS position is estimated between the ROI's of the structures of each layer in operation **608**. As shown for the structures **206**, an initial estimate of COS **210** may be positioned between structures **206**a and **206**b. Two linear arrays are then obtained by measuring across the two sets of structures at positions that are equal distances from the initial COS. The structures **206**a and **206**b will tend to each result in a periodic signal with three peak intensity values. The two obtained linear arrays are then flipped horizontally and vertically and matched and a metric of correlation such as the product is calculated. The arrays are moved with respect to one another and the metric is calculated for each offset. The metric is then plotted and the correct COS is located by finding the maximum of the correlation metric. Intelligent searching algorithms (e.g., a binary search) may also be used to efficiently locate the correct COS position.

Said in another way, for each ROI set of each layer, its 180° rotation counterpart is automatically placed based on the initial COS in operation **610**. The COS is continually moved for each layer until the best correlation is found between the rotated image and original images of each layer in operation **612**. After the best correlation is found, the COS is found.

After the COS is found using any suitable technique, it is then determined whether the COS of the first layer structures differs from the COS of the second layer structures by more than a predetermined value in operation **614**. If they do not differ by more than the predetermined value, it is determined that the x or y target under analysis in not out of specification in operation **618**. However, if they do differ by more than the predetermined amount, it is determined that the x or y target under analysis is out of specification in operation **616**. The procedure for determining whether the target is out of specification then ends.

The techniques of the present invention may be implemented in any suitable combination of software and/or hardware system. Regardless of the system's configuration, it may employ one or more memories or memory modules configured to store data, program instructions for the general-purpose inspection operations and/or the inventive techniques described herein. The program instructions may control the operation of an operating system and/or one or more applications, for example. The memory or memories may also be configured to store layout patterns, layout constraint rules and target rules.

Because such information and program instructions may be employed to implement the systems/methods described herein, the present invention relates to machine readable media that include program instructions, state information, etc. for performing various operations described herein. Examples of machine-readable media include, but are not limited to, magnetic media such as hard disks, floppy disks, and magnetic tape; optical media such as CD-ROM disks; magneto-optical media such as floptical disks; and hardware devices that are specially configured to store and perform program instructions, such as read-only memory devices (ROM) and random access memory (RAM). The invention may also be embodied in a carrier wave traveling over an appropriate medium such as airwaves, optical lines, electric lines, etc. Examples of program instructions include both machine code, such as produced by a compiler, and files containing higher level code that may be executed by the computer using an interpreter.

Although the foregoing invention has been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. Therefore, the described embodiments should be taken as illustrative and not restrictive, and the invention should not be limited to the details given herein but should be defined by the following claims and their full scope of equivalents.

What is claimed is:

1. A semiconductor target for determining a relative shift between two or more successive layers of a substrate, the target comprising:

a plurality of first structures formed in a first layer, and the first structures having a first center of symmetry (COS), the first structures being aperiodic; and

a plurality of second structures formed in a second layer, and the second structures having a second COS, the second structures being aperiodic,

wherein the difference between the first COS and the second COS corresponds to an overlay error between the first and second layer and wherein the first and second structures have a 180° rotational symmetry, without having a 90° rotational symmetry, with respect to the first and second COS, respectively.

2. The target of claim **1**, wherein the first and second structures are in the form of device structures.

3. The target of claim **1**, wherein the first structures include a first set of sub-structures that each has a first shape and a second set of sub-structures that each has a second shape that differs from the first shape.

4. The target of claim **3**, wherein the second structures include a third set of sub-structures that each has a third shape and a fourth set of sub-structures that each has a fourth shape that differs from the third shape.

5. The target of claim **4**, wherein the first, second, third, and fourth shapes differ from each other.

6. The target of claim **1**, wherein the first and second structures are image-based overlay targets.

7. The target of claim **1**, wherein a difference between the first COS and the second COS that is greater than a known offset between the first and second COS corresponds to an overlay error between the first and second layer.

8. The target of claim **1**, further comprising an opaque layer deposited over the first or second structures.

9. The target of claim **1**, wherein the first or second layer is a dummy layer.

10. A wafer having the target of claim **1** and a plurality of dies, wherein the target is formed in a scribe line located between at least some of the dies.

11. A wafer having the target of claim **1** and a plurality of dies, wherein the target is formed within a one of the dies.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : RE45,245 E
APPLICATION NO. : 13/875160
DATED : November 18, 2014
INVENTOR(S) : Mark Ghinovker

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page, first column, "Related U.S. Application Data" Section, Item (60), delete the entire present Item (60) and enter the following updated Item (60):

(60) Reissue of application 12/410,317, now Pat. No. 8,138,498, which is a Division of application No. 11/227,764, filed on Sep. 14, 2005, now Pat. No. 7,541,201, which is a continuation-in-part of application No. 10/785,396, now Pat. No. 7,385,699, which is a continuation-in-part of application No. 10/729,838, filed on Dec. 5, 2003, now Pat. No. 7,317,531. Said application No. 11/227,764 is a continuation-in-part of application No. 09/894,987, filed on Jun. 27, 2001, now Pat. No. 7,068,833, and a continuation-in-part of application No. 10/729,838.

In the Specification

In column 1, Lines 40-54, replace

"for all purposes. Application Ser. No. 12/410,317 also is a... application Ser. No. 60/498,524, filed on 27 Aug. 2003."

with

--for all purposes. Application No. 11/227,764, filed 14 September 2005, now U.S. Pat. No. 7,541,201, issued on 2 June 2009 is also a Continuation-in-Part application and claims priority of application Ser. No. 10/785,396, filed on 23 February 2004, now U.S. Pat. No. 7,385,396, issued 10 June 2008, which is a Continuation-in-Part application and claims priority of application Ser. No. 10/729,838, filed on 5 December 2003, now U.S. Pat. No. 7,317,531, issued on 8 Jan. 2008, which claims priority of application Ser. No. 60/431,314, filed on 5 Dec. 2002, application Ser. No. 60/440,970, filed on 17 Jan. 2003, application Ser. No. 60/504,093, filed on 19 Sept. 2003, application Ser. No. 60/449,496, filed 22 Feb. 2003, and application Ser. No. 60/498,524, filed on 27 Aug.
2003.--

Signed and Sealed this
Twentieth Day of October, 2015

Michelle K. Lee

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Director of the United States Patent and Trademark Office