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(54) **SPACER STRUCTURES OF A SEMICONDUCTOR DEVICE**

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H01L 27/088	(2006.01)

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See application file for complete search history.

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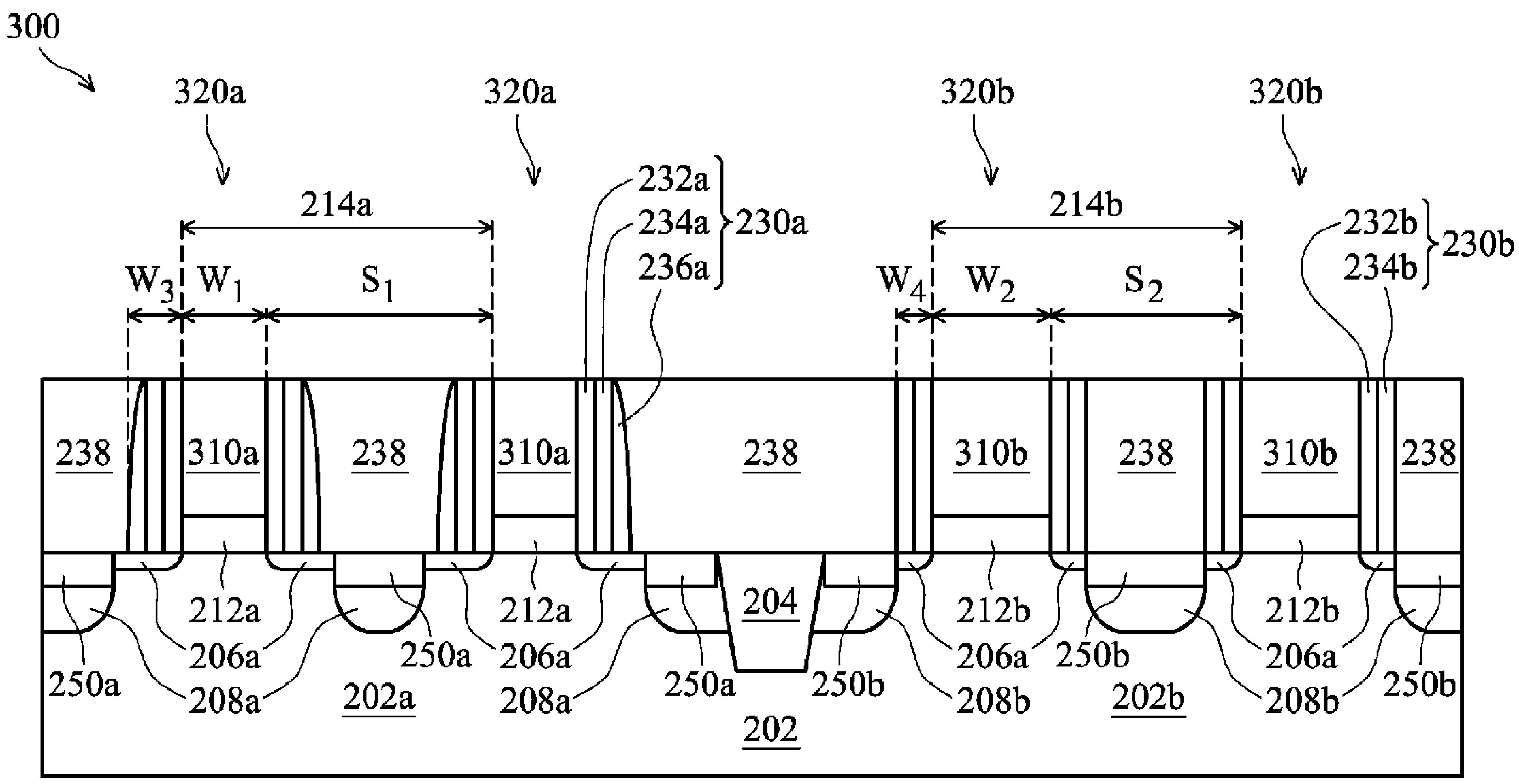
(57) **ABSTRACT**

The disclosure relates to spacer structures of a semiconductor device. An exemplary structure for a semiconductor device comprises a substrate having a first active region and a second active region; a plurality of first gate electrodes having a gate pitch over the first active region, wherein each first gate electrode has a first width; a plurality of first spacers adjoining the plurality of first gate electrodes, wherein each first spacer has a third width; a plurality of second gate electrodes having the same gate pitch as the plurality of first gate electrodes over the second active region, wherein each second gate electrode has a second width greater than the first width; and a plurality of second spacers adjoining the plurality of second gate electrodes, wherein each second spacer has a fourth width less than the third width.

21 Claims, 13 Drawing Sheets



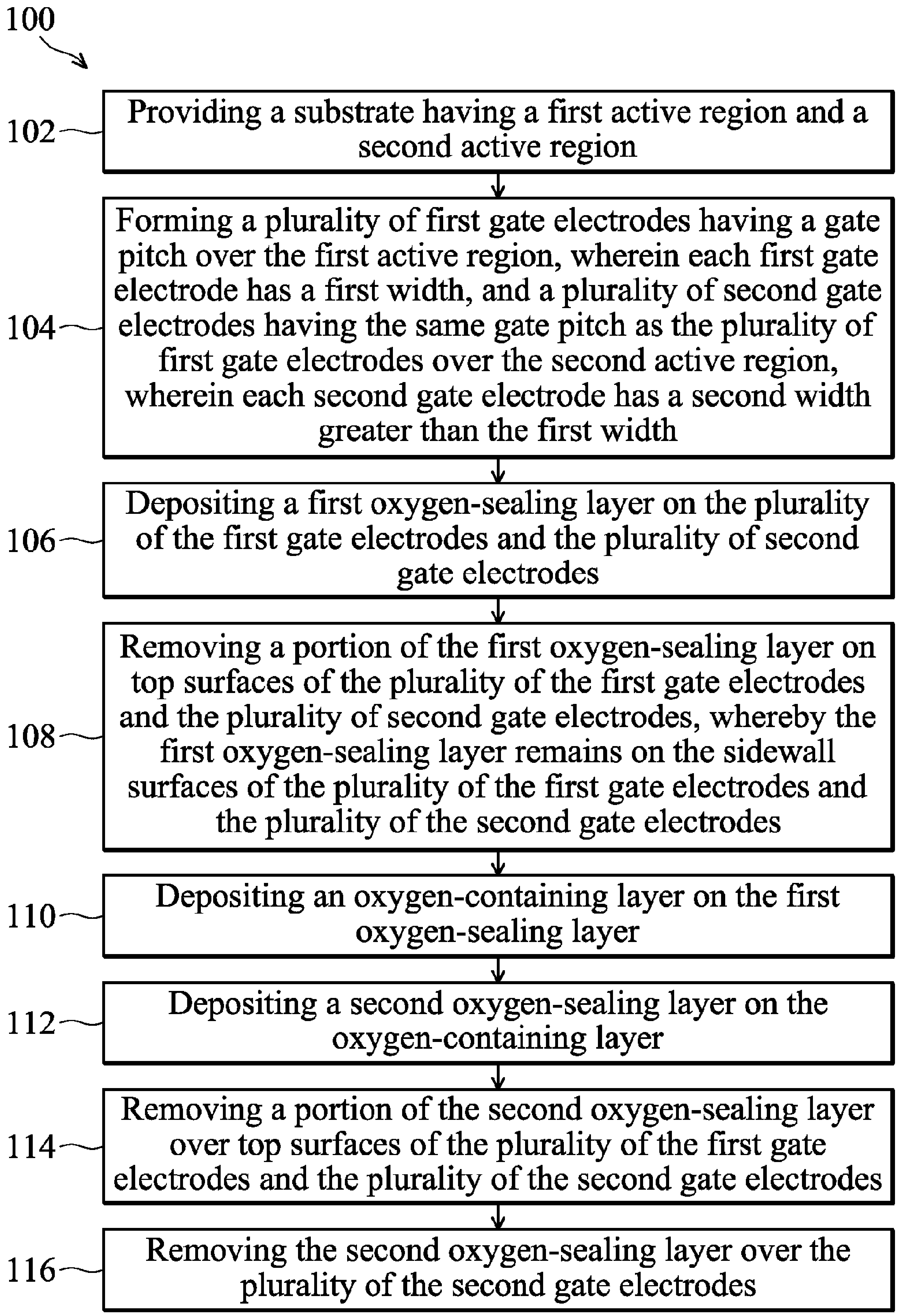

100
102
Providing a substrate having a first active region and a second active region
104
Forming a plurality of first gate electrodes having a gate pitch over the first active region, wherein each first gate electrode has a first width, and a plurality of second gate electrodes having the same gate pitch as the plurality of first gate electrodes over the second active region, wherein each second gate electrode has a second width greater than the first width
106
Depositing a first oxygen-sealing layer on the plurality of the first gate electrodes and the plurality of second gate electrodes
108
Removing a portion of the first oxygen-sealing layer on top surfaces of the plurality of the first gate electrodes and the plurality of second gate electrodes, whereby the first oxygen-sealing layer remains on the sidewall surfaces of the plurality of the first gate electrodes and the plurality of the second gate electrodes
110
Depositing an oxygen-containing layer on the first oxygen-sealing layer
112
Depositing a second oxygen-sealing layer on the oxygen-containing layer
114
Removing a portion of the second oxygen-sealing layer over top surfaces of the plurality of the first gate electrodes and the plurality of the second gate electrodes
116
Removing the second oxygen-sealing layer over the plurality of the second gate electrodes

FIG. 1

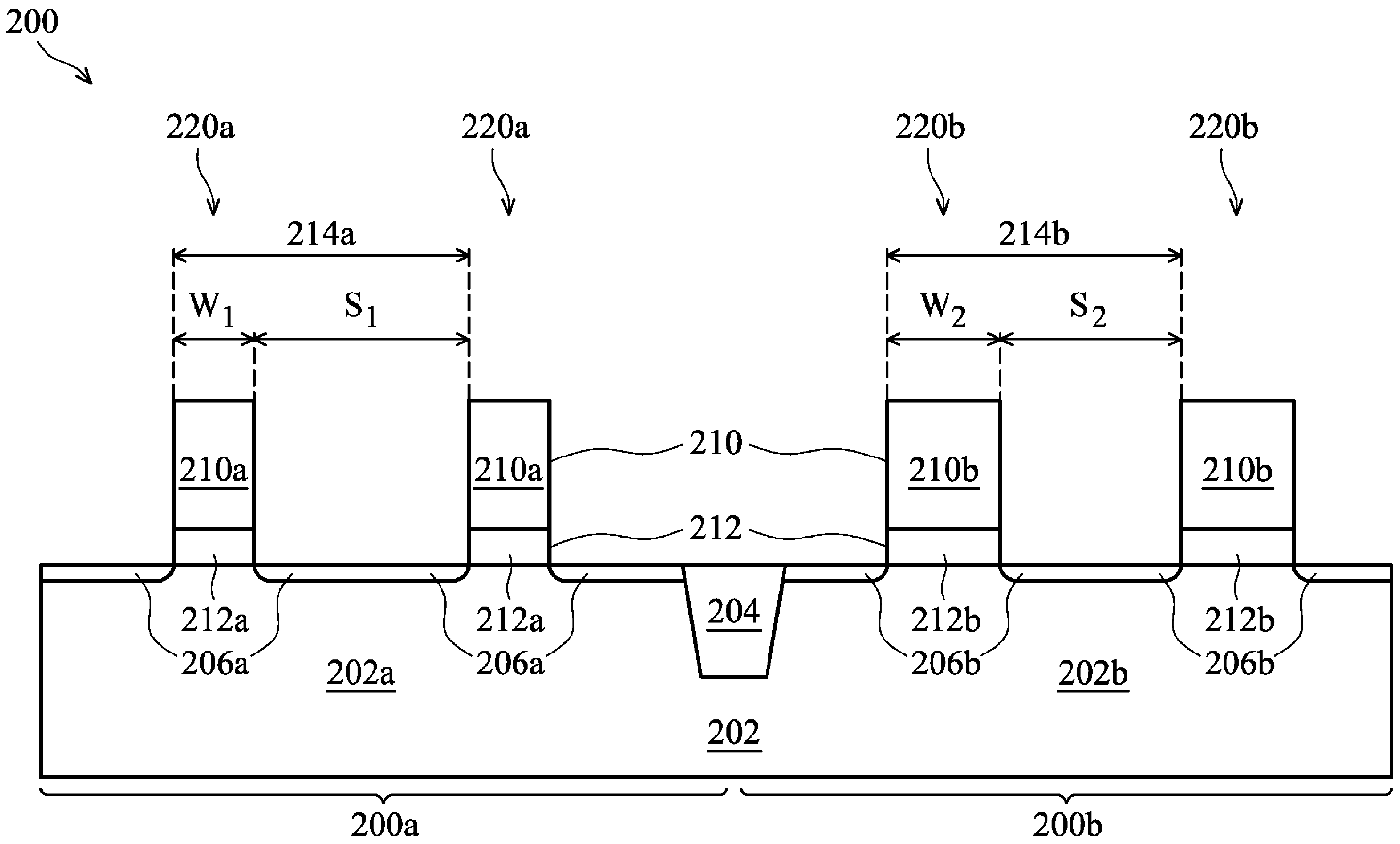

200
220a
220a
220b
220b
214a
214b
W_1
S_1
W_2
S_2
210a
210a
210
210b
210b
212
212a
212a
212b
212b
206a
206a
206b
206b
204
202a
202b
202
200a
200b

FIG. 2A

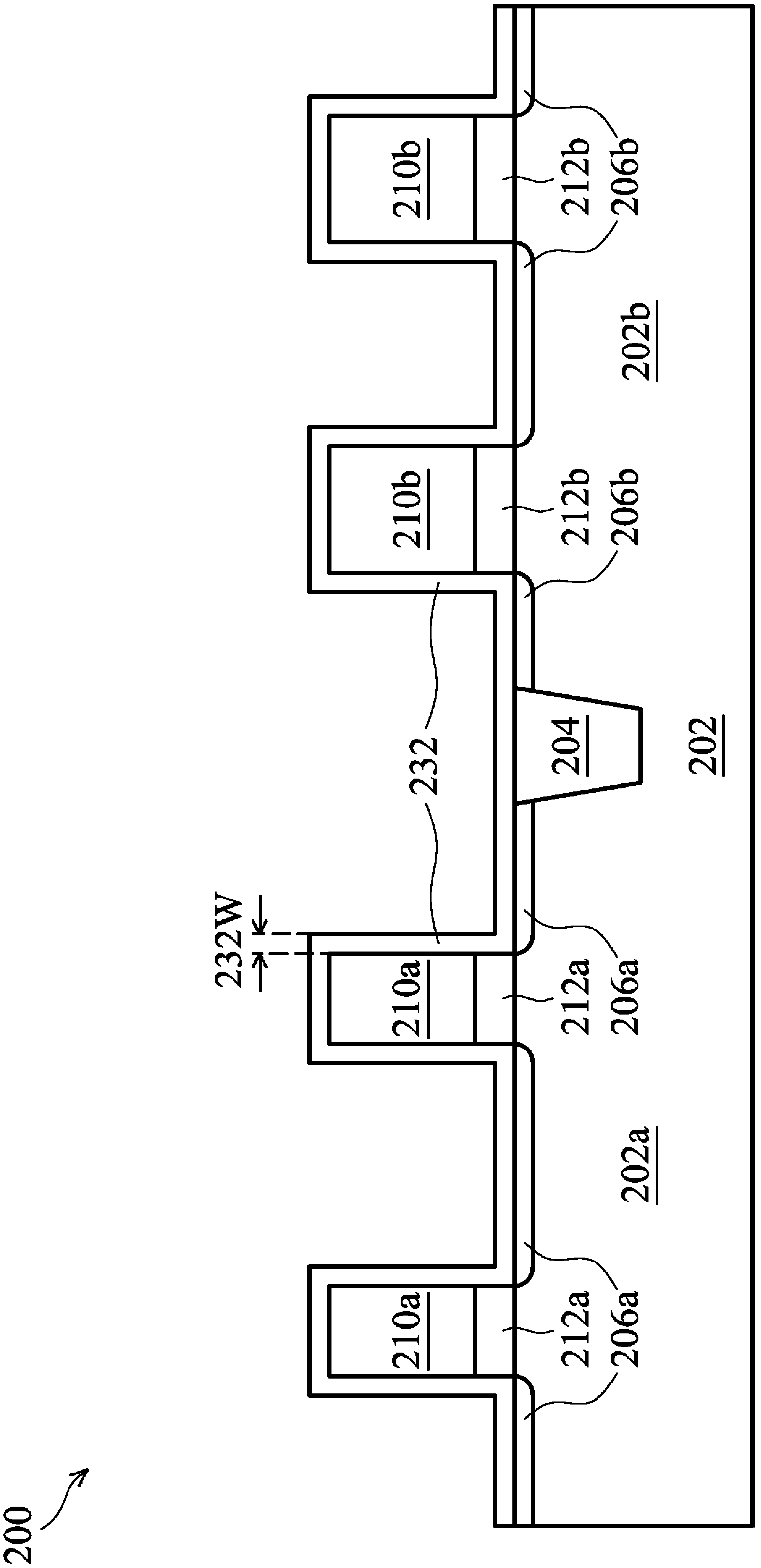

200
210a
212a
206a
202a
210a
212a
206a
232W
232
204
202
210b
212b
206b
202b
210b
212b
206b

FIG. 2B

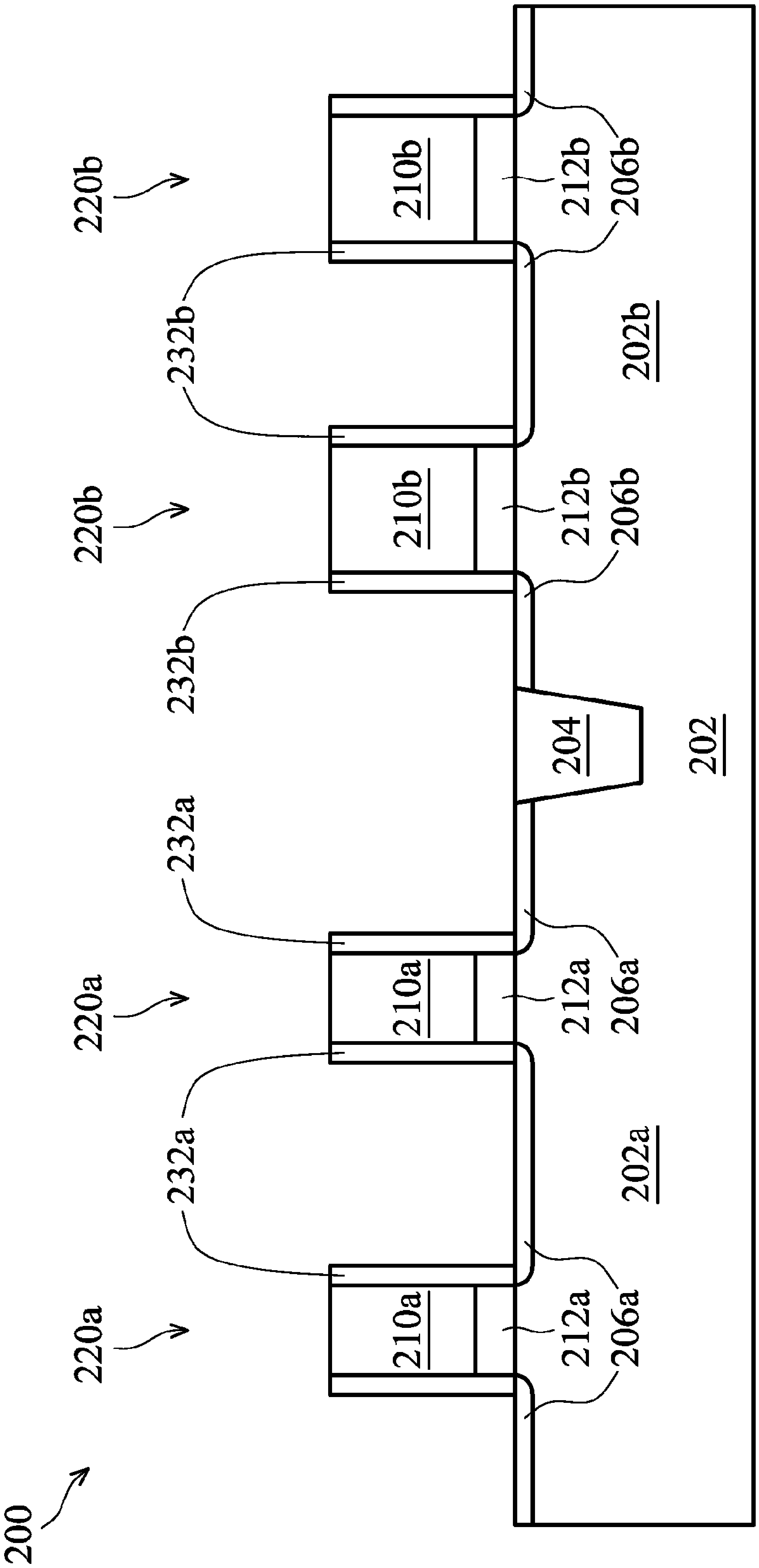

200
220a
210a
212a
206a
232a
202a
220a
210a
212a
206a
232a
204
202
232b
220b
210b
212b
206b
232b
202b
220b
210b
212b
206b

FIG. 2C

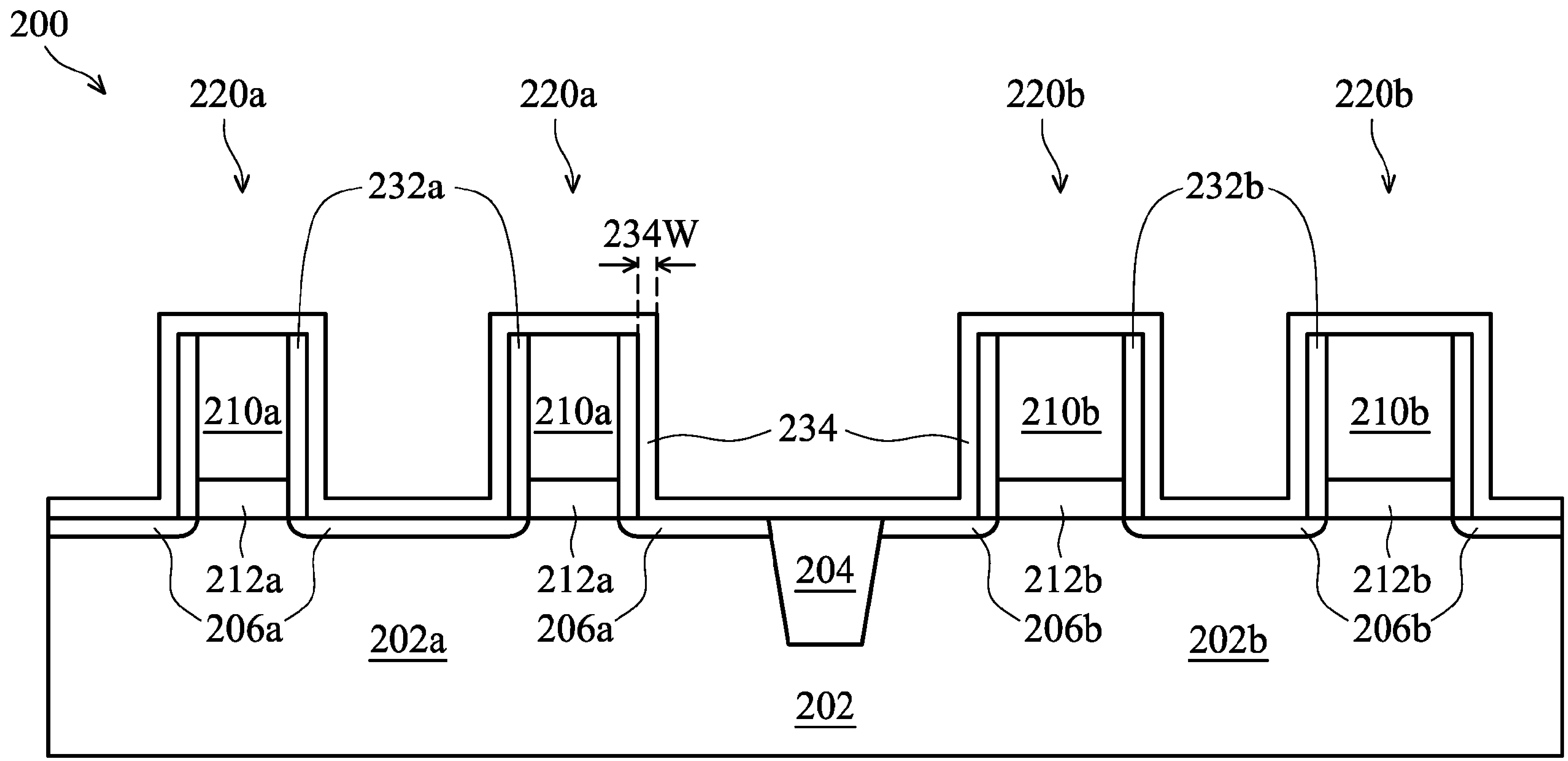

200
220a
220a
220b
220b
232a
232b
234W
210a
210a
234
210b
210b
204
212a
206a
212a
206a
212b
206b
212b
206b
202a
202b
202

FIG. 2D

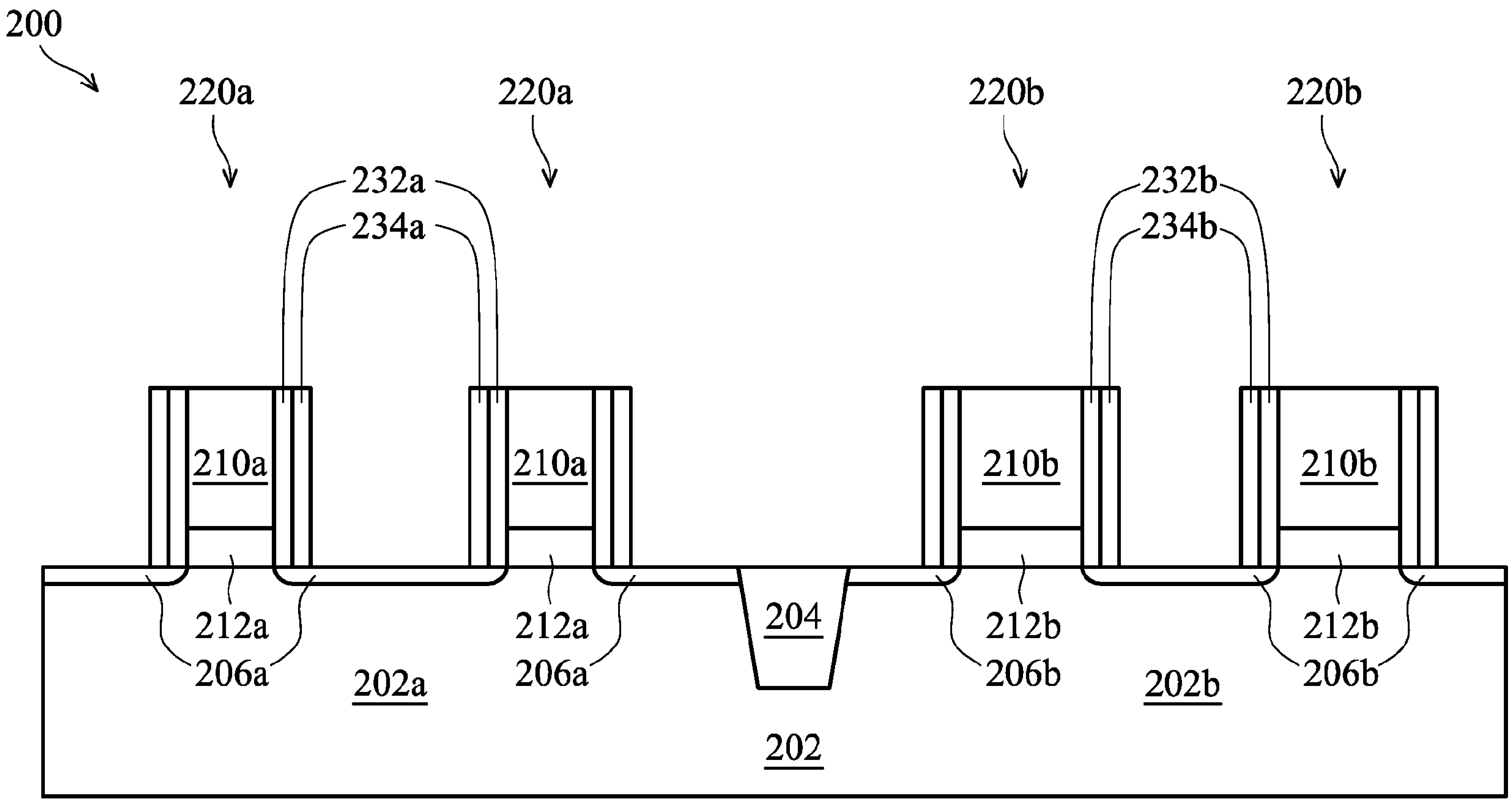

200
220a
220a
220b
220b
232a
234a
232b
234b
210a
210a
210b
210b
212a
206a
212a
206a
204
212b
206b
212b
206b
202a
202b
202

FIG. 2E

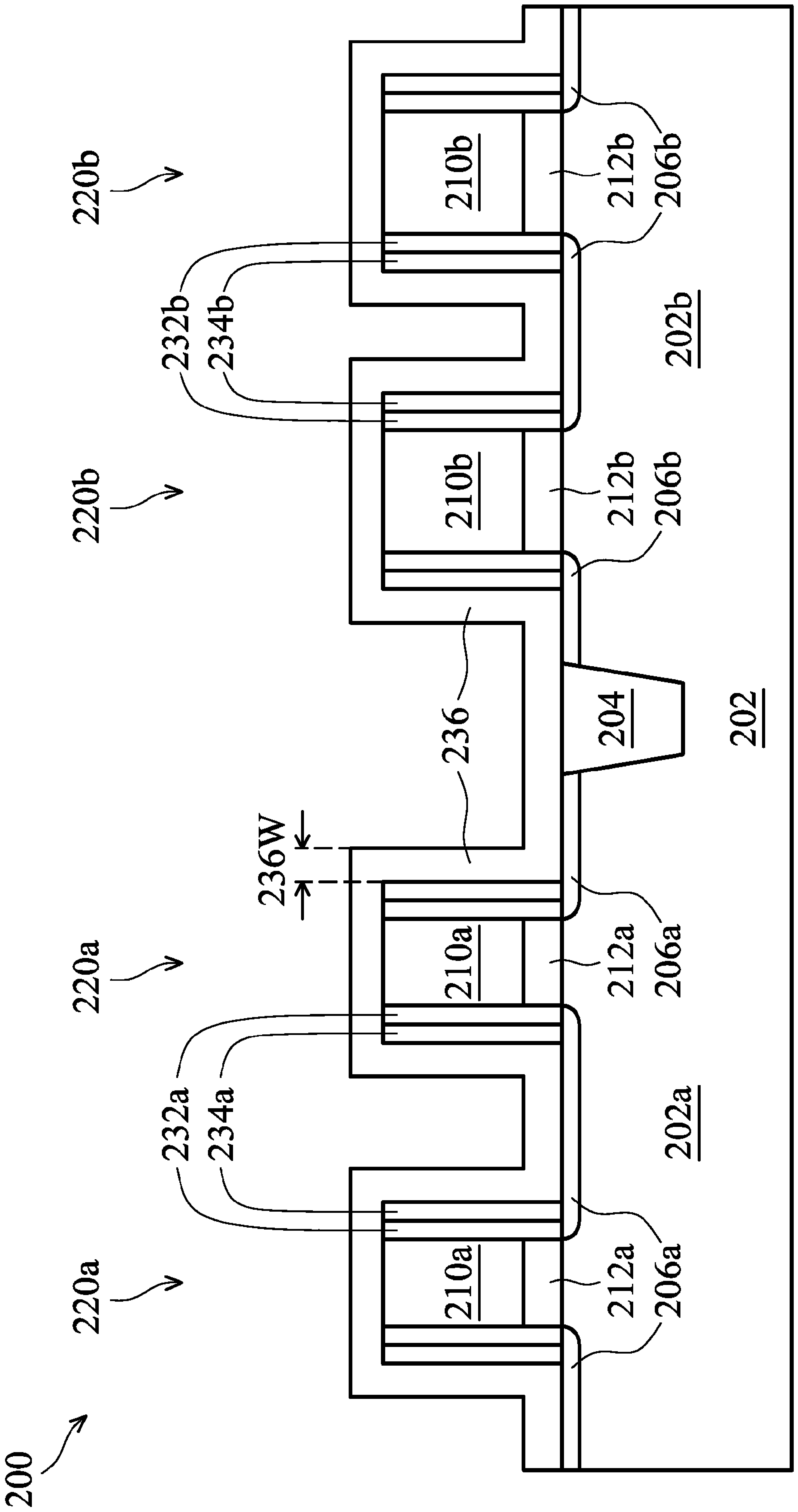

200
220a
220a
220b
220b
232a
234a
232b
234b
236W
236
236
210a
210a
210b
210b
212a
212a
212b
212b
206a
206a
206b
206b
202a
202b
204
202

FIG. 2F

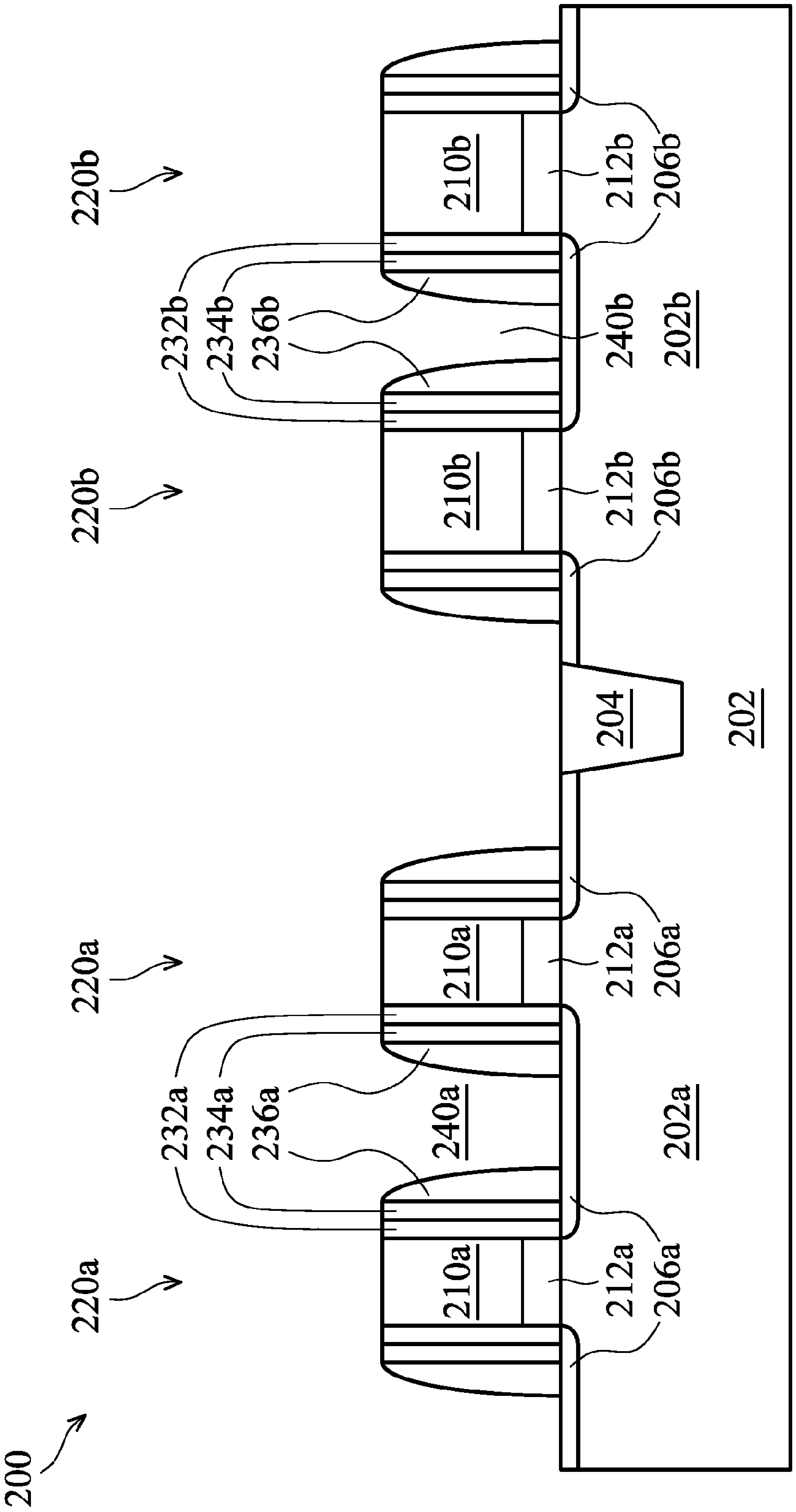

200
220a
220a
220b
220b
232a
234a
236a
232b
234b
236b
210a
210a
210b
210b
212a
212a
212b
212b
206a
206a
206b
206b
240a
240b
202a
202b
204
202

FIG. 2G

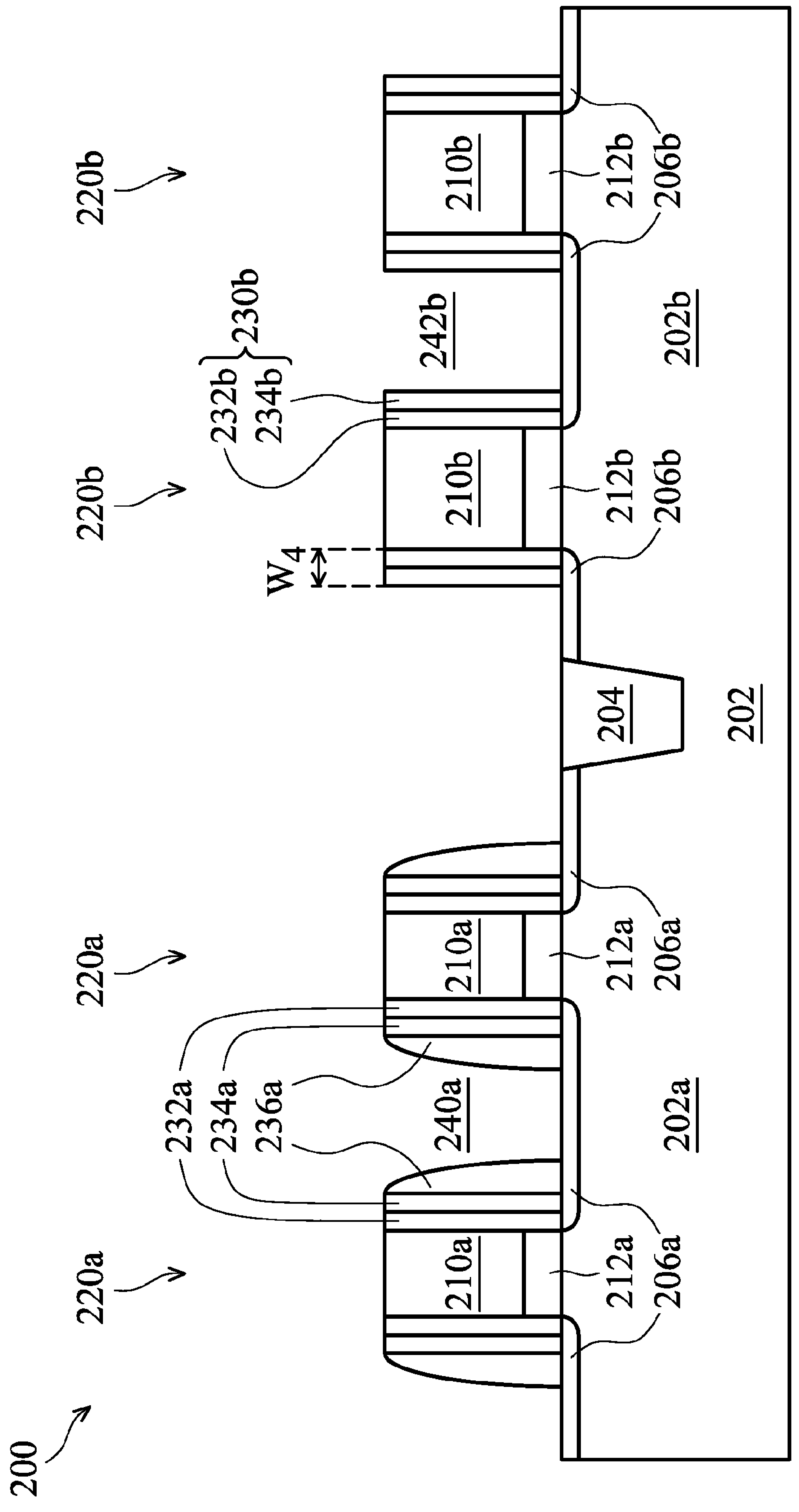

200
220a
220a
220b
220b
232a
234a
236a
240a
210a
210a
212a
212a
206a
206a
202a
204
202
W4
232b
234b
230b
242b
210b
210b
212b
212b
206b
206b
202b

FIG. 2H

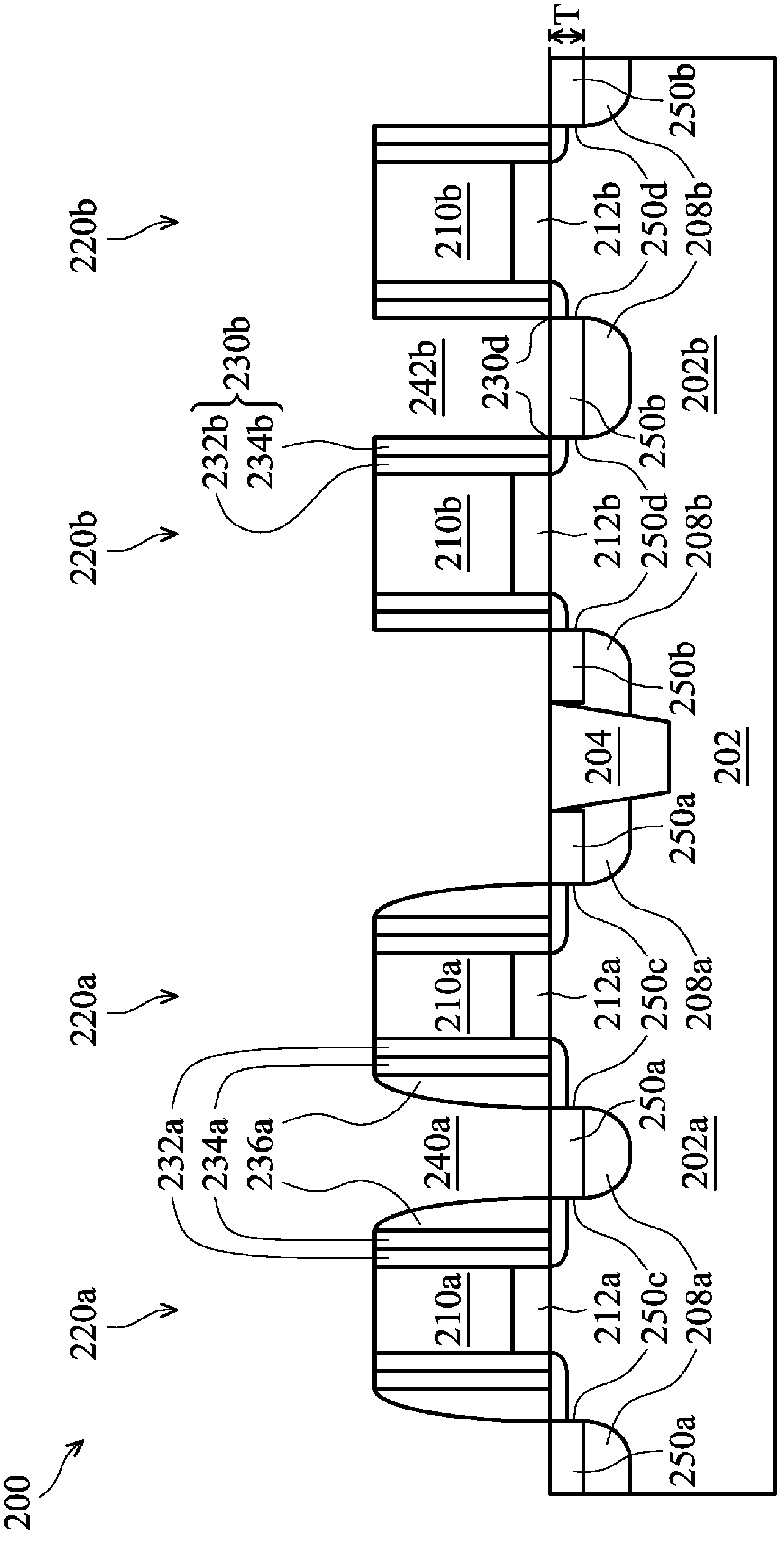

200
220a
220a
220b
220b
232a
234a
236a
240a
232b
234b
230b
242b
230d
210a
210a
210b
210b
212a
212a
212b
212b
250a
250a
250a
250b
250b
250b
250c
250c
250d
250d
208a
208a
208b
208b
202a
202
202b
204
T

FIG. 2I

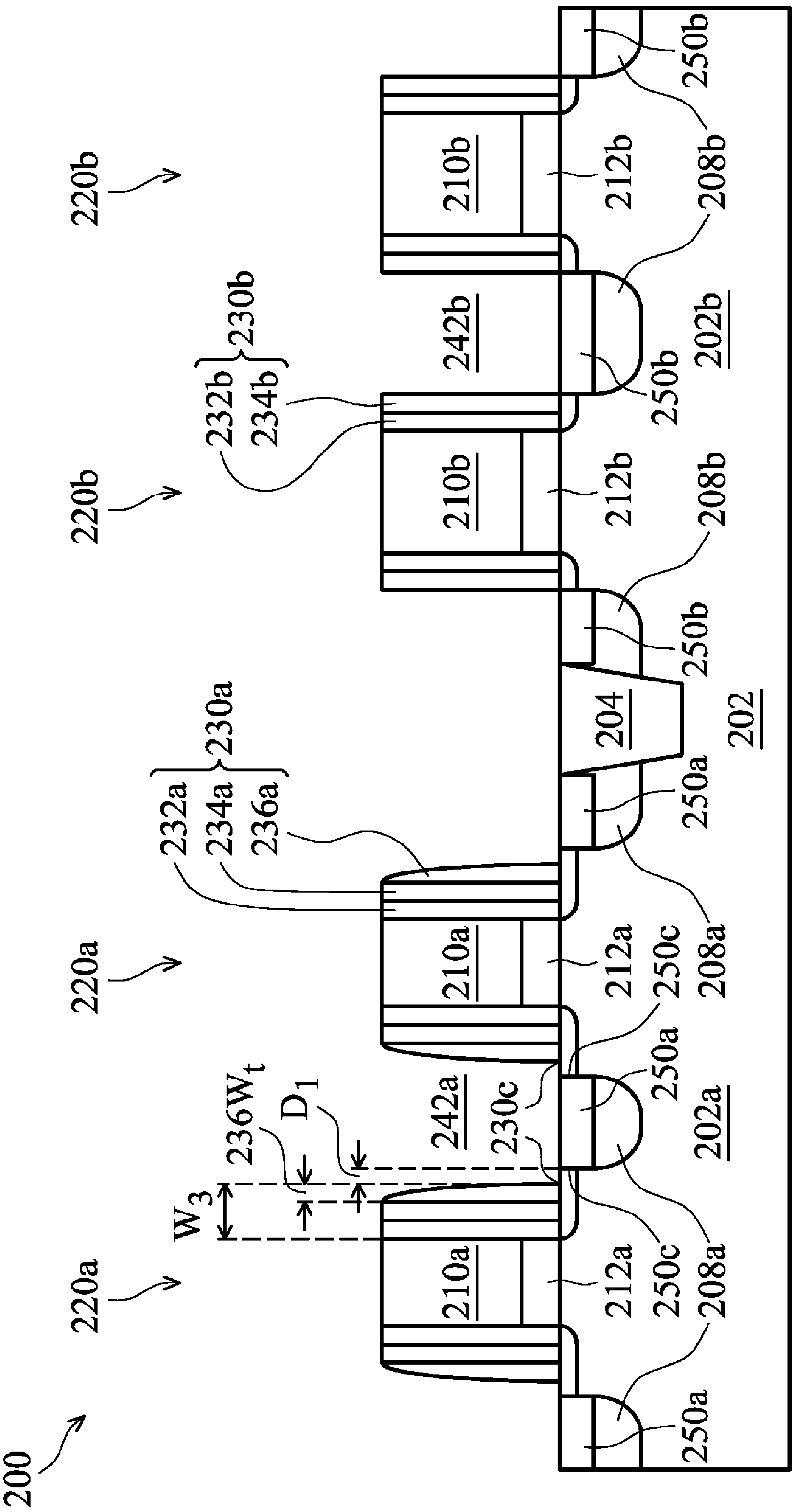

200
220a
220a
220b
220b
210a
210a
210b
210b
212a
212a
212b
212b
250a
250a
250a
250b
250b
250b
250c
250c
208a
208a
208b
208b
202a
202b
202
204
230c
242a
242b
232a
234a
236a
230a
232b
234b
230b
W3
236Wt
D1

FIG. 2J

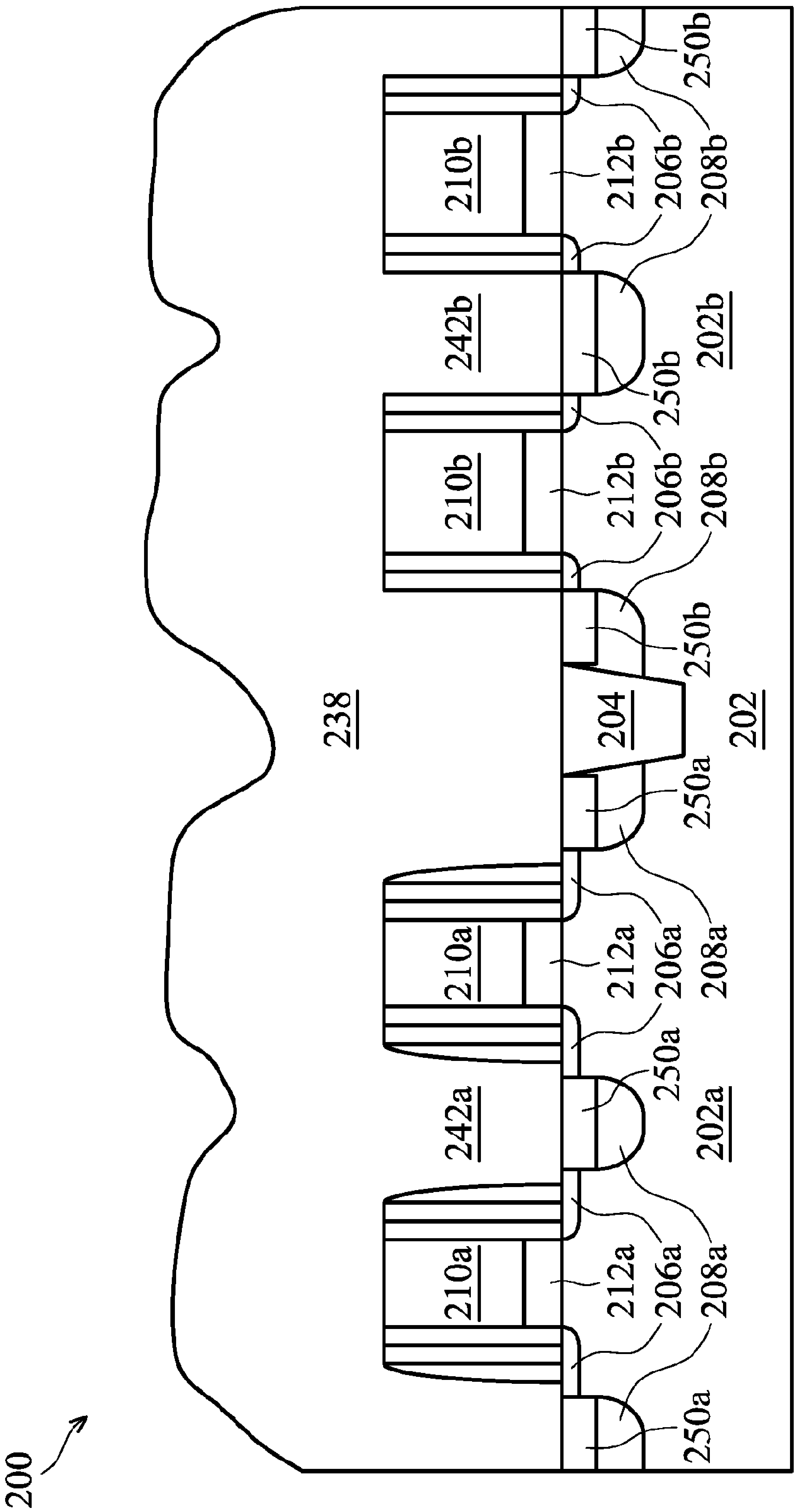

200
238
210a
212a
206a
208a
250a
242a
202a
210a
212a
206a
208a
250a
204
202
250b
210b
212b
206b
208b
242b
202b
250b
210b
212b
206b
208b
250b

FIG. 2K

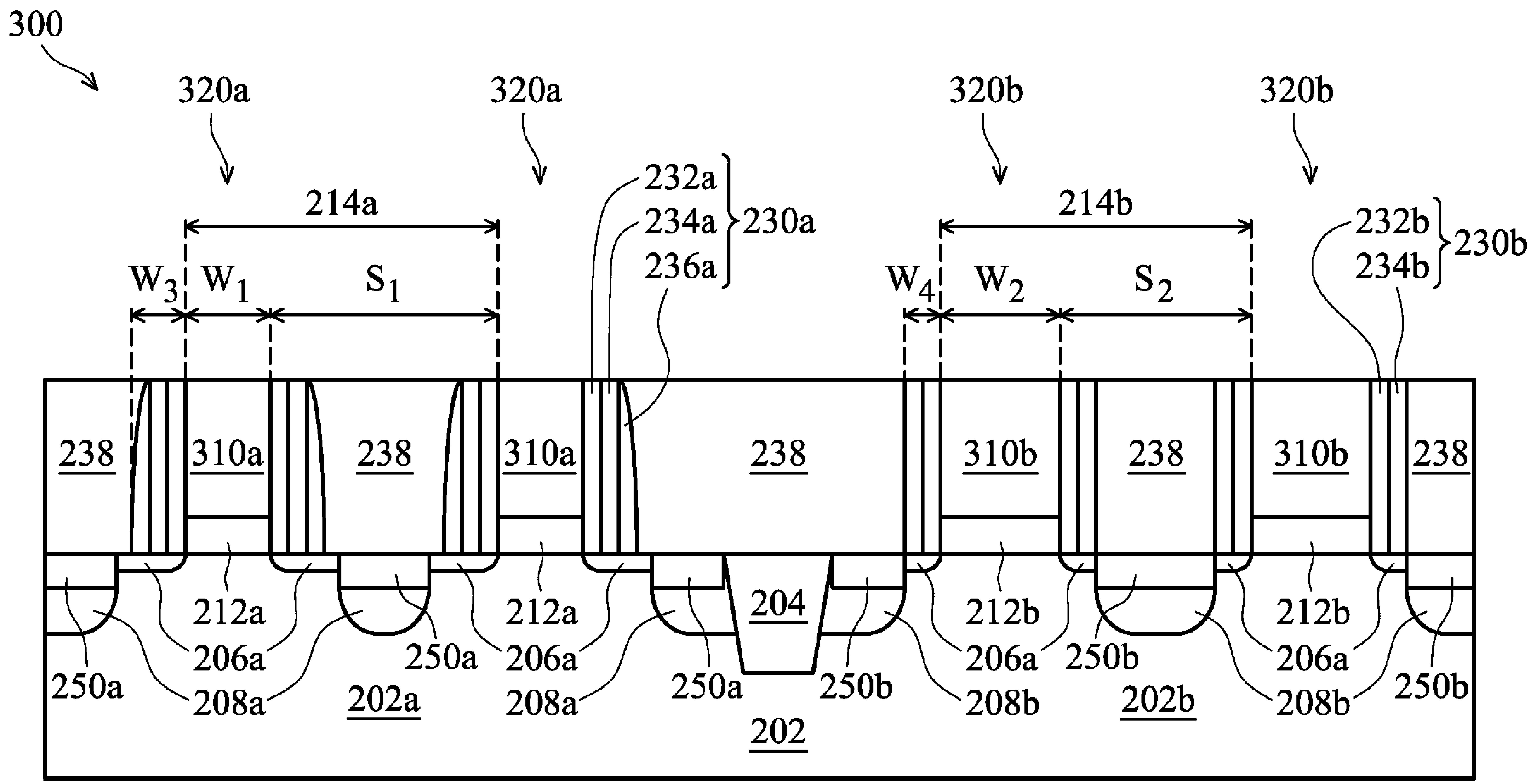

300
320a
320a
320b
320b
214a
214b
232a
234a
236a
230a
232b
234b
230b
W_3
W_1
S_1
W_4
W_2
S_2
238
310a
238
310a
238
310b
238
310b
238
212a
212a
204
212b
212b
250a
206a
208a
202a
250a
206a
208a
250a
250b
206a
208b
202b
250b
206a
208b
250b
202

FIG. 3

SPACER STRUCTURES OF A SEMICONDUCTOR DEVICE

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

TECHNICAL FIELD

The disclosure relates to integrated circuit fabrication, and more particularly to a semiconductor device with spacer structures.

BACKGROUND

As the technology nodes shrink, in some integrated circuit (IC) designs, there has been a desire to replace the typically polysilicon gate electrode with a metal gate electrode to improve device performance with the decreased feature sizes. One process of forming a metal gate structure is termed a "gate last" process in which the final gate structure is fabricated "last" which allows for a reduced number of subsequent processes, including high temperature processing, that must be performed after formation of the gate. Additionally, as the dimensions of transistors decrease, the thickness of the gate oxide must be reduced to maintain performance with the decreased gate length. In order to reduce gate leakage, high-dielectric-constant (high-k) gate dielectric layers are also used which allow greater physical thicknesses while maintaining the same effective thickness as would be provided by a thinner layer of the gate oxide used in larger technology nodes.

However, there are challenges to implementing such features and processes in complementary metal-oxide-semiconductor (CMOS) fabrication. As the gate length and spacing between devices decrease, these problems are exacerbated. For example, in a "gate last" fabrication process, voids may be generated during deposition of an inter-layer dielectric (ILD) layer for gap filling due to a high aspect ratio opening between gate spacers. Accordingly, what is needed is an improved device and method of spacer formation.

SUMMARY

In one embodiment, a semiconductor device comprises a substrate having a first active region and a second active region; a plurality of first gate electrodes having a gate pitch over the first active region, wherein each first gate electrode has a first width; a plurality of first spacers adjoining the plurality of first gate electrodes, wherein each first spacer has a third width; a plurality of second gate electrodes having the same gate pitch as the plurality of first gate electrodes over the second active region, wherein each second gate electrode has a second width greater than the first width; and a plurality of second spacers adjoining the plurality of second gate electrodes, wherein each second spacer has a fourth width less than the third width.

In another embodiment, a semiconductor device comprises a substrate having a first active region and a second active region; a plurality of first gate electrodes having a gate pitch over the first active region, wherein each first gate electrode has a first width; a plurality of first spacers adjoining the plurality of first gate electrodes, wherein each first spacer has a third width; a plurality of second gate electrodes having the same gate pitch as the plurality of first gate electrodes over the second active region, wherein each second gate electrode has a second width greater than the first width; a plurality of second spacers adjoining the plurality of second gate electrodes, wherein each second spacer has a fourth width less than the third width; a plurality of first sicilide regions in the first active region on opposite sides of the plurality of first gate electrodes, wherein an inner edge of each first silicide region is offset from an outer edge of the each first spacer; and a plurality of second silicide regions in the second active region on opposite sides of the plurality of the second gate electrodes, wherein an inner edge of each second silicide region is substantially aligned with an outer edge of the each second spacer.

In still another embodiment, a method of fabricating a semiconductor device comprises providing a substrate having a first active region and a second active region; forming a plurality of first gate electrodes having a gate pitch over the first active region, wherein each first gate electrode has a first width, and a plurality of second gate electrodes having the same gate pitch as the plurality of first gate electrodes over the second active region, wherein each second gate electrode has a second width greater than the first width; depositing a first oxygen-sealing layer on the plurality of the first gate electrodes and the plurality of second gate electrodes; depositing an oxygen-containing layer on the first oxygen-sealing layer; depositing a second oxygen-sealing layer on the oxygen-containing layer; removing a portion of the second oxygen-sealing layer over top surfaces of the plurality of the first gate electrodes and the plurality of the second gate electrodes; and removing the second oxygen-sealing layer over the second active region.

BRIEF DESCRIPTION OF THE DRAWINGS

The present disclosure is best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale and are used for illustration purposes only. In fact, the dimensions of the various features in the drawings may be arbitrarily increased or reduced for clarity of discussion.

FIG. **1** is a flowchart illustrating a method for fabricating spacer structures of a semiconductor device according to various aspects of the present disclosure;

FIGS. **2**A-K show schematic cross-sectional views of spacer structures of a semiconductor device at various stages of fabrication according to various aspects of the present disclosure; and

FIG. **3** is a cross-sectional view of a semiconductor device fabricated using the steps shown in FIG. **2**A-K according to various aspects of the present disclosure.

DESCRIPTION

It is understood that the following disclosure provides many different embodiments, or examples, for implementing different features of the invention. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. Various features may be arbitrarily drawn in different scales for simplicity and clarity. In addition, the present disclosure provides examples based on a "gate last" metal gate structure, however, one skilled in the art may recognize applicability to other structures and/or use of other materials.

FIG. **1** is a flowchart illustrating a method **100** for fabricating spacer structures **230**a, **230**b (shown in FIGS. **2**J and **2**K) of a semiconductor device **200** according to various aspects of the present disclosure. FIGS. **2**A-K show schematic cross-sectional views of spacer structures **230**a, **230**b of a semiconductor device **200** at various stages of fabrication according to various aspects of the present disclosure. In some embodiments, the semiconductor device of FIG. **1** may be further processed using CMOS technology processing. Accordingly, it is understood that additional processes may be provided before, during, and after the method **100** of FIG. **1**, and that some other processes may only be briefly described herein. Also, FIGS. **1** through **2**K are simplified for a better understanding of the inventive concepts of the present disclosure. For example, although the figures illustrate the spacer structures **230**a, **230**b for a semiconductor device **200**, it is understood the semiconductor device may be part of an IC that further comprises a number of other devices such as resistors, capacitors, inductors, fuses, etc.

Referring to FIG. **1**, the method **100** begins at step **102** wherein a substrate **202** having a first active region **202**a and a second active region **202**b is provided. The substrate **202** may comprise a silicon substrate. The substrate **202** may alternatively comprise silicon germanium, gallium arsenic, or other suitable semiconductor materials. The substrate **202** may further comprise other features such as various doped regions, a buried layer, and/or an epitaxy layer. Furthermore, the substrate **202** may be a semiconductor on insulator such as silicon on insulator (SOI) or silicon on sapphire. In other embodiments, the substrate **202** may comprise a doped epi layer, a gradient semiconductor layer, and/or may further include a semiconductor layer overlying another semiconductor layer of a different type such as a silicon layer on a silicon germanium layer. In other examples, a compound semiconductor substrate **202** may comprise a multilayer silicon structure or a silicon substrate may include a multilayer compound semiconductor structure.

The first and second active regions **202**a, **202**b may include various doping configurations depending on design requirements. In some embodiments, the first and second active regions **202**a, **202**b may be doped with p-type or n-type dopants. For example, the first and second active regions **202**a, **202**b may be doped with p-type dopants, such as boron or BF_2; n-type dopants, such as phosphorus or arsenic; and/or combinations thereof. The two active regions **202**a, **202**b may be the same doping type, or different doping types. The first and second active regions **202**a, **202**b may be configured for an N-type metal-oxide-semiconductor transistor (referred to as an NMOS) or for a P-type metal-oxide-semiconductor transistor (referred to as a PMOS). In the present embodiment, the first active region **202**a may be configured for a logic device to form a logic region **200**a and the second active region **202**b may be configured for a memory device to form a static random access memory (SRAM) region **200**b.

In some embodiments, isolation structure **204** may be formed on the substrate **202** to isolate the first active region **202**a and second active region **202**b. The isolation structure **204** may utilize isolation technology, such as local oxidation of silicon (LOCOS) or shallow trench isolation (STI), to define and electrically isolate the first active region **202**a and second active region **202**b. In the present embodiment, the isolation structure **204** comprises a STI. The isolation structure **204** may comprise silicon oxide, silicon nitride, silicon oxynitride, fluoride-doped silicate glass (FSG), a low-k dielectric material, other suitable materials, and/or combinations thereof. The isolation structure **204**, and in the present embodiment, the STI, may be formed by any suitable process. In at least one embodiment, the formation of the STI may include patterning the semiconductor substrate **202** by a photolithography process, etching a trench in the substrate **202** (for example, by using a dry etching, wet etching, and/or plasma etching process), and filling the trench (for example, by using a chemical vapor deposition process) with a dielectric material. In some embodiments, the filled trench may have a multi-layer structure such as a thermal oxide liner layer filled with silicon nitride or silicon oxide.

Next step **104** is performed to fabricate a plurality of first and second electrodes. An example of a structure resulting from the step **104** is shown in FIG. **2**A. As depicted in FIG. **2**A, a gate dielectric layer **212** is formed over the substrate **202**. In some embodiments, the gate dielectric layer **212** may comprise silicon oxide, high-k dielectric material or combination thereof. A high-k dielectric material is defined as a dielectric material with a dielectric constant greater than that of SiO_2. The high-k dielectric layer comprises metal oxide. The metal oxide is selected from the group consisting of oxides of Li, Be, Mg, Ca, Sr, Sc, Y, Zr, Hf, Al, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, or mixtures thereof. The gate dielectric layer **212** may be grown by a thermal oxidation process, a chemical vapor deposition (CVD) process, an atomic layer deposition (ALD) process, and may have a thickness less than 2 nm.

In some embodiments, the gate dielectric layer **212** may further comprise an interfacial layer (not shown) to minimize stress between the gate dielectric layer **212** and the substrate **202**. The interfacial layer may be formed of silicon oxide or silicon oxynitride grown by a thermal oxidation process. In at least one embodiment, the interfacial layer is grown by a rapid thermal oxidation (RTO) process or in a conventional annealing process comprising oxygen.

And then, a dummy gate electrode layer **210** may be formed over the gate dielectric layer **212**. In some embodiments, the dummy gate electrode layer **210** may comprise a single layer or multilayer structure. In the present embodiment, the dummy gate electrode layer **210** may comprise poly-silicon. Further, the dummy gate electrode layer **210** may be doped poly-silicon with the uniform or gradient doping. The dummy gate electrode layer **210** may have any suitable thickness. In the present embodiment, the dummy gate electrode layer **210** has a thickness in the range of about 30 nm to about 60 nm. The dummy gate electrode layer **210** may be formed using a low-pressure chemical vapor deposition (LPCVD) process. In at least one embodiment, the LPCVD process can be carried out in a standard LPCVD furnace at a temperature of about 580° C. to 650° C. and at a pressure of about 200 mTorr to 1 Torr, using silane (SiH_4), disilane (Si_2H_6), trisilane (Si_3H_8) or dichlorosilane (SiH_2Cl_2) as the silicon source gas.

In the present embodiment, a plurality of first gate stacks **220**a and a plurality of second gate stacks **220**b are thus formed by patterning the blanket films of the gate dielectric layer **212** and dummy gate electrode layer **210**. After a hard mask layer (not shown) is deposited, the hard mask layer is patterned using a photo-sensitive layer (not shown). Then a plurality of the first and second gate stacks **220**a, **220**b are patterned through the hard mask layer using a reactive ion etching (RIE) or a high density plasma (HDP) process, exposing a portion of the substrate **202**. In the present embodiment, a plurality of the first gate stacks **220**a comprises a plurality of the first gate electrodes **210**a and the gate dielectric layer

212a. A plurality of the second gate stacks **220**b comprises a plurality of the second gate electrodes **210**b and the gate dielectric layer **212**b.

In some embodiments, the hard mask layer (not shown) may be formed over the dummy gate electrode layer **210** to protect the dummy gate electrode layer **210**. The hard mask layer may include silicon nitride. The hard mask layer can be deposited by, for example, a CVD process, or a LPCVD process. The hard mask layer may have a thickness of about 100 to 400 Å.

Still referring to FIGS. **1** and **2**A, the method **100** continues with step **104** in which a plurality of first gate electrodes **210**a having a first gate pitch **214**a is formed over the first active region **202**a, wherein each first gate electrode **210**a has a first width W_1, and a plurality of second gate electrodes **210**b having a gate pitch **214**b which is the same as that **214**a of the plurality of the first gate electrodes **210**a is formed over the second active region **202**b, wherein each second gate electrode **210**b has a second width W_2 greater than the first width W_1.

A gate pitch is defined as a summation of a gate width and a gate space. In the present embodiment, the first gate pitch **214**a is a summation of the first gate width W_1 and a first gate space S_1 in the logic region **200**a, and the second gate pitch **214**b is a summation of the second gate width W_2 and a second gate space S_2 in the SRAM region **200**b. In at least one embodiment, the first gate width W_1 may be in the range of about 10 to 30 nm. The first gate space S_1 may be in the range of about 30 to 100 nm. The first gate pitch **214**a may be in the range of about 40 to 130 angstroms. The ratio of the first gate width W_1 to the first gate pitch **214**a is from 0.20 to 0.25. In another embodiment, the second gate width W_2 may be in the range of about 12 to 40 nm. The second gate space S_2 may be in the range of about 28 to 90 nm. The second gate pitch **214**b may be in the range of about 40 to 130 angstroms, which is the same as the first gate pitch **214**a of the plurality of the first gate electrodes **210**a. The ratio of the second gate width W_2 to the second gate pitch **214**b is from 0.27 to 0.32.

In some embodiments, the first gate pitch **214**a is same as the second gate pitch **214**b for chip area saving. Further, in order to lower SRAM Vccmin ( ), the second width W_2 of each second gate electrode **210**b is greater than the first width W_1 of each first gate electrode **210**a, thereby the second space S_2 of each second gate electrode **210**b is less than the first space S_1 of each first gate electrode **210**a.

Also shown in FIG. **2**A, after formation of a plurality of the first and second gate stacks **220**a, **220**b, lightly doped source and drain (LDD) regions **206**a, **206**b may be created in the first and second active regions **202**a, **202**b. This is accomplished via ion implantation of boron or phosphorous, at an energy between about 5 to 100 KeV, at a dose between about 1E11 to 1E 14 atoms/cm^2.

The method **100** in FIG. **1** continues with step **106** in which the structure in FIG. **2**B is produced by depositing a first oxygen-sealing layer **232** on the plurality of first gate electrodes **210**a and the plurality of second gate electrodes **210**b. In the present embodiment, the first oxygen-sealing layer **232** comprises silicon nitride or carbon-doped silicon nitride. The first oxygen-sealing layer **232** has a width **232**w in the range of about 3 to 10 nm. In some embodiments, the first oxygen-sealing layer **232** may be deposited using a molecular layer deposition (MLD) process. The MLD process of the present invention is generally carried out under a pressure less than 10 mTorr and in the temperature range from about 350° C. to 500° C., such as about 450° C. in some embodiments. In at least one embodiment, the silicon nitride is deposited on the plurality of the first gate electrodes **210**a and the plurality of second gate electrodes **210**b by reacting a silicon source compound and a nitrogen source. The silicon source compound provides silicon to the deposited silicon nitride and may be silane (SiH_4) or tetrathoxysilane (TEOS). The nitrogen source provides nitrogen to the deposited silicon nitride and may be ammonia (NH_3) or nitrogen gas (N_2). In another embodiment, the carbon-doped silicon nitride is deposited on the plurality of the first gate electrodes **210**a and the plurality of second gate electrodes **210**b by reacting a carbon source compound, a silicon source compound, and a nitrogen source. The carbon source compound may be an organic compound, such as a hydrocarbon compound, e.g., ethylene (C_2H_6).

The method **100** in FIG. **1** continues with step **108** in which the structure in FIG. **2**C is produced by removing a portion of the first oxygen-sealing layer **232** on top surfaces of the plurality of the first gate electrodes **210**a and the plurality of second gate electrodes **210**b using a dry etching process (e.g., anisotropic etching), whereby the remaining first oxygen-sealing layer **232**a, **232**b remains on the sidewall surfaces of the plurality of the first gate electrodes **210**a and the plurality of second gate electrodes **210**b.

In some embodiments, the remaining first oxygen-sealing layers **232**a, **232**b may seal the plurality of the first gate stacks **220**a and the plurality of the second gate stacks **220**b from oxygen-containing structures and/or ambient oxygen in further process steps, so may prevent the transport of oxygen into the region beneath the gate stacks **220**a, **220**b. This prevention of oxygen transport beneath the gate stacks **220**a, **220**b may at least partially prevent oxidation of the substrate **202**, which could result in the formation of an undesired oxide, such as silicon oxide, beneath the gate stacks **220**a, **220**b. Such an undesired oxide could be of a thickness enough to degrade device performance if its formation is not prevented. In some embodiments, the dry etching process may have a high selectivity such that the dry etching process does not etch into the surface of the substrate **202**. For example, the dry etching process for a silicon nitride film may be performed under a source power of about 150 to 220 W, and a pressure of about 10 to 45 mTorr, using CH_2F_2, O_2, He, and Ar as etching gases. In this way, according to some embodiments, the remaining first oxygen-sealing layer **232**a, **232**b for the semiconductor device **200** is formed with almost no recess in the substrate surface.

The method **100** in FIG. **1** continues with step **110** in which the structure in FIG. **2**D is produced by depositing an oxygen-containing layer **234** on the first oxygen-sealing layer **232**a, **232**b and top surfaces of the plurality of the first gate electrodes **210**a and the plurality of second gate electrodes **210**b. In at least one embodiment, the oxygen-containing layer **234** may comprise silicon oxide or silicon oxynitride. The oxygen-containing layer **234** may have any suitable width. In the present embodiment, a maximum width **234**w of the oxygen-containing layer **234** is in the range of about 3 to 25 nm. The oxygen-containing layer **234** can be deposited using a CVD or an ALD process. For example, the oxygen-containing layer **234** comprising silicon oxide can be deposited under a pressure less than 10 mTorr and a temperature of about 350° C. to 500° C., such as about 450° C. in some embodiments, using silane (SiH_4) and N_2O as reacting precursors.

Referring to FIG. **2**E, a portion of the oxygen-containing layer **234** on the top surfaces of the plurality of the first gate electrodes **210**a and the plurality of second gate electrodes **210**b is removed using a dry etching process (e.g., anisotropic etching), whereby the remaining oxygen-containing layer **234**a, **234**b abuts the first oxygen-sealing layer **232**a, **232**b. The dry etching process has a high selectivity such that the dry etching process does not etch into the top surfaces of the gate electrodes **210**a, **210**b and the substrate **202**. In at least one embodiment, the dry etching process to etch an oxygen-containing layer **234** comprising silicon oxide may be performed under a glow discharge and a pressure of about 10 mTorr to 3 Torr, using fluorocarbon gas, such as CF_4, C_2F_6, C_3F_8, CHF_3, or CH_2F_2, as etching gases.

The method **100** in FIG. **1** continues with step **112** in which the structure in FIG. **2**F is produced by depositing a second oxygen-sealing layer **236** on the oxygen-containing layer **234**a, **234**b. In some embodiments. the second oxygen-sealing layer **236** may comprise silicon nitride or carbon-doped silicon nitride. The second oxygen-sealing layer **236** may have any suitable width. In the present embodiment, the second oxygen-sealing layer **236** has a width **236**w in the range of about 10 to about 35 nm. In some embodiments, the second oxygen-sealing layer **236** can be deposited using a molecular layer deposition (MLD) process. In at least one embodiment, the MLD process of the present invention is generally carried out under a pressure less than 10 mTorr and in the temperature range from about 350° C. to 500° C., such as about 450° C. In at least one embodiment, the silicon nitride is deposited on the oxygen-containing layer **234**a, **234**b by reacting a silicon source compound and a nitrogen source. The silicon source compound provides silicon to the deposited silicon nitride and may be silane (SiH_4) or tetrathoxysilane (TEOS). The nitrogen source provides nitrogen to the deposited silicon nitride and may be ammonia (NH_3) or nitrogen gas (N_2). In another embodiment, the carbon-doped silicon nitride is deposited on the oxygen-containing layer **234**a, **234**b by reacting a carbon source compound, a silicon source compound, and a nitrogen source. The carbon source compound may be an organic compound, such as a hydrocarbon compound, e.g., ethylene (C_2H_6).

The method **100** in FIG. **1** continues with step **114** in which the structure in FIG. **2**G is produced by removing a portion of the second oxygen-sealing layer **236** over top surfaces of the plurality of the first gate electrodes **210**a and the plurality of second gate electrodes **210**b using a dry etching process (e.g., anisotropic etching), whereby the remaining second oxygen-sealing layer **236**a, **236**b abuts the oxygen-containing layer **234**a, **234**b, whereby a first opening **240**a is formed between the plurality of the first gate electrodes **210**a and a second opening **240**b is formed between the plurality of the second gate electrodes **210**b. The dry etching process may have a high selectivity such that the dry etching process may stop at the oxygen-containing layer **234**a, **234**b, the top surfaces of the gate electrodes **210**a, **210**b and the substrate **202**. For example, in some embodiments, the dry etching process may be performed under a source power of about 150 to 220 W, and a pressure of about 10 to 45 mTorr, using CH_2F_2, O_2, He, and/or Ar as etching gases.

The method **100** in FIG. **1** continues with step **116** in which the structure in FIG. **2**H is produced by removing the second oxygen-sealing layer **236**b over the second active region **202**b using a wet etching process. In the present embodiment, the plurality of the first gate electrodes **210**a is covered using a photo-sensitive layer. Then, the wet etching process is accomplished via a phosphoric acid treatment. The wet etching process may form an opening **242**b. Aspect ratio of the opening **242**b is lower than that of the opening **240**b in FIG. **2**G. The high aspect ratio of the opening **240**b in FIG. **2**G makes it more likely that voids will form in subsequently formed layers as there is no enough space between the second oxygen-sealing layer **236**b to allow the subsequently formed layer (such as an ILD layer) to fill the small region between the second oxygen-sealing layer **236**b. On the other hand, the lower aspect ratio of the opening **242**b may impede void formation in the ILD layer (described below with respect to FIG. **2**K) thereby decreasing the likelihood of device instability and/or device failure. Further, the first oxygen-sealing layer **232**b and the oxygen-containing layer **234**b are hereinafter referred to as a plurality of second spacers **230**b. A fourth width W_4 of each second spacer **230**b is in the range of about 6 to 35 nm.

After the device in FIG. **2**H has been fabricated, in some embodiments, contacts to connect the device to other IC components may be fabricated. Shown in FIG. **2**I is the creation of a plurality of first heavily doped source and drain (S/D) regions **208**a in the first active region **202**a and a plurality of second S/D regions **208**b in the second active region **202**b for low resistance contact. This is achieved via ion implantation of boron or phosphorous, at an energy level between about 5 to 150 KeV, at a dose between about 1E15 to 1E 16 atoms/cm^2.

Still referring to FIG. **2**I, a plurality of first sicilide regions **250**a in the first active region **202**a on opposite sides of the plurality of first gate electrodes **210**a and a plurality of second silicide regions **250**b in the second active region **202**b on opposite sides of the plurality of the second gate electrodes **210**b are depicted according to some embodiments. In some embodiments, the plurality of the first and second silicide regions **250**a, **250**b are formed on the S/D regions **208**a, **208**b by a self-aligned silicide (salicide) process. For example, the self-aligned silicide (salicide) process may comprise 2 steps. First, a metal material may be deposited via sputtering to the substrate surface at a temperature ranging from 500° C. to 900° C., causing a reaction between the underlying silicon and metal material to form the plurality of the first and second silicide regions **250**a, **250**b. And then, the un-reacted metal material may be etched away.

The plurality of the first and second silicide regions **250**a, **250**b may comprise a material selected from titanium silicide, cobalt silicide, nickel silicide, platinum silicide, erbium silicide, or palladium silicide. In some embodiments, a maximum thickness T of the first and second silicide regions **250**a, **250**b is in the range of about 30 to 50 nm. In addition, each first silicide region **250**a on each side of the gate stack **220**a comprises an inner edge **250**c closest to the first gate stack **220**a. Each second silicide region **250**b on each side of the gate stack **220**b comprises an inner edge **250**d closest to the second gate stack **220**b. The inner edge **250**d is substantially aligned to an outer edge **230**d of the each second spacer **230**b.

In some embodiment, it may be desirable to reduce the aspect ratio of the opening **240**a by thinning the second oxygen-sealing layer **236**a. Referring to FIG. **2**J, the second oxygen-sealing layer **236**a over the plurality of the first gate electrodes **210**a is thinned using a wet etching. The wet etching process may have a high selectivity such that the wet etching process may stop at the STI **204**, the oxygen-containing layer **234**b, the plurality of the first and second gate electrodes **210**a, **210**b, and the plurality of the first and second silicide regions **250**a, **250**b. For example, the high selectivity may be accomplished via a phosphoric acid (H_3PO4) treatment for a suitable time. The wet etching process may form an opening **242**a. Aspect ratio of the opening **242**a is lower than that of the opening **240**a in FIG. **2**I. The high aspect ratio of opening **240**a in FIG. **2**I may cause voids to form in subsequently formed layers as there is not enough space between the second oxygen-sealing layer **236**a to allow the subsequently formed layer (such as an ILD layer) to fill the small region between the second oxygen-sealing layer **236**a. On the other hand, the lower aspect ratio of the opening **242**a may impede void formation in the ILD layer (described below with respect to FIG. 2K), thereby decreasing the likelihood of device instability and/or device failure.

A maximum width **236** wt of the thinned second oxygen-sealing layer **236**a is in the range of about 5 to 30 nm. Further, the first oxygen-sealing layer **232**a, oxygen-containing layer **234**a, and thinned second oxygen-sealing layer **236**a are hereinafter referred to as a plurality of first spacers **230**a. A third width W_3 of each first spacer **230**a is in the range of about 12 to 60 nm. Each second spacer **230**b has the fourth width W_4 less than the third width W_3 of each first spacer **230**a. Additionally, the inner edge **250**c of each first silicide region **250**a is offset from the outer edge **230**c of the each first spacer **230**a by a distance D_1 ranging about 120 to 200 angstroms.

In at least some embodiments, devices are encapsulated in ILD layer. In some embodiment, as shown in FIG. **2**K, an ILD layer **238** is formed over the structure of depicted in FIG. **2**J to a sufficient thickness to form a void-free dielectric layer within the openings **242**a, **242**b that having decreased aspect ratios according to the exemplary fabrication method depicted in FIGS. **2**A-**2**J. For example, the ILD layer **238** may be deposited to a thickness of 3000 to 4500 Å. In at least one embodiment, the ILD layer **238** may be formed using a CVD process, such as high density plasma (HDP) CVD process or sub-atmospheric CVD (SACVD) process.

Referring to FIG. **3**, illustrates a cross-sectional view of a semiconductor device **300** fabricated using the steps shown in FIG. **2**A-K according to various aspects of the present disclosure. Similar features in FIGS. **3** and **2**K are numbered the same for the sake of simplicity and clarity. FIG. **2**K shows the result of a “gate last” process up to the step of depositing the ILD layer **238**. Subsequent CMOS processing steps applied to the semiconductor device **200** of FIG. **2**K may comprise a chemical mechanical polishing (CMP) on the ILD layer **238** to expose the plurality of the first and second gate stacks **220**a, **220**b as shown in FIG. **3**. The plurality of the first and second gate electrodes **210**a, **210**b may then be removed from the plurality of the first and second gate stacks **220**a, **220**b, thereby forming a plurality of trenches.

After the dummy gates are removed, a metal layer may be formed to fill in the trenches. The metal layer may include any metal material suitable for forming a plurality of first and second metal gate electrodes **310**a, **310**b or portion thereof, including barriers, work function layers, liner layers, interface layers, seed layers, adhesion layers, barrier layers, etc. In some embodiments, the metal layer may include suitable metals, such as TiN, WN, TaN, or Ru that properly perform in the PMOS device. In some alternative embodiments, the metal layer may include suitable metals, such as Ti, Ag, Al, TiAl, TiAlN, TaC, TaCN, TaSiN, Mn, or Zr that properly perform in the NMOS device. Another CMP is performed on the metal layer to form the plurality of the first and second metal gate electrodes **310**a, **310**b of the semiconductor devices **300**. The plurality of first metal gate electrodes **310**a and first gate dielectric layer **212**a are hereinafter referred to as a first metal gate stacks **320**a. The plurality of second metal gate electrodes **310**b and first and second gate dielectric layer **212**b are hereinafter referred to as a second metal gate stacks **320**b. Then, in some embodiments, subsequent processes, including interconnect processing, are performed after forming the semiconductor device **300** to complete the IC fabrication. Accordingly, the disclosed methods of fabricating spacer structures of the semiconductor device **300** may fabricate low aspect ratio openings to form a void-free ILD layer, thereby enhancing the device performance.

In at least some embodiments, the invention can be used to form or fabricate spacer structures for a semiconductor device. In this way, ILD layers with fewer voids for a semiconductor device may be formed.

While the invention has been described by way of example and in terms of the various embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

What is claimed is:

1. A semiconductor device, comprising:

a substrate having a first active region and a second active region;

a plurality of first gate electrodes having a gate pitch over the first active region, wherein each first gate electrode has a first width;

a plurality of first spacers adjoining the plurality of first gate electrodes, wherein each first spacer has a third width;

a plurality of second gate electrodes having the same gate pitch as the plurality of first gate electrodes over the second active region, wherein each second gate electrode has a second width greater than the first width; and

a plurality of second spacers adjoining the plurality of second gate electrodes, wherein each second spacer has a fourth width less than the third width.

2. The semiconductor device of claim **1**, wherein the first width is in the range of about 10 to 30 nm.

3. The semiconductor device of claim **1**, wherein a ratio of the first width to the gate pitch is from 0.20 to 0.25.

4. The semiconductor device of claim **1**, wherein the first and second spacers comprise a first oxygen-sealing layer and an oxygen-containing layer abutting the first oxygen-sealing layer.

5. The semiconductor device of claim **4**, wherein the first oxygen-sealing layer comprises silicon nitride or carbon-doped silicon nitride.

6. The semiconductor device of claim **4**, wherein the oxygen-containing layer comprises silicon oxide or silicon oxynitride.

7. The semiconductor device of claim **4**, wherein a maximum width of the oxygen-containing layer is in the range of about 3 to 25 nm.

8. The semiconductor device of claim **4**, wherein the first spacer further comprises a second oxygen-sealing layer abutting the oxygen-containing layer.

9. The semiconductor device of claim **8**, wherein the second oxygen-sealing layer comprises silicon nitride or carbon-doped silicon nitride.

10. The semiconductor device of claim **8**, wherein a maximum width of the second oxygen-sealing layer is in the range of about 5 to 30 nm.

11. The semiconductor device of claim **1** further comprising

a plurality of first sicilide regions in the first active region on opposite sides of the plurality of first gate electrodes, wherein an inner edge of each first silicide region is offset from an outer edge of the each first spacer; and

a plurality of second silicide regions in the second active region on opposite sides of the plurality of the second gate electrodes, wherein an inner edge of each second silicide region is substantially aligned with an outer edge of the each second spacer.

12. The semiconductor device of claim **11**, wherein the first and second silicide regions comprise a material selected from titanium silicide, cobalt silicide, nickel silicide, platinum silicide, erbium silicide, or palladium silicide.

13. The semiconductor device of claim **11**, wherein a maximum thickness of the first and second silicide regions is in the range of about 30 to 50 nm.

14. The semiconductor device of claim **11**, wherein the inner edge of each first silicide region is offset from the outer edge of the each first spacer by about 120 to 200 angstroms.

15. The semiconductor device of claim **11**, wherein the plurality of first gate electrodes is in a logic area and the plurality of second gate electrodes is in a memory area.

16. A semiconductor device, comprising:

a substrate;

a first set of gate electrodes over the substrate, adjacent gate electrodes of the first set of gate electrodes separated by a first gap width, and each gate electrode of the first set of gate electrodes having a first gate width;

a first set of spacer structures on sidewalls of the first set of gate electrodes and having a first spacer width;

a second set of gate electrodes over the substrate, adjacent gate electrodes of the second set of gate electrodes separated by a second gap width less than the first gap width, and each gate electrode of the second set of gate electrodes having a second gate width greater than the first gate width; and

a second set of spacer structures on sidewalls of the second set of gate electrodes and having a second spacer width less than the first spacer width.

17. The semiconductor device of claim **16**, wherein the first gate width ranges from 10 nm to 30 nm, and the second gate width ranges from 12 nm to 40 nm.

18. The semiconductor device of claim **16**, wherein the first gap width ranges from 30 nm to 100 nm, and the second gap width ranges from 28 nm to 90 nm.

19. The semiconductor device of claim **16**, wherein the first set of spacer structures each comprise an inner layer and an outer-most layer having a composition different from that of the inner layer of the first set of spacer structures.

20. The semiconductor device of claim **19**, wherein the second set of spacer structures each comprise an outer-most layer having a composition the same as that of the inner layer of the first set of spacer structures.

21. A semiconductor device, comprising:

a substrate;

a plurality of first gate electrodes having a gate pitch over the substrate, wherein each first gate electrode has a first width;

a plurality of first spacers adjoining the plurality of first gate electrodes, wherein each first spacer has a third width;

a plurality of second gate electrodes having the same gate pitch as the plurality of first gate electrodes over the substrate, wherein each second gate electrode has a second width greater than the first width; and

a plurality of second spacers adjoining the plurality of second gate electrodes, wherein each second spacer has a fourth width less than the third width.

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