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(54) **VERIFICATION CIRCUITS AND METHODS FOR PHASE CHANGE MEMORY ARRAY**

(71) Applicant: **Higgs Opl. Capital LLC**, Dover, DE (US)

(72) Inventors: **Wen-Pin Lin**, Dacun Township (TW); **Shyh-Shyuan Sheu**, Taichung (TW); **Pei-Chia Chiang**, Taipei (TW)

(73) Assignee: **Higgs Opl. Capital LLC**, Dover, DE (US)

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CPC ***G11C 13/0064*** (2013.01); *G11C 13/0002* (2013.01); *G11C 13/0004* (2013.01)
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See application file for complete search history.

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Primary Examiner — Tan T. Nguyen
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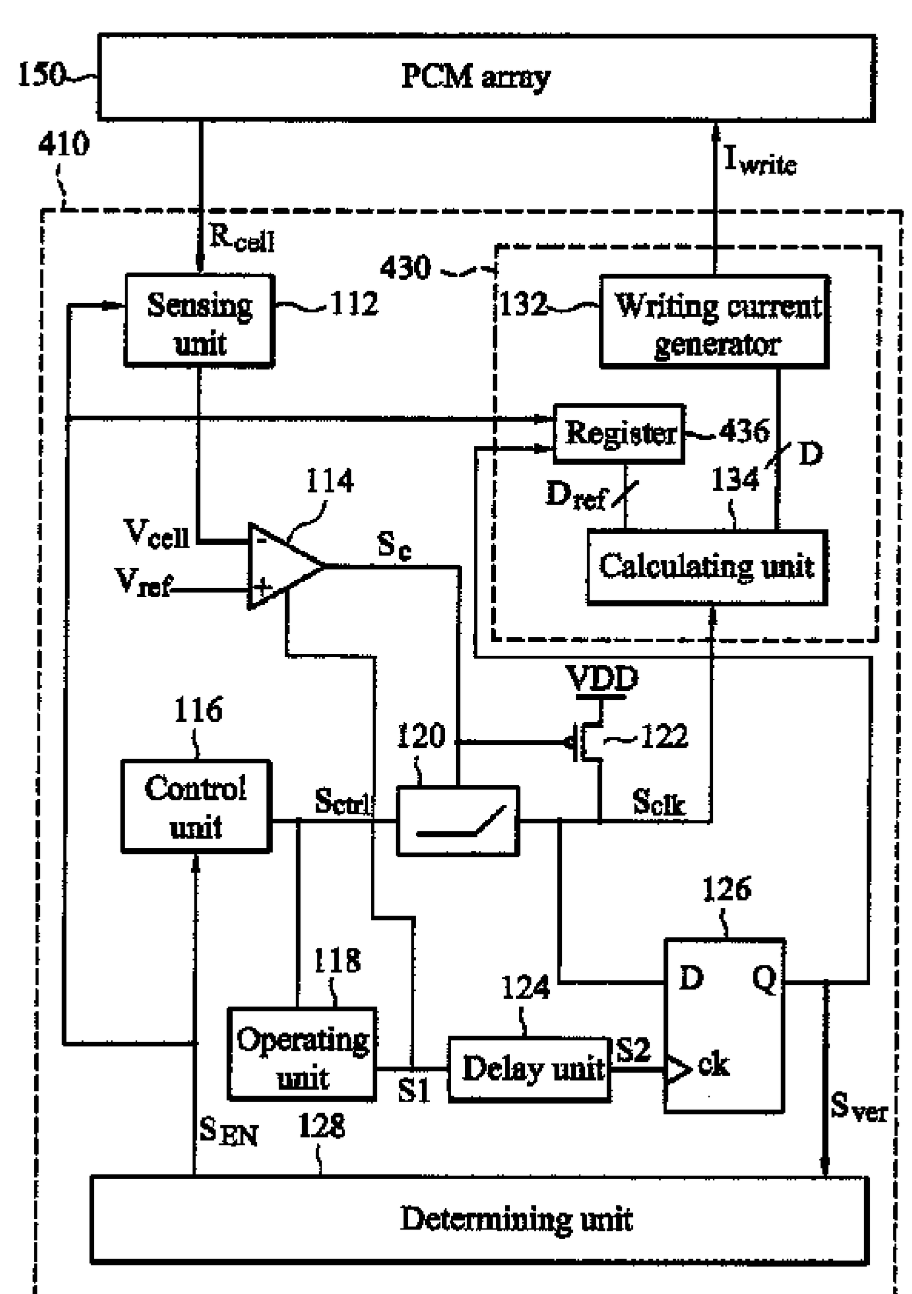
(57) **ABSTRACT**

A verification circuit for a phase change memory array is provided. A sensing unit senses a sensing voltage from a memory cell of the phase change memory array according to an enable signal. A comparator generates a comparing signal according to the sensing voltage and a reference voltage, so as to indicate whether the memory cell is in a reset state. A control unit generates a control signal according to the enable signal. An operating unit generates a first signal according to the control signal, so as to indicate whether the comparator is active. An adjustment unit provides a writing current to the cell, and increases the writing current according to the control signal until the comparing signal indicates that the memory cell is in a reset state.

29 Claims, 10 Drawing Sheets



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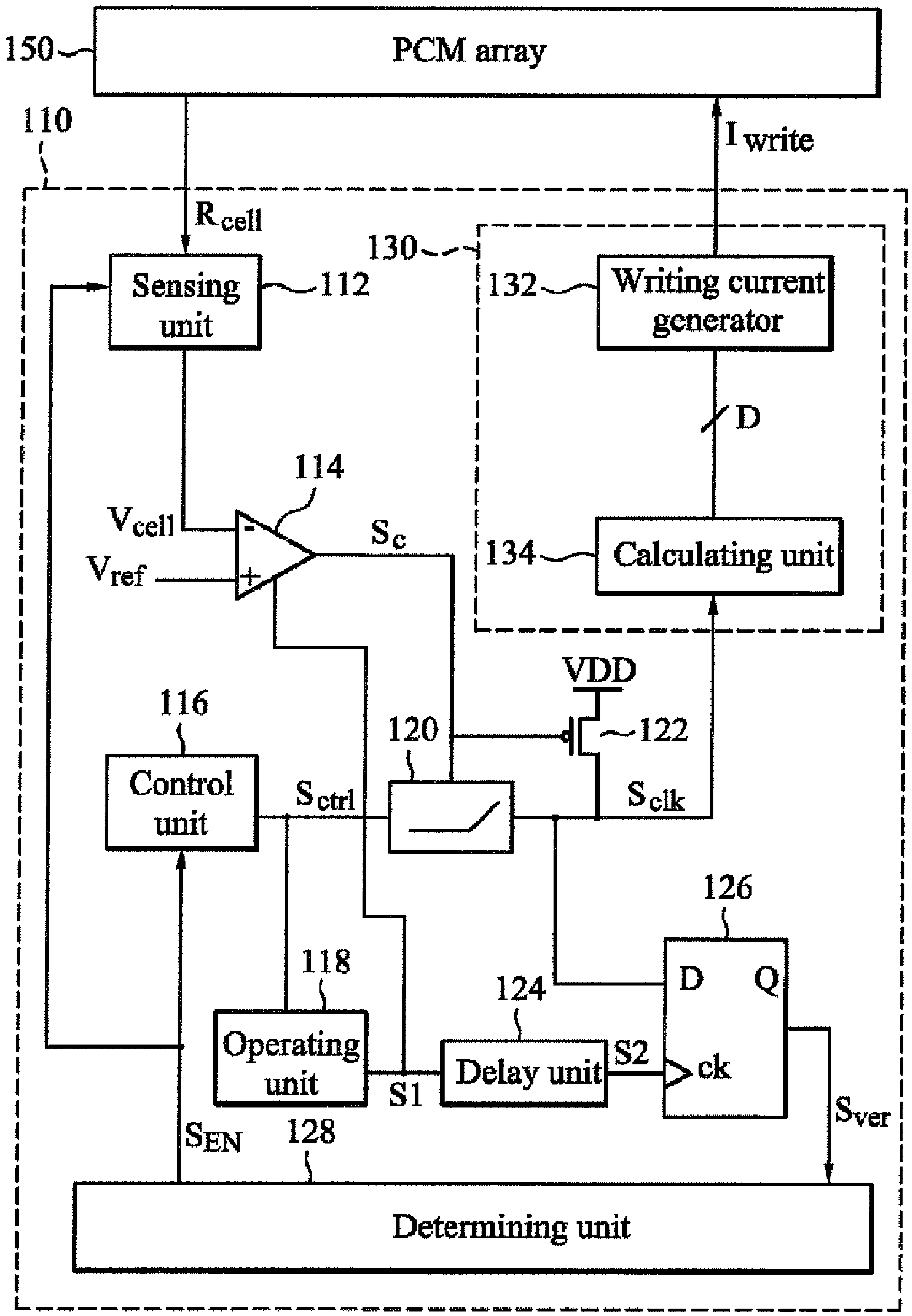
150
PCM array
110
I_{write}
R_{cell}
130
Sensing unit
112
132
Writing current generator
D
114
V_{cell}
V_{ref}
-
+
S_c
134
Calculating unit
VDD
116
120
122
Control unit
S_{ctrl}
S_{clk}
126
118
124
D
Q
Operating unit
S1
Delay unit
S2
ck
S_{ver}
S_{EN}
128
Determining unit

FIG. 1

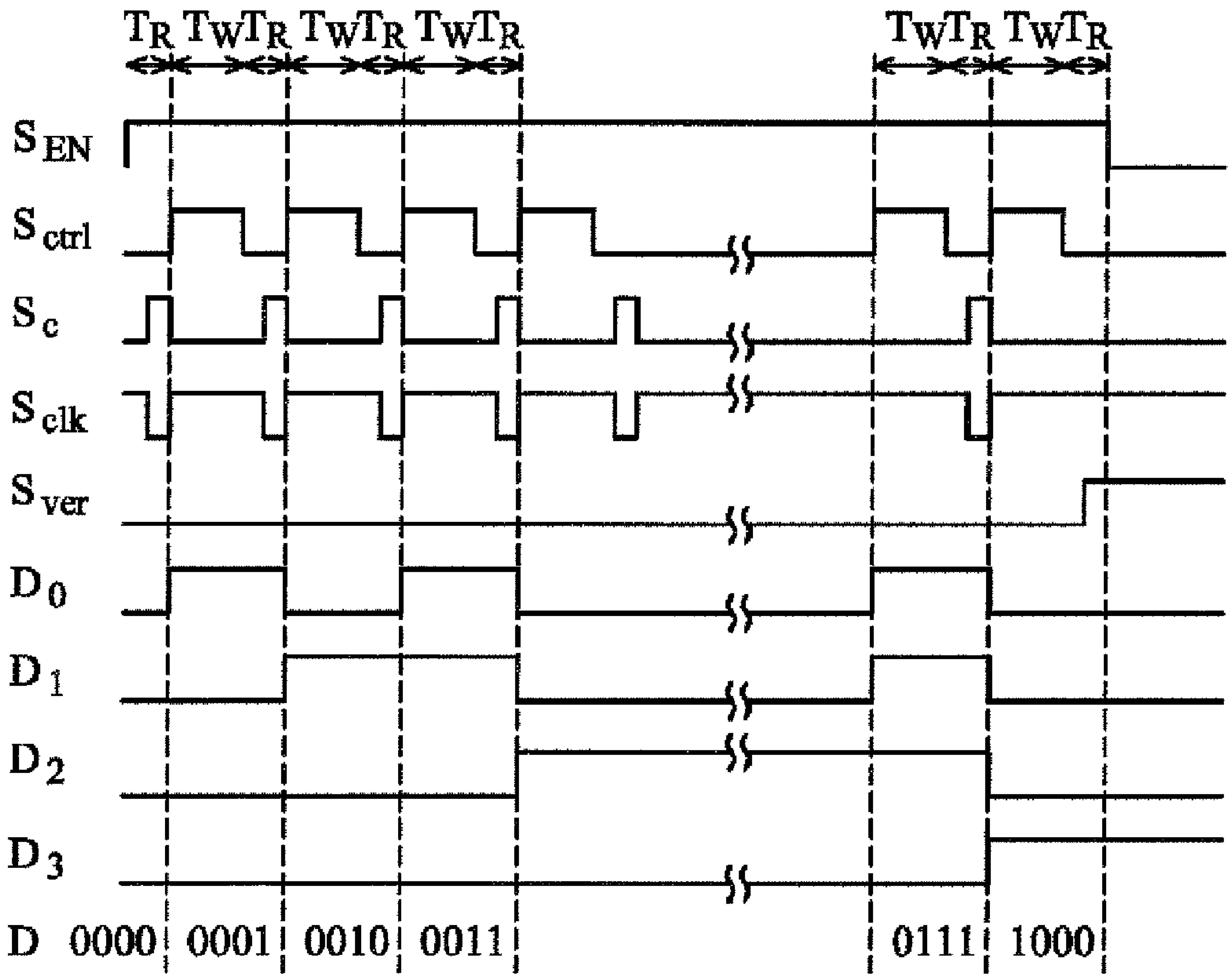
TR TW TR TW TR TW TR
TW TR TW TR
SEN
Sctrl
Sc
Sclk
Sver
D0
D1
D2
D3
D 0000 0001 0010 0011
0111 1000

FIG. 2

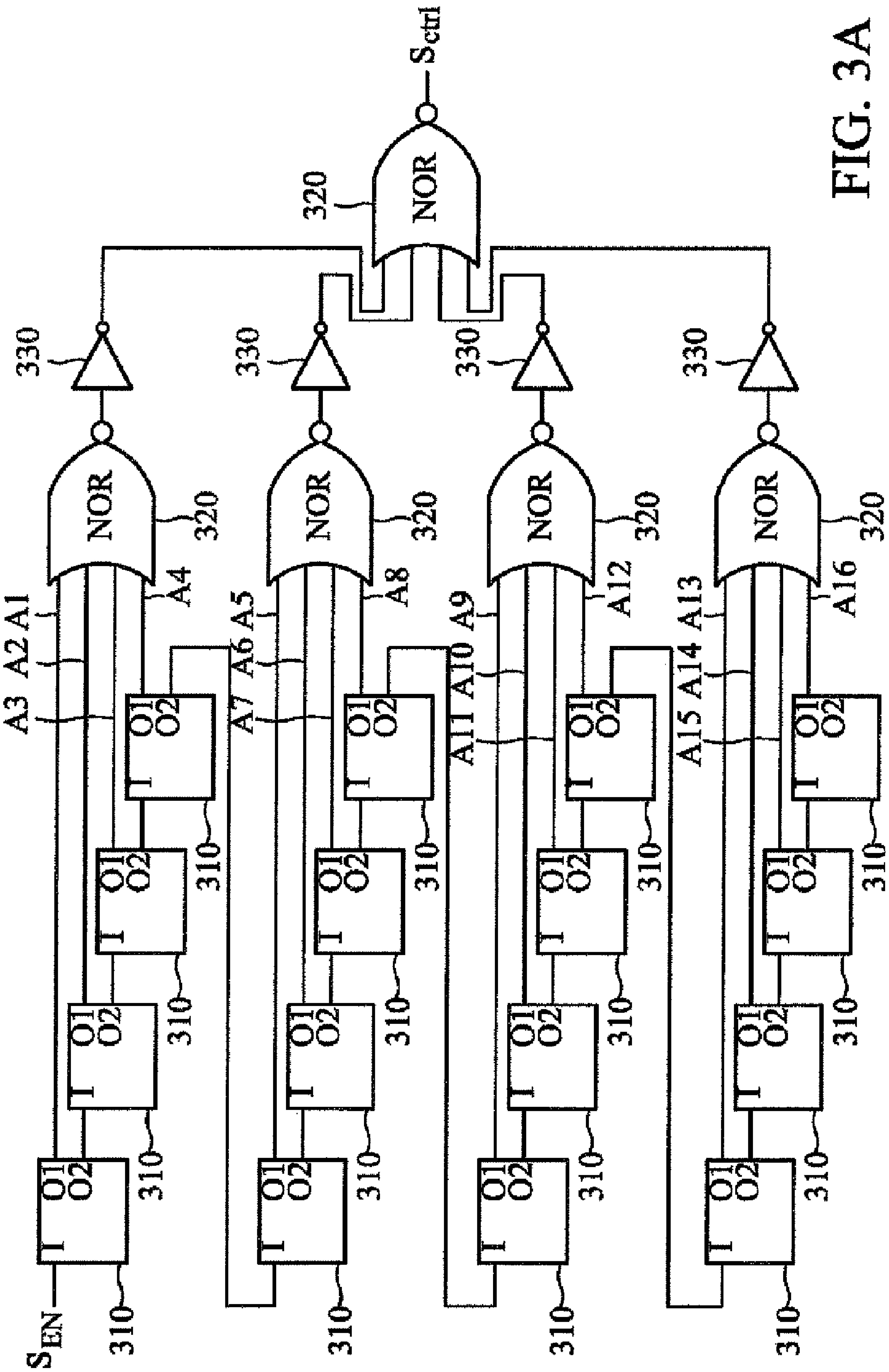
S_{ctrl}
NOR
320
330
A1 A2 A3 A4
A5 A6 A7 A8
A9 A10 A11 A12
A13 A14 A15 A16
I
O1
O2
310
S_{EN}

FIG. 3A

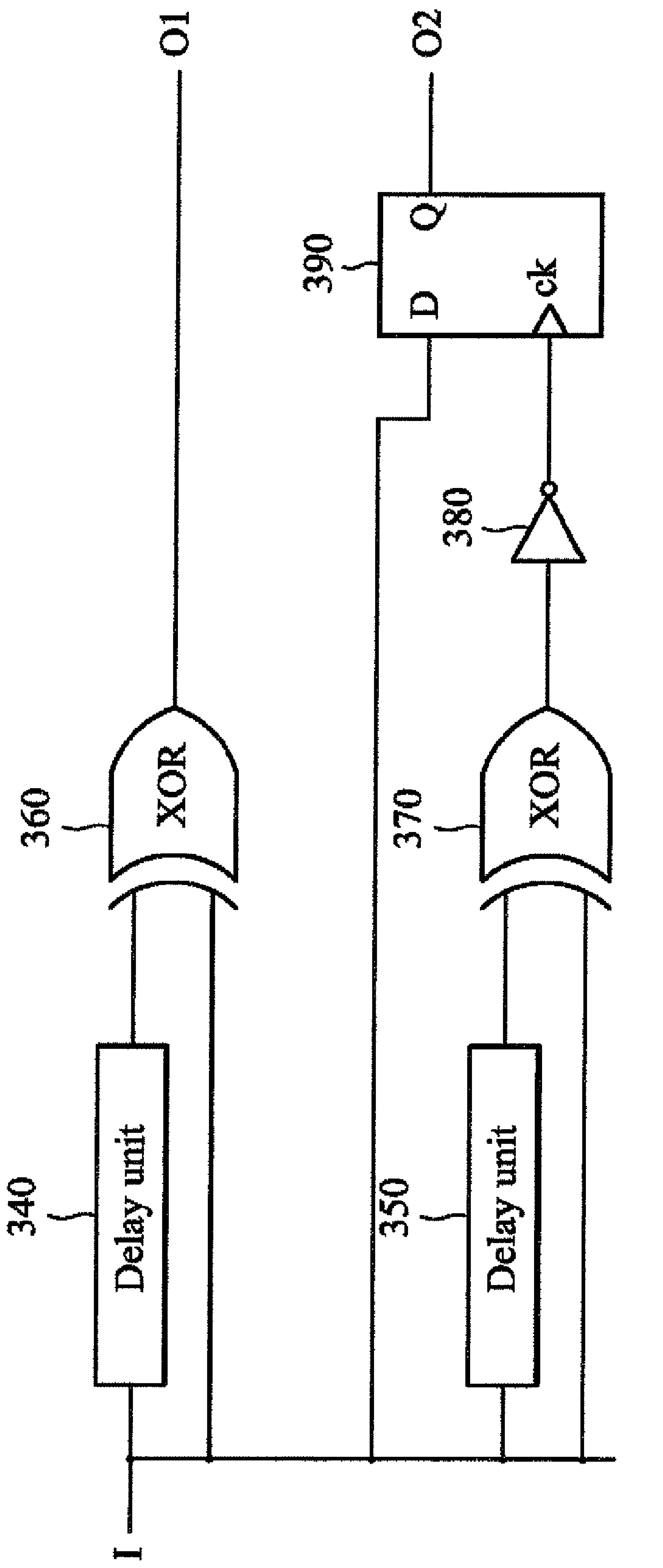
O1
O2
390
D
Q
ck
380
360
XOR
370
XOR
340
Delay unit
350
Delay unit
I

FIG. 3B

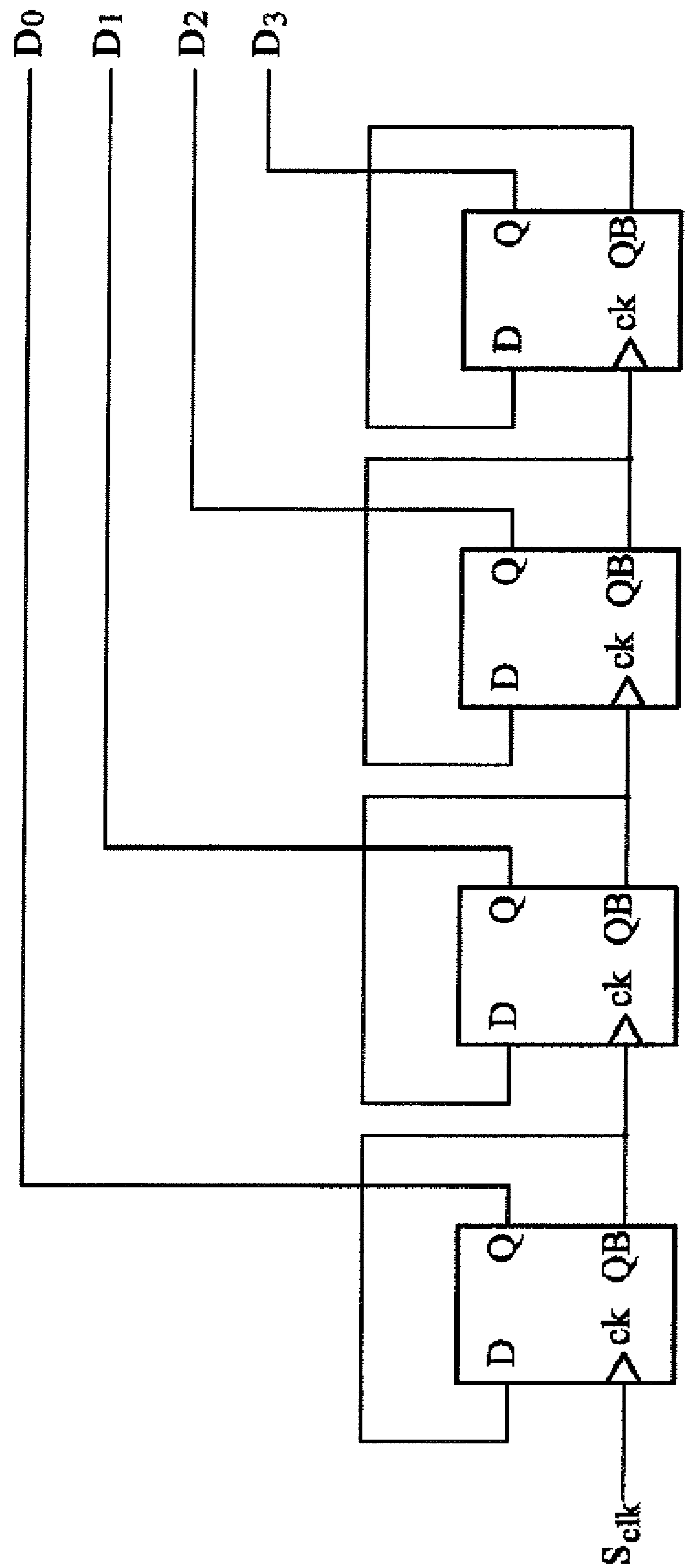

FIG. 3C

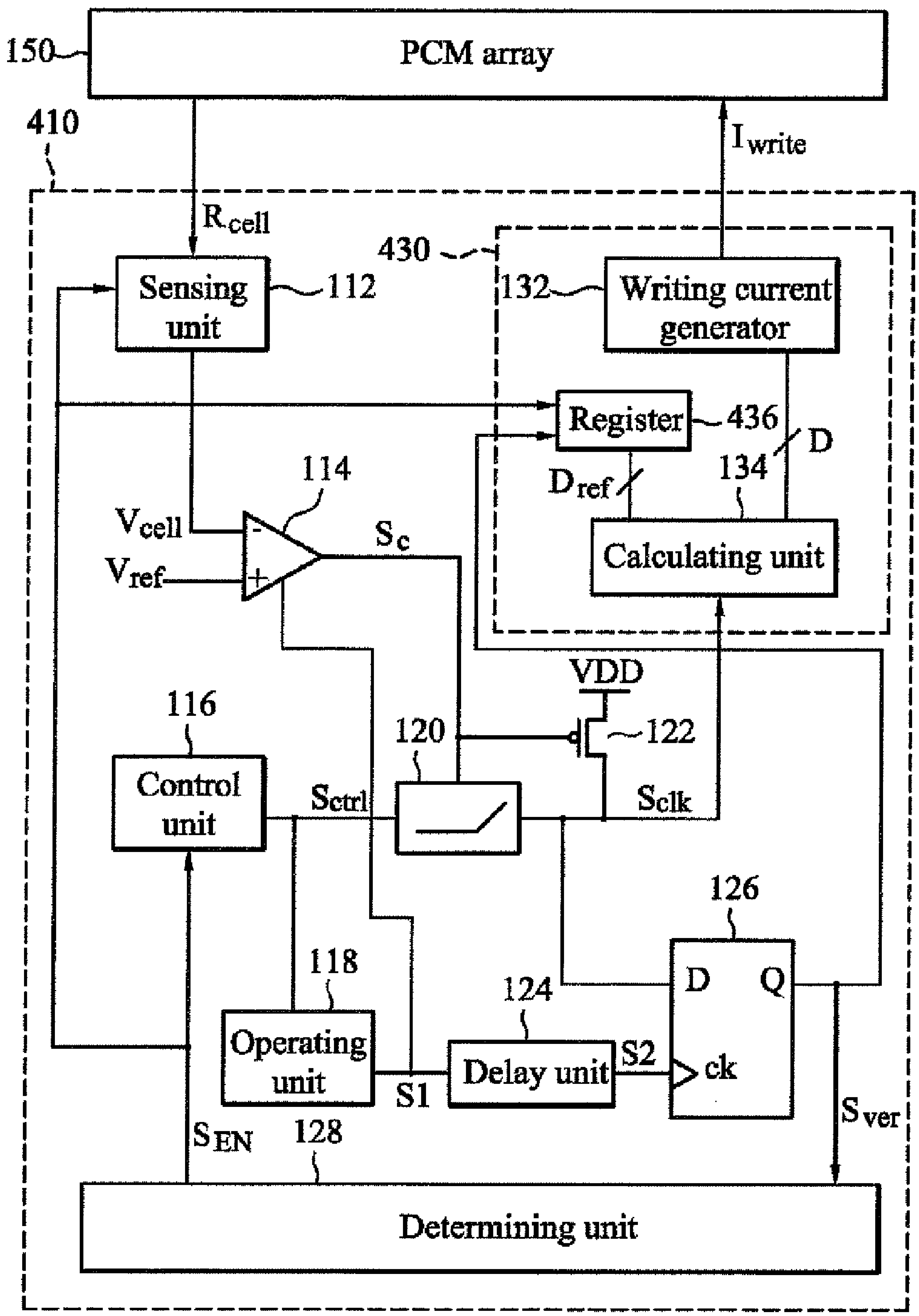
150
PCM array
410
I_{write}
R_{cell}
430
Sensing unit
112
132
Writing current generator
Register
436
D
134
114
D_{ref}
V_{cell}
S_c
Calculating unit
V_{ref}
VDD
116
120
122
Control unit
S_{ctrl}
S_{clk}
126
118
124
D
Q
Operating unit
Delay unit
S2
ck
S1
S_{EN}
128
S_{ver}
Determining unit

FIG. 4

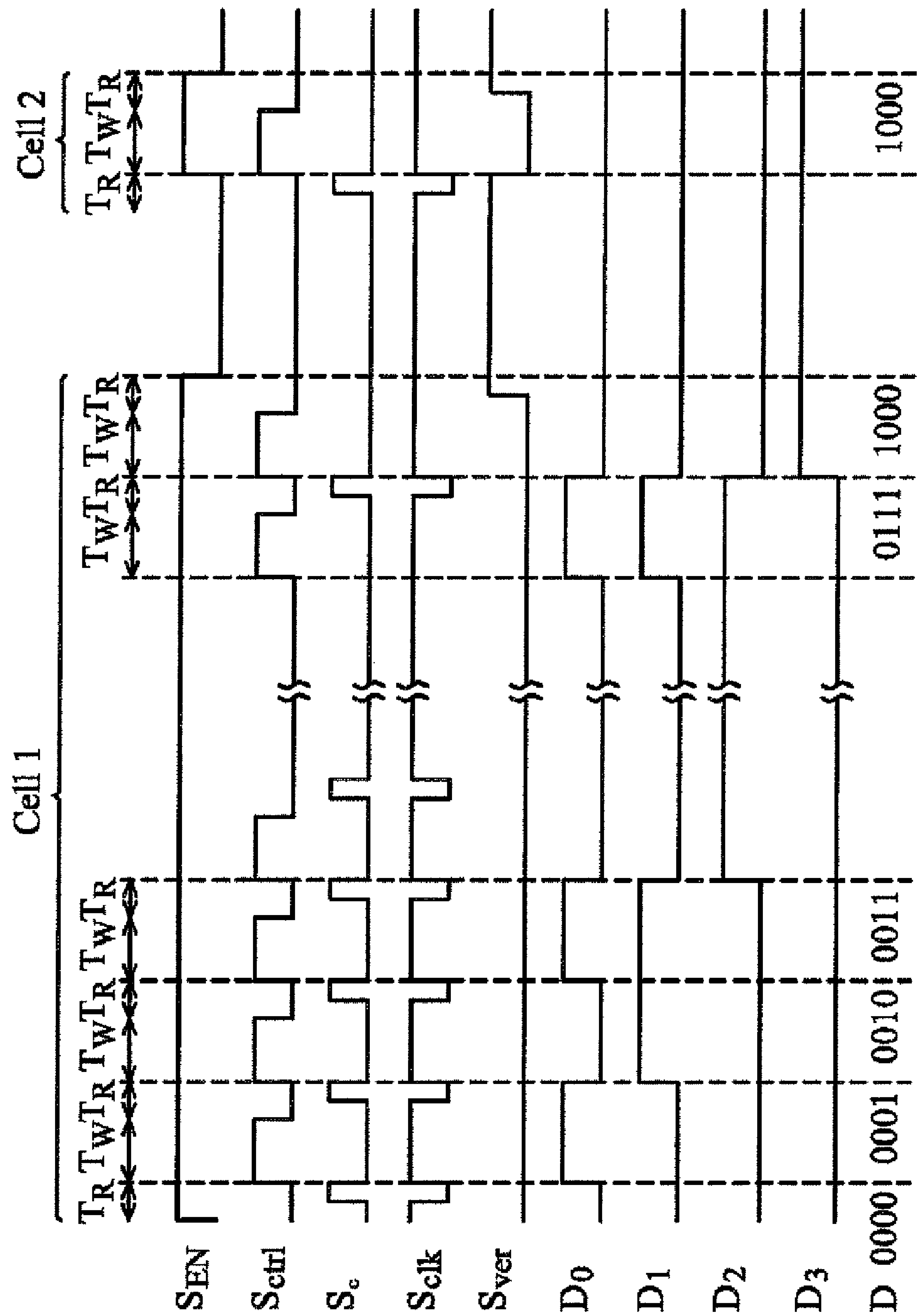
Cell 1
Cell 2
TR TW TR TW TR TW TR TW TR
TW TR TW TR
TR TW TR
SEN
Sctrl
Sc
Sclk
Sver
D0
D1
D2
D3
D 0000 0001 0010 0011 0111 1000 1000

FIG. 5A

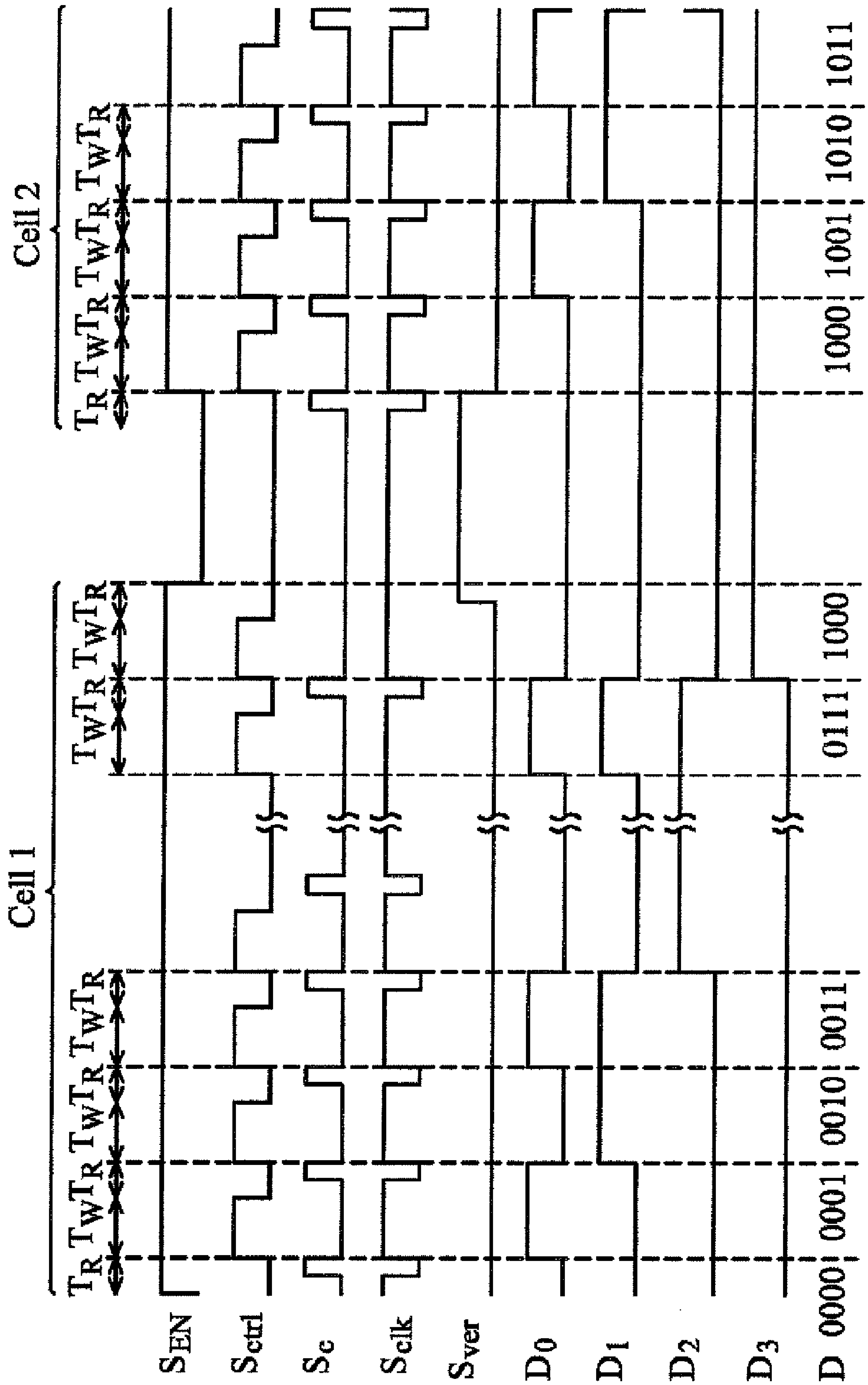
Cell 1
Cell 2
TR TW TR
SEN
Sctrl
Sc
Sclk
Sver
D0
D1
D2
D3
D 0000 0001 0010 0011 0111 1000 1000 1001 1010 1011

FIG. 5B

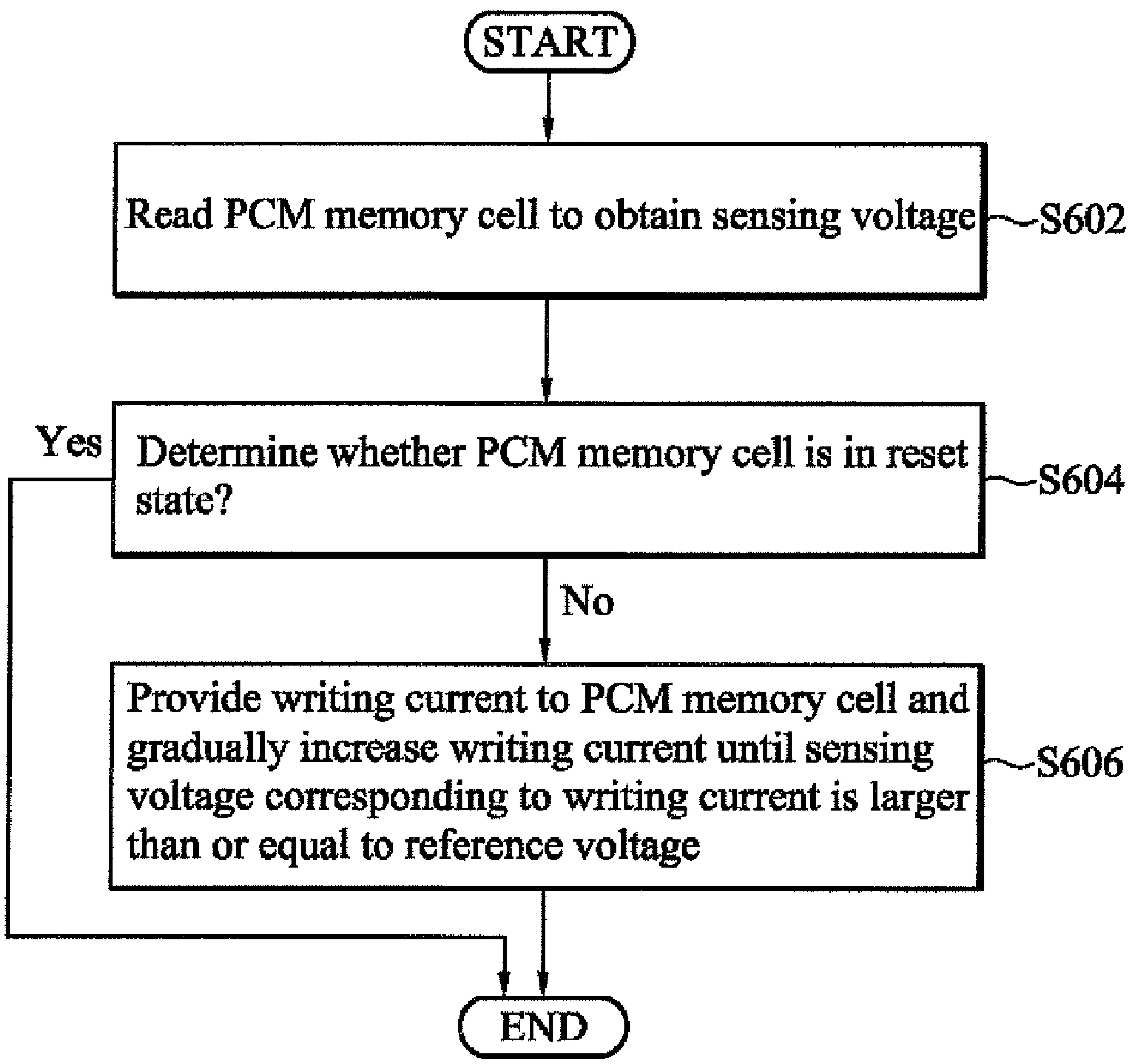
START
Read PCM memory cell to obtain sensing voltage
S602
Determine whether PCM memory cell is in reset state?
S604
Yes
No
Provide writing current to PCM memory cell and gradually increase writing current until sensing voltage corresponding to writing current is larger than or equal to reference voltage
S606
END

FIG. 6

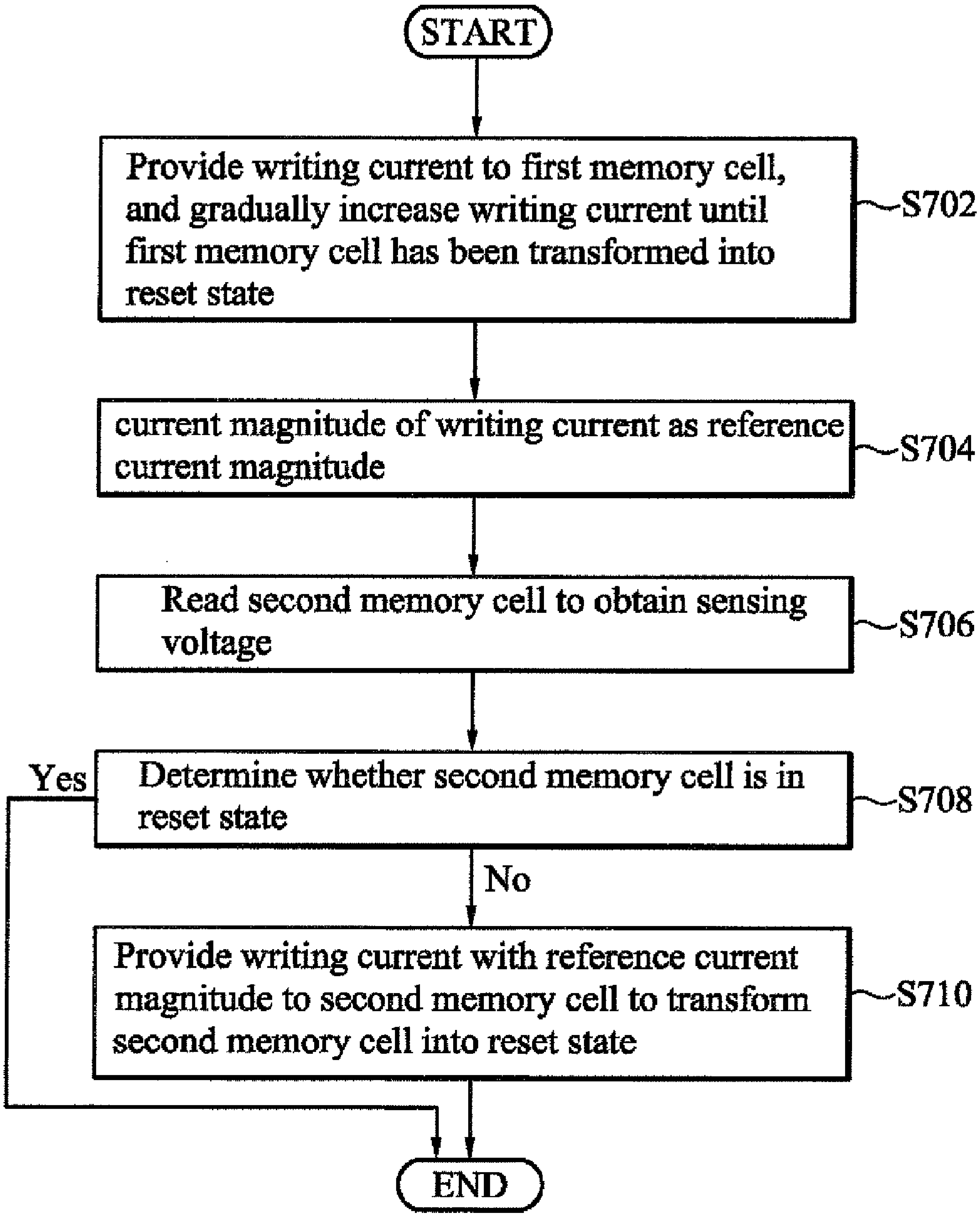
START
Provide writing current to first memory cell, and gradually increase writing current until first memory cell has been transformed into reset state
S702
current magnitude of writing current as reference current magnitude
S704
Read second memory cell to obtain sensing voltage
S706
Yes
Determine whether second memory cell is in reset state
S708
No
Provide writing current with reference current magnitude to second memory cell to transform second memory cell into reset state
S710
END

FIG. 7

VERIFICATION CIRCUITS AND METHODS FOR PHASE CHANGE MEMORY ARRAY

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

CROSS REFERENCE TO RELATED APPLICATIONS

This Application *is a reissue of U.S. patent application Ser. No. 12/485,720, filed Jun. 16, 2009, now U.S. Pat. No. 7,974,122, issued Jul. 5, 2011, which* claims priority of Taiwan Patent Application No. 097151378, filed on Dec. 30, 2008, the entirety of which **[**is**]** *are* incorporated by reference herein.

BACKGROUND

1. Technical Field

The present disclosure relates to a verification circuit, and more particularly to a verification circuit for a phase change memory array.

2. Description of the Related Art

A Phase Change Memory (PCM) is a non-volatile memory with high speed, high capacity and low energy consumption, wherein a plurality of PCM cells of the PCM cell is formed by phase change material, such as chalcogenide etc. The phase change material can be switched between two states, a crystalline state and an amorphous state, with the application of heat, wherein the phase change material has different resistances corresponding to the crystalline and amorphous states respectively, and the resistances respectively represent different stored data.

In general, different writing currents are provided to heat a PCM cell to change its resistance, such that data can be stored into the PCM cell. Furthermore, for a PCM cell, it is necessary for a writing current to transform the PCM cell into a reset state. Therefore, a verification circuit for verifying a PCM array is desired, which is used to verify that the memory cells of the PCM array have been transformed from a non-reset state to a reset state.

BRIEF SUMMARY

Verification circuits and verification methods for a phase change memory array are provided. An exemplary embodiment of such a verification circuit for a phase change memory array comprises: a sensing unit, sensing a first sensing voltage from a first memory cell of the phase change memory array according to an enable signal; a comparator, generating a comparing signal according to the first sensing voltage and a reference voltage, so as to indicate whether the first memory cell is in a reset state; a control unit, generating a control signal according to the enable signal; an operating unit, generating a first signal according to the control signal, so as to indicate whether the comparator is active; and an adjusting unit, providing a writing current to the first memory cell and adjusting the writing current according to the control signal until the comparing signal indicates that the first memory cell is in a reset state.

Furthermore, an exemplary embodiment of a verification method for a phase change memory array is provided. A memory cell of the phase change memory array is read to obtain a sensing voltage. The sensing voltage is compared with a reference voltage. When the sensing voltage is smaller than the reference voltage, a writing current is provided to the memory cell and the writing current is gradually increased until the sensing voltage corresponding to the writing current is larger than or equal to the reference voltage.

Moreover, another exemplary embodiment of a verification method for a phase change memory array is provided. A writing current is provided to a first memory cell of the phase change memory array and the writing current is gradually increased until a first sensing voltage sensed from the first memory cell is larger than or equal to a reference voltage. The current magnitude of the writing current is recorded as a reference current magnitude when the first sensing voltage is larger than or equal to a reference voltage. A second memory cell of the phase change memory array is read to obtain a second sensing voltage. It is determined whether the second memory cell is in a reset state by comparing the second sensing voltage and the reference voltage. The writing current with the reference current magnitude is provided to the second memory cell to transform the second memory cell into a reset state when the second memory cell is in a non-reset state.

A detailed description is given in the following exemplary embodiments with reference to the accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

FIG. **1** shows a verification circuit according to an exemplary embodiment;

FIG. **2** shows a waveform diagram of the signals of the verification circuit shown in FIG. **1**;

FIG. **3**A shows a schematic diagram of a control unit according to an exemplary embodiment;

FIG. **3**B shows a schematic diagram of a detecting unit according to an exemplary embodiment;

FIG. **3**C shows a schematic diagram of a calculating unit according to an exemplary embodiment;

FIG. **4** shows a verification circuit according to another exemplary embodiment;

FIGS. **5**A and **5**B show a waveform diagram illustrating the verification circuit of FIG. **4** performing a verification procedure for different memory cells, respectively;

FIG. **6** shows a verification method for a PCM array according to an exemplary embodiment; and

FIG. **7** shows a verification method for a PCM array according to another exemplary embodiment.

DETAILED DESCRIPTION

The following description is made for the purpose of illustrating the general principles of the disclosure and should not be taken in a limiting sense. The scope of the embodiments is best determined by reference to the appended claims and their equivalents.

FIG. **1** shows a verification circuit **110** for verifying whether each memory cell of a phase change memory (PCM) army **150** is in a reset state according to an exemplary embodiment. The verification circuit **110** comprises a sensing unit **112**, a comparator **114**, a control unit **116**, an operating unit **118**, a delay unit **124**, a flip-flop **126**, a determining unit **128**, an adjusting unit **130** and two switches **120** and **122**. The operating unit **118** is coupled between the control unit **116** and the delay unit **124**, and the operating unit **118** is used to receive a control signal S_{ctrl} to generate a signal S**1**, so as to indicate that the comparator **114** is active or not. The delay unit **124** receives and delays the signal S**1** to generate a signal S**2** and then provides the signal S**2** to a clock input terminal of the flip-flop **126**. In addition, the flip-flop **126** further comprises a data input terminal coupled to the switch **120** and a data output terminal coupled to the determining unit **128**.

When receiving an enable signal S_{EN} provided by the determining unit **128**, the sensing unit **112** may read a memory cell of the PCM array **150** to sense a resistance R_{cell} of the memory cell, so as to obtain a sensing voltage V_{cell} corresponding to the resistance R_{cell}. Next, the comparator **114** may compare the sensing voltage V_{cell} with a reference voltage V_{ref}, so as to generate a comparing signal S_c to indicate the state of the read memory cell. For example, the comparing signal S_c indicates that the read memory cell is in a non-reset state when the sensing voltage V_{cell} is smaller than the reference voltage V_{ref}, and the comparing signal S_c indicates that the read memory cell has be transformed into a reset state when the sensing voltage V_{cell} is larger than or equal to the reference voltage V_{ref}.

Furthermore, the determining unit **128** also provides the enable signal S_{EN} to the control unit **116** to generate the control signal S_{ctrl}. Next, the operating unit **118** generates the signal **S1** according to the control signal S_{ctrl}, so as to control the comparator **114** to operate or not. Next, the comparing signal S_c may control the switches **120** and **122** to turn on or off. The switch **120** is coupled between the control unit **116** and the adjusting unit **130** and the switch **122** is coupled between a voltage VDD and the switch **120**, wherein the switches **120** and **122** are controlled by the comparing signal S_c. Therefore, the comparing signal S_c may control the switches **120** and **122** to change the control signal S_{ctrl} into a signal S_{clk} and provide the signal S_{clk} to the adjusting unit **130** and the flip-flop **126**. Referring to FIG. **1** and FIG. **2** together, FIG. **2** shows a waveform diagram of the signals of the verification circuit **110** shown in FIG. **1**. The control signal S_{ctrl} and the signal S_{clk} are the pulse signals with identical frequencies but different duty cycles. In addition, the adjusting unit **130** comprises a writing current generator **132** and a calculating unit **134**. The calculating unit **134** may count/calculate the pulse number of the signal S_{clk} to generate an adjusting signal D comprising a plurality of bits. In the embodiment show in FIG. **2**, the adjusting signal D comprises four bits D_0, D_1, D_2 and D_3. Next, the writing current generator **132** generates a writing current I_{write} to the memory cell of the PCM array **150** according to the adjusting signal D, so as to transform the state of the memory cell. Furthermore, the writing current generator **132** may also adjust a current magnitude of the writing current I_{write} according to the adjusting signal D, i.e. the writing current I_{write} has the current magnitude corresponding to the adjusting signal D. In the present disclosure, the bit number of the adjusting signal D may determine accuracy of the current magnitude for the writing current I_{write}.

Referring to FIG. **2**, in a reading period T_R, the control signal S_{ctrl} is at a low voltage level, Simultaneously, the sensing unit **112** may sense the sensing voltage V_{cell} from the memory cell, i.e. the memory cell is read by the verification circuit **110**. In a writing period T_W, the adjusting unit **130** may provide the writing current I_{write} having the current magnitude corresponding to the adjusting signal D to the memory cell, so as to change the resistance of the memory cell. For example, for the duration that the data value of the adjusting signal D is "0010", the verification circuit **110** may provide the writing current I_{write} with the current magnitude corresponding to "0010" to the memory cell in a writing period T_W. Next, in a reading period T_R, the verification circuit **110** may sense and determine whether the memory cell is in a reset state. If not, the verification circuit **110** may provide the writing current I_{write} with the current magnitude corresponding to "0011" to the memory cell in a next writing period T_W. Therefore, the verification circuit **110** may gradually increase the writing current I_{write} until the memory cell is transformed from a non-reset state to a reset state. For example, for the duration that the data value of the adjusting signal D is "1000", the verification circuit **110** may provide the writing current I_{write} with the current magnitude corresponding to "1000" to the memory cell in a writing period T_W. Next, the verification circuit **110** may read the memory cell to obtain the sensing voltage V_{cell} corresponding to the current magnitude "1000" in a reading period T_R. The comparing signal S_c may indicate that the read memory cell has been transformed into a reset state when the sensing voltage V_{cell} corresponding to the current magnitude "1000" is larger than or equal to the reference voltage V_{ref}. Next, the flip-flop **126** may provide a verification signal S_{ver} to the determining unit **128**, so as to provide a next enable signal S_{EN} to the sensing unit **112** for verifying another memory cell.

FIG. **3**A shows a schematic diagram of a control unit according to an exemplary embodiment. Corresponding to an adjusting signal D with four bits, the control unit comprises sixteen detecting units **310**, five NOR gates **320** and four inverters **330**. FIG. **3**B shows a schematic diagram of a detecting unit according to an exemplary embodiment. The detecting unit comprises two delay units **340** and **350**, two XOR gates **360** and **370**, an inverter **380** and a flip-flop **390**. In a verification circuit, a period time of a writing period T_W is determined by the delay unit **340**, and an entire period time of a writing period T_W and a reading period T_R is determined by the delay unit **350**. FIG. **3**C shows a schematic diagram of a calculating unit according to an exemplary embodiment. In one embodiment, the calculating unit is an accumulator comprising four flip-flops.

FIG. **4** shows a verification circuit **410** according to another exemplary embodiment. Compared with the adjusting unit **130** of the verification circuit **110** in FIG. **1**, an adjusting unit **430** further comprises a register **436**. As described above, when the comparing signal S_c indicates that the read memory cell has been transformed into a reset state, the flip-flop **126** may generate the verification signal S_{ver} to the determining unit **128** to verify another memory cell. Simultaneously, the flip-flop **126** may also provide the verification signal S_{ver} to the register **436**, so as to store an adjusting signal D corresponding to the present current magnitude of the writing current I_{write} as a reference adjusting signal D_{ref}. Next, the determining unit **128** may provide a next enable signal S_{EN} to the register **436**, so as to provide the reference adjusting signal D_{ref} stored in the register **436** to the calculating unit **134**. Next, the calculating unit **134** may set the data value of the adjusting signal D according to the data value of the reference adjusting signal D_{ref} such that the writing current generator **132** may provide a writing current I_{write} corresponding to the reference adjusting signal D_{ref} to the another memory cell to be verified.

FIGS. **5**A and **5**B show a waveform diagram illustrating the verification circuit **410** of FIG. **4** performing a verification procedure for different memory cells, respectively. Referring to FIG. **4** and FIG. **5**A together, first, the verification circuit **410** starts to verify a memory cell Cell **1** of the PCM array **150**. As described above, for the duration that the data value of the adjusting signal D is "1000", the verification circuit **410** senses that the memory cell Cell **1** has been transformed into a reset state. Next, the register **436** may store "1000" as the data value of the reference adjusting signal D_{ref} according to the verification signal S_{ver}. Next, the verification circuit **410** starts to verify another memory cell Cell **2** of the PCM array **150**. The register **436** may provide the reference adjusting signal D_{ref} to the calculating unit **134** as an initial value of the adjusting signal D according to an enable signal S_{EN} corresponding to the memory cell Cell **2**. For the memory cell Cell

2, first, the verification circuit **410** may read the memory cell Cell **2**. Next, when sensing that the memory cell Cell **2** is in a non-reset state, the verification circuit **410** may provide a writing current I_{write} corresponding to the reference adjusting signal D_{ref}, i.e. the calculating unit **134** may provide the adjusting signal D which has data value "1000" to the writing current generator **132**, so as to generate the writing current I_{write}. Next, in a reading period T_R, the verification circuit **410** may read the memory cell **2** to obtain a sensing voltage V_{cell} corresponding to "1000". The comparing signal S_c indicates that the memory cell Cell **2** has been transformed into a reset state when the sensing voltage V_{cell} is larger than or equal to the reference voltage V_{ref}. Next, the flip-flop **126** generates the verification signal S_{ver} to the determining unit **128** to notify that the memory cell Cell **2** has been completely verified. Next, a next memory cell is verified until each memory cell of the PCM array has been completely verified. Accordingly, a verification time of a PCM memory array is decreased.

Referring to FIG. **4** and FIG. **5**B together, after the memory cell Cell **1** has been verified, the data value "1000" of the adjusting signal D is stored into the register **436** as the data value of the reference adjusting signal D_{ref}. Next, when sensing that the memory cell Cell**2** is in a non-reset state, the verification circuit **410** may provide the writing current I_{write} with a current magnitude corresponding to the reference adjusting signal D_{ref} to the memory cell Cell **2**. Next, in a reading period T_R, the verification circuit **410** may read the memory cell **2** to obtain a sensing voltage V_{cell} corresponding to "1000". When the sensing voltage V_{cell} is smaller than the reference voltage V_{ref} (i.e. the memory cell Cell **2** is in a non-reset state), the verification circuit **410** may gradually increase the writing current I_{write} according to the adjusting signal D until the memory cell Cell **2** is transformed into a reset state, as shown in FIG. **5**B. In one embodiment, the calculating unit **134** may use the data value "1000" of the reference adjusting signal D_{ref} as the initial value of the adjusting signal D, and increase the data value of the adjusting signal D according to the pulse number of the signal S_{clk}.

FIG. **6** shows a verification method for a PCM array according to an exemplary embodiment. First, in step S**602**, a memory cell of the PCM array is read to obtain a sensing voltage. Next, it is determined whether the memory cell has been transformed into a reset state by comparing the sensing voltage with a reference voltage (step S**604**). Next, in step **S606**, a writing current is provided to the memory cell when the sensing voltage is smaller than the reference voltage (i.e. the memory cell is in a non-reset state), and the writing current is gradually increased until the sensing voltage corresponding to the writing current is larger than or equal to the reference voltage, i.e. the memory cell is in a reset state, thus the memory cell is completely verified.

FIG. **7** shows a verification method for a PCM array according to another exemplary embodiment. First, in step **S702**, a writing current is provided to a first memory cell of the PCM array, and the writing current is gradually increased until a sensing voltage sensed from the first memory cell is larger than or equal to a reference voltage, i.e. the first memory cell has been transformed into a reset state. Next, a current magnitude of the writing current is recorded and stored as a reference current magnitude when the first memory cell has been transformed into a reset state (step **S704**). Next, a second memory cell of the PCM array is read to obtain a second sensing voltage (step S**706**). Next, it is determined whether the second memory cell is in a reset state by comparing the second sensing voltage with a reference voltage (step S**708**). A writing current with the reference current magnitude is provided to the second memory cell when the second memory cell is in a non-reset state, so as to transform the second memory cell from a non-reset state to a reset state (step S**710**). The second memory cell is in a non-reset state when the second sensing voltage corresponding to the writing current is smaller than the reference voltage. Therefore, the writing current is gradually increased until the second sensing voltage corresponding to the writing current is larger than or equal to the reference voltage, such that the second memory cell is transformed into a reset state.

While the disclosure has been described by way of example and in terms of embodiments, it is to be understood that the disclosure is not limited thereto. It will be apparent to those skilled in the art that various modifications and variations can be made in the disclosure. It is intended that the embodiments described be considered as exemplary only, with the true scope of the embodiments being indicated by the following claims and their equivalents.

What is claimed is:

1. A verification circuit for a phase change memory array, comprising:

a sensing unit, sensing a first sensing voltage from a first memory cell of the phase change memory array according to an enable signal;

a comparator, generating a comparing signal according to the first sensing voltage and a reference voltage to indicate whether the first memory cell is in a reset state;

a control unit, generating a control signal according to the enable signal; an operating unit, generating a first signal according to the control signal to indicate whether the comparator is active; and

an adjusting unit, providing a writing current to the first memory cell and adjusting the writing current according to the control signal until the comparing signal indicates that the first memory cell is in a reset state.

2. The verification circuit as claimed in claim **1**, wherein the comparing signal indicates that the first memory cell is in a non-reset state when the first sensing voltage is smaller than the reference voltage, and the comparing signal indicates that the first memory cell is in a reset state when the first sensing voltage is larger than or equal to the reference voltage.

3. The verification circuit as claimed in claim **2**, wherein when the comparing signal indicates that the first memory cell is in a non-reset state, the adjusting unit gradually increases the writing current according to the control signal.

4. The verification circuit as claimed in claim **1**, wherein the control signal is a pulse signal, and wherein the sensing unit senses the first sensing voltage from the first memory cell when the control signal is at a first voltage level, and the adjusting unit provides the writing current to the first memory cell when the control signal is at a second voltage level.

5. The verification circuit as claimed in claim **4**, further comprising:

a first switch, having a first terminal coupled to the control unit and a second terminal coupled to the adjusting unit, wherein the first switch is controlled to transmit the control signal of the control unit to the adjusting unit according to the comparing signal; and

a second switch coupled between a specific voltage and the second terminal, having a control terminal for receiving the comparing signal.

6. The verification circuit as claimed in claim **5**, further comprising:

a delay unit, delaying the first signal to generate a second signal;

a flip-flop, having a data input terminal coupled to the second terminal, a clock input terminal for receiving the second signal, and a data output terminal for providing a verification signal; and

a determining unit, providing the enable signal to the control unit.

7. The verification circuit as claimed in claim **6**, wherein the adjusting unit further comprises:

a calculating unit, calculating the pulse number of the control signal to generate an adjusting signal with a plurality of bits; and

a writing current generator, generating the writing current which has a current magnitude corresponding to the adjusting signal, and wherein the current magnitude of the writing current is of reference current magnitude when the comparing signal indicates that the first memory cell is in a reset state.

8. The verification circuit as claimed in claim **7**, wherein the adjusting unit further comprises:

a register, storing the reference current magnitude.

9. The verification circuit as claimed in claim **6**, wherein when the comparing signal indicates that the first memory cell is in a reset state, the determining unit provides the enable signal to the sensing unit according to the verification signal such that the sensing unit senses a second sensing voltage from a second memory cell of the phase change memory array according to the enable signal.

10. The verification circuit as claimed in claim **9**, wherein when the comparing signal indicates that the first memory cell is in a reset state, the determining unit provides the enable signal to the control unit according to the verification signal such that the control unit generates the control signal according to the enable signal.

11. The verification circuit as claimed in claim **10**, wherein the adjusting unit provides the writing current with the reference current magnitude to the second memory cell according to the control signal.

12. The verification circuit as claimed in claim **11**, wherein the comparator generates the comparing signal according to the reference voltage and the second sensing voltage corresponding to the reference current magnitude, so as to indicate whether the second memory cell is in a reset state.

13. The verification circuit as claimed in claim **12**, wherein the comparing signal indicates that the second memory cell is in a reset state when the second sensing voltage is larger than or equal to the reference voltage, and wherein the comparing signal indicates that the second memory cell is in a non-reset state when the second sensing voltage is smaller than the reference voltage.

14. The verification circuit as claimed in claim **13**, wherein when the comparing signal indicates that the second memory cell is in a non-reset state, the adjusting unit gradually increases the writing current provided to the second memory cell according to the control signal such that the current magnitude of the writing current is larger than the reference current magnitude.

15. A verification method for a phase change memory array, comprising:

providing a writing current to a first memory cell of the phase change memory array and gradually increasing the writing current until a first sensing voltage sensed from the first memory cell is larger than or equal to a reference voltage;

recording the current magnitude of the writing current as a reference current magnitude when the first sensing voltage is larger than or equal to a reference voltage;

reading a second memory cell of the phase change memory array to obtain a second sensing voltage;

determining whether the second memory cell is in a reset state by comparing the second sensing voltage and the reference voltage; and

providing the writing current with the reference current magnitude to the second memory cell to transform the second memory cell into a reset state when the second memory cell is in a non-reset state.

16. The verification method as claimed in claim **15**, further comprising:

when the second sensing voltage corresponding to the reference current magnitude is smaller than the reference voltage, gradually increasing the writing current until the second sensing voltage corresponding to the writing current is larger than or equal to the reference voltage.

17. The verification method as claimed in claim **16**, wherein the second memory cell is in a reset state when the second sensing voltage corresponding to the writing current is larger than or equal to the reference voltage, and wherein the second memory cell is in a non-reset state when the second sensing voltage corresponding to the writing current is smaller than the reference voltage.

18. A method, comprising:

increasing a writing current applied to a first memory cell of a non-volatile memory until a first sensing voltage is larger than or equal to a reference voltage;

identifying a magnitude of the writing current as a reference current magnitude;

determining that a second memory cell of the non-volatile memory is in a non-reset state by comparing a second sensing voltage and the reference voltage; and

providing the writing current with the reference current magnitude to the second memory cell in response to said determining.

19. The method of claim 18, wherein the non-volatile memory comprises a memory which has different resistances corresponding to at least two switchable states of the non-volatile memory.

20. The method of claim 19, wherein the two switchable states comprise a crystalline state and an amorphous state indicative of stored data in the non-volatile memory.

21. The method of claim 18, wherein the non-volatile memory comprises a phase change memory.

22. The method of claim 18, further comprising determining that the first memory cell is in a reset state if the first sensing voltage is larger than or equal to the reference voltage, wherein said identifying comprises identifying the magnitude of the writing current in response to determining that the first memory cell is in the reset state.

23. The method of claim 18, further comprising transforming the second memory cell into a reset state in response to providing the writing current with the reference current magnitude.

24. A circuit, comprising:

a sensing unit configured to identify a sensing voltage associated with a first memory cell of a non-volatile memory;

a writing current generator configured to increase a writing current applied to the first memory cell until the first sensing voltage is larger than or equal to a reference voltage, wherein a magnitude of the writing current is configured to be identified as a reference current magnitude; and

a comparator configured to compare a second sensing voltage and the reference voltage, wherein the writing current with the reference current magnitude is applied *to a second memory cell of the non-volatile memory in response to determining that the second memory cell is in a non-reset state.*

25. The circuit of claim 24, wherein the non-volatile memory comprises a memory device which changes resistance according to a switched state of the non-volatile memory.

26. The circuit of claim 25, wherein the switched state comprises a crystalline state or an amorphous state indicative of stored data in the non-volatile memory.

27. The circuit of claim 24, wherein the non-volatile memory comprises a phase change memory.

28. The circuit of claim 24, wherein the comparator is further configured to determine that the first memory cell is in a reset state if the first sensing voltage is larger than or equal to the reference voltage, and wherein the magnitude of the writing current is configured to be identified in response to determining that the first memory cell is in the reset state.

29. The circuit of claim 24, wherein the second memory cell is configured to be transformed into a reset state in response to applying the writing current with the reference current magnitude.

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