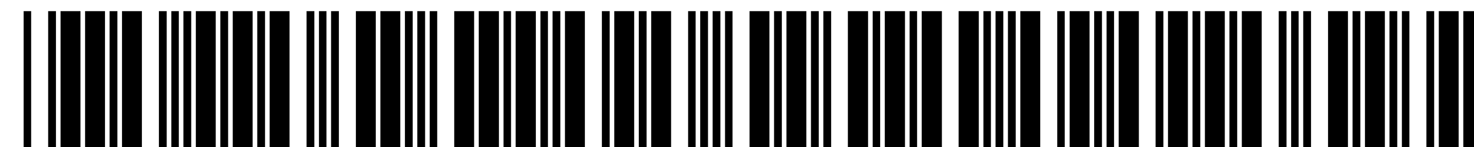

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(54) **SEMICONDUCTOR INTEGRATED CIRCUIT HAVING PADS LAYOUT FOR INCREASING SIGNAL INTEGRITY AND REDUCING CHIP SIZE**

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H01L 23/49 (2006.01)
H01L 23/52 (2006.01)
H01L 23/495 (2006.01)

(52) **U.S. Cl.**
USPC **257/692**; 257/666; 257/672; 257/695; 257/735; 257/E23.013; 257/E23.043; 438/123

(58) **Field of Classification Search**
USPC 257/666, 692, E23.013, E23.043, 672, 257/695, 735; 438/123
See application file for complete search history.

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(57) **ABSTRACT**

A semiconductor integrated circuit device includes a semiconductor chip having a memory cell array region surrounded with a peripheral circuit region and includes a plurality of bonding pads disposed at least in one row on only one side of the semiconductor chip. The circuit device may include first leads group disposed adjacent to the bonding pad side and a second leads group disposed opposite the first leads group. The second leads group may be formed over a portion of the semiconductor chip (lead-on-chip structure). A plurality of bonding wires connect the first and second leads group with the plurality of bonding pads respectively.

26 Claims, 5 Drawing Sheets

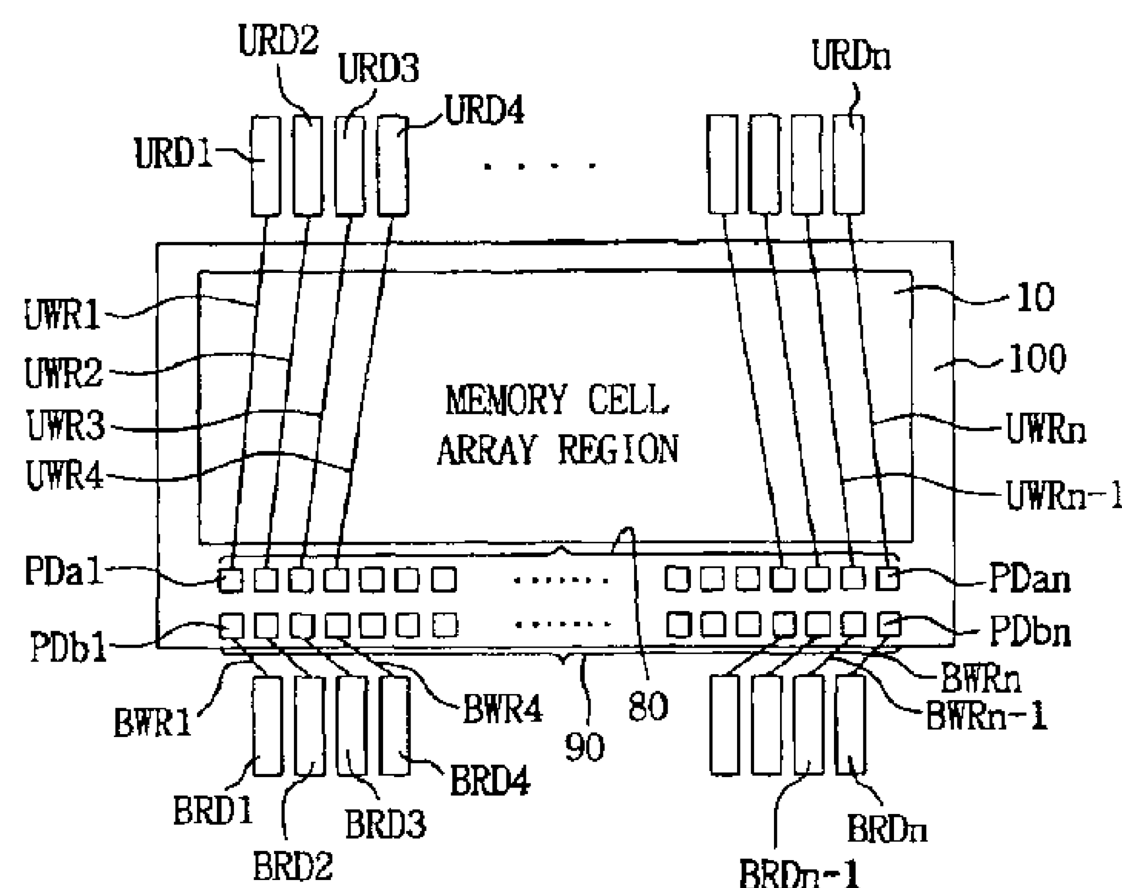


FIG. 1 (PRIOR ART)

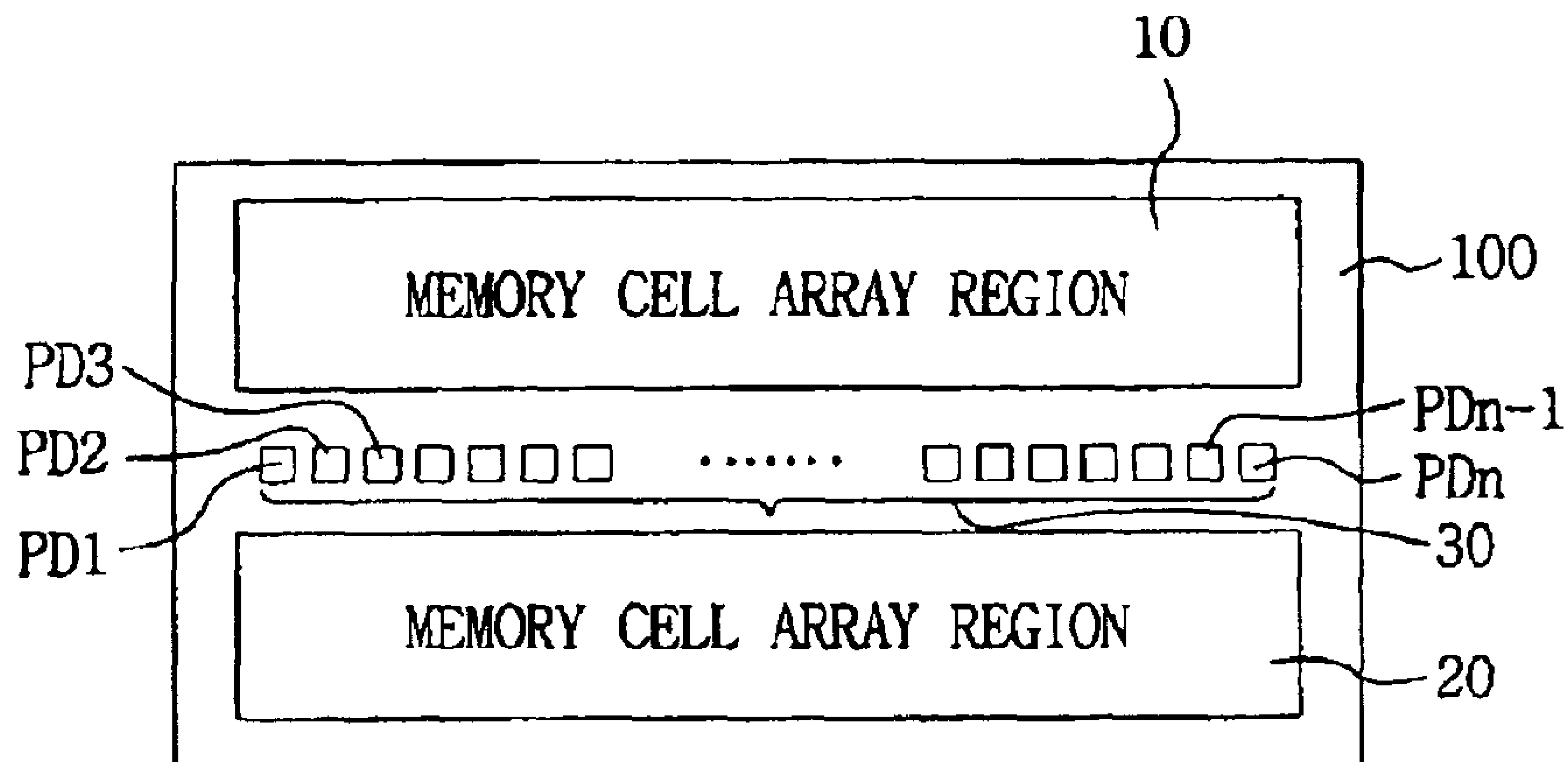


FIG. 2a (PRIOR ART)

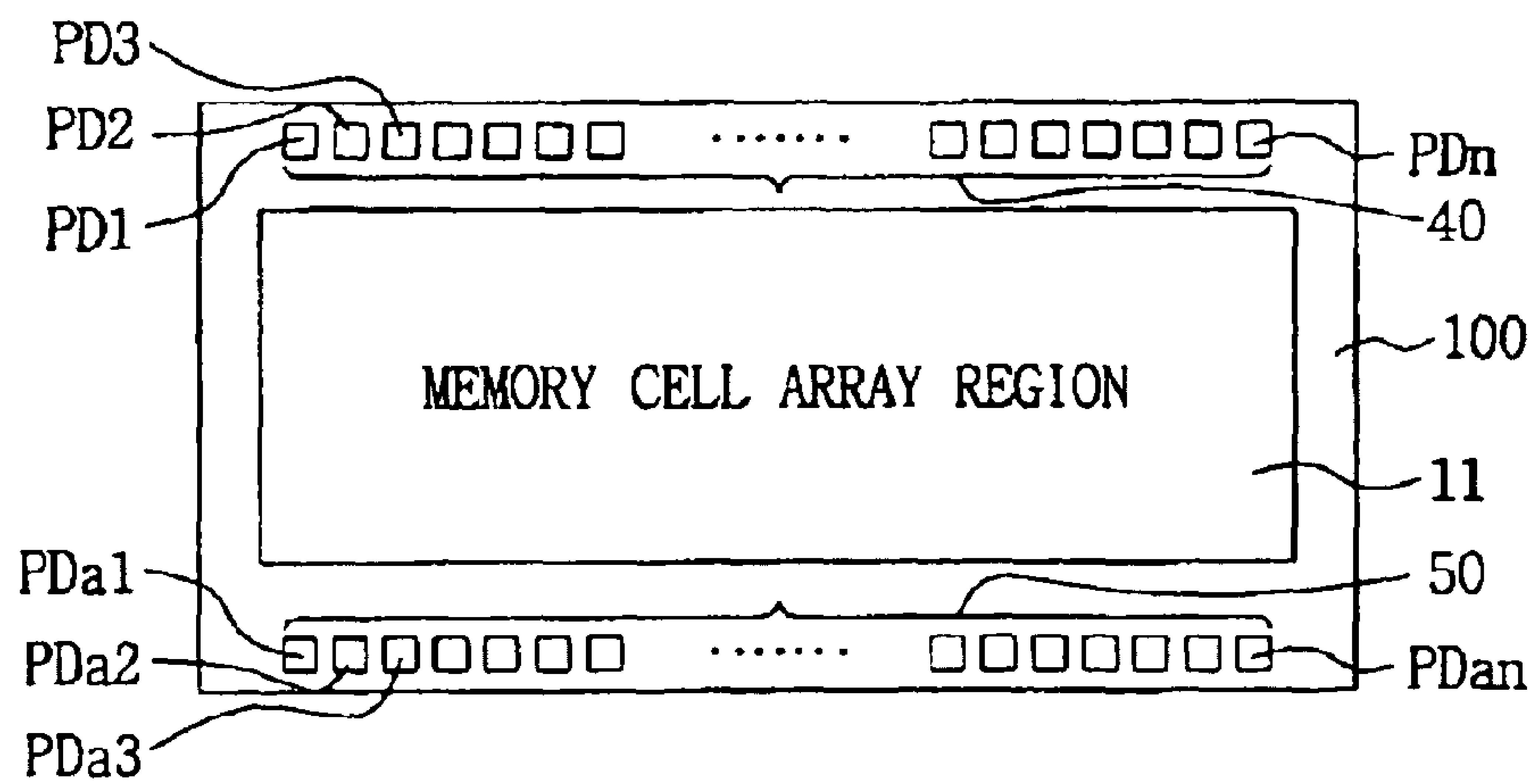


FIG.2b (PRIOR ART)

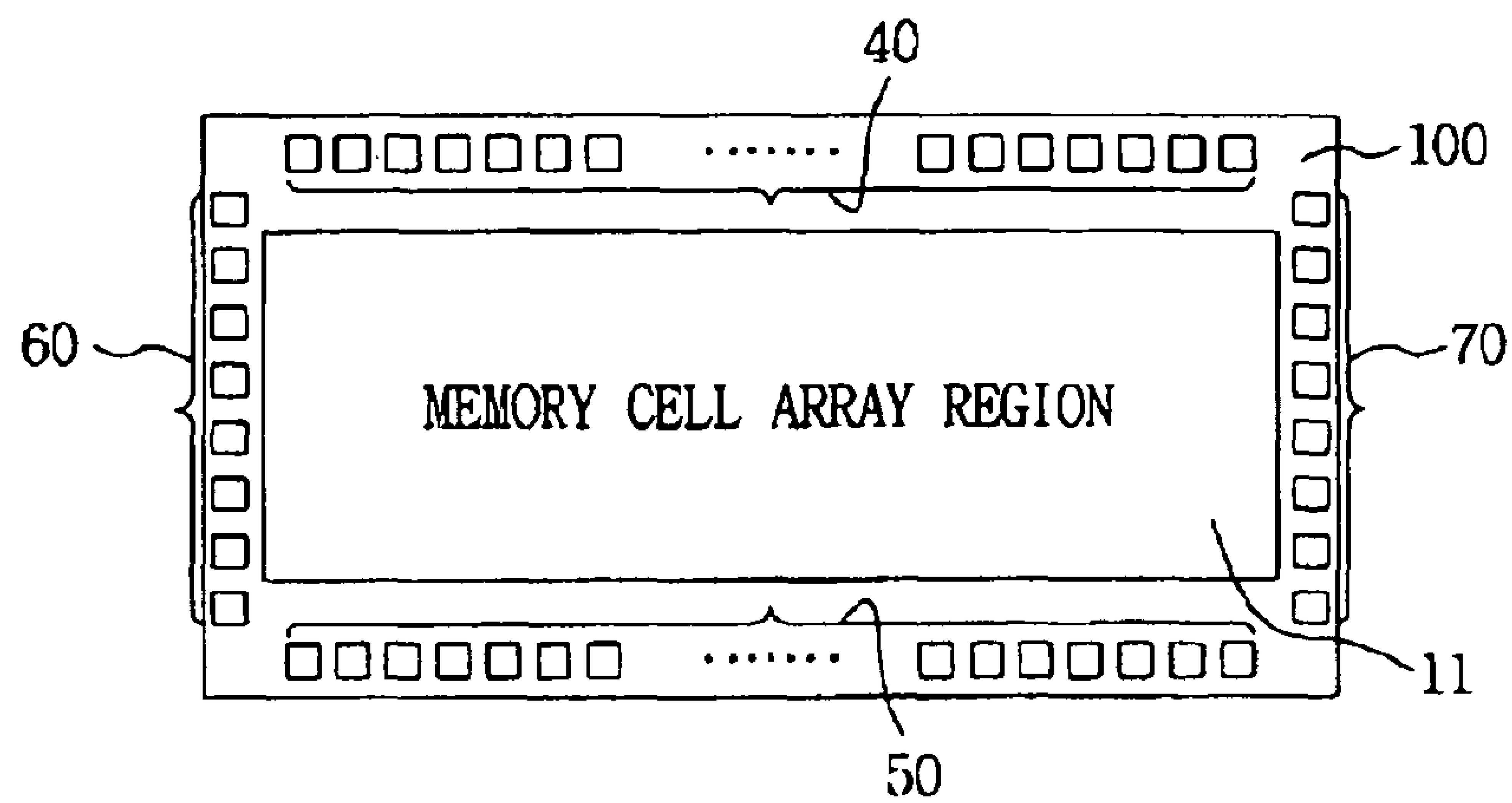


FIG.3

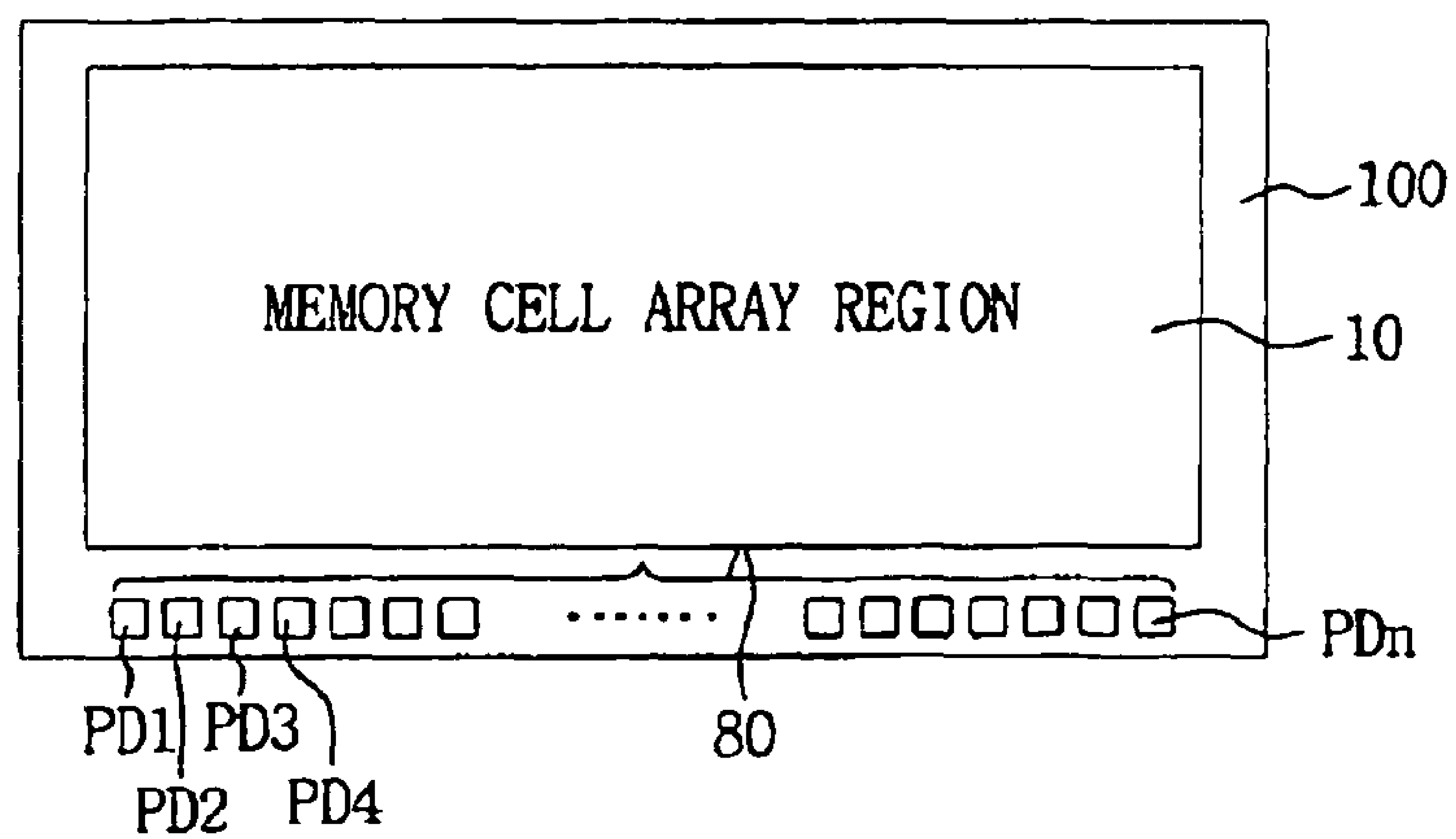


FIG.4

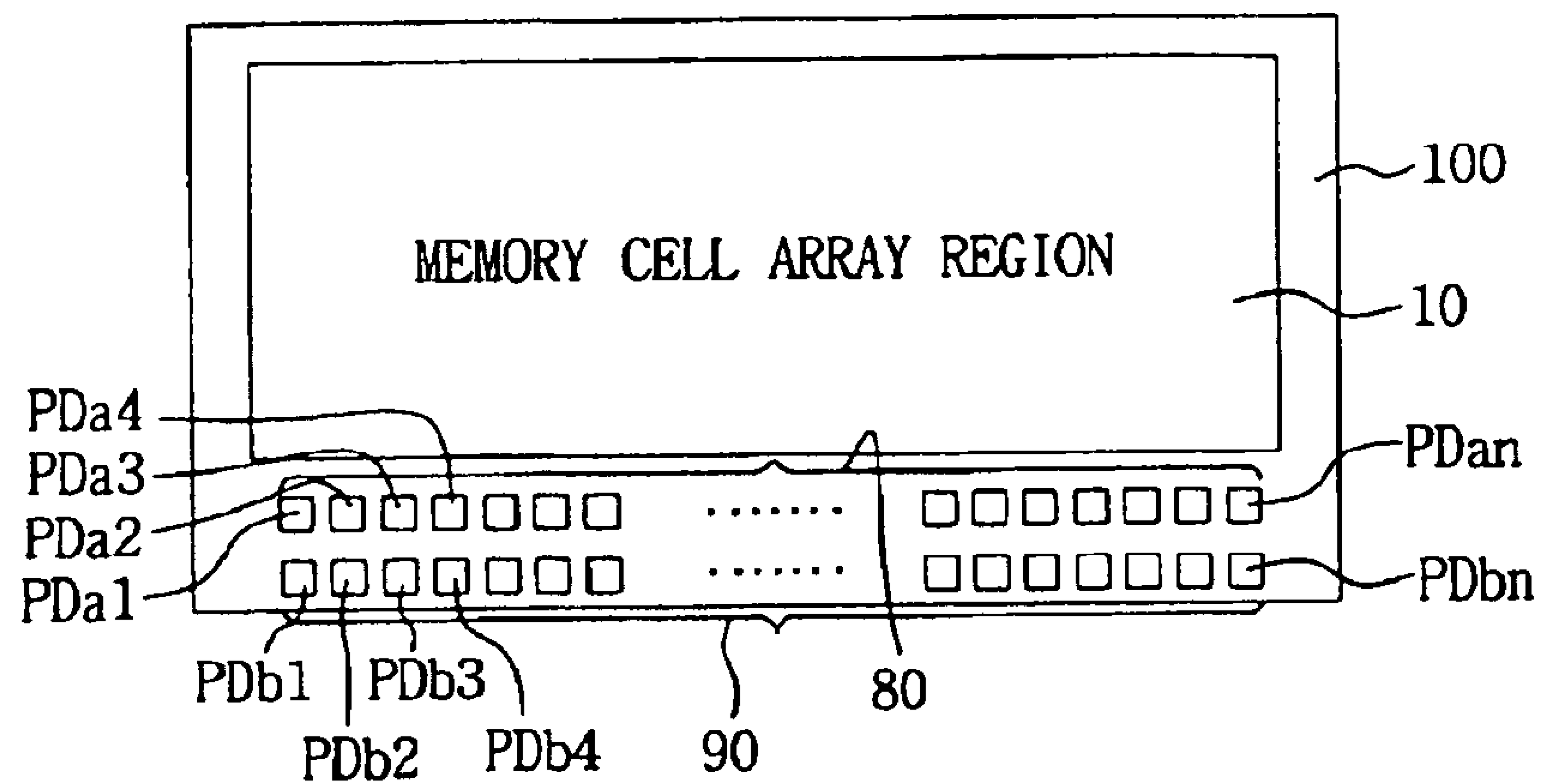


FIG.5

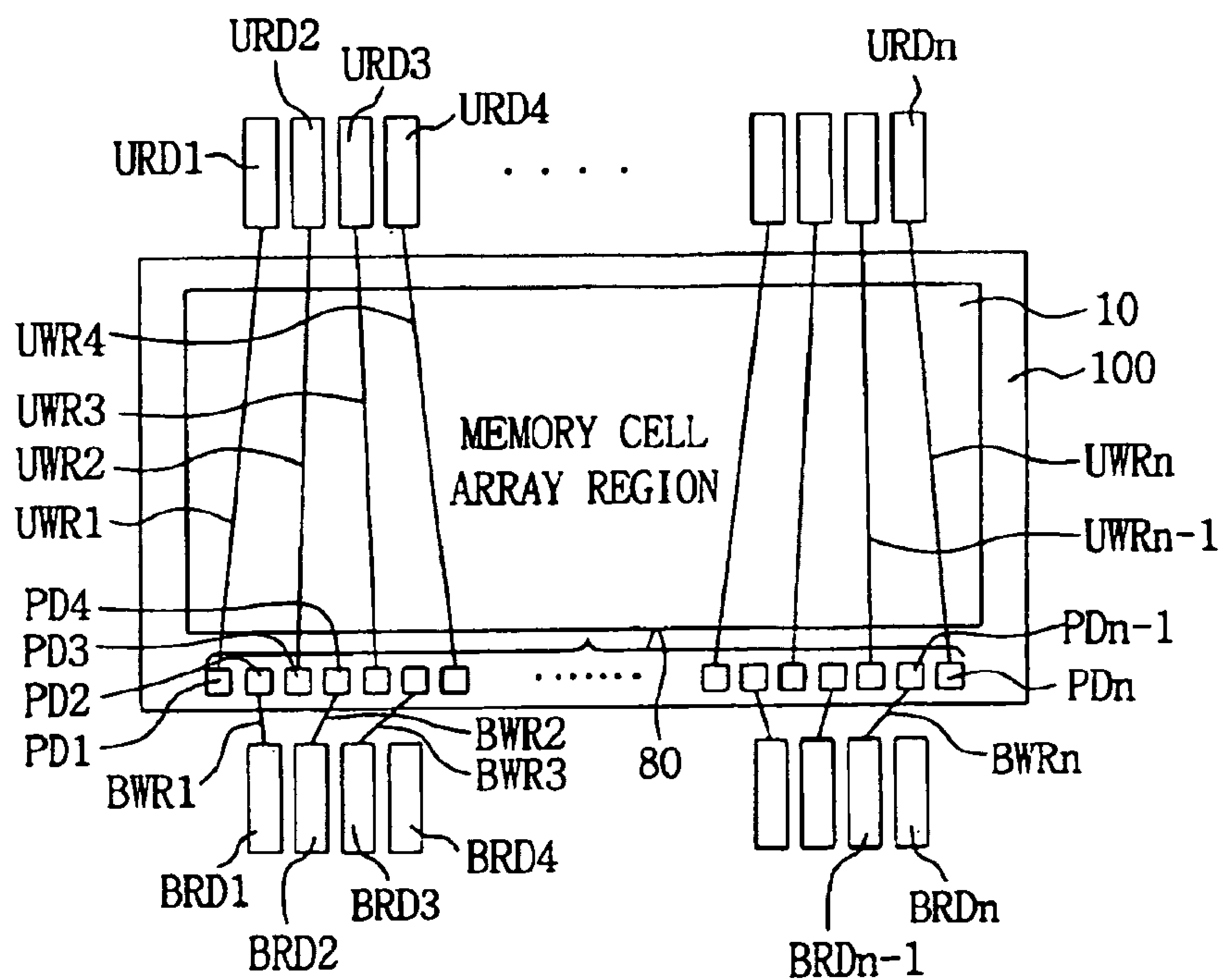


FIG.6

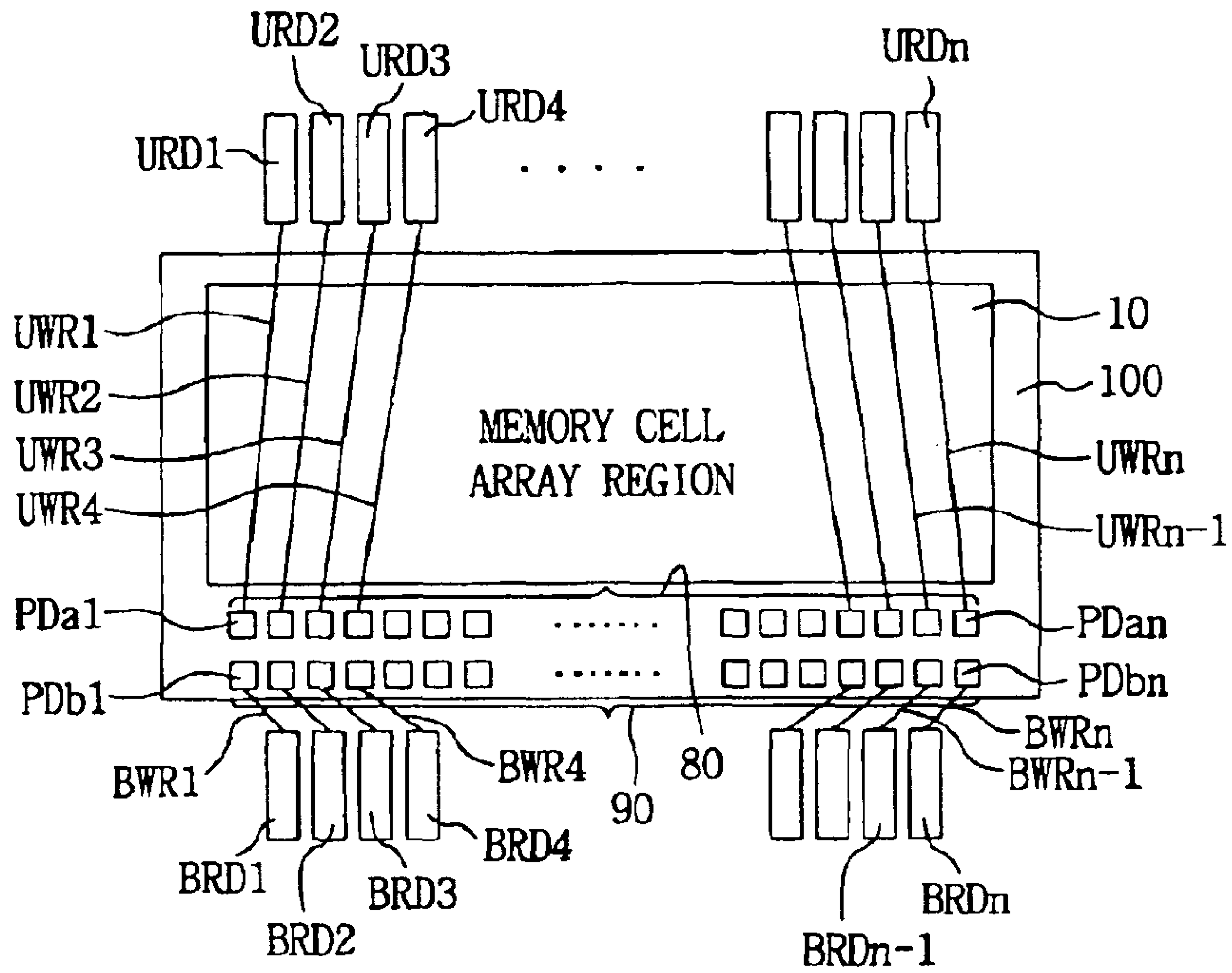


FIG.7

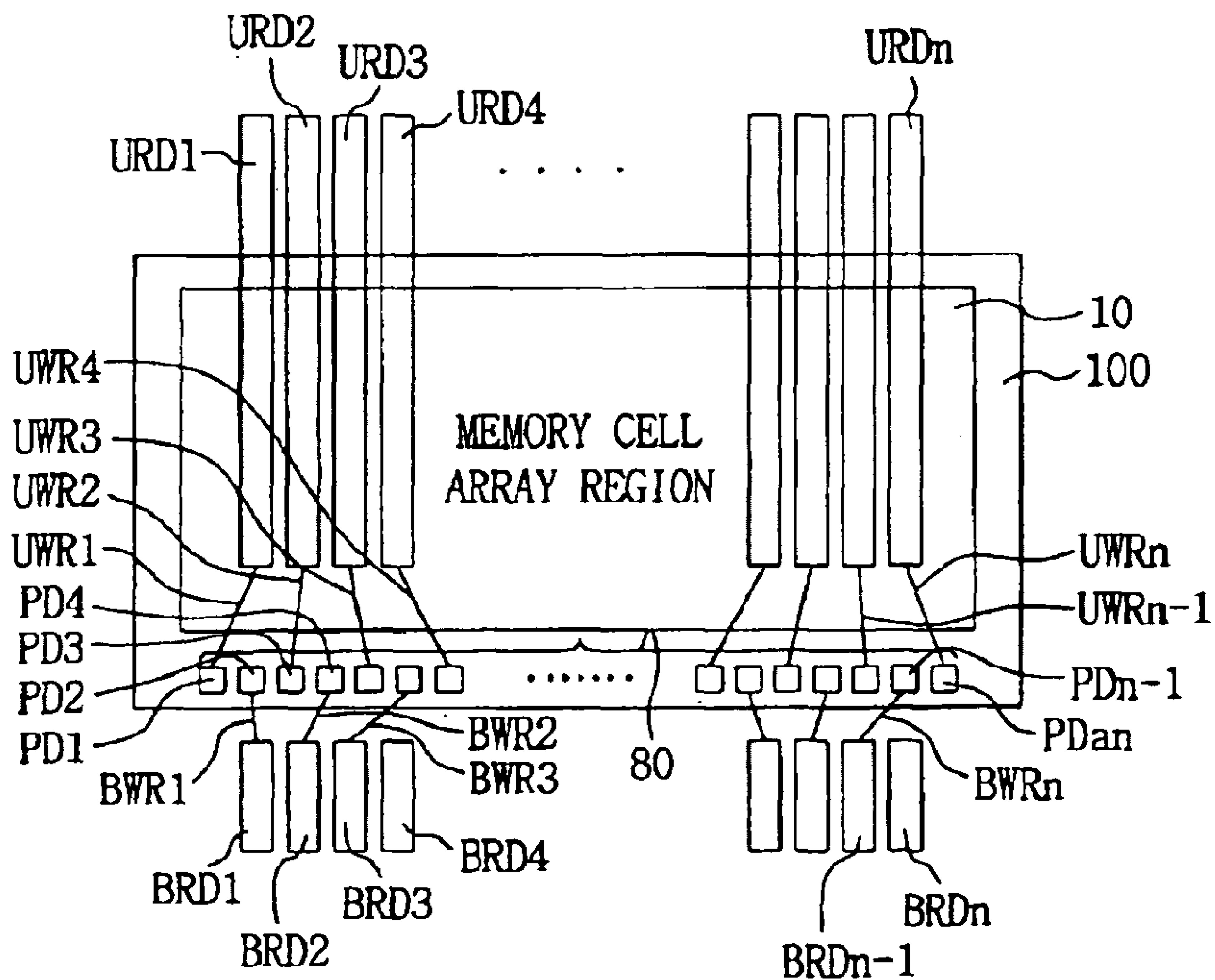
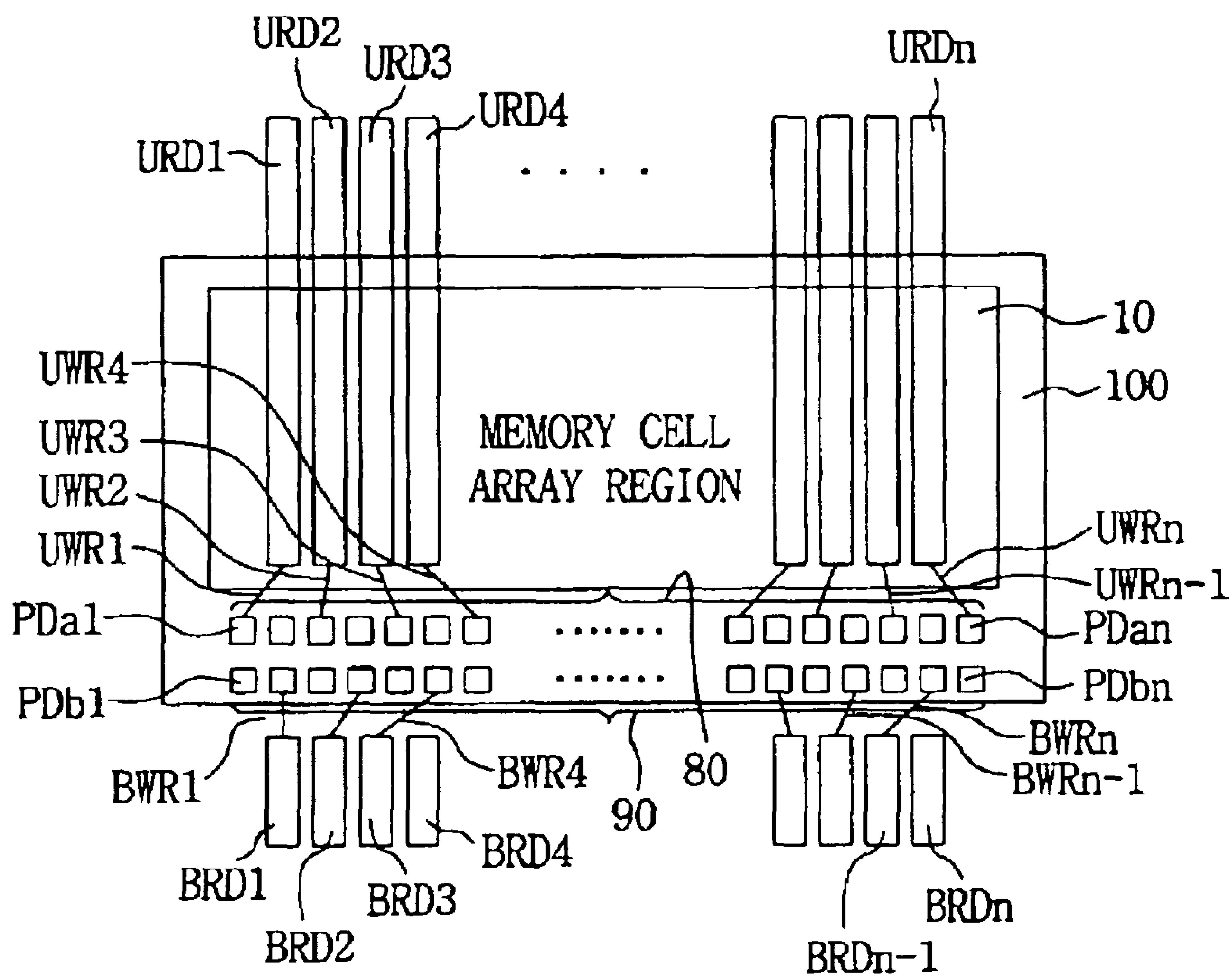


FIG.8



SEMICONDUCTOR INTEGRATED CIRCUIT HAVING PADS LAYOUT FOR INCREASING SIGNAL INTEGRITY AND REDUCING CHIP SIZE

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

This application is a reissue application for U.S. Pat. No. 6,975,020 issued on Dec. 13, 2005 on U.S. Ser. No. 10/750,686 filed Jan. 5, 2004.

This U.S. nonprovisional patent application claims priority under 35 U.S.C. §119 of Korean Patent Application 2003-11686 filed on Feb. 25, 2003, the entire contents of which is hereby incorporated by reference.

FIELD OF THE INVENTION

The present invention relates to a semiconductor integrated circuit device, and more particularly to a pad layout and a wire bonding in a semiconductor integrated circuit device, such as a semiconductor memory device etc.

DESCRIPTION OF THE RELATED ART

A semiconductor integrated circuit, such as a semiconductor memory device generally has bonding pads on an upper surface of a chip to allow for an external electrical connection with another chip. Electrical signals, such as command input signals, data read and data write operation signals are input or output the chip through the bonding pads.

Even though a degree of integration for elements mounted in the semiconductor chip may be increased, e.g., doubled, the number of bonding pads may not be increased by much. An area occupied by the bonding pads may be not so important in a high integration degree memory device etc., but may be a more important factor in a low integration degree memory device. As a result, fabrication processes have been improved to reduce chip size, while, the actual size of bonding pads has not been reduced. That is, even if the size of a chip may be reduced, a size of the bonding pads may not be easily reduced because of problems such as reinvestment in bonding equipment and test equipment using the bonding pads. Therefore, the area occupied by the bonding pads in the chip has tended to increase.

FIG. **1** is a plan view illustrating the exterior of a semiconductor integrated circuit device **100** having a general structure of pads with a center layout. Referring to FIG. **1**, bonding pads PD**1**,PD**2**~PDn are disposed in one row between memory cell array regions **10**, **20**. A place where the bonding pads PD**1**,PD**2**~PDn are located becomes an upper part of a peripheral circuit region **30**. Such a layout of the bonding pads is called a pads center layout system. Wire bonding for pads with the pads center layout structure may be performed over upper parts of the memory cell array region **10** and the memory cell array region **20** on chip **100**. In other words, part of the leads from a lead frame may be disposed close to the memory cell array region **10**, and the remaining leads may be disposed close to the memory cell array region **20**. Wires connecting between each of the leads and each of the pads may be formed over an upper part of the memory cell array regions **10**, **20** thus undergo a bonding operation. The pads center layout structure has a shortcoming in that cell array regions are separated from each other because the pads PD**1**~PDn are disposed between the memory cell array regions **10**, **20**, and this detrimentally influences signal integrity.

FIGS. **2**a and **2**b are plan views showing the exterior of a semiconductor integrated circuit device having a general structure of an edge pad layout system. FIG. **2**a illustrates a layout of bonding pads PD**1**~PDn, PDa**1**~PDan disposed in parallel only on two sides of the chip **100**. While, FIG. **2**b illustrates a layout of bonding pads disposed on all four sides of the chip **100**. In wire bonding pads of an edge pad layout system, there may be no wire formed over an upper part of a memory cell array region **11**, but a reduction of the chip size may be difficult to realize because the pads are disposed on several sides of the chip **100**. Also, signal integrity may be reduced by the dispersed layout of the bonding pads.

Accordingly, a desire exists in the industry to dispose bonding pads more efficiently to reduce a chip size and increase signal integrity.

SUMMARY OF THE INVENTION

Exemplary embodiments of the present invention provide a semiconductor integrated circuit device having a bonding pads layout structure capable of increasing signal integrity and reducing a chip size.

Exemplary embodiments of the present invention provide a semiconductor integrated circuit device including a semiconductor chip having a memory cell region and a peripheral region, and a plurality of bonding pads disposed on only one side of the semiconductor chip.

In an exemplary embodiment, a plurality of bonding pads may be disposed in at least one row on one side of a semiconductor chip.

In another exemplary embodiment, a plurality of bonding pads may be disposed in two rows on one side of a semiconductor chip.

In another exemplary embodiment, a semiconductor integrated device includes a plurality of bonding pads disposed in one row on one side of a chip, a first leads group disposed to the bonding pad side of the chip and a second leads group disposed opposite the first leads group. A plurality of bonding wires electrically connect the two leads group with the bonding pads respectively.

In another exemplary embodiment, a semiconductor integrated device includes a plurality of bonding pads disposed in two rows on one side of a chip, a first leads group disposed to the bonding pad side of the chip and a second leads group disposed opposite the first leads group. A plurality of bonding wires electrically connect the two leads group with the bonding pads respectively.

In another exemplary embodiment, a semiconductor integrated device includes a plurality of bonding pads disposed in one row on one side of a chip, a first leads group disposed to the bonding pad side of the chip and a second leads group formed over a portion of the semiconductor chip. A plurality of bonding wires electrically connect the two leads group with the bonding pads respectively.

In another exemplary embodiment, a semiconductor integrated device includes a plurality of bonding pads disposed in two rows on one side of a chip, a first leads group disposed to the bonding pad side of the chip and a second leads group formed over a portion of the semiconductor chip. A plurality of bonding wires electrically connect the two leads group with the bonding pads respectively.

The pad layout structure of the semiconductor integrated circuit device may increase a signal integrity for signals input

and output through circuits of a peripheral circuit region, by using a pads layout on only one side of the chip, and may reduce a chip size by using a concentrated layout of bonding pads and circuit elements constituting the peripheral circuit region on only one side of the chip.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other features of the present invention will become readily apparent from the description of exemplary embodiments that follows with reference to the accompanying drawings, in which like reference numerals and symbols designate like elements, in which:

FIG. **1** is a plan view illustrating the exterior of a semiconductor integrated circuit device having a conventional structure of pads center layout;

FIGS. **2**a and **2**b are plan views illustrating the exterior of a semiconductor integrated circuit device having a conventional structure of an edge pad layout system;

FIG. **3** is a plan view showing the exterior of a semiconductor integrated circuit device having one side pad layout according to an exemplary embodiment of the present invention;

FIG. **4** is a plan view showing the exterior of a semiconductor integrated circuit device having one-side dual pad layout structure according to an exemplary embodiment of the present invention;

FIGS. **5** and **6** are plan views showing the exterior of a semiconductor integrated circuit device with a wire bonding corresponding to each pad layout of FIGS. **3** and **4**; and

FIGS. **7** and **8** are plan views illustrating the exterior of a semiconductor integrated circuit device with a wire bonding provided on a lead on chip(LOC) structure according to exemplary embodiments varied from FIGS. **5** and **6**.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS OF THE INVENTION

The present invention and exemplary embodiments thereof are more fully described below with reference to the accompanying drawings. This invention may, however, be embodied in many different forms and should not be construed as being limited to the exemplary embodiments set forth herein; rather, these exemplary embodiments are provided so that this disclosure is thorough and complete, and conveys the concept of the invention to those skilled in the art.

According to exemplary embodiments of the present invention, a semiconductor integrated circuit device having one-side layout structure of bonding pads is provided.

FIG. **3** is a plan view illustrating the exterior of a semiconductor integrated circuit device having a one side pad layout structure according to an exemplary embodiment of the present invention. Referring to FIG. **3**, the semiconductor integrated circuit device includes a semiconductor chip **100**, and the semiconductor chip **100** has a memory cell array region **10** surrounded with peripheral circuit regions. A plurality of bonding pads PD**1**~PDn are disposed only on one side of the semiconductor chip **100** in the region **80** among the peripheral circuit regions. Though the drawing shows that the plurality of bonding pads PD**1**~PDn are disposed on one side of the chip **100** where the peripheral circuit region **80** is located, the bonding pads may instead be disposed on one of the other three sides of the chip **100**.

FIG. **4** is a plan view showing the exterior of a semiconductor integrated circuit device having a one-side dual pad layout structure according to an exemplary embodiment of the present invention. Referring to FIG. **4**, the bonding pads are disposed in more than one row, as compared to the layout structure of FIG. **3**. The layout structure of FIG. **4** indicates the plurality of bonding pads PDa**1**~PDan, PDb**1**~PDbn disposed in two rows on one side of the chip **100**.

FIGS. **5** and **6** are plan views illustrating the exterior of a semiconductor integrated circuit device with wire bonding corresponding to a layout of pads shown in FIGS. **3** and **4**. Referring first to FIG. **5**, in one side bonding pad layout referred to FIG. **3**, first leads group BRD**1**~BRDn drawn from a lead frame are disposed adjacently to the one side of the semiconductor chip **100**. Thus, wire bonding of a first group of wires BWR**1**~BWRn for correspondingly connecting the pads PD**2**,PD**4**~PDn-**1** of the plurality of bonding pads PD**1**~PDn with the first leads group BRD**1**~BRDn is performed over an upper part of the peripheral circuit region **80**. That is, the wire bonding of the first group wires BWR**1**~BWRn is not performed over an upper part of the memory cell array region **10**.

The second group leads URD**1**~URDn drawn from the lead frame are disposed adjacently a side opposing the side with the bonding pads PD**1**~PDn. Thus, wire bonding of a second group of wires UWR**1**~UWRn for correspondingly connecting the remaining bonding pads PD**1**,PD**3**~PDn of the plurality of bonding pads PD**1**~PDn with the second group leads URD**1**~URDn is performed over an upper part of the memory cell array region **10**.

With reference to FIG. **6**, a wire bonding relationship in a one-side two-rows bonding pad layout shown in FIG. **4** is illustrated. The bonding pads adjacent to one another in the one-side one-line layout of the semiconductor chip as shown in FIG. **3**, are wire-bonded alternately with the first and second group leads BRD**1**~BRDn, URD**1**~URDn as shown in FIG. **5**. In case of the bonding pads disposed in two rows on one side of the semiconductor chip as shown in FIG. **4**, the bonding pads PDa**1**~PDan of the first row and the bonding pads PDb**1**~PDbn of the second row are wire-bonded to the first and second group leads BRD**1**~BRDn and URD**1**~URDn, respectively as shown in FIG. **6**.

Consequently, a chip size may be reduced because the bonding pads are disposed on one side of the chip **100**, and signal integrity for signals input and output through circuits provided within the peripheral circuit region is increased because of the concentrated layout of the bonding pads.

FIGS. **7** and **8** are plan views illustrating the exterior of a semiconductor integrated circuit device having a LOC (Lead-On-Chip) structure according to an exemplary embodiments varied from FIGS. **5** and **6** respectively. Such a layout may be more advantageously applicable to the LOC structure.

The bonding wire and lead arrangement of FIG. **7** is the same as the arrangement of FIG. **5**, except that the second group leads URD**1**~URDn extend over the chip **100** consistent with on a LOC structure. In this structure, the wire bonding between the second group leads URD**1**~URDn and the bonding pads is performed over a portion of the memory cell array region **10** closest to the bonding pads. Such a wire bonding arrangement substantially reduces a length of wires UWR**1**~UWRn as compared with FIG. **5**.

The bonding wire and lead arrangement of FIG. **8** is the same as the arrangement of FIG. **6**, except that the second group leads URD**1**~URDn extend over the chip **100** consistent with a LOC structure. Here, a length of the bonding wires UWR**1**~UWRn is also substantially reduced as compared with FIG. **6**.

In FIGS. **7** and **8**, the bonding pads are disposed in one or two rows on one side of the chip **100**, thus a chip size is reduced and signal integrity for signals input and output

through circuits provided within the peripheral circuit region is increased because of a concentrated layout of the bonding pads.

As described above, a pads layout structure of a semiconductor integrated circuit device increases signal integrity for signals input and output through circuits provided within a peripheral circuit region by a one-side pad layout of a chip. Additionally, a concentrated layout of the bonding pads and circuit elements constituting the peripheral circuit region on only one side of a chip reduces a chip size.

While the present invention has been particularly shown and described with reference to the exemplary embodiments described above, it will be understood by those skilled in the art that these exemplary embodiments do not limit the scope of the present invention. For instance, a shape or array relationship of pads may be varied. Thus, various changes in form and details may be made without departing from the spirit and scope of the invention as defined by the appended claims.

What is claimed is:

1. A semiconductor integrated circuit device, comprising:

a semiconductor chip having a memory cell array region and a peripheral circuit region surrounding the memory cell array region;

a plurality of bonding pads disposed on only **[**one**]** *a first* side of the semiconductor chip on the peripheral circuit region; and

a plurality of leads formed on *both the one side of the semiconductor chip on which the bonding pads are disposed and* a *second* side of the semiconductor chip opposite the *first* side on which the bonding pads are disposed for connection with the bonding pads*;*

the plurality of leads including a first leads group on the first side of the semiconductor chip on which the bonding pads are disposed and a second leads group on the second side of the semiconductor chip opposite the first side on which the bonding pads are disposed;

a plurality of bonding wires having a first plurality of bonding wires and a second plurality of bonding wires electrically connecting the first leads group and the second leads group, respectively, with the plurality of bonding pads;

wherein the first plurality of bonding wires only cross the peripheral circuit region and;

wherein the second plurality of bonding wires or the second plurality of bonding wires and the second leads group cross the memory cell array region.

2. The device of claim **1**, wherein the plurality of bonding pads are disposed in at least one row.

3. The device of claim **2**, wherein the plurality of bonding pads are disposed in two rows.

[4. The device of claim **1**, further comprising:

a plurality of bonding wires electrically connecting the plurality of leads, respectively, with a portion of the bonding pads so as to cross the memory cell array region.**]**

5. A semiconductor integrated circuit device, comprising:

a semiconductor chip having a memory cell array region and a peripheral circuit region surrounding the memory cell array region;

a plurality of bonding pads disposed in at least one row on only **[**one**]** *a first* side of the semiconductor chip on the peripheral circuit region;

a first leads group disposed adjacent to the **[**bonding pad**]** *first* side of the semiconductor chip;

a second leads group disposed opposite the first leads group; and

a plurality of bonding wires having a first plurality of bonding wires and a second plurality of bonding wires electrically connecting the first leads group and the second leads group, respectively, with the plurality of bonding pads*;*

wherein the first plurality of bonding wires only cross the peripheral circuit region and;

wherein the second plurality of bonding wires or the second plurality of bonding wires and the second leads group cross the memory cell array region.

6. The device of claim **5**, wherein the second leads group disposed opposite the first leads group are located to a *second* side of the semiconductor chip opposite the **[**bonding pad**]** *first* side.

7. The device of claim **5**, wherein the plurality of bonding pads are electrically connected alternately with the first leads group and the second leads group by the first plurality of bonding wires and the second plurality of bonding wires, respectively, the first plurality of bonding wires being disposed over the peripheral circuit region, the second plurality of bonding wires being disposed over the memory cell array region.

8. The device of claim **5**, wherein the plurality of bonding pads are disposed in a first row and a second row, the first row of bonding pads and the second row of bonding pads being electrically connected to the first leads group and the second leads group, respectively, by the first plurality of bonding wires and the second plurality of bonding wires, the first plurality of bonding wires being disposed over the peripheral circuit region, and the second plurality of bonding wires being disposed over the memory cell array region.

[9. The device of claim **5**, wherein the second leads group extends over a portion of the semiconductor chip region.**]**

10. **[**The device of claim **9**,**]** *A semiconductor integrated circuit device, comprising:*

a semiconductor chip having a memory cell array region and a peripheral circuit region surrounding the memory cell array region;

a plurality of bonding pads disposed in at least one row on only a first side of the semiconductor chip on the peripheral circuit region;

a first leads group disposed adjacent to the first side of the semiconductor chip;

a second leads group disposed opposite the first leads group; and

a plurality of bonding wires having a first plurality of bonding wires and a second plurality of bonding wires electrically connecting the first leads group and the second leads group, respectively, with the plurality of bonding pads;

wherein the first plurality of bonding wires only cross the peripheral circuit region and;

wherein the second plurality of bonding wires or the second plurality of bonding wires and the second leads group cross the memory cell array region, wherein the plurality of bonding pads are electrically connected alternately with the first leads group and the second leads group by the first plurality of bonding wires and the second plurality of bonding wires, respectively**[**, the first plurality of bonding wires being disposed over the peripheral circuit region, the second plurality of bonding wires being disposed over the memory cell array region**]**.

11. **[**The device of claim **9**,**]** *A semiconductor integrated circuit device, comprising:*

a semiconductor chip having a memory cell array region and a peripheral circuit region surrounding the memory cell array region;

a plurality of bonding pads disposed in at least one row on only a first side of the semiconductor chip on the peripheral circuit region;

a first leads group disposed adjacent to the first side of the semiconductor chip;

a second leads group disposed opposite the first leads group; and

a plurality of bonding wires having a first plurality of bonding wires and a second plurality of bonding wires electrically connecting the first leads group and the second leads group, respectively, with the plurality of bonding pads;

wherein the first plurality of bonding wires only cross the peripheral circuit region and;

wherein the second plurality of bonding wires or the second plurality of bonding wires and the second leads group cross the memory cell array region, wherein the plurality of bonding pads are disposed in a first row and a second row, the first row of bonding pads and a second row of bonding pads being electrically connected to the first leads group and the second leads group, respectively, by the first plurality of bonding wires and the second plurality of bonding wires[, the first plurality of bonding wires being disposed over the peripheral circuit region, and the second plurality of bonding wires being disposed over the memory cell array region].

12. A semiconductor integrated circuit device, comprising:

a semiconductor chip having a memory cell array region;

a plurality of bonding pads disposed on only [one] *a first* side of the semiconductor chip; and

a plurality of leads formed on *both the first side of the semiconductor chip on which the bonding pads are disposed and* a *second* side of the semiconductor chip opposite the [one] *first* side on which the bonding pads are disposed for connection with the bonding pads*;*

the plurality of leads including a first leads group on the first side of the semiconductor chip on which the bonding pads are disposed and a second leads group on the second side of the semiconductor chip opposite the first side on which the bonding pads are disposed;

a plurality of bonding wires having a first plurality of bonding wires and a second plurality of bonding wires electrically connecting the first leads group and the second leads group, respectively, with the plurality of bonding pads;

wherein the first plurality of bonding wires do not cross the memory cell array region and;

wherein the second plurality of bonding wires or the second plurality of bonding wires and the second leads group cross the memory cell array region.

[**13**. The device of claim **12**, further comprising:

a plurality of bonding wires electrically connecting the plurality of leads to corresponding bonding pads disposed on the one side so as to cross the memory cell array region.]

14. The device of claim **12**, wherein the plurality of bonding pads are disposed in at least one row.

15. The device of claim **14**, wherein the plurality of bonding pads are disposed in two rows.

16. The device of claim **12**, wherein

the semiconductor chip includes a peripheral circuit region surrounding the memory cell array region, and

the bonding pads are disposed on the [one] *first* side of the semiconductor chip on the peripheral circuit region.

17. A semiconductor integrated circuit device, comprising:

a semiconductor chip having a memory cell array region and a peripheral circuit region on a front surface of the semiconductor chip, the front surface including a first side and a second side opposite to the first side;

a plurality of bonding pads disposed in the peripheral circuit region, the bonding pads being adjacent to and along only the first side;

a first leads group adjacent to the first side;

a second leads group adjacent to the second side; and

a plurality of bonding wires having a first plurality of bonding wires and a second plurality of bonding wires electrically connecting the first leads group and the second leads group, respectively, with the plurality of bonding pads;

wherein the plurality of bonding pads include a first bonding pads group and a second bonding pads group, the first bonding pads group is connected to the first leads group by the first plurality of bonding wires and the second bonding pads group is connected to the second leads group by the second plurality of bonding wires, respectively; and

wherein the first bonding pads group is only on a first region of the peripheral circuit region and the second bonding pads group is only on a second region of the peripheral circuit region, the first region is separated from the second region by a space.

18. The device of claim 17, wherein the second leads group is opposite the first leads group.

19. The device of claim 17, wherein the second leads group is located to a side of the semiconductor chip opposite the bonding pad side.

20. The device of claim 17, wherein the plurality of bonding pads are electrically connected alternately with the first leads group and the second leads group by the first plurality of bonding wires and the second plurality of bonding wires, respectively.

21. The device of claim 17, wherein the plurality of bonding pads are in a first row and a second row, the first row of bonding pads and the second row of bonding pads being electrically connected to the first leads group and the second leads group, respectively, by the first plurality of bonding wires and the second plurality of bonding wires.

22. The device of claim 17, wherein the second leads group extends over a portion of the semiconductor chip.

23. The device of claim 22, wherein the plurality of bonding pads are electrically connected alternately with the first leads group and the second leads group by the first plurality of bonding wires and the second plurality of bonding wires, respectively, the first plurality of bonding wires being over the peripheral circuit region, the second plurality of bonding wires being over at least a portion of the memory cell array region.

24. The device of claim 22, wherein the plurality of bonding pads are in a first row and a second row, the first row of bonding pads and a second row of bonding pads being electrically connected to the first leads group and the second leads group, respectively, by the first plurality of bonding wires and the second plurality of bonding wires, the first plurality of bonding wires being over the peripheral circuit region, and the second plurality of bonding wires being over at least a portion of the memory cell array region.

25. The device of claim 17, wherein at least one of the first and second leads groups extends across the semiconductor chip.

26. The device of claim 17, wherein only the first plurality of bonding wires extend across a side of the semiconductor chip.

27. The device of claim 17, wherein the front surface further comprises a third side and a fourth side opposite to the third side, the first side is longer than the third side.

28. The device of claim 27, wherein the second leads group extends over a portion of the semiconductor chip.

29. The device of claim 28, wherein one end of each lead of the second leads group is adjacent to and outside of the semiconductor chip and the other end of each lead of the second leads group is adjacent to the first side.

* * * * *