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**H01K 3/10** (2006.01)

(52) **U.S. Cl.**  
USPC ..... **29/852**; 29/832; 29/841; 29/851;  
257/737; 257/738; 257/778; 257/E21.503;  
361/760; 361/764; 361/820; 438/63; 438/64

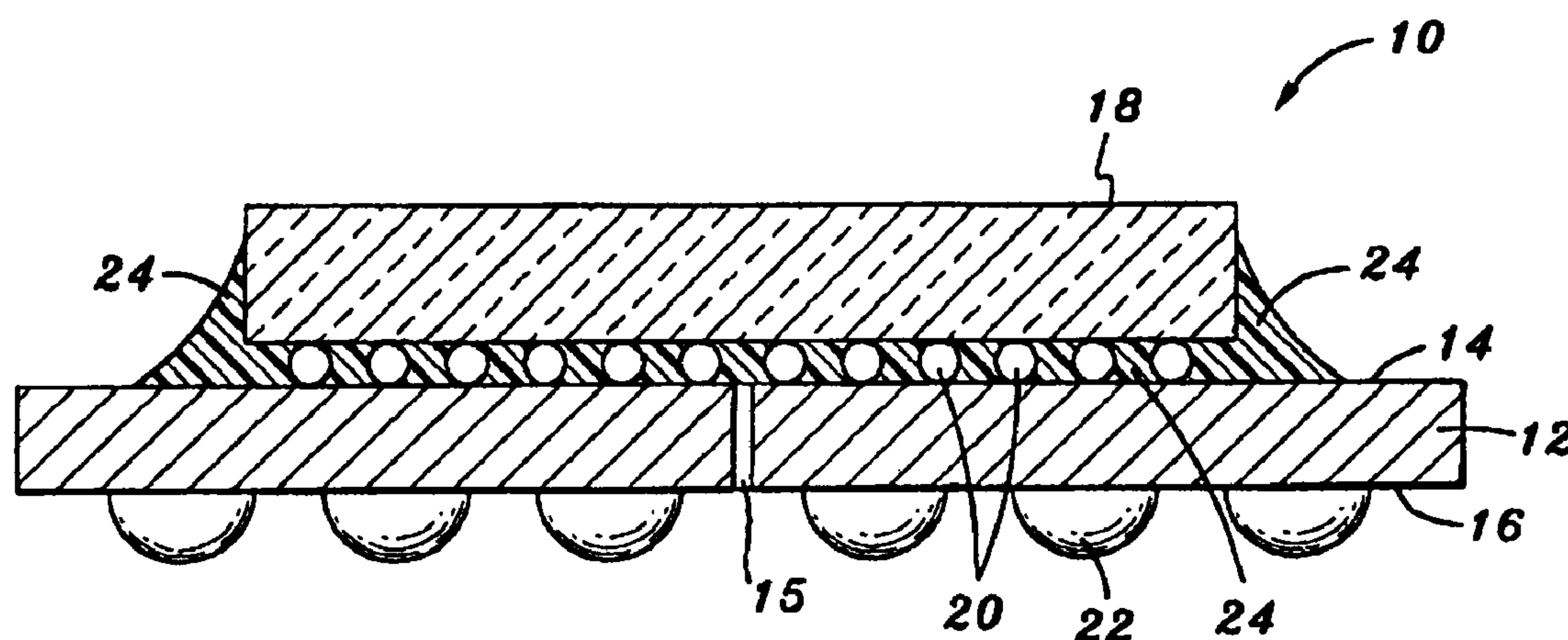
(58) **Field of Classification Search**  
USPC ..... 29/852, 832, 841, 844, 851; 156/281,  
156/327; 257/737, 738, E21.503, 778;  
361/760, 764, 820; 438/63, 64

See application file for complete search history.

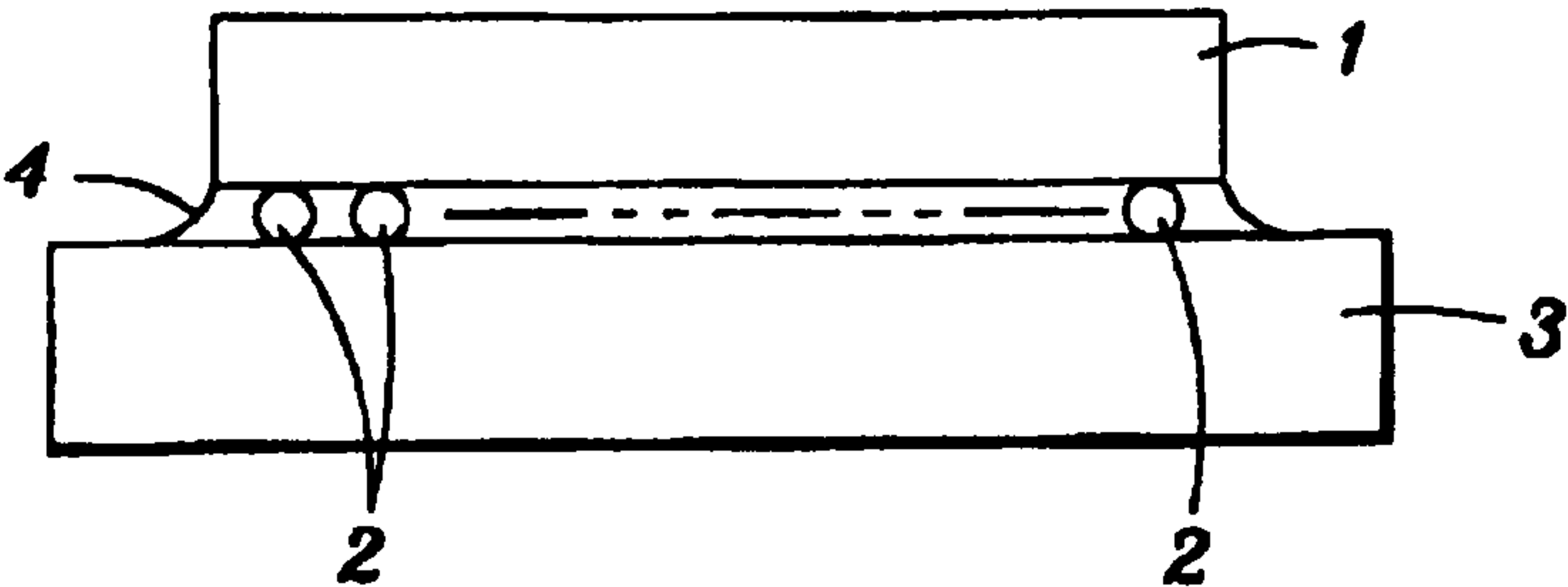
(57) **ABSTRACT**

The present invention involves a method of providing an integrated circuit package having a substrate with a vent opening. The integrated circuit package includes a substrate having an opening and an integrated circuit mounted to the substrate. An underfill material is dispensed between the substrate and the integrated circuit.

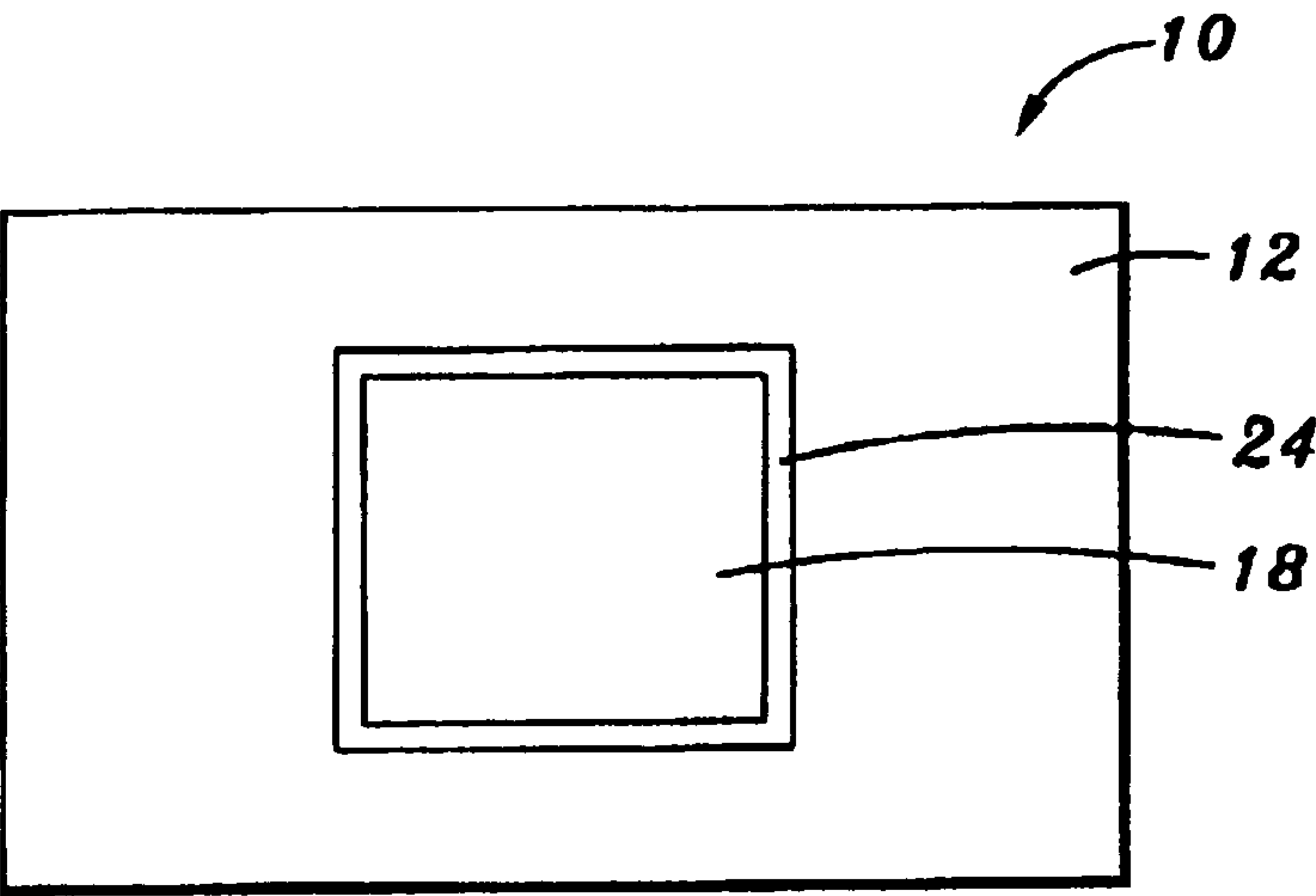
**16 Claims, 3 Drawing Sheets**



**FIG. 1**  
(PRIOR ART)



**FIG. 2A**



**FIG. 2B**

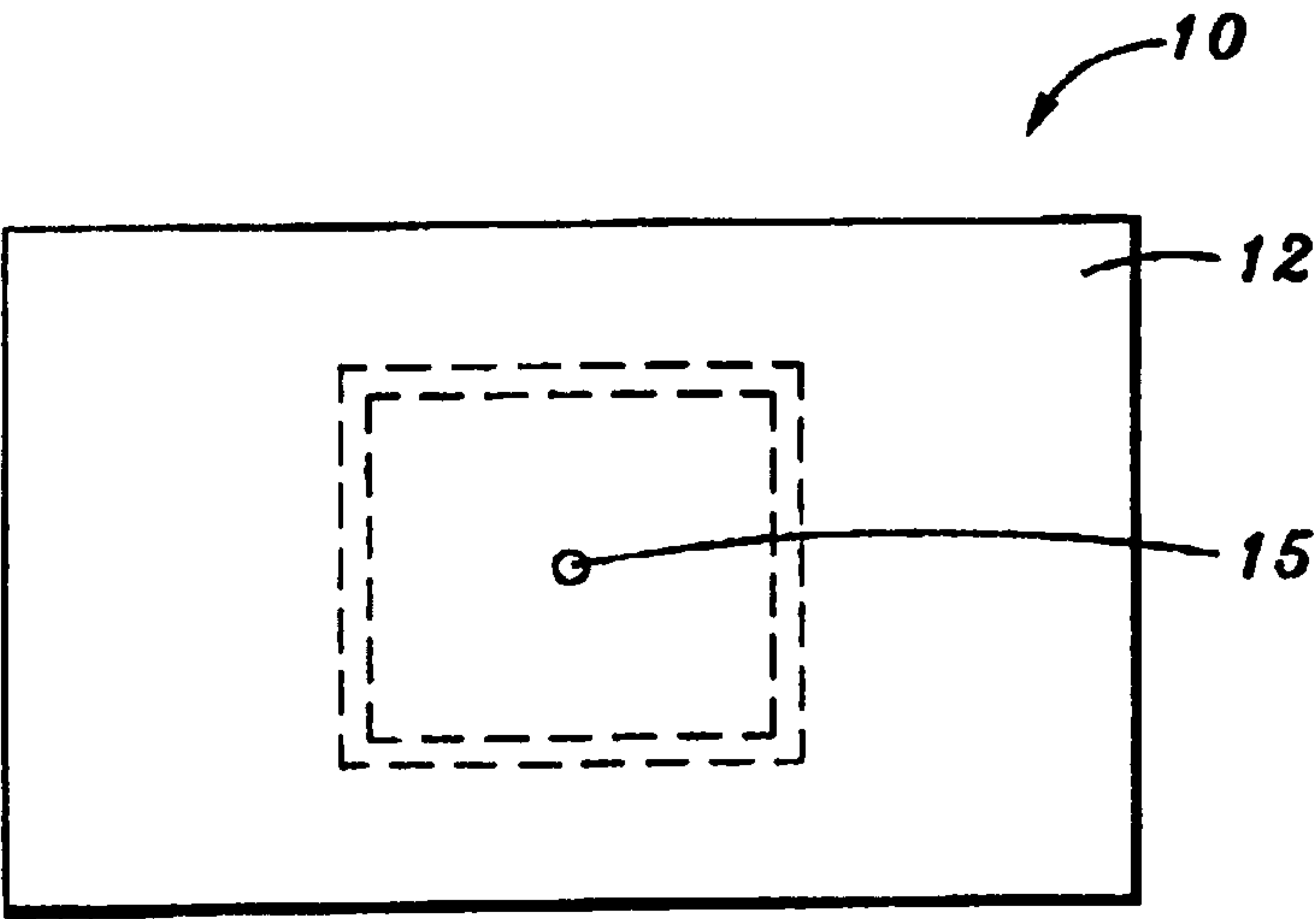


FIG. 3

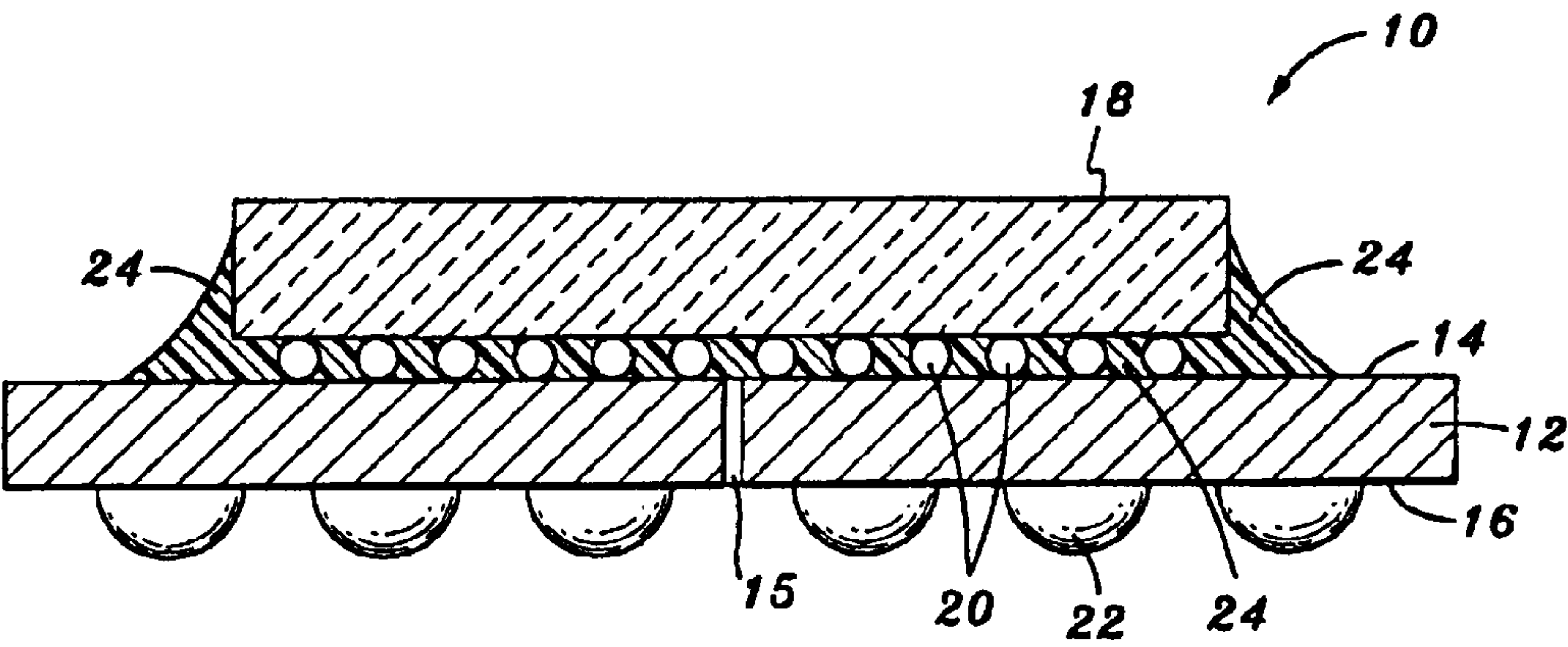


FIG. 4A

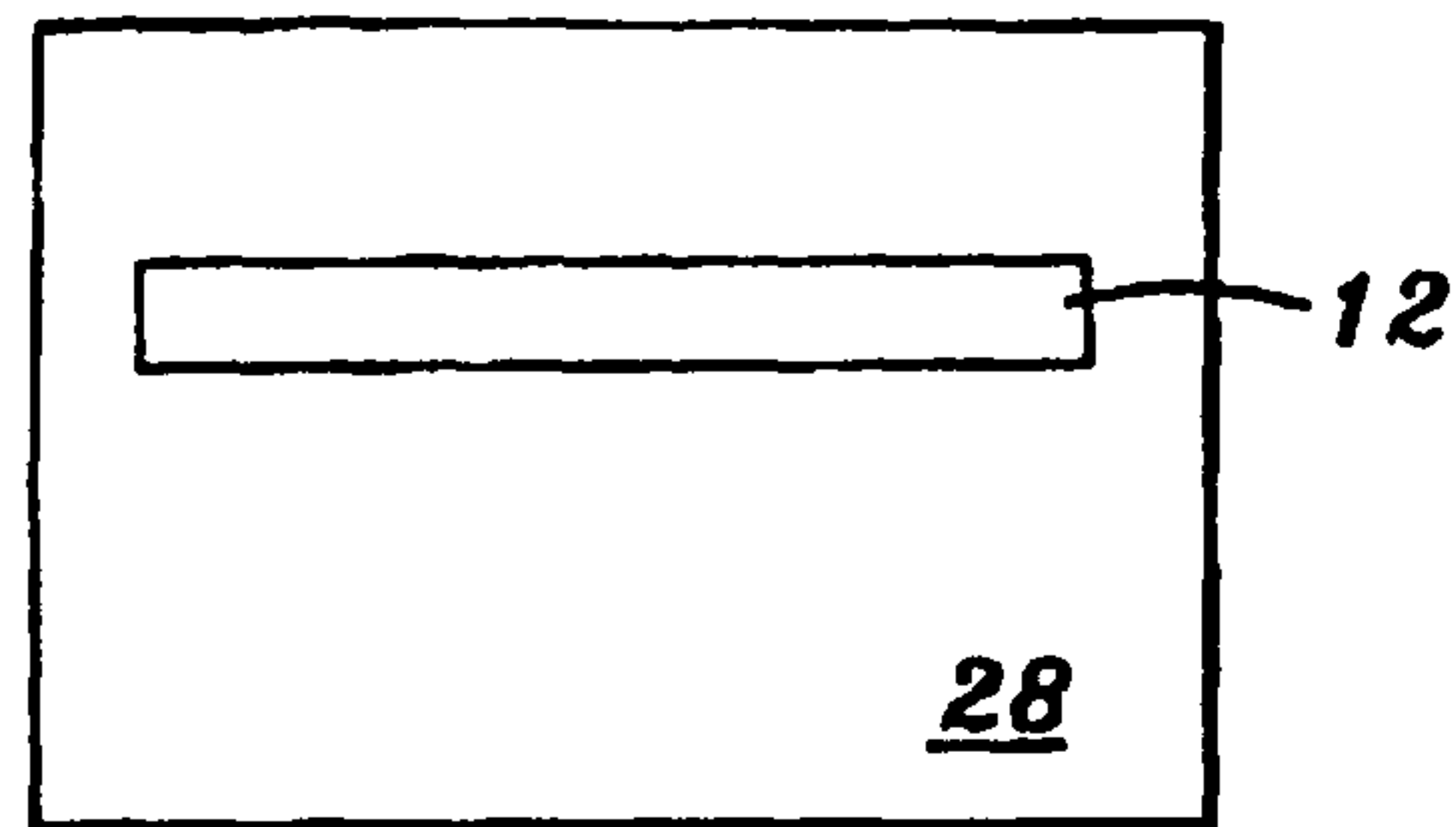


FIG. 4B

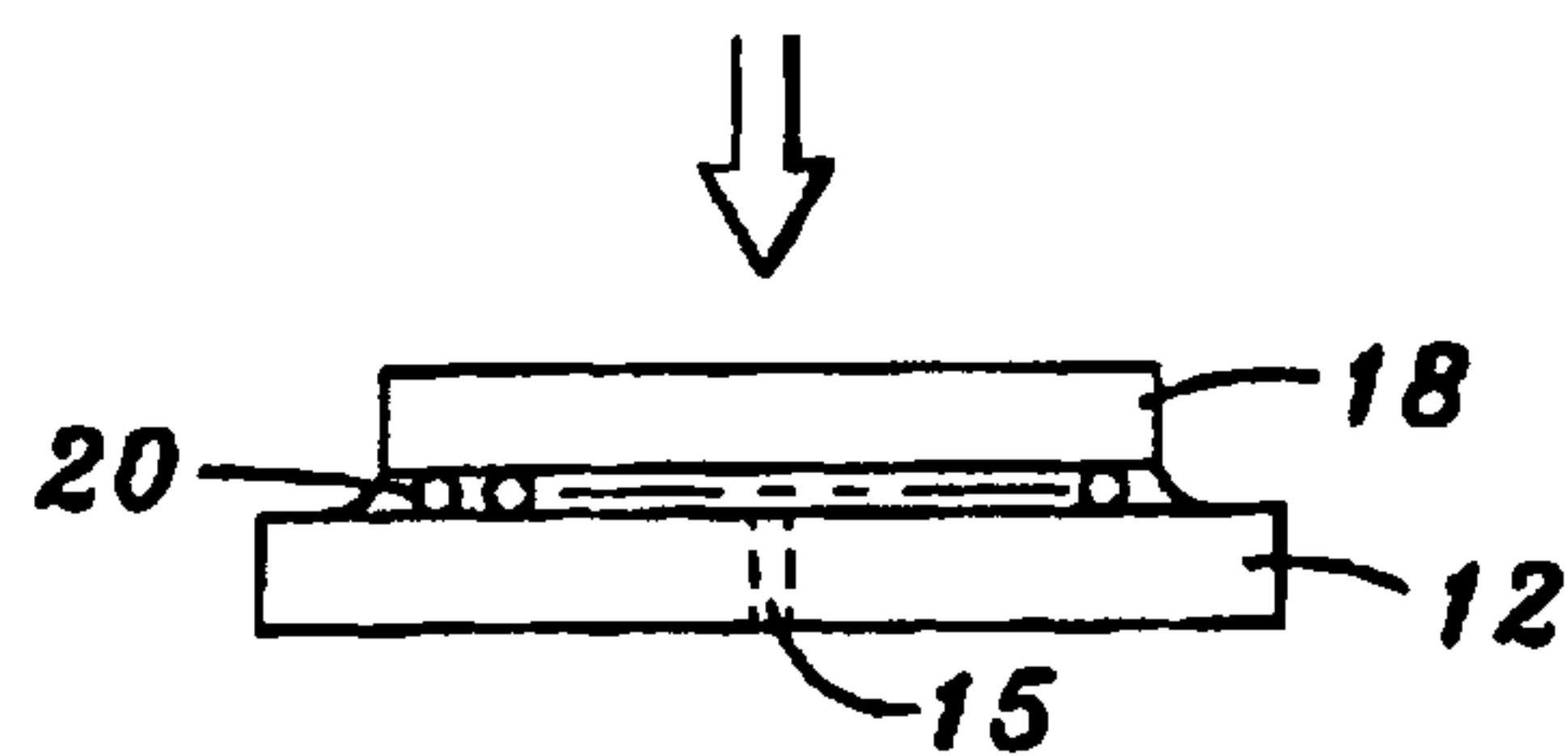
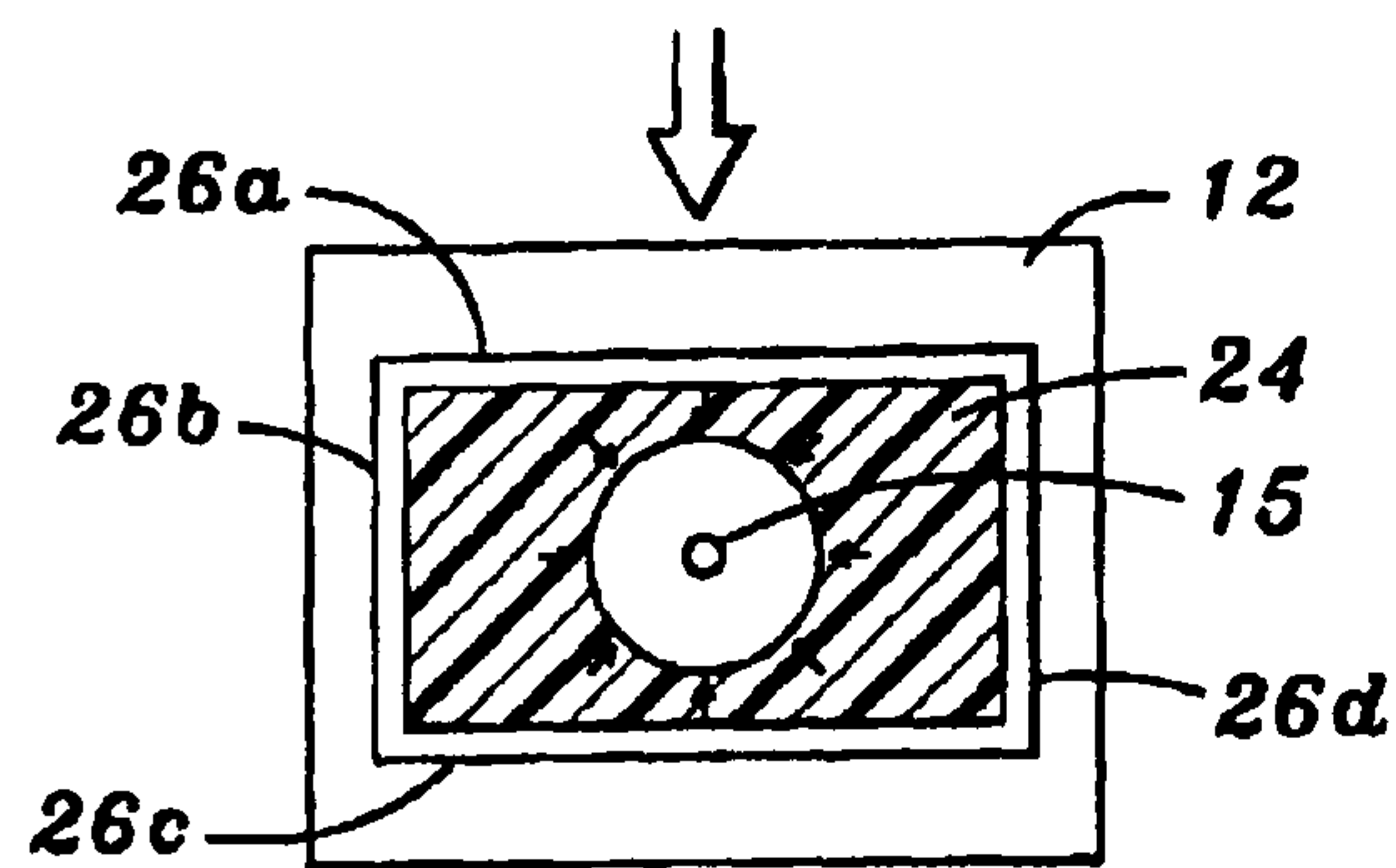
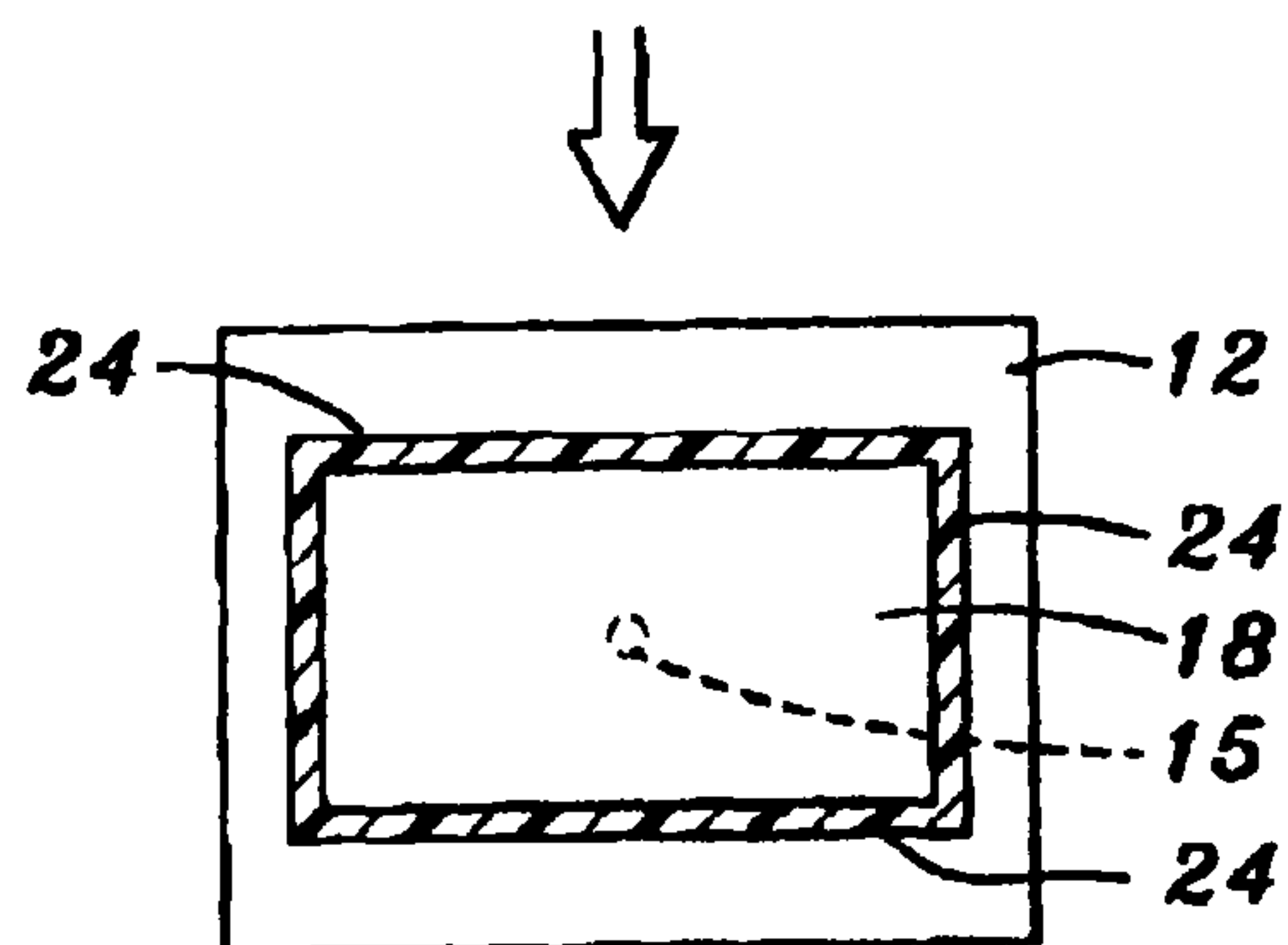


FIG. 4C



STATION  
30

FIG. 4D



STATION  
30



## 1

# PROCESS FOR ASSEMBLING AN INTEGRATED CIRCUIT PACKAGE HAVING A SUBSTRATE VENT HOLE

**Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.**

## CROSS REFERENCE TO RELATED APPLICATION

*This reissue application is a reissue of U.S. Pat. No. 6,490,166 B1 that issued on Dec. 3, 2002 from U.S. patent application Ser. No. 09/330,373 which was filed on Jun. 11, 1999 by Ramalingam et al.*

## BACKGROUND

### 1. Field of the Invention

This invention relates in general to an integrated circuit package, and more particularly, to an integrated circuit package having a substrate vent hole.

### 2. Description of Related Art

Integrated circuits are typically assembled into a package that is soldered to a printed circuit board. FIG. 1 illustrates a type of integrated circuit package that is commonly referred to as flip chip or C4 package. The integrated circuit 1 contains a number of solder bumps 2 that are soldered to a top surface of a substrate 3.

The package may include an underfill material 4 that is located between the integrated circuit 1 and the substrate 3. The underfill material 4 is typically an epoxy which strengthens the solder joint reliability and the thermo-mechanical moisture stability of the IC package.

The package may have hundreds of solder bumps 2 arranged in a two-dimensional array across the bottom of the integrated circuit 1. The epoxy 4 is typically applied to the solder bump interface by dispensing a single line of uncured epoxy material along one side of the integrated circuit. The epoxy then flows between the solder bumps. The epoxy must be dispensed in a manner that covers all of the solder bumps 2.

It is desirable to dispense the epoxy 4 at only one side of the integrated circuit to insure that air voids are not formed in the underfill. Air voids weaken the structural integrity of the integrated circuit/substrate interface. Such air voids are typically formed from trapped air or from gasses released during the underfill cure process. Moisture released during the underfill process may also be absorbed by the substrate, resulting in delamination and other reliability-related failures during the surface mount process. Moreover, the bumps may extrude into the voids during thermal loading, particularly for packages with a relatively high bump density.

Accordingly, there is a need in the technology for an apparatus and method for providing an integrated circuit package that avoids the aforementioned problems.

## SUMMARY

The present invention involves a method of providing an integrated circuit package having a substrate with a vent opening. The integrated circuit package includes a substrate having an opening and an integrated circuit mounted to the substrate. An underfill material is dispensed between the substrate and the integrated circuit.

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## BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the present invention will become apparent from the following detailed description of the present invention in which:

FIG. 1 is a side view of an integrated circuit package of the prior art.

FIG. 2A is a top view of an embodiment of an integrated circuit package of the present invention.

FIG. 2B is a bottom view of the integrated circuit package as shown in FIG. 2A.

FIG. 3 is an enlarged side view of one embodiment of the integrated circuit package of FIGS. 2A and 2B.

FIGS. 4A-D are schematics showing a process for assembling the integrated circuit package of FIGS. 2A and 2B.

## DESCRIPTION

In the following description, for purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that these specific details are not required in order to practice the present invention. In other instances, well-known electrical structures and circuits are shown in block diagram form in order not to obscure the present invention unnecessarily.

FIGS. 2A and 2B are respectively, a top and bottom view of an integrated circuit package of the present invention. FIG. 3 is an enlarged side view of one embodiment of the integrated circuit package of FIGS. 2A and 2B. With reference to FIGS. 2A-2B and 3, the package 10 may include a substrate 12 which has a first surface 14 and a second opposite surface 16. An integrated circuit 18 may be attached to the first surface 14 of the substrate 12 by a plurality of solder bumps 20. The solder bumps 20 may be arranged in a two-dimensional array across the integrated circuit 18 and to the substrate 12 with a process commonly referred to as controlled collapse chip connection (C4).

The solder bumps 20 may carry electrical current between the integrated circuit 18 and the substrate 12. In one embodiment the substrate 12 may include an organic dielectric material. The package 10 may include a plurality of solder balls 22 that are attached to the second surface 16 of the substrate 12. The solder balls 22 can be reflowed to attach the package 10 to a printed circuit board (not shown).

The substrate 12 may contain routing traces, power/ground planes, vias, etc., which electrically connect the solder bumps 20 on the first surface 14 to the solder balls 22 on the second surface 16. The substrate 12 also includes a substrate vent opening 15 that is provided through the substrate at a predetermined location. In one embodiment, the substrate vent opening 15 is located at a low stress area of the substrate. In another embodiment, the substrate vent opening 15 is located at the center of the substrate 12. In a further embodiment, the substrate vent opening 15 is sized to provide efficient outgassing of moisture, while preserving the stability and integrity of the substrate 12. In one embodiment, the substrate opening is selected from a range from 20-62 [mm] micrometers in diameter, although in alternate embodiments, the size of the substrate vent opening 15 may be determined according to need and other design specifications.

The package 10 may include an underfill material 24 that is located between the integrated circuit 18 and the substrate 12. The underfill material 24 may form a circumferential fillet that surrounds and seals the edges of the IC 18. The uniform sealing function of the underfill material 24 may inhibit moisture migration, and cracking of the IC 18. The seal process



may also reduce delamination. The underfill material **24** also reduces stresses on the solder bumps **20**. In one embodiment, the underfill material **24** is an epoxy. The integrated circuit **18** may be encapsulated by an encapsulant (not shown). The encapsulant may be an injection molded material. Additionally, the package **10** may incorporate a thermal element (not shown) such as a heat slug or a heat sink to remove heat generated by the integrated circuit **18**.

FIGS. 4A-D illustrates a process for assembling the package **10**. In one embodiment, the process is a single pass four-sided dispensing process. In particular, the use of a vent hole **15** in implementing the IC package **10** facilitates the use of a single pass four-sided dispensing process.

A substrate vent opening **15** is first drilled or [lazed] *lased* into the substrate **12** at a predetermined location during the substrate manufacturing process. The substrate **12** may then be baked in an oven **28** to remove moisture from the substrate material, as shown in FIG. 4A. The substrate **12** is preferably baked at a temperature greater than the process temperatures of the underfill process steps to insure that moisture is not released from the substrate **12** in the subsequent steps. By way of example, the substrate **12** may be baked at 163 degrees Centigrade (C).

The integrated circuit **18** may then be mounted onto the substrate **12**, as shown in FIG. 4B. The integrated circuit **18** is typically mounted by reflowing the solder bumps **20**.

The underfill material **24** may be dispensed onto the substrate **12** along all four sides **26a-d** of the IC **18** at a dispensing station **30**, as shown in FIGS. 4C and 4D. FIG. 4C illustrates the flow of a typical underfill material **24** when the underfill material **24** is dispensed along all four sides **26a-d** of the IC **18**. FIG. 4D illustrates a top view of the underfilled IC package **10** having a substrate vent hole **15**.

The underfill material **24** may be dispersed in a manner which creates a fillet that encloses and seals the IC **18**. One advantage of using the four-sided dispense pattern is that it is able to form a uniform fillet at all four sides of the IC **18**. A non-uniform fillet can result to cracking of the IC **18**. In addition, the use of a four sided dispense process typically results in a fillet that provides a tight seal, so that delamination between the IC **18** and the underfill material **24** and/or between the underfill material **24** and the substrate **12** does not occur. This in turn results in strong adhesion between the IC **18** and the underfill material **24** and/or between the underfill material **24** and the substrate **12**. The process control for forming this uniform fillet is simple and the process yield is high. By way of example, the underfill material **24** may be dispensed at a temperature of approximately 80°-120° C.

The use of a single pass dispense pattern reduces the underfill material interaction effects of multiple passes. During multiple passes, the underfill material is subjected to heating and gelling before subsequent passes. The use of a single pass dispense process results in a more robust process, reduced processing time and eliminates the need for tight material gelling control.

The underfill material **24** may be cured into a hardened state. The underfill material **24** may be cured at a temperature of approximately 150° C. After the underfill material **24** is cured, solder balls **22** can then be attached to the substrate **12**, typically with a reflow process, to complete the package **10**.

The implementation of the present invention reduces void formation by allowing [out-gassing of] trapped air from the center of the substrate **12** to vent when the underfill material **24** is dispensed at four sides of the IC **18**. In addition, the vent hole **15** allows the underfill material **24** to flow under capillary effect before and during the curing process. As a result, the time control of the underfill material **24** is not as critical as

compared to existing processes in which multiple passes are required. This provides the opportunity for eliminating infrared (IR) and/or convective heating, which are typically required in processes utilizing multiple passes, so as to enhance the underfill material **24** flow for subsequent dispense passes.

The use of a substrate vent hole **15** also shortens the flow travel distance to half, since a four sided dispense process may be used, as described above. This in turn reduces the time needed for providing a full underfill and thus provides the opportunity for eliminating a flow enhancement heating process, such as the IR and BTU heating processes, after underfill dispensing. The use of a vent hole **15** reduces the characterization work needed for underfill process development, which in turn reduces the intense handling and timing interaction associated with the equipment and process. As a result, operational costs are reduced, while manufacturing yields are increased.

While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as other embodiments of the invention, which are apparent to persons skilled in the art to which the invention pertains are deemed to lie within the spirit and scope of the invention.

What is claimed is:

1. A process for assembling an integrated circuit, comprising:

providing [an] a single opening through a substrate having a first surface having a portion upon which the integrated circuit is mounted and a second surface, said single opening being non-occluded at the second surface and having a diameter ranging from about 20 micrometers to about 62 micrometers;

attaching an integrated circuit to said substrate, said integrated circuit having four sides;

out-gassing through [the] said opening while dispensing an underfill material [at at least one side of the] along said four sides of said integrated circuit, [the] said underfill material completely filling a space between said integrated circuit and said substrate, said dispensing comprising a single pass dispensing pattern.

2. The process of claim 1, wherein the act of providing comprises:

drilling said opening through said substrate, a first end of said opening having a diameter substantially equal to a diameter of a second end of said opening.

3. The process of claim 1, wherein the act of providing comprises [lazing] *lasing* said opening through said substrate, a first end of said opening having a diameter substantially equal to a diameter of a second end of said opening.

4. The process of claim 1, wherein the act of providing comprises providing said opening [of] at a predetermined location of said substrate.

5. The process of claim 1, wherein [in] the act of providing comprises providing said opening at a low-stress location of said substrate.

6. The process of claim 1, wherein the act of providing comprises providing said opening at a center of said substrate.

7. The process of claim 1, further comprising attaching a solder ball to said substrate.

8. A process for underfilling an integrated circuit, comprising:

providing a substrate having a single vent opening, said single vent opening having a diameter ranging from about 20 [mm] micrometers to about 62 [mm] micrometers with a first end of said single vent opening at a top



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*surface of said substrate being substantially equal in diameter to a second end of said single vent opening at a bottom surface of said substrate and said second end of said single vent opening being non-occluded;*

mounting said integrated circuit to said *top surface of the* 5  
substrate, said integrated circuit having four sides; and  
out-gassing through said single vent opening while dispensing an underfill material along said four sides of said integrated circuit, said underfill material being attached to said integrated circuit and said substrate, said underfill material completely filling a space between 10  
said integrated circuit and said substrate[;], and said dispensing comprising a single pass dispensing pattern.

9. The process of claim 8, further comprising:  
curing said underfill material.

10. A process comprising:

providing a single vent opening through a substrate, said single vent opening having a diameter ranging from about 20 [mm] micrometers to 62 [mm] micrometers with a top of the single vent opening being substantially uniform in diameter to a bottom of the single vent opening and said single vent opening being non-occluded at the bottom of the single vent opening;

attaching [and] an integrated circuit to said substrate above the top of the single vent opening, said integrated circuit having four sides; and

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out-gassing through said single vent opening while dispensing an underfill material along said four sides of said integrated circuit, said underfill material completely filling a space between said integrated circuit and said substrate, and said dispensing comprising a single pass dispensing pattern.

11. The process of claim 10, wherein the act of providing comprises drilling said opening through said substrate, *the bottom of the single vent opening is non-occluded.*

12. The process of claim 10, wherein the act of providing comprises [lazing] *lasing* said opening through said substrate.

13. The process of claim 10, wherein the act of providing comprises providing said opening at a low-stress location of said substrate. 15

14. The process of claim 10, wherein the act of providing comprises providing said opening at a center of said substrate.

15. The process of claim 10, further comprising attaching a solder ball to said substrate. 20

16. The process of claim 10, wherein said substrate has a first surface and a second opposite surface, said opening extending from the first surface to the second opposite surface.

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