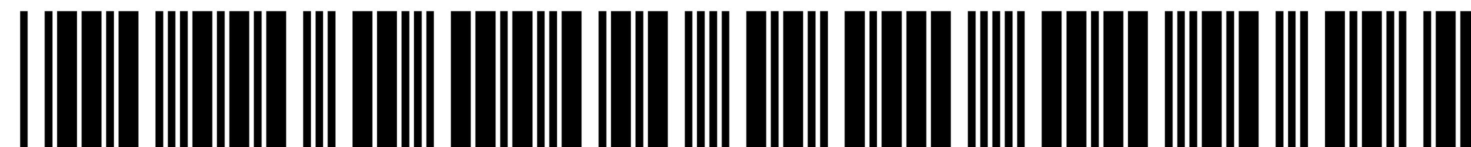

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(54) **PASSIVATION LAYER FOR A CIRCUIT DEVICE AND METHOD OF MANUFACTURE**

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(22) Filed: **Aug. 2, 2012**

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H01L 21/31 (2006.01)
H01L 23/58 (2006.01)
H01L 21/76 (2006.01)

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USPC **438/758**; 438/703; 438/761; 438/778; 257/635; 257/632; 257/638; 257/640; 257/E21.54

(58) **Field of Classification Search**
USPC 438/758, 703, 761, 778; 257/635, 257/632, 638, 640, E21.54
See application file for complete search history.

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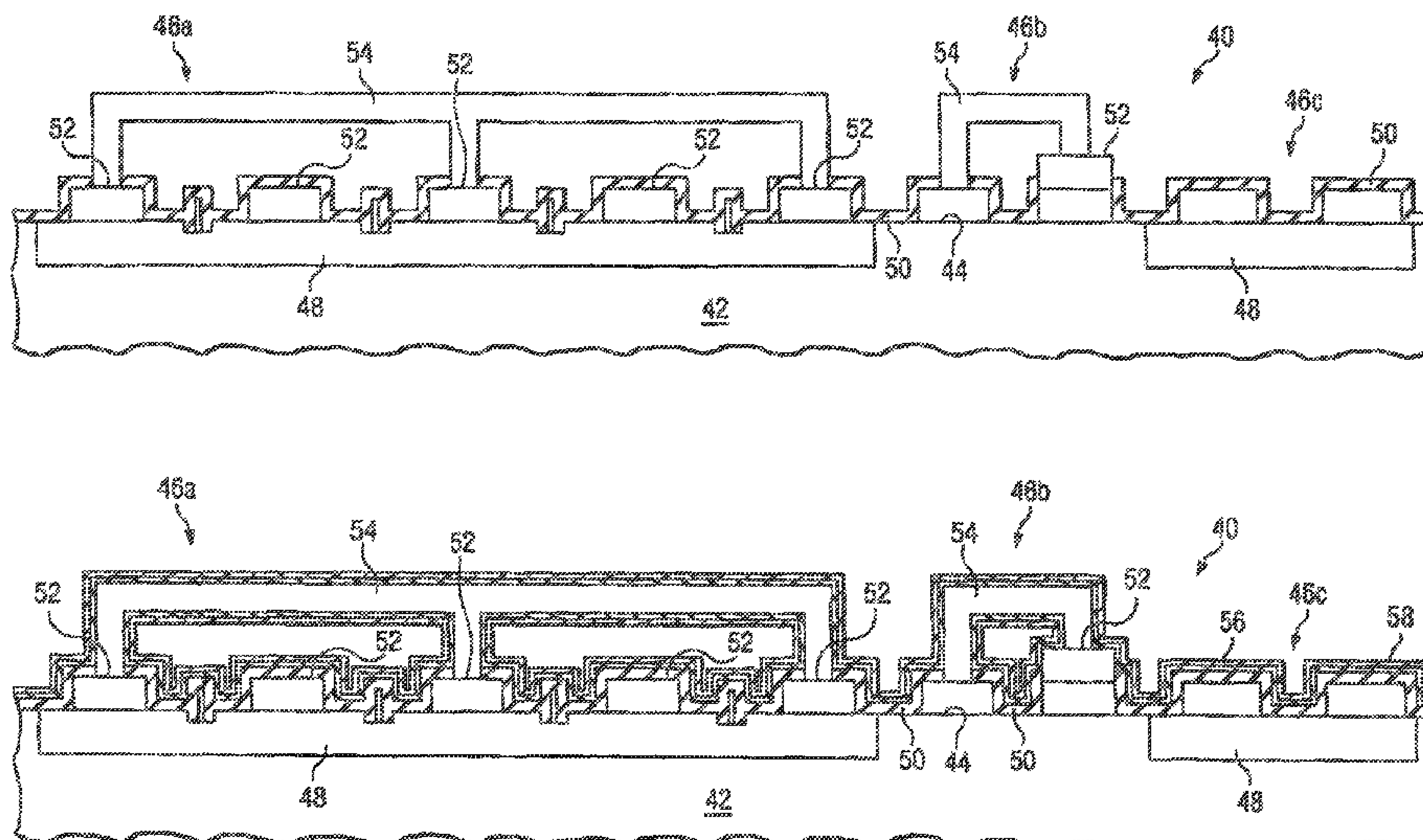
(57) **ABSTRACT**

According to one embodiment of the disclosure, a method for passivating a circuit device generally includes providing a substrate having a substrate surface, forming an electrical component on the substrate surface, and coating the substrate surface and the electrical component with a first protective dielectric layer. The first protective dielectric layer is made of a generally moisture insoluble material having a moisture permeability less than 0.01 gram/meter^2/day, a moisture absorption less than 0.04 percent, a dielectric constant less than 10, a dielectric loss less than 0.005, a breakdown voltage strength greater than 8 million volts/centimeter, a sheet resistivity greater than 10^{15} ohm-centimeter, and a defect density less than 0.5/centimeter^2.

3 Claims, 9 Drawing Sheets



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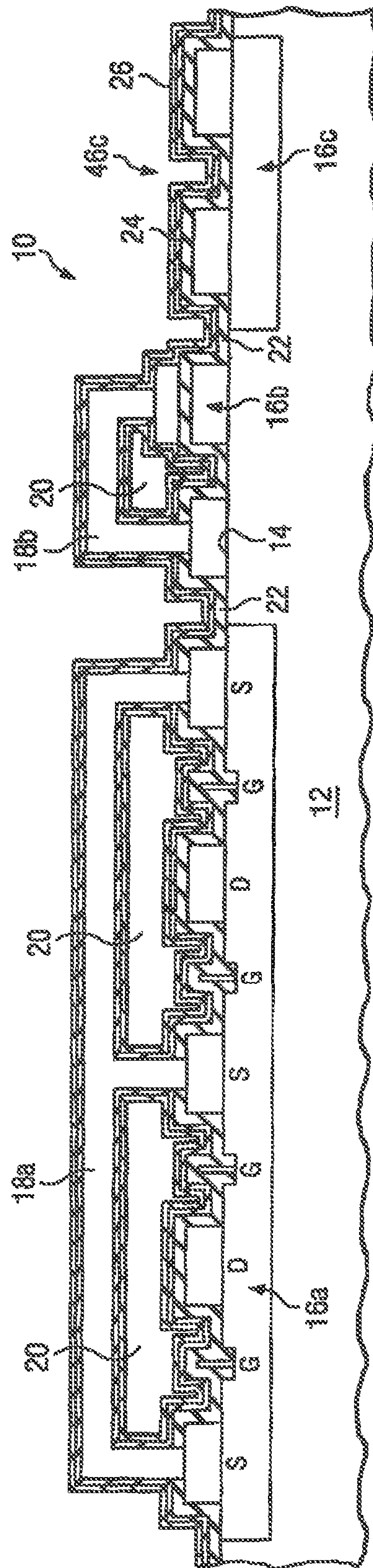

FIG. 1

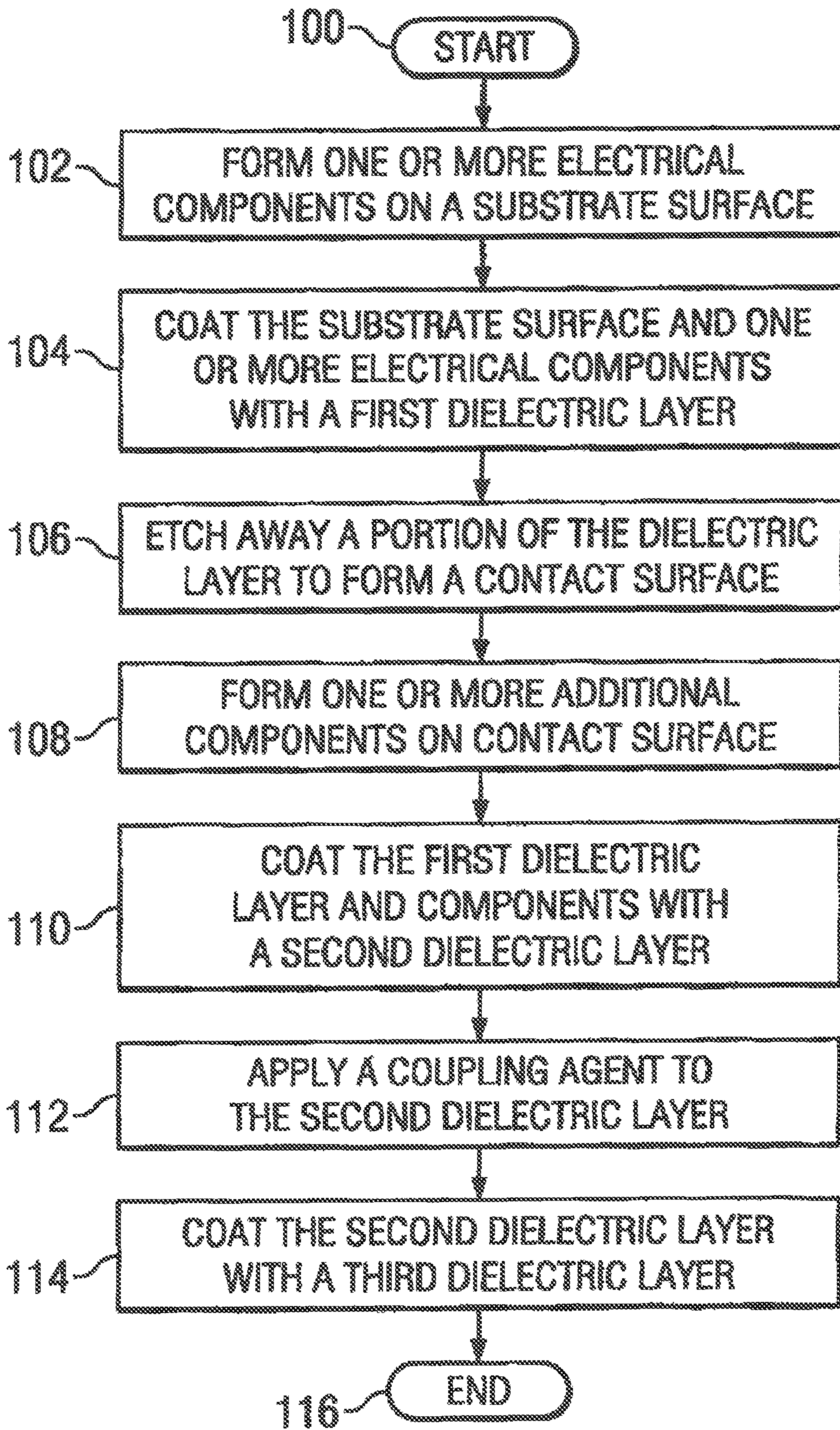

FIG. 2

WAFER LEVEL COATING PROCESS				
EMBODIMENT	FIGURE 1 REFERENCE	ALUMINA THICKNESS ANGSTROMS	SILICA THICKNESS ANGSTROMS	PARYLENE HT THICKNESS ANGSTROMS
EMBODIMENT 1				
DIELECTRIC LAYER 1	22	50-2000	0	0
DIELECTRIC LAYER 2	24	0	0	0
DIELECTRIC LAYER 3	26	0	0	0
EMBODIMENT 2				
DIELECTRIC LAYER 1	22	50-2000	0	0
DIELECTRIC LAYER 2	24	50-2000	0	0
DIELECTRIC LAYER 3	26	0	0	0
EMBODIMENT 3				
DIELECTRIC LAYER 1	22	50-2000	0	0
DIELECTRIC LAYER 2	24	50-2000	0	0
DIELECTRIC LAYER 3	26	0	50-1000	0
EMBODIMENT 4				
DIELECTRIC LAYER 1	22	50-2000	0	0
DIELECTRIC LAYER 2	24	50-2000	0	0
DIELECTRIC LAYER 3	26	0	0	200-500
EMBODIMENT 5				
DIELECTRIC LAYER 1	22	50-2000	0	0
DIELECTRIC LAYER 2	24		0	50-2000
DIELECTRIC LAYER 3	26	0	0	0

FIG. 3

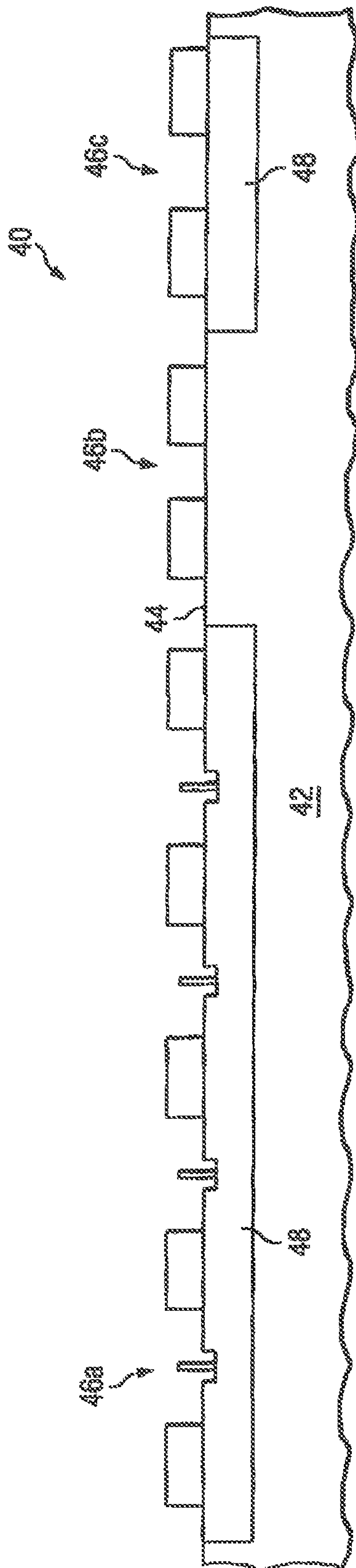

FIG. 4A

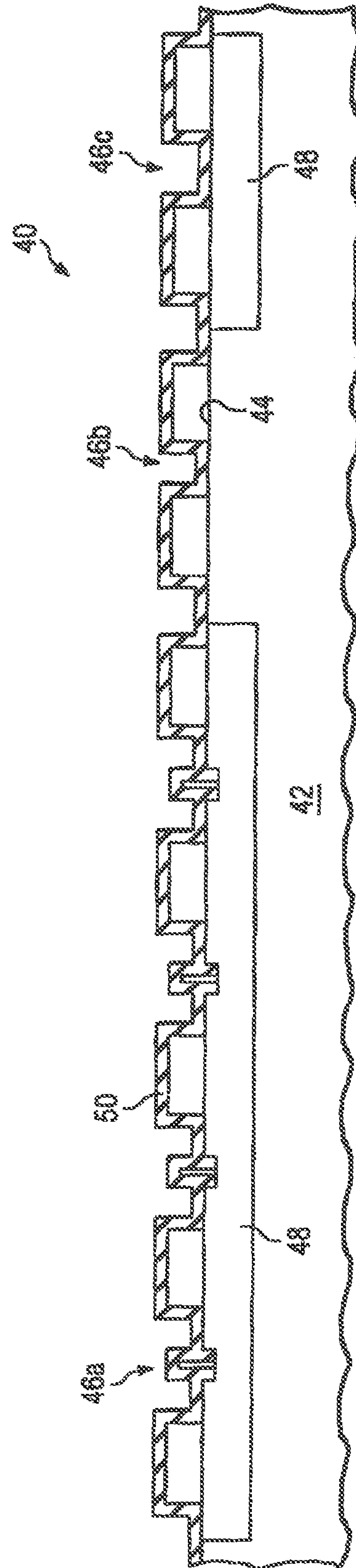

FIG. 4B

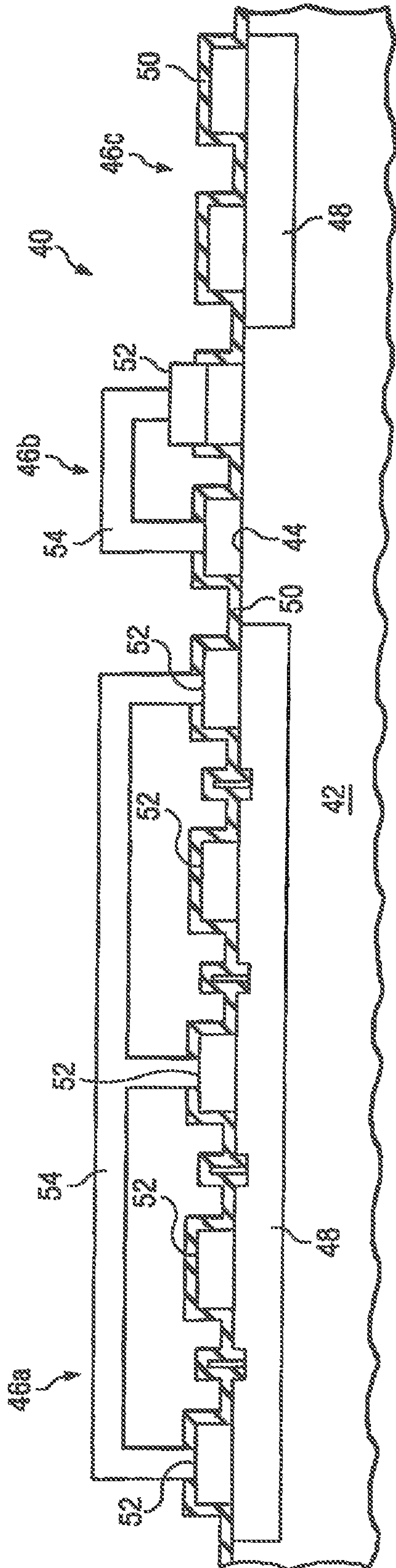

FIG. 4C

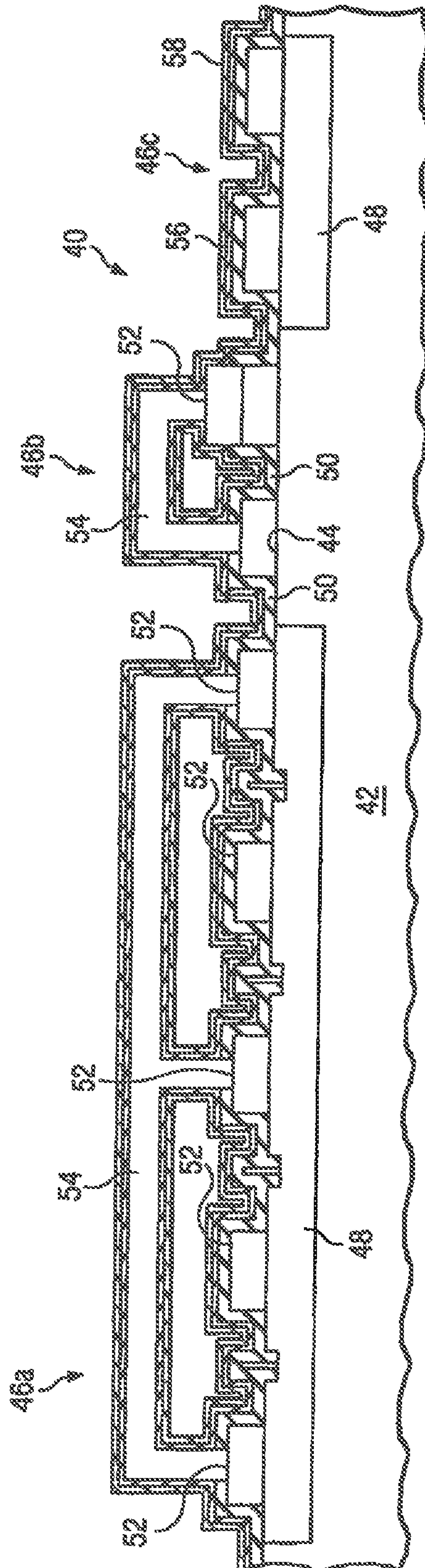

FIG. 4D

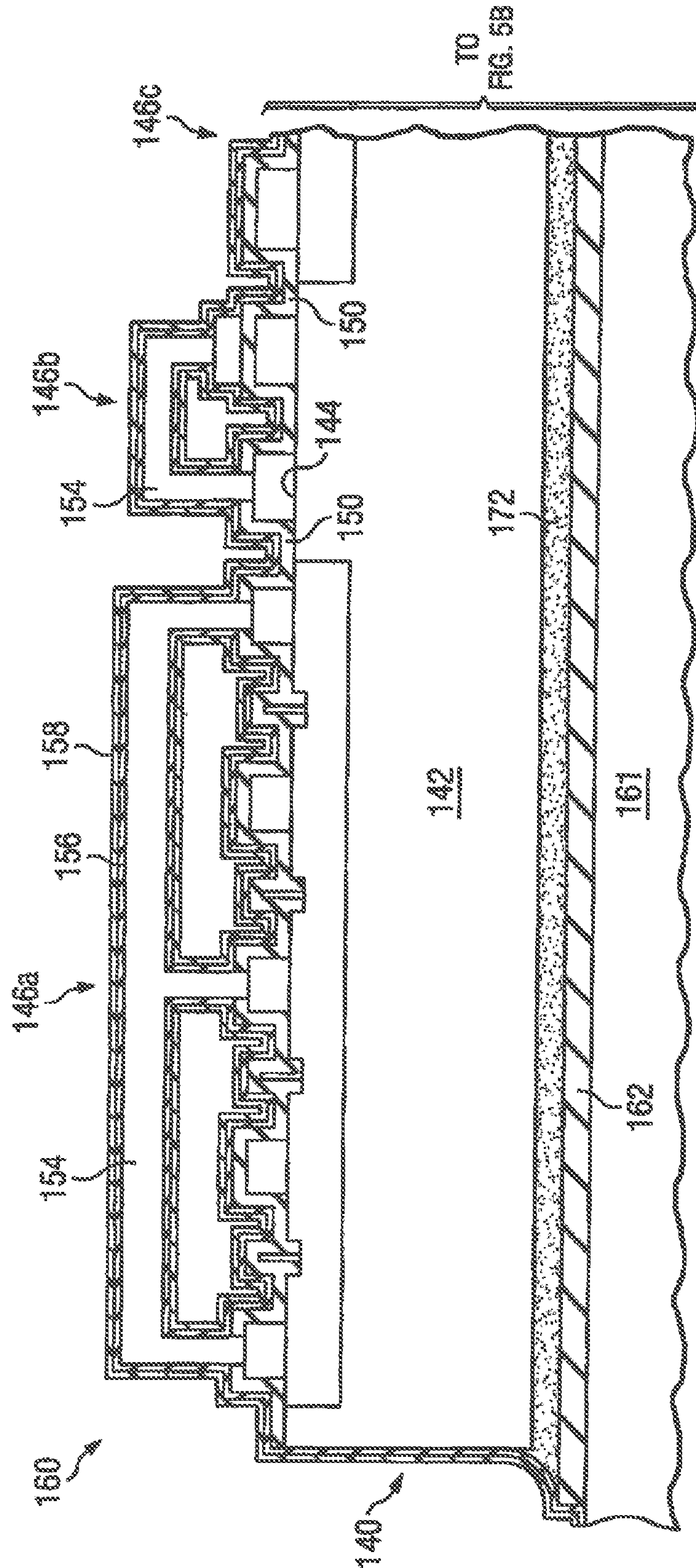

FIG. 5A

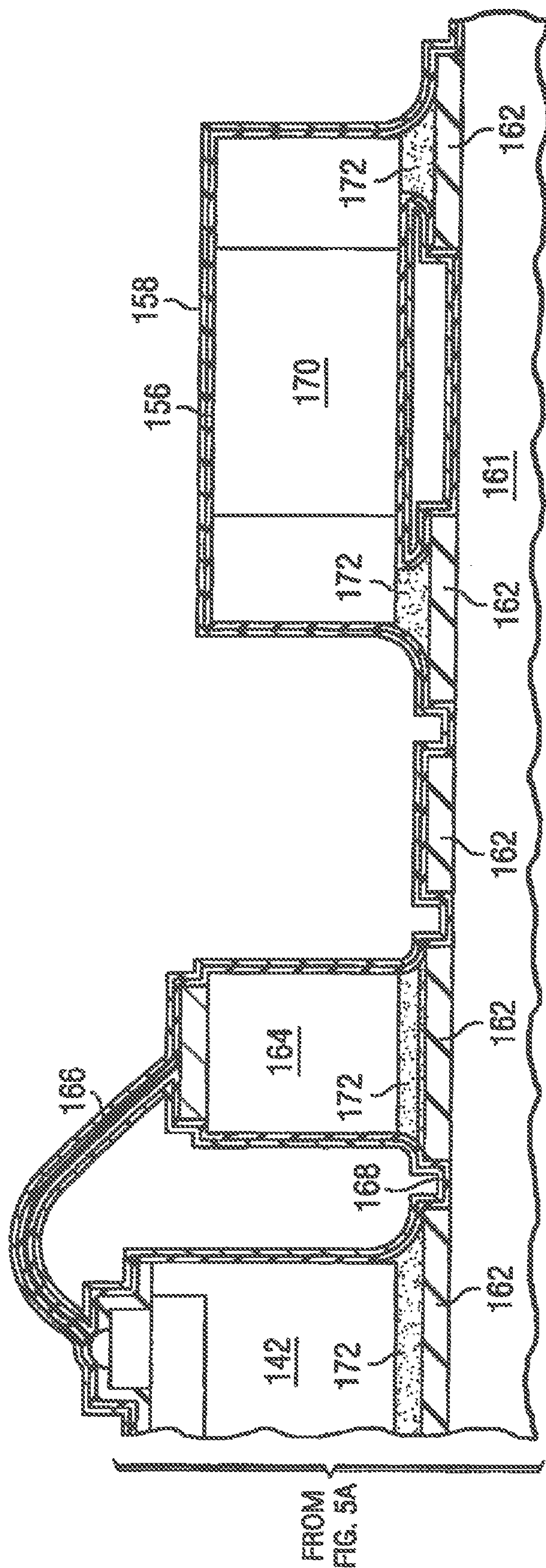

FIG. 5B

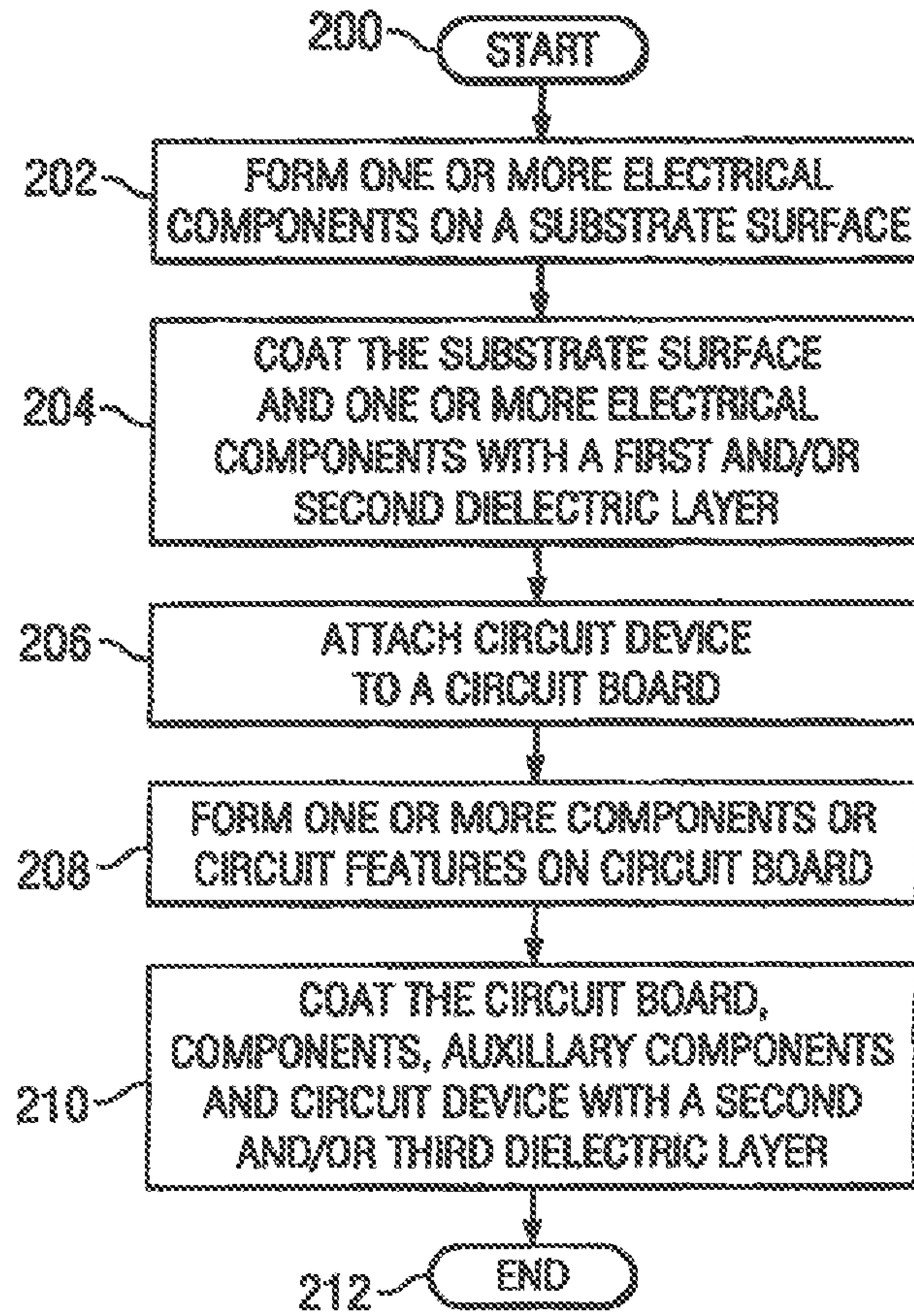

FIG. 6

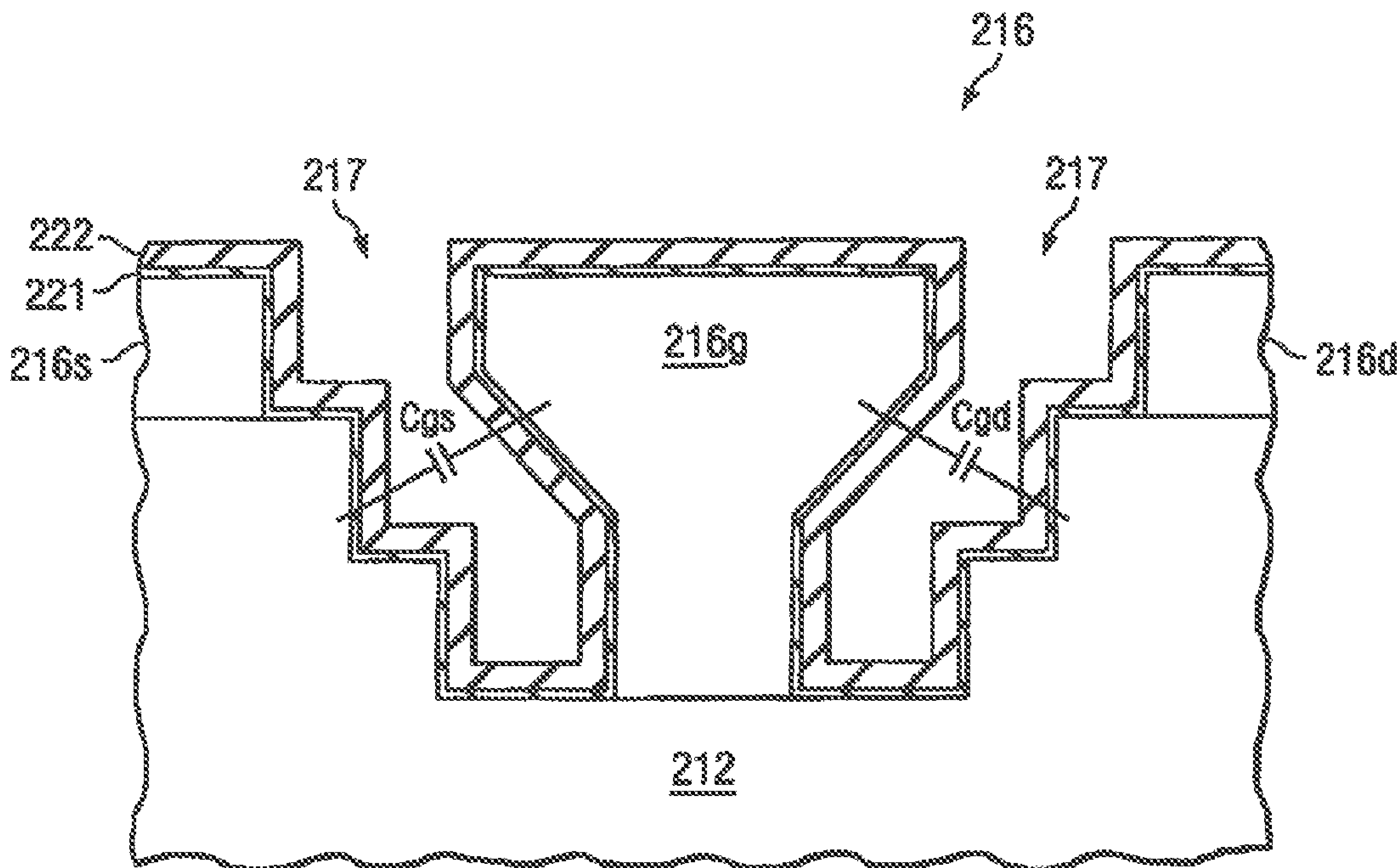

FIG. 8

FIG. 7

COMBINED WAFER AND ASSEMBLY LEVEL COATING PROCESS							
		WAFER LEVEL COATING			ASSEMBLY LEVEL COATING		
EMBODIMENT	FIG 1 REF	ALUMINA THICKNESS ANGSTROMS	SILICA THICKNESS ANGSTROMS	FLUORINATED PARYLENE ANGSTROMS	ALUMINA THICKNESS ANGSTROMS	SILICA THICKNESS ANGSTROMS	FLUORINATED PARYLENE ANGSTROMS
EMBODIMENT 1a							
DIELECTRIC LAYER 1	150	50-2000	0	0	0	0	0
DIELECTRIC LAYER 2	158		0	0	50-2000	0	0
DIELECTRIC LAYER 3	158	0	0	0	0	0	0
EMBODIMENT 1b							
DIELECTRIC LAYER 1	150	50-2000	0	0	0	0	0
DIELECTRIC LAYER 2	156		0	0	0	0	50-2000
DIELECTRIC LAYER 3	158	0	0	0	0	0	0
EMBODIMENT 1c							
DIELECTRIC LAYER 1	150	50-2000	0	0	0	0	0
DIELECTRIC LAYER 2	158		0	0	0	50-2000	
DIELECTRIC LAYER 3	158	0	0	0	0	0	0
EMBODIMENT 1d							
DIELECTRIC LAYER 1	150	50-2000	0	0	0	0	0
DIELECTRIC LAYER 2	156	0	0	0	50-2000	0	0
DIELECTRIC LAYER 3	158	0	0	0	0	0	50-2000
EMBODIMENT 1e							
DIELECTRIC LAYER 1	150	50-2000	0	0	0		0
DIELECTRIC LAYER 2	156		0	0	50-2000	0	0
DIELECTRIC LAYER 3	158	0	0	0	0	50-2000	0
EMBODIMENT 2a							
DIELECTRIC LAYER 1	150	50-2000		0		0	0
DIELECTRIC LAYER 2	156	50-2000	0	0	0	0	0
DIELECTRIC LAYER 3	158	0	0	0			50-2000
EMBODIMENT 2b							
DIELECTRIC LAYER 1	150	50-2000	0	0		0	0
DIELECTRIC LAYER 2	156	50-2000	0	0	0	0	0
DIELECTRIC LAYER 3	158	0	0	0	50-2000	0	
EMBODIMENT 2c							
DIELECTRIC LAYER 1	150	50-2000	0	0		0	0
DIELECTRIC LAYER 2	158	50-2000	0	0	0	0	0
DIELECTRIC LAYER 3	158	0	0	0	0	50-2000	

PASSIVATION LAYER FOR A CIRCUIT DEVICE AND METHOD OF MANUFACTURE

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

RELATED APPLICATIONS

This application claims priority under 35 U.S.C. 119(e) of U.S. Provisional Application Ser. No. 60/888,720, entitled "PASSIVATION LAYER FOR A CIRCUIT DEVICE AND METHOD OF MANUFACTURE," filed Feb. 7, 2007.

TECHNICAL FIELD OF THE DISCLOSURE

This disclosure relates generally to circuit devices, circuit boards, and more particularly, to a passivation system for a circuit device and/or circuit board and method of manufacturing the same.

BACKGROUND OF THE DISCLOSURE

Circuit devices having electrical components that are integrally formed on a substrate have enjoyed wide acceptance due to the wide variety of uses they may provide. Uses for these circuit devices may include applications where operation in a protected environment is not readily available, is costly and/or limits system performance. For such applications, passivation techniques may be employed such that the electrical performance of the components are improved and the components of the circuit device may be protected against harmful contaminants such as moisture, humidity, particulates, or ionic impurities, such as those produced from sodium or chlorine based gases, elements or compounds. Such techniques enable the elimination of costly hermetic enclosures or packages and allow circuit functions to be packaged in closer proximity, thus enabling higher packaging densities, lower weights and higher frequency performance.

SUMMARY OF THE DISCLOSURE

According to one embodiment of the disclosure, a method for passivating a circuit device generally includes providing a substrate having a substrate surface, forming an electrical component on the substrate surface, and coating the substrate surface and the electrical component with a first protective dielectric layer. The first protective dielectric layer is made of a generally moisture insoluble material having a moisture permeability less than 0.01 gram/meter^2/day, a moisture absorption less than 0.04 percent, a dielectric constant less than 10, a dielectric loss less than 0.005, a breakdown voltage strength greater than 8 million volts/centimeter, and a sheet resistivity greater than 10^{15} ohm-centimeter.

According to another embodiment of the disclosure, a circuit device generally includes a substrate and a first protective dielectric layer. The substrate has a substrate surface on which at least one electrical circuit component is formed. The first protective dielectric layer is made of a generally moisture insoluble material having a moisture permeability less than 0.01 gram/meter^2/day, a moisture absorption less than 0.04 percent, a dielectric constant less than 10, a dielectric loss less than 0.005, a breakdown voltage strength greater than 8 million volts/centimeter, and a sheet resistivity greater than 10^{15} ohm-centimeter.

Embodiments of the disclosure may provide numerous technical advantages. Some, none, or all embodiments may benefit from the below described advantages. According to one embodiment, a system and method are provided for passivation of a circuit device having electrical components or other additional components that are formed on the substrate during differing processing steps. The proposed technique for dielectric application results, in some embodiments, in relatively precise control of absolute thickness and thickness uniformity across the substrate or wafer as well as superior conformality over three dimensional features. The precise control of thickness results in both superior electrical performance and superior moisture and contaminant protection. Use of the proposed technique eliminates the need for conventional hermetic packaging techniques and enclosures and also improves performance and reliability for both hermetic and non-hermetic applications.

Other technical advantages will be apparent to one of skill in the art.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of embodiments of the disclosure will be apparent from the detailed description taken in conjunction with the accompanying drawings in which:

FIG. **1** is an side elevational view of one embodiment of an integrated circuit device incorporating a passivation system according to the teachings of the present disclosure;

FIG. **2** is a flowchart showing several acts that may be performed in order to manufacture the embodiment of FIG. **1**;

FIG. **3** is a tabular summary of various wafer level embodiments of the present disclosure;

FIGS. **4**A through **4**D are side elevational views shown during various phases of manufacture of the circuit device of FIG. **1** that may be manufactured according to the teachings of the disclosure;

FIGS. **5**A and **5**B are cut-away perspective views of one embodiment of a passivation layer system for a circuit assembly of the present disclosure;

FIG. **6** is a flowchart showing several acts that may be performed in order to manufacture the embodiment of FIGS. **5**A and **5**B;

FIG. **7** is a tabular summary of certain assembly level embodiments of the present disclosure; and

FIG. **8** is an enlarged, partial view of a transistor having a passivation system according to another embodiment of the invention.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS OF THE DISCLOSURE

Referring to the drawings, FIG. **1** shows one embodiment of a circuit device **10** constructed according to the teachings of the present disclosure. Circuit device **10** generally includes a substrate **12** having a substrate surface **14** on which several electrical components **16** are integrally formed. Substrate **12** of FIG. **1** may be formed from any semi-conductor material suitable for the manufacture of circuit devices **10**, which may be, for example, silicon (Si), gallium-arsenide (GaAs), Gallium-Nitride (GaN), germanium (Ge), silicon-carbide (SiC), or indium-phosphide (InP). Each of these types of materials may be provided in a generally planar-shaped surface **14** on which electrical components **16** may be formed.

Electrical components **16** may include any component that may be formed on substrate surface **14** that may be, for example, transistors, capacitors, resistors, inductors, and the

like. In the particular embodiment shown, electrical components **16** may be several transistors **16**a, a capacitor **16**b, and a resistor **16**c; however, circuit device **10** may include other types of electrical components without departing form the teachings of the disclosure. In one embodiment, transistors **16**a may be a pseudomorphic high electron mobility transistor (pHEMT) device having a source region S, gate region G, and a drain region D, respectively. An air bridge **18**a is illustrated joining the source regions S of each of the transistors **16**a. Another air bridge **18**b is provided for electrical connection of capacitor **16**b. Air bridges **18**a and **18**b may be referred to herein as additional components **18**. Additional components **18** may refer to any suitable component that overlies components **16** for various purposes, such as but not limited to, electrical connection of components **16**, heat conduction, and/or structural reinforcement.

Overlying the substrate surface **14** and electrical components **16**, is a first protective dielectric layer **22**, a second protective dielectric layer **24**, and a third dielectric layer **26**. As described in greater detail below, the first protective dielectric layer **22**, second protective dielectric layer **24**, and third dielectric layer **26** are operable to passivate the substrate **12** and components **16** and **18** from various harmful charge traps and contaminants such as moisture, humidity, particulates, corrosive materials, and ionic impurities, such as sodium, potassium, or chlorine.

Known implementations of circuit devices have provided for passivation of electrical components from harmful contaminants using a dielectric layer that is disposed directly on the electrical components and substrate surface. This dielectric layer may have been formed from insulating materials, such as silicon-nitride (Si_3N_4) or silicon-dioxide (SiO_2). These known dielectric materials suffer, however, in that their ability to prevent moisture degradation is generally less than desirable. Therefore, usage of silicon-nitride material requires application of a relatively thick layer in order to provide adequate protection for the circuit device in an environmentally unprotected or non-hermetic environment. A problem with this approach is that only moderate passivation of the circuit assembly is achieved in spite of the material's relatively large thickness. Additionally, the relatively large thickness may adversely affect the performance of the circuit device due to an increase in the internode capacitance between active regions of the device such as source S, gate G, and drain D regions of transistors. Additionally, the relatively thick layer of silicon-nitride or other conventional dielectric results in high stress which can induce device or dielectric cracking, delamination and/or piezoelectric effects that degrade device performance.

As an alternative to thick silicon-nitride for moisture protection, approaches have been implemented that utilize a second or third passivation layer of a material such as chemical vapor deposition (CVD) of silicon-carbide or atomic layer deposition (ALD) of aluminum-oxide followed by a layer of silicon-dioxide. Use of the additional silicon-carbide or ALD protection layers on top of a first layer of silicon-nitride further increases internode capacitance beyond that associated with the underlying silicon-nitride and thus degrades device performance. Further the silicon-nitride and/or silicon-carbide can still be attacked over time due to their high moisture susceptibility.

It is also known that the first protective dielectric layer, **22**, may provide protection of the gate region from charge traps and contamination that can occur in subsequent processing steps. Hence the first protective dielectric layer **22** is applied immediately before and/or immediately after gate fabrication. Consequently subsequent fabrication steps such as the formation of air bridges **18** and RF and DC conductors or interconnections may leave exposed metal lines which may be susceptible to shorting due to particulates, electrochemical or galvanic corrosion. Approaches proposed to address potential corrosion of such exposed metal lines have included chemical vapor deposition of silicon-nitride or silicon-carbide. One problem associated with the conventional chemical vapor deposition process may be line-of-sight deposition with respect to dielectric coverage. Hence regions beneath air bridges may not be adequately coated and may therefore be susceptible to corrosive attack or to the formation of leakage currents in the presence of moisture. Additionally, a second protective dielectric layer of silicon-nitride and/or silicon-carbide may be susceptible to moisture degradation. Use of an atomic layer deposition coating over the silicon-nitride layer would provide conformality on three dimensional surface features but, as noted previously, would also increase internode capacitance and degrade device performance. Certain embodiments, such as high performance microwave and millimeter wave monolithic microwave integrated circuits (MMICs) may not tolerate significant reduction in radio frequency (RF) performance.

In one embodiment of the present disclosure, dielectric layers **22** and **24** may be provided that implement a moisture impermeable material superior to the moisture protective characteristics of known dielectric materials. In particular embodiments, protective dielectric layers **22** and **24** may be provided that implement a moisture impermeable material with superior voltage breakdown characteristics of known dielectric materials. That is, use of materials having relatively high voltage breakdown characteristics may allow formation of protective dielectric layers **22** and **24** that are thinner than conventionally used to achieve similar voltage breakdown performance. Given these characteristics, a layer of dielectric material that is significantly thinner than known passivation systems may be deposited on the electrical components **16**, additional components **18**, and substrate surface **14** in order to provide passivation from moisture and other contaminants.

In one embodiment, the first protective dielectric layer is made of a generally moisture insoluble material having a moisture permeability less than 0.01 $gram/meter^2/day$, a moisture absorption less than 0.04 percent, a dielectric constant less than 10, a dielectric loss less than 0.005, a breakdown voltage strength greater than 8 million volts/centimeter, and a sheet resistivity greater than 10^{15} ohm-centimeter. In a particular embodiment, first protective dielectric layer **22** may be formed of alumina (Al_2O_3). Alumina may be deposited in a relatively thin layer in a consistent manner. Alumina also possesses relatively high voltage breakdown characteristics. In another embodiment, first protective dielectric layer **22** may be formed of other materials, such as high density silicon-nitride, tantalum-oxide, beryllium-oxide, and hafnium-oxide.

In a particular embodiment, first protective dielectric layer **22** is formed of alumina and has a thickness in the range of 50 to 2000 angstroms. At this thickness range, the first protective dielectric layer **22** may provide adequate protection of the circuit device **10** from moisture without undue effect on the apparent capacitance of electrical components **16**. In one embodiment, the thickness of this layer may be precisely controlled to maintain repeatable performance of many circuit devices **10** that may constructed according to the various embodiments.

The second protective dielectric layer **24** may be operable to passivate additional components **18**. Application of a second protective dielectric layer **24** provides for passivation of additional components **18** that were not passivated by first

protective dielectric layer **22**. In a particular embodiment in which an additional component **18** is an air bridge, application of the first protective dielectric layer **22** prior to formation of the air bridge provides for relatively concise control over the thickness of first protective dielectric layer **22** that may be confined in an air cavity **20** following formation of the air bridge. Additionally, second protective dielectric layer **24** may provide passivation for portions of the first protective dielectric layer **22** that may be inadvertently damaged by additional processing steps, such as, for example, sawing, scribing moats, or providing interconnections to other devices.

The second protective dielectric layer **24** may be made of the same dielectric material, but in some embodiments may be made of dielectric materials described above with respect to the first protective dielectric layer **22**. In other embodiments, the second protective dielectric layer **24** may also be made of any material that is described below with respect to the third dielectric layer **26**. In one embodiment, the second protective dielectric layer **24** may have a thickness in the range of 50 to 2000 angstroms. Other particular embodiments are described in greater detail below with respect to FIG. **3**.

Although alumina may be moisture impermeable, its surface may exhibit chemical attack in the presence of high humidity, low humidity for extended periods and/or condensed moisture. Thus a third dielectric layer **26** may be provided. Third dielectric layer **26** may be formed of any material that is chemically stable in the presence of high humidity, extended humidity, and/or moist condensation and vapor permeation. In one embodiment, third dielectric layer **26** may be formed of silicon-dioxide (SiO_2). In another embodiment, third dielectric layer **26** may be formed of parylene. Parylene C, parylene F (poly-tetrafluoro-p-xylylene), aromatic-fluorinated VT-4, parylene HT® (trademark of Specialty Coating Systems), or other fluorinated parylene-like films, may retard moisture from reaching first **22** and/or second **24** protective dielectric layers and be used for layer **26**. These materials may exhibit superior moisture retarding characteristics and remain functionally stable over a wider temperature range than other types of parylene. These materials may not develop high film stress due to high temperature exposure. These materials may also have a lower dielectric constant than silicon-dioxide. In one embodiment, the third dielectric layer **26** may have a thickness in the range of approximately 100 to 1000 angstroms. Rather than these parylene materials, any material exhibiting the characteristics described below for layers **156** or **158** with respect to FIG. **5** may also be used for third dielectric layer **26**.

Thus, passivation for a circuit device **10** may be provided by first protective dielectric layer **22**, second protective dielectric layer **24**, and an optional third dielectric layer **26**. Each of these layers **22**, **24**, and **26** may be sufficiently thin to not adversely affect the performance characteristics of circuit device **10** while providing adequate protection from gaseous, liquid and solid contaminants including moisture.

FIG. **2** depicts a series of actions that may be performed in order to manufacture one embodiment of a circuit device **10** according to the present disclosure. In act **100**, the method for providing an electrical and environmental protection coating system is initiated. In act **102**, one or more electrical components **16** may be formed on a substrate surface **14** using known integrated circuit manufacturing techniques. In act **104**, a first protective dielectric layer **22** may be deposited on the substrate surface **14** and electrical components **16**. In one embodiment, the thickness of the first protective dielectric layer **22** may have a thickness in the range of 50 to 2000 angstroms. First protective dielectric layer **22** may comprise certain materials as described above.

Acts **106** through **110** may provide one approach for forming one or more additional components **18** on the circuit device **10**. To provide a contact surface for attachment of additional components **18**, selected portions of the first protective dielectric layer **22** may be etched away from the circuit device **10** in act **106**. Next in act **108**, one or more additional components **18** are formed on these contact surfaces. A second protective dielectric layer **24** may then be deposited over the first protective dielectric layer **22** and any additional components **18** that have been formed on the circuit device **10** in act **110**. In one embodiment, the second protective dielectric layer **24** may have a thickness in the range of 50 to 2000 angstroms. Thus, the cumulative thickness of the first **22** and second **24** protective dielectric layers may have a thickness in the range of 100 to 4000 angstroms.

In one embodiment, an adhesion promoter may be applied over the second protective dielectric layer **24** to improve adhesion of the third dielectric layer **26** to the second protective dielectric layer **24** in act **112**. In one embodiment, the adhesion promoter may be a layer of silicon dioxide used independently or in conjunction with gamma-methacryloxypropyltrimethoxysilane; however, other adhesion promoters may be used. Third dielectric layer **26** may then be applied to the second protective dielectric layer **24** in act **114**. In one embodiment, the thickness of the third dielectric layer **26** may be in the range of 100 to 1000 angstroms.

In act **116**, the method for application of a passivation layer has been completed and the circuit device **10** may then be used. Acts **100** through **116** describe one embodiment of a method for manufacture of a circuit device **10** in which the protective dielectric layers **22** and **24** are applied in multiple processing steps. Using this approach, the thickness of first protective dielectric layer **22** adjacent electrical components **16** within air cavity **20** may be easily controlled. By application of first protective dielectric layer **22** prior to forming additional components **18** such as air bridges, the thickness of the first protective dielectric layer **22** proximate electrical components **16** may be easily controlled using a variety of deposition techniques known in industry.

FIG. **3** is a table that summarizes various embodiments **1** through **5** of the present disclosure that may provide enhanced electrical performance and enhanced environmental protection over known passivation systems. Each embodiment **1** through **5** shows various combinations of materials (e.g., alumina, silica, and/or parylene F, aromatic-fluorinated VT-4, parylene HT®, or other fluorinated parylene-like films) that may be used form the first **22**, second **24**, and/or third **26** dielectric layers.

As described above with respect to FIG. **1**, the first protective dielectric layer **22** in embodiments **1** through **5** may be formed of a generally moisture insoluble material having a moisture permeability less than 0.01 gram/meter^2/day, a moisture absorption less than 0.04 percent, a dielectric constant less than 10, a dielectric loss less than 0.005, a breakdown voltage strength greater than 8 million volts/centimeter, a sheet resistivity greater than 10^{15} ohm-centimeter. In one particular embodiment, first protective dielectric layer **22** is formed of alumina, which has a relatively lower moisture permeability, relatively lower ionic mobility, and relatively higher voltage breakdown strength characteristics than other known materials, such as standard silicon-nitride or silicon-dioxide. The first protective dielectric layer **22** may be deposited by a number of deposition techniques, such as physical vapor deposition (PVD), chemical vapor deposition (CVD) and atomic layer deposition. Atomic level deposition may be

used because it may provide relatively precise control of thickness, superior conformality on the substrate surface **14** and components **16** and **18**, and elimination of physical or radiation induced damage during dielectric deposition.

As described above with respect to FIG. **1**, additional layers of dielectric protection can be added depending on the specific device and/or assembly packaging approach. The thickness of the dielectric layers **22**, **24**, and **26** may also be a function of device design, frequency of operation and performance requirements. Embodiments **1** through **5** shown in FIG. **3** may be particularly tailored for radio frequency (RF) integrated circuits that may include components such as field effect transistors (FETs) including pseudomorphic high electron mobility transistor devices (pHEMTs) and bipolar transistors such as heterojunction bipolar transistors (HBTs). In general, a relatively lower dielectric thickness improves device performance associated with dielectric loading effects such as internode capacitance, increases capacitance per unit area of integrated capacitors and thereby decreases capacitor size. A relatively higher dielectric thickness decreases moisture permeability and improves protection against particulates, physically induced damage, ionic impurities, and corrosive contaminants whether in solid, liquid or gaseous form. The thicknesses of dielectric layers **22**, **24**, and **26** shown in FIG. **3** may be tailored for radio frequency (RF) integrated circuits where control of internode capacitance and control of dielectric loading effects are important to circuit performance. Other combinations of materials and thicknesses may be selected according to the teachings of this disclosure.

Embodiment **1** of FIG. **3** utilizes only a first protective dielectric layer **22** made of alumina. Embodiment **1** may provide enhanced electrical performance due to minimal internode capacitance of a single dielectric layer while providing electrical, physical and environmental protection of the source region S, gate region G, and drain region D of transistor **16**a of FIG. **1**. Embodiment **1** may also provide enhanced electrical performance over known materials, such as silicon-nitride or silicon-dioxide in both hermetic and non-hermetic environments. Enhanced performance may be provided since a thinner dielectric than conventional silicon-nitride or silicon-dioxide can be utilized. Embodiment **1** may also be desirable in environments where partial control of temperature and or humidity is provided at the system level such that conditions are provided that minimize or eliminate water condensation on active circuitry and/or minimize or eliminate high temperature and humidity exposure of active circuitry for prolonged periods of time. Such protection may be achieved at the system level by humidification control through dehumidifiers or desiccants.

Embodiment **2** provides first **22** and second **24** protective dielectric layers formed of alumina. The second protective dielectric layer **24** covers unprotected additional components **18** such as air bridges and thick metal lines, which may be formed after the first protective dielectric layer **22** is applied. Embodiment **2** may also be desirable in hermetic or less severe humidity environments where protection against conductive or corrosive solid, liquid or gases materials may be present.

Embodiments **3** and **4** provide a third dielectric layer **26** that may be formed of silica, parylene F, parylene HT®, or other fluorinated parylene-like film as described above. The third dielectric layer **26** formed of silica or parylene F, parylene HT®, or other fluorinated parylene-like film protects the first **22** and/or second **24** protective dielectric layers from high humidity, extended humidity and/or condensed moisture which may break down the first **22** and/or second **24** protective dielectric layers **24** and expose the underlying components **16** and **18**. Parylene F or parylene HT® may have a lower dielectric constant than silica and may therefore have less impact on electrical performance. Parylene F or parylene HT®, like ALD deposited silica, can be vapor deposited and is highly conformal penetrating into the smallest recesses and may be applied with a relative uniform thickness beneath air bridges and other additional components **18** having high aspect ratio recesses. The first **22** and/or second **24** protective dielectric layers made of alumina may also serve as an adhesion promoter since parylene F or parylene HT® may not adhere well to many surfaces even with an adhesion promoter. As described above, an adhesion promoter may be applied to the second protective dielectric layer **24** prior to deposition of the third dielectric layer **26**. The adhesion promoter may be any suitable material that enhances adhesion of the third dielectric layer **26**, and in one particular embodiment is a layer of silicon dioxide used independently or in conjunction with gamma-methacryloxypropyltrimethoxysilane. Silicon dioxide provides an ideal surface for bonding to adhesion promoters such as gamma-methacryloxypropyltrimethoxysilane and bonds well to alumina and to parylene F or parylene HT®.

Embodiment **5** utilizes parylene F or parylene HT® as the second protective dielectric layer **24** of FIG. **1**. Parylene F or parylene HT® covers unprotected additional features, such as air bridges and thick metal lines that may be formed after the first protective dielectric layer **22**. The parylene F or parylene HT® also protects the underlying first protective dielectric layer **22** from being dissolved or attacked by moisture condensation. Parylene F or parylene HT® has the advantage of having a lower dielectric constant compared to silica or other inorganic materials and lower than most organic materials.

FIGS. **4**A through **4**D are cross-sectional drawings shown during various phases of manufacture of a circuit device **40** according to the teachings of the present disclosure. Circuit device **40** is generally analogous to circuit device **10** in FIG. **1**. In FIG. **4**A, a substrate **42** having a substrate surface **44** is shown with gate recess and gate metal applied for a number of transistor fingers **46**a, cap bottom applied for a capacitor **46**b, and a resistor **46**c. Isolation implant has previously been accomplished to form isolated active channel regions **48** for the transistors **46**a and resistor **46**c. As described above in conjunction with FIG. **1**, in one embodiment, transistors **46**a may be pseudomorphic high electron mobility transistors (pHEMTs). The electrical components **46** and associated substrate **42** of FIG. **4**A may be manufactured according to act **100** of FIG. **2**.

FIG. **4**B shows the circuit device **40** of FIG. **4**A in which a first protective dielectric layer **50** has been applied according to act **102**. As can be seen, each electrical component **46** may be exposed to a generally line-of-sight deposition, thus allowing uniform thickness deposition of the first protective dielectric layer **50**. That is, accesses to features of the electrical components are not generally encumbered by additional devices such as air bridges **54**.

FIG. **4**C shows the results of a circuit device **40** on which acts **104** through **108** are performed on the circuit device **40** of FIG. **3**B. Contact surfaces **52** have been created by etching away a portion of the first protective dielectric layer **50** for attachment of additional components **54** such as air bridges. The air bridges may be used to make parallel connection to the source transistor fingers **46**a and thereby increase output power and to make connection to the top plate of the capacitor **46**b.

FIG. **4**D shows the circuit device **40** of FIG. **4**C in which a second protective dielectric layer **56** and third dielectric layer **58** has been applied in order to passivate the substrate surface

44, electrical components **46**, and additional components **54** according to act **110** through act **114**. Thus, a system and method is provided whereby a circuit device **40** having additional components **54** may be effectively sealed from harmful contaminants while not sacrificing performance of the circuit device **40**.

FIGS. **5**A and **5**B show one embodiment of a circuit board assembly **160** that may be passivated according to another embodiment of the teachings of the present disclosure. Circuit board assembly **160** generally includes a circuit device **140** and several discrete electrical components **164** and **170** that are attached to a circuit board **161**. Circuit board assembly **160** may also have several assembly level features including board traces **162** and wire interconnections **166** that provide electrical interconnection between circuit device **140** and electrical components **164** and **170**. Overlying the circuit board assembly **160** is a dielectric layer **156** and a second protective dielectric layer **158**. Circuit device **140** has a dielectric layer **150** that was applied during device fabrication, prior to assembly on the circuit board. As will be described below, passivation may be provided at the assembly level of production for protection of circuit device **140** and electrical components **164** and **170** of the circuit board assembly **160** by applying the second protective dielectric layer **156** and/or the third dielectric layer **158** during the assembly level phase of production.

Circuit board **161** may be any suitable device in which a number of discrete electrical components **164** and **170** may be configured on. Generally, circuit board **161** may be a rigid or flexible substrate in structure for securing discrete electrical components **164** and **170** in a fixed physical relationship relative to one another. In one embodiment, circuit board **161** has a generally planar-shaped outer surface **168** on which the discrete electrical components **164** and **170** and circuit device **140** may be attached using an adhesive **172**, such as an isotropically conductive adhesive, or with solder. Circuit board **161** may also have board traces **162** formed of conductive material for interconnecting particular discrete electrical components **164** and **170** to one another and/or to the circuit device **140**. The circuit device **140** may be analogous to circuit devices **10** and **40** of FIG. **1** and FIGS. **4**A through **4**D, respectively.

Discrete electrical components **164** and **170** refer to electrical components that are manufactured independently of one another. That is, each discrete electrical component **164** or **170** may be manufactured on a substrate according to a particular process that may be different from other discrete electrical components configured on the circuit board assembly **160**. Examples of discrete electrical components include, but are not limited to, resistors, capacitors, inductors, diodes, transistors, and the like.

The circuit device **140** and discrete electrical components **164** and **170** may be electrically coupled together on the circuit board **161** using board traces **162** and/or interconnections **166** for producing any desirable effect. The circuit device **140** and discrete electrical components **164** and **170** may be configured on the circuit board **161** during the assembly level phase of production. The circuit device **140** may be coated with a first **150** and/or second **156** protective dielectric layers as described above with respect to the first **22** and/or second **24** protective dielectric layers, respectively, of FIG. **1**.

In many cases, additional processing techniques of circuit device **140** may be desirable following manufacture at the wafer level. For example, the circuit device **140** may be severed from the wafer using saws or other cutting tools in which scribe moats may be created. Interconnections **166** from the circuit device **140** to component **164** may be formed at the assembly level that may be susceptible to harmful contaminants, such as those described above. Thus, the lack of dielectric protection in the scribe moats, device edges and interconnections **166** may render the circuit device **140** susceptible to moisture attack, particulates or other contaminants.

The circuit board **161** may also require environmental protection to perform reliably in a non-hermetic enclosure and/or one where physical particulates cannot be adequately controlled. Known passivation systems use a relatively thick layer of parylene C, D or N that may have a thickness, for example, of 10 microns (100,000 Angstroms) or greater in thickness. This relatively thick layer of parylene may be unsatisfactory for microwave and millimeter wave circuits where the dielectric loading may alter and/or degrade circuit performance. Parylene C, D, or N may not tolerate high temperatures well. Exposures to high temperatures, which may occur on high power devices, may increase the crystallinity of parylene C, D or N. Increases in crystallinity increase stress in the parylene film and at the parylene interface to circuit board assembly **160**. Such increases in stress can cause de-lamination of the parylene material resulting in failure or degradation in performance.

One embodiment of the present disclosure provides for application of a second protective dielectric layer **156** and/or third dielectric layer **158** at the assembly level as opposed to the wafer level phase of production. By combining the wafer level coating with the assembly level coating, assembly level features, such as discrete electrical components **164** and **170**, circuit device **140**, board traces **162**, metal interconnections **166**, scribe moats, die edges, and external interconnections to the circuit board assembly **160**, such as wire or ribbon bonds, and other assembled components can all be coated simultaneously. Further, the required dielectric thickness using certain embodiments of the present disclosure may be, in many instances, two orders of magnitude or more lower than known passivation systems using parylene, silicone, or urethane coatings. This reduced thickness may thus minimize degradation in circuit performance in certain embodiments.

According to one embodiment, the second **156** and/or third **158** protective dielectric layers may be coated with a dielectric material having modulus of elasticity less than 3.5 GigaPascal (GPa), dielectric constant less than 3.0, dielectric loss less than 0.008, breakdown voltage strength in excess of 2 million volts/centimeter (MV/cm), temperature stability to 3000 Celsius, pinhole free in films greater than 50 Angstroms, hydrophobic with a wetting angle greater than 45 degrees, and capable of being deposited conformally over and under 3D structures with thickness uniformity less than or equal to 30%. This dielectric material may be applied during the assembly level phase of production to passivate the circuit board **161**, board traces **162**, circuit device **140**, discrete electrical components **164** and **170**, and assembly level features from the environment. This dielectric material may be applied as the second protective dielectric layer **156** or third dielectric layer **158**. The dielectric material is generally chemically stable with respect to vapor or liquid water, thus protecting the first protective dielectric layer **150** and/or second protective dielectric layer **156**. The dielectric material has superior moisture retarding characteristics and is functionally stable over a wider temperature range than other known passivation materials described above. The dielectric material also has a lower intrinsic dielectric constant than other known passivation materials. In one embodiment, the third dielectric layer **26** may have a thickness in the range of approximately 100 to 1000 angstroms. In one embodiment, the dielectric material is parylene F, aromatic-fluorinated VT-4, parylene HT®, or other fluorinated parylene-like film.

The coating materials of this embodiment may tolerate higher temperatures than known passivation systems using parylene C, D or N and thus may not degrade as rapidly with exposure to temperature extremes. The additional assembly level dielectric layer(s) may also add further protection to the active device regions. By proper selection of the first protective dielectric layer **150** thickness applied at the wafer level of production in conjunction with the second protective dielectric layer **156** and/or third dielectric layer **158** applied at the assembly level of production, passivation of the circuit board assembly **160** may be tailored to suit many types of applications.

Additionally, the first protective dielectric layer **150** formed of alumina, tantalum-oxide, beryllium-oxide, hafnium-oxide, or high density silicon-nitride, and nanolaminates of these materials with silicon dioxide whereby the dielectric constant is adjusted by controlling the thickness of the nanolaminate layers or other suitable material according to the teachings of this disclosure, may be able to retard growth of tin whiskers, which is an inherent problem associated with the use of low-lead solder formulations. Tin whisker growth has been associated with the presence of moisture and stress conditions which can be aggravated by moisture.

FIG. **6** illustrates a series of actions that may be performed in order to manufacture one embodiment of a circuit device **160**, shown and described above with respect to FIGS. **5**A and **5**B. In act **200**, the method for providing an electrical and environmental protection coating system is initiated. In act **202**, one or more electrical components **146** may be formed on a substrate **142** using known integrated circuit manufacturing techniques. In act **204**, first **150** and/or second **156** protective dielectric layers may be deposited on the substrate **142** and electrical components **146**. Acts **202** and **204** described actions that may be performed during the wafer level phase of production.

Acts **206** through **214** describe actions that may be performed during the assembly level phase of production. In act **206**, the circuit device **142** may be attached to a circuit board **161**. In act **208**, one or more discrete electrical components **164** and/or **170**, and/or one or more assembly level features, such as interconnections **166** may be formed on the circuit board **161**. Additionally, other circuit features, such as scribe moats or die edges may be formed on the circuit device **140**.

In act **210**, a second protective dielectric layer **156** and/or a third dielectric layer **158** may then be deposited over the first **150** and/or second **156** protective dielectric layers, respectively, and any discrete electrical components or assembly level features that have been formed on the circuit board assembly **160**. In one embodiment, the second protective dielectric layer **150** or third dielectric layer **158** may be made of a dielectric material, and in a particular embodiment, may be parylene F or parylene HT®. In one particular embodiment in which the second protective dielectric layer **156** and/or a third dielectric layer **158** is made of parylene F or parylene HT® and is adjacent an underlying layer made of alumina, an adhesion promoter may be applied between the second protective dielectric layer **156** and third dielectric layer **158**. In another embodiment, the adhesion promoter may be a layer of silicon dioxide used independently or in conjunction with gamma-methacryloxypropyltrimethoxysilane.

In act **212**, the method for application of a passivation layer has been completed and thus the circuit board assembly **160** may then be used.

FIG. **7** shows a number of embodiments **1**a through **2**c in which various combinations of first protective dielectric layer **150**, a second protective dielectric layer **156**, and a third dielectric layer **158** that may be applied at the wafer level and at the assembly level phase of production. Embodiments **1**a through **2**c utilize a first protective dielectric layer **150** that is formed during the wafer level phase of production. As described above with respect to FIG. **3**, the material and method of application of the first protective dielectric layer **150** is similar to embodiments **1** through **5** of FIG. **3**.

Embodiments **1**a, **1**b, **1**c, **1**d, **1**e of FIG. **7** have the second protective dielectric layer **156** deposited at the assembly level and hence the second protective dielectric layer **156** may provide protection for assembly level features that are added or modified during the assembly level of production. Examples of assembly level features that may be added or modified at the assembly level include processing of the substrate **142**, addition of circuit board components **164** and **170**, and forming interconnections **166**.

Embodiment **1**a shows second protective dielectric layer **156** made of alumina. Application of the second protective dielectric layer **156** at the assembly level may provide enhanced environmental protection compared to known organic dielectrics and hence may minimize dielectric loading effects on components added at the assembly level. Such effects become increasingly important as the frequency of operation increases to microwave and millimeter wave frequencies.

Embodiment **1**b utilizes a second protective dielectric layer **156** made of parylene F or parylene HT® with no third dielectric layer **158**. In this particular embodiment, an adhesion promoter may be applied prior to application of the second protective dielectric layer **156**. Embodiment **1**b may provide relatively little electrical impact to the operation of the circuit board assembly **160** due to the low dielectric constant of parylene F or parylene HT®. Embodiment **1**c utilizes a second protective dielectric layer **156** made of silica with no third dielectric layer **158**.

Embodiment **1**d utilizes a second protective dielectric layer **156** of alumina with a third dielectric layer **158** made of parylene F or parylene HT®. As described previously, the alumina layer provides relatively good adhesion to circuit assembly **160** and to parylene F or parylene HT® especially when used in conjunction with an adhesion promoter such as a layer of silicon dioxide used independently or in conjunction with gamma-methacryloxypropyltrimethoxysilane.

Embodiments **2**a, **2**b, **2**c have first protective dielectric layer **150** and second protective dielectric layer **156** applied at the wafer level and the third dielectric layer **158** applied at the assembly level of production. Certain embodiments using this process may provide an advantage in that the devices may be electrically measured at the wafer level and only known good die provided to the assembly level.

Another embodiment of the present disclosure includes a relatively thin initial layer of high density (greater than 2.5 gm/cm3) and/or low hydrogen content (less than 15 atomic percent) silicon-nitride or silicon dioxide films deposited by techniques well known in the industry including conventional chemical vapor deposition (CVD), High Density plasma enhanced CVD techniques including deposition by Electron Cyclotron Resonance Plasma Enhanced CVD (ECR PECVD), Inductively Coupled Plasma Enhanced CVD (ICPECVD), high density inductively coupled plasma chemical vapor deposition (HDICPCVD), reactive magnetron sputtering, hot wire chemical vapor deposition or PECVD using hydrogen free precursor gases. High density and/or low hydrogen content silicon-nitride may have inherently higher breakdown voltage and resistance to water permeation. The selection of conventional chemical vapor deposition or high density plasma chemical vapor deposition techniques may be

based upon the device structure of the circuit board assembly. This initial layer, made of silicon-nitride or silicon-dioxide, has been well developed and characterized in industry to reduce charge traps and other surface interface defects. The thicker first protective dielectric layer deposited over the initial silicon-nitride or silicon dioxide layer would provide the improved performance and protection benefits described above. An example of this embodiment is illustrated in FIG. **8**.

FIG. **8** is an enlarged view showing a component **216**, which in this particular case is a field effect transistor (FET). Component **216** has a source **216**s, a gate **216**g, and a drain **216**d that are separated from each other by air gap **217**. To achieve superior performance, the air gap **217** is maintained by design of gate recess and gate geometry in conjunction with protective dielectric layer **222** and a thin initial layer **221** of silicon-nitride. As can be seen, the combined thicknesses of the first protective dielectric layer **222** and thin initial layer **221** maintain air gaps **17** such that internode capacitance Cgs and Cgd may be reduced. In one particular embodiment this passivation layer includes a thin layer **221** of silicon-nitride in the range of 25 to 400 Angstroms and a low permeability layer **222** of amorphous alumina having a thickness in the range of 50 to 2000 Angstrom. First dielectric layer **222** may also be formed of any of the same materials as first protective dielectric layer **22**, described above.

Silicon-nitride has proven to be a relatively good and well characterized dielectric for microwave devices with respect to device stability. Alumina has also shown to be a relatively good dielectric with respect to moisture permeability and breakdown voltage. The combination of these two materials with the appropriate thickness and physical properties described in this disclosure may result in an enhanced passivation system over known passivation systems. In one embodiment, a thin layer of silicon-nitride may be used with a nanolaminate. The nanolaminate may include alternate layers of alumina and silicon-dioxide, alumina and parylene F, aromatic-fluorinated VT-4, parylene HT®, or other fluorinated parylene-like film, or alumina and acrylic. In another embodiment, the nanolaminate may include alternate layers of alumina and vapor deposited Teflon (PFTE) and acrylic monomers.

Silicon-nitride, silicon dioxide and alumina have low dielectric constants, especially when deposited under relatively low temperature conditions and with atomic layer deposition. The low dielectric constant further minimizes internode capacitance, changes in performance between coated and uncoated devices and results in improvement in high frequency performance.

Other materials may be substituted for those shown in FIGS. **1-8** according to the teachings of the present disclosure. Other protective dielectric materials that may be suited for such applications may include but are not limited to standard density silicon-nitride, high density silicon-nitride, tantalum-oxide, and beryllium-oxide, hafnium-oxide.

Although the present disclosure has been described in several embodiments, a myriad of changes, variations, alterations, transformations, and modifications may be suggested to one skilled in the art, and it is intended that the present disclosure encompass such changes, variations, alterations, transformations, and modifications as falling within the spirit and scope of the appended claims.

What is claimed is:

1. A method for manufacturing an integrated circuit comprising:

providing a substrate having a substrate surface;

forming an electrical component comprising at least a transistor or a capacitor on the substrate surface;

coating the substrate surface and electrical component with a first protective dielectric layer made of alumina, the first protective dielectric layer having a thickness that is in the range of approximately 50 to 2000 angstroms;

etching a portion of the first protective dielectric layer from the substrate surface or the electrical component in order to form a contact surface;

forming an air bridge on the contact surface;

coating the first protective dielectric layer, the electrical component, and the air bridge with a second protective dielectric layer made of alumina, the second protective dielectric layer having a thickness that is in the range of approximately 50 to 2000 angstroms;

applying an adhesion promoter to the second protective dielectric layer; and

coating the second protective dielectric layer with a third dielectric layer made of *a material selected from the group consisting of* alumina, silica, parylene F, aromatic-fluorinated VT-4, and parylene HT®, the third dielectric layer having a thickness that is in the range of approximately 100 to 1000 angstroms.

2. The method of claim **1**, wherein the act of applying an adhesion promoter comprises applying an adhesion promoter comprising a layer of silicon dioxide used independently or in conjunction with gamma-methacryloxypropyltrimethoxysilane.

3. The method of claim **1**, wherein the act of providing a substrate comprises providing a substrate made of a material selected from the group consisting of silicon (Si), gallium-arsenide (GaAs), Gallium-Nitride (GaN), germanium (Ge), silicon-carbide (SiC), and indium-phosphide (InP).

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