US00RE43330E

(19) **United States**

(12) **Reissued Patent**

Avery et al.

(10) **Patent Number: US RE43,330 E**

(45) **Date of Reissued Patent: May 1, 2012**

(54) **CIRCUIT BOARD VIA ARRANGEMENT FOR DIFFERENTIAL SIGNAL CONNECTOR**

(75) Inventors: **Hazelton P. Avery**, Lisle, IL (US); **Patrick R. Casher**, Lisle, IL (US); **Richard A. Nelson**, Lisle, IL (US); **Kent E. Regnier**, Lisle, IL (US)

(73) Assignee: **Molex Incorporated**, Lisle, IL (US)

(21) Appl. No.: **12/977,286**

(22) Filed: **Dec. 23, 2010**

Related U.S. Patent Documents

Reissue of:

(64) Patent No.: **7,649,146**
Issued: **Jan. 19, 2010**
Appl. No.: **11/901,284**
Filed: **Sep. 14, 2007**

U.S. Applications:

(62) Division of application No. 11/359,739, filed on Feb. 22, 2006, now Pat. No. 7,422,483.

(60) Provisional application No. 60/655,051, filed on Feb. 22, 2005.

(51) **Int. Cl.**
H05K 1/11 (2006.01)

(52) **U.S. Cl.** **174/262**; 174/260; 439/69; 439/608

(58) **Field of Classification Search** 174/250–268; 361/760, 792–795
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,417,578	A	5/1995	Mroczkowski et al.	
5,522,727	A *	6/1996	Saito et al.	439/65
6,273,751	B1 *	8/2001	Francaviglia	439/511
6,350,134	B1 *	2/2002	Fogg et al.	439/79
6,607,402	B2 *	8/2003	Cohen et al.	439/608
6,848,917	B2	2/2005	Lang et al.	
2003/0014864	A1 *	1/2003	Gazelot et al.	29/852

OTHER PUBLICATIONS

European Search Report for EP 06735673.

* cited by examiner

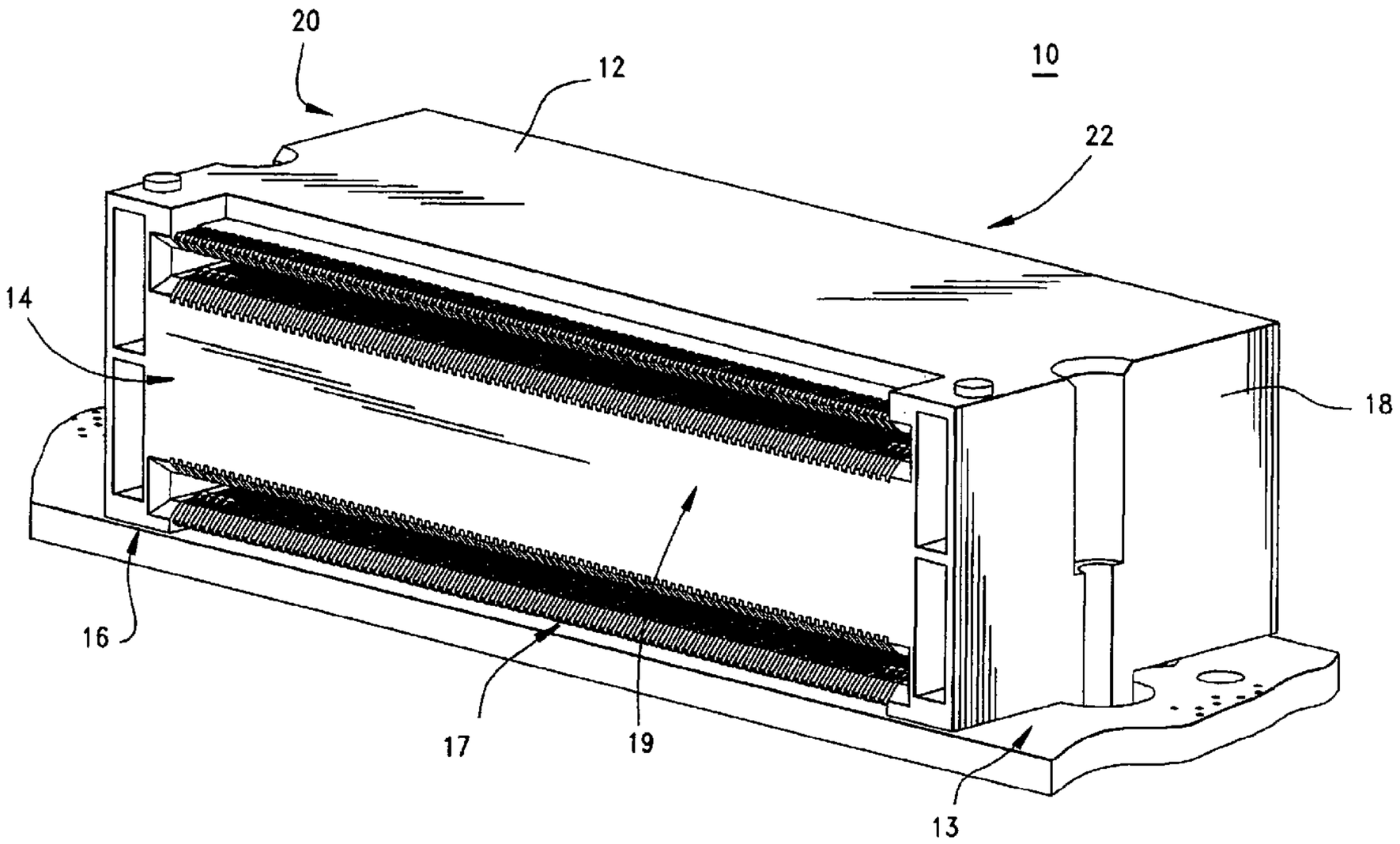
Primary Examiner — Ishwarbhai Patel

(74) *Attorney, Agent, or Firm* — Stephen L. Sheldon

(57) **ABSTRACT**

Stacked receptacles in a connector that each provide side-by-side differential signal contacts, are attached to a circuit board without additional width to accommodate multiple layers of differential signals by using connector wafer inserts that rotate the side-by-side positioned differential signal contacts to front-to-back contacts, *the circuit board including a substrate having a plurality of openings to make electrical contact with conductive terminal tail portion inserted therein, the openings being divided into first and second groups of openings, the first group of openings receiving differential signal terminal tails therein and the second group of openings receiving ground terminal tail therein, when a connector is mounted to said circuit board.*

19 Claims, 17 Drawing Sheets



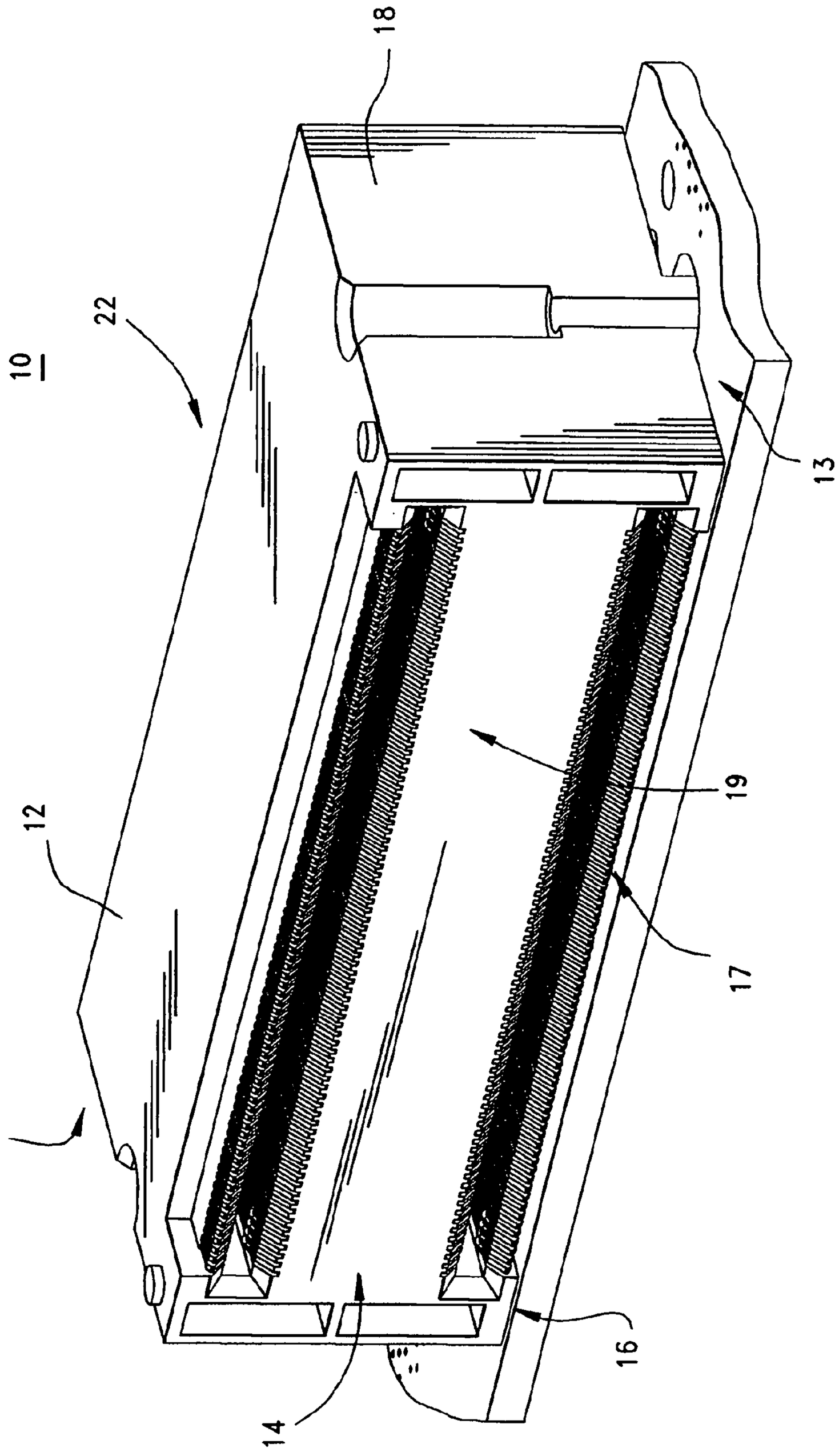


FIG. 1

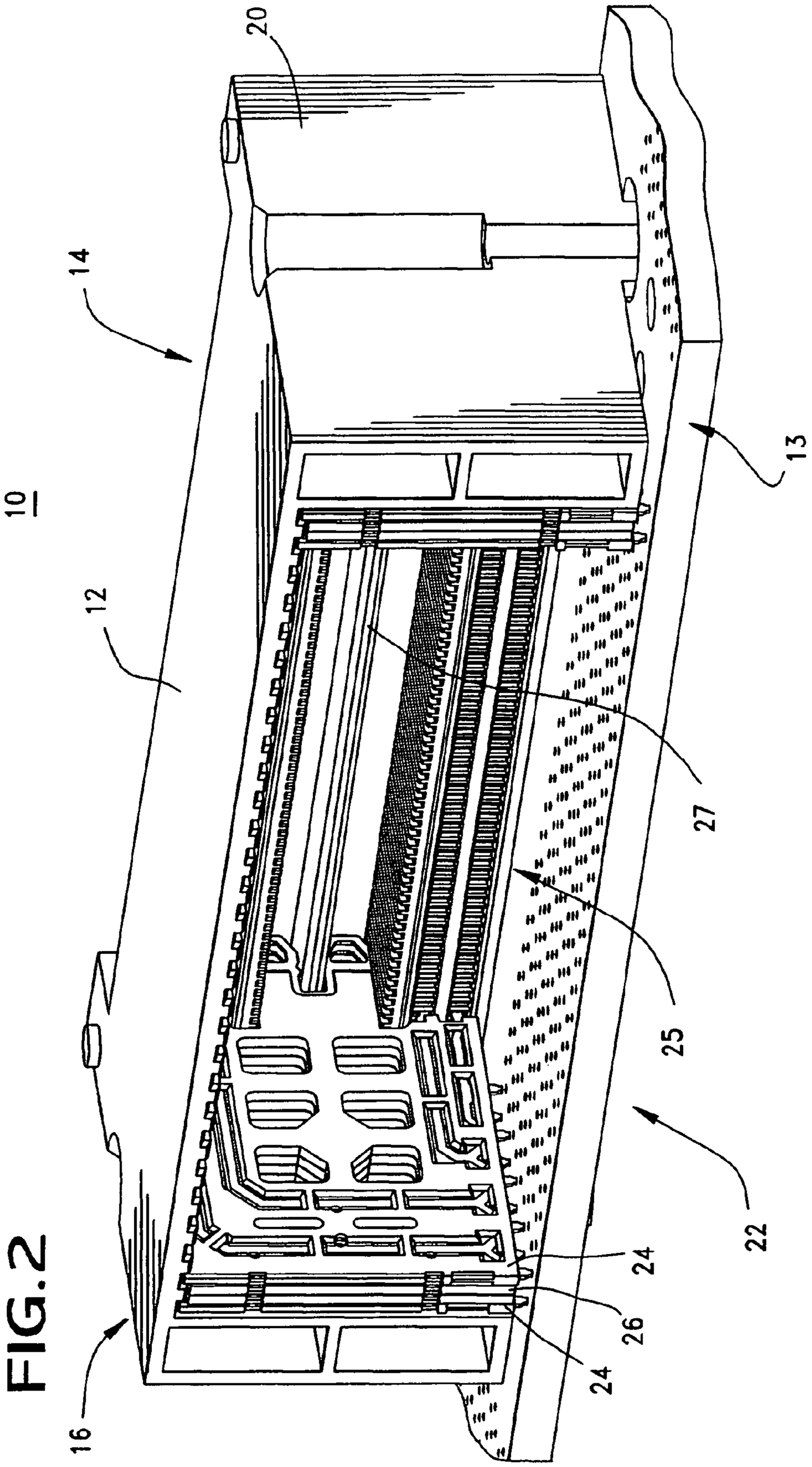


FIG.2

FIG.3

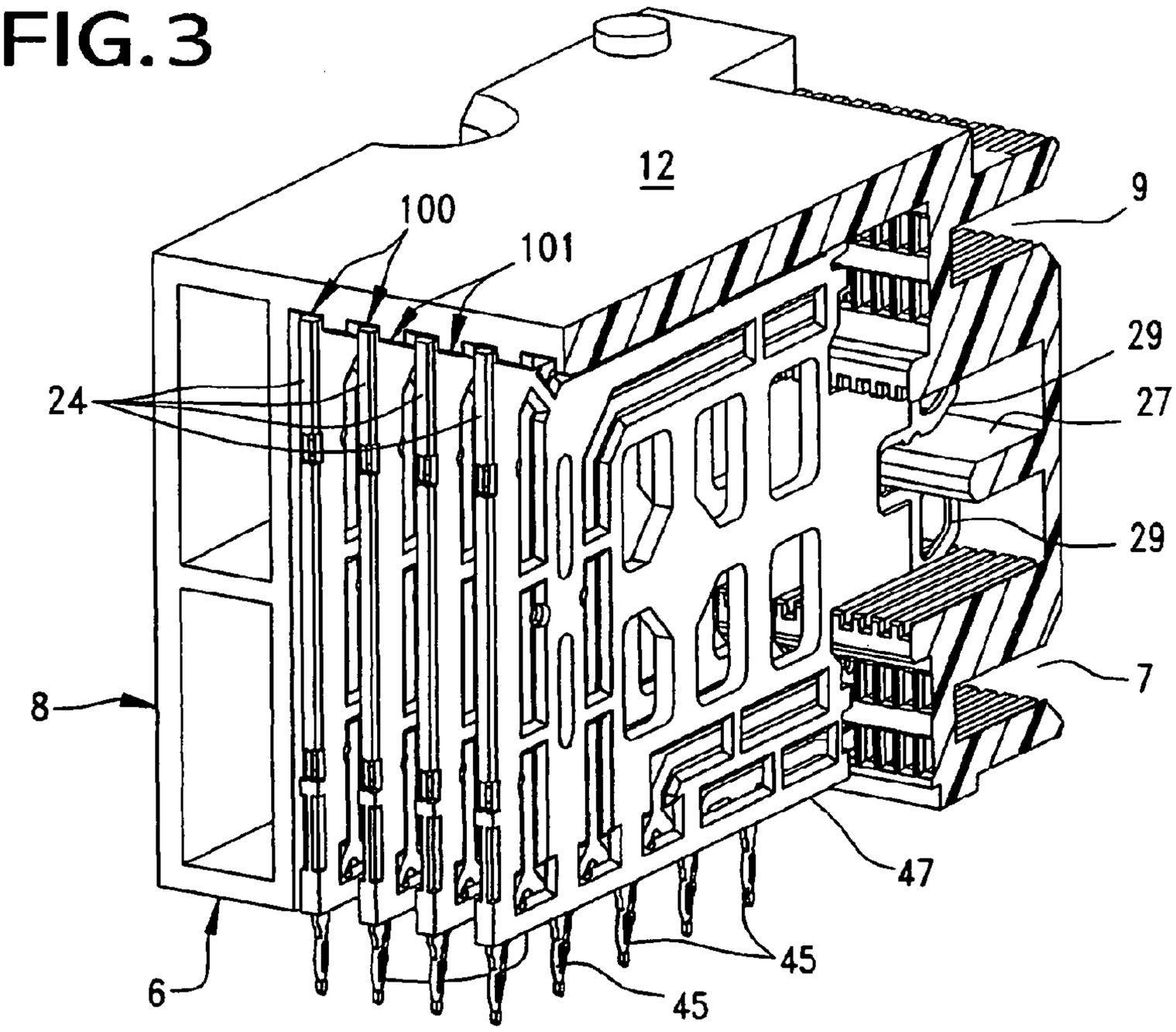
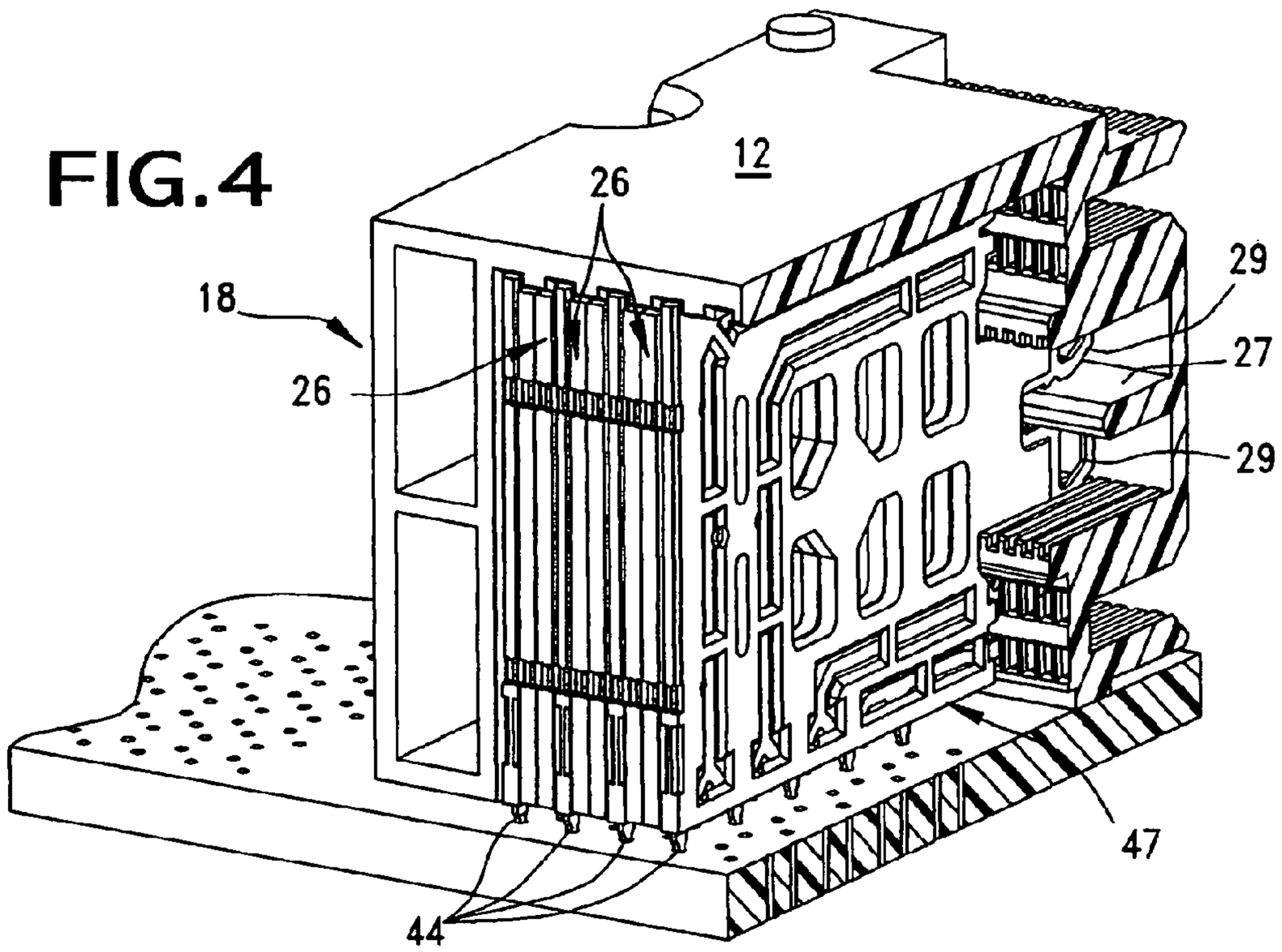


FIG.4



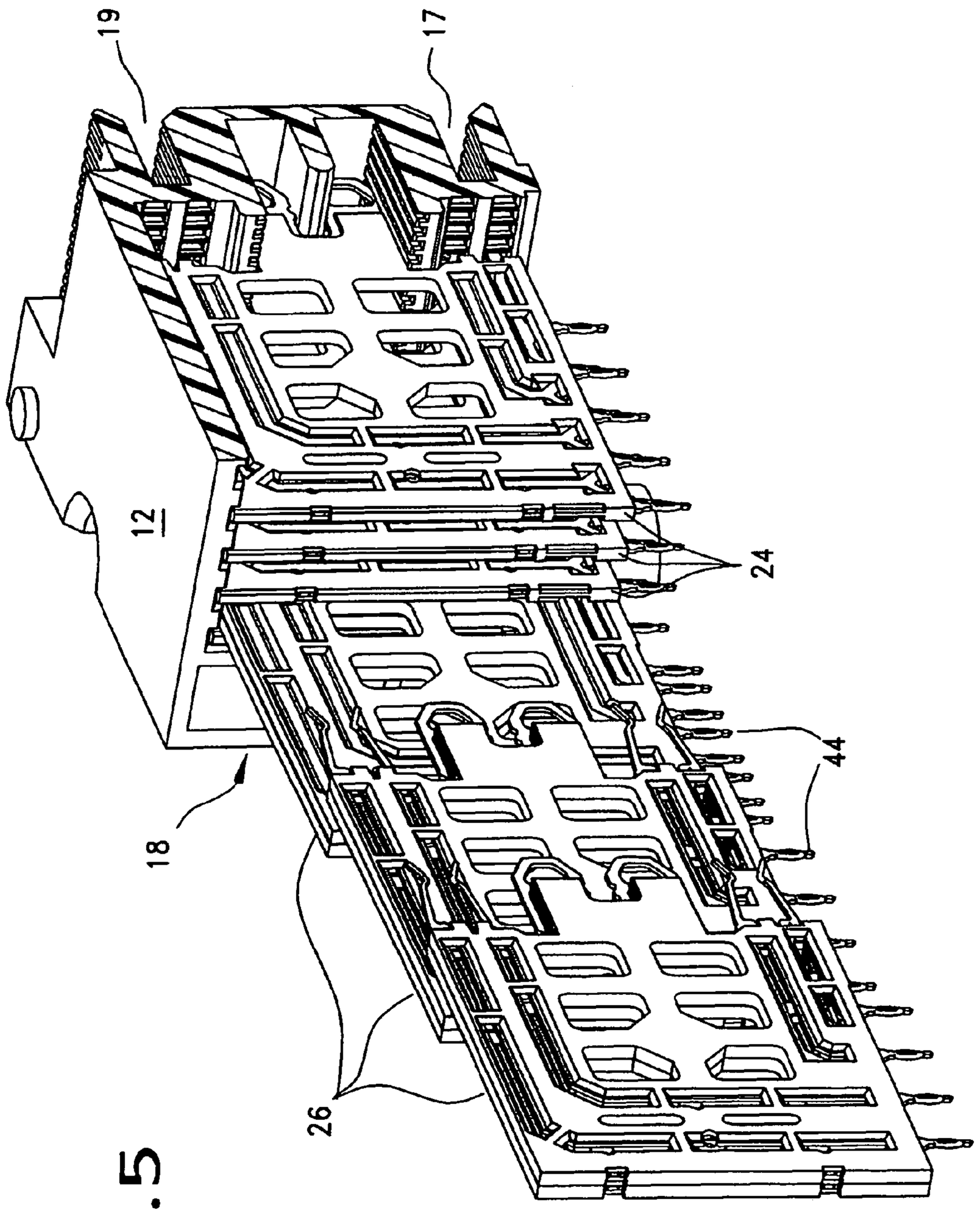


FIG.5

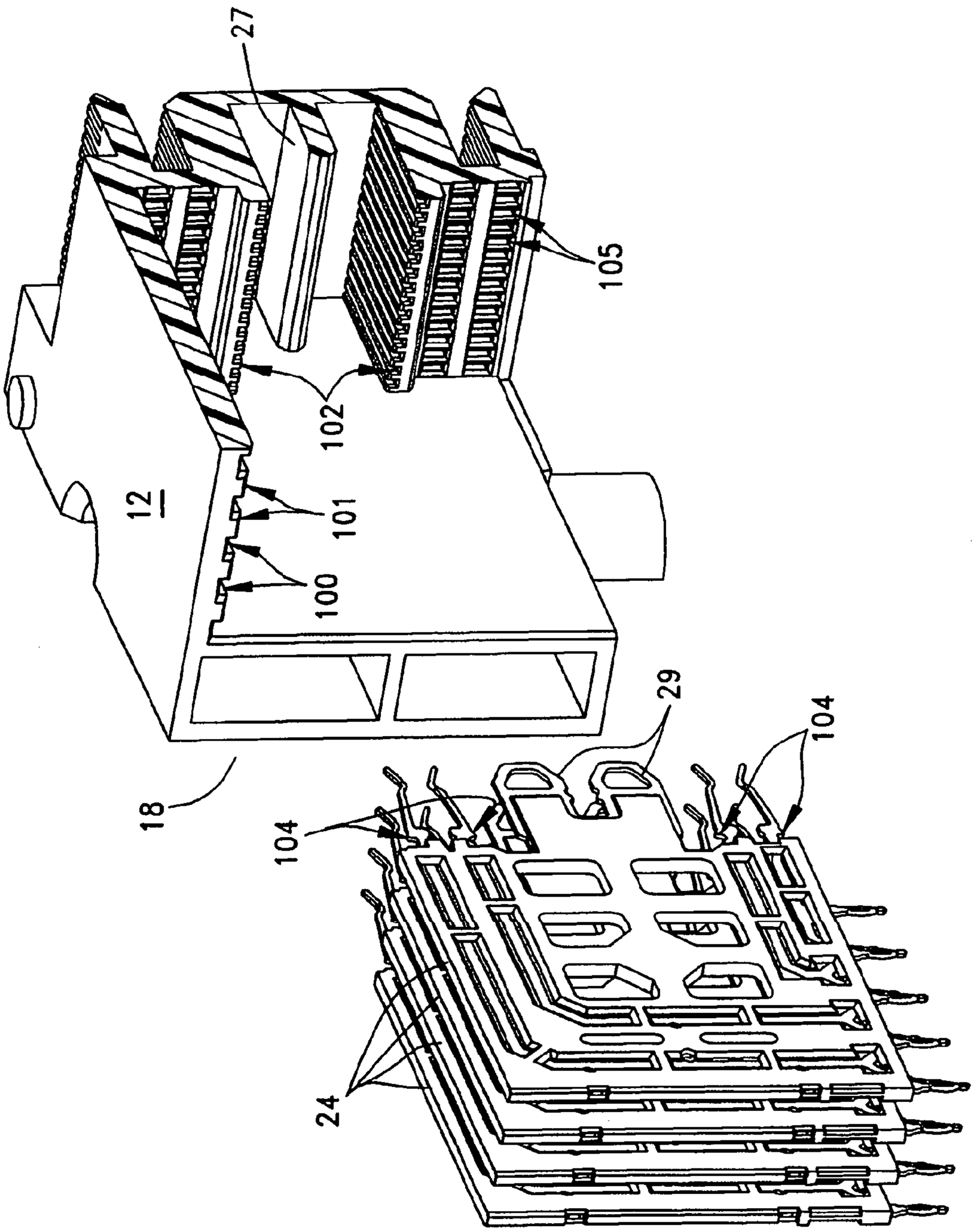


FIG.6

FIG. 7

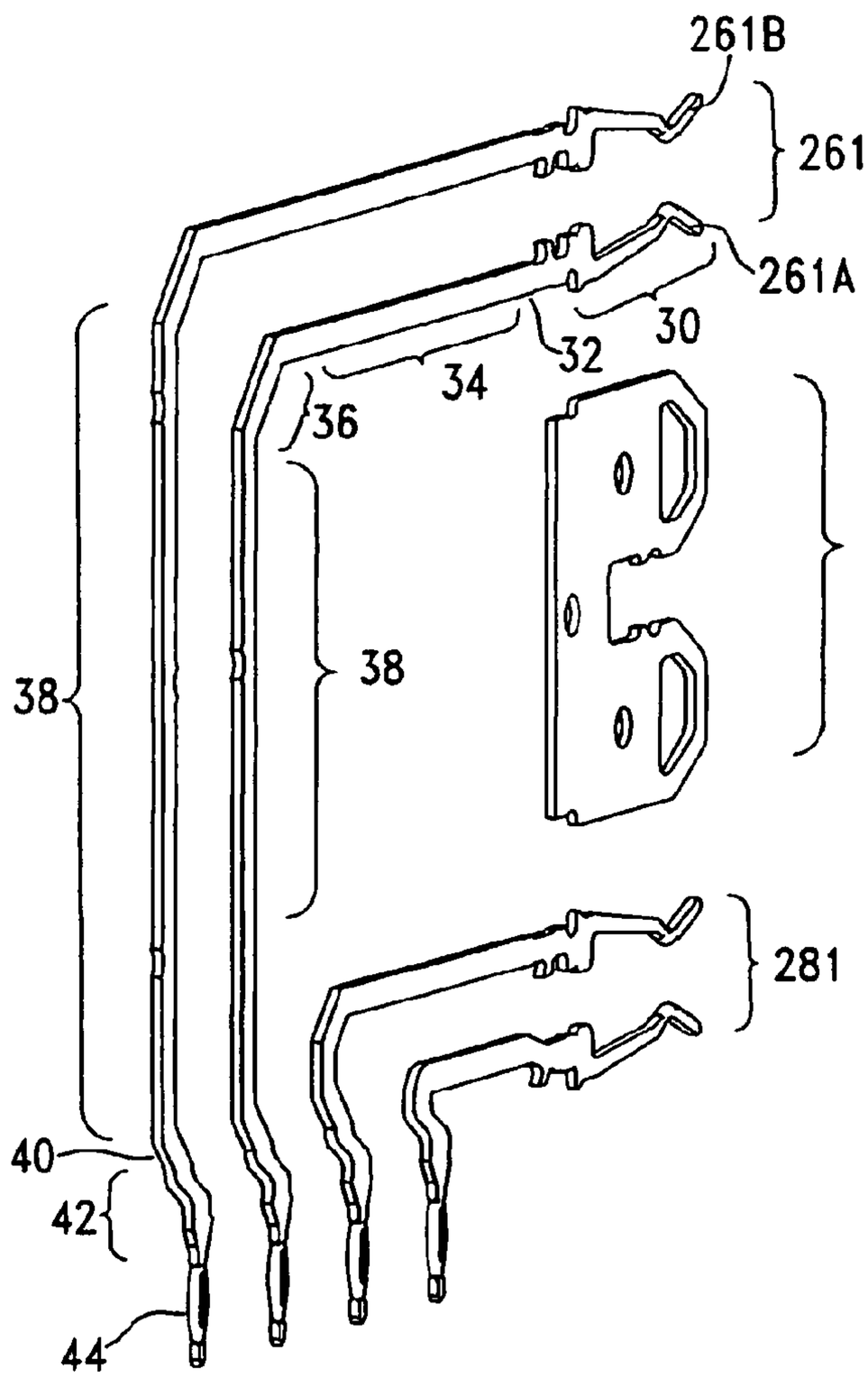

261B
261
261A
30
32
34
36
38
38
29
281
40
42
44

FIG. 12

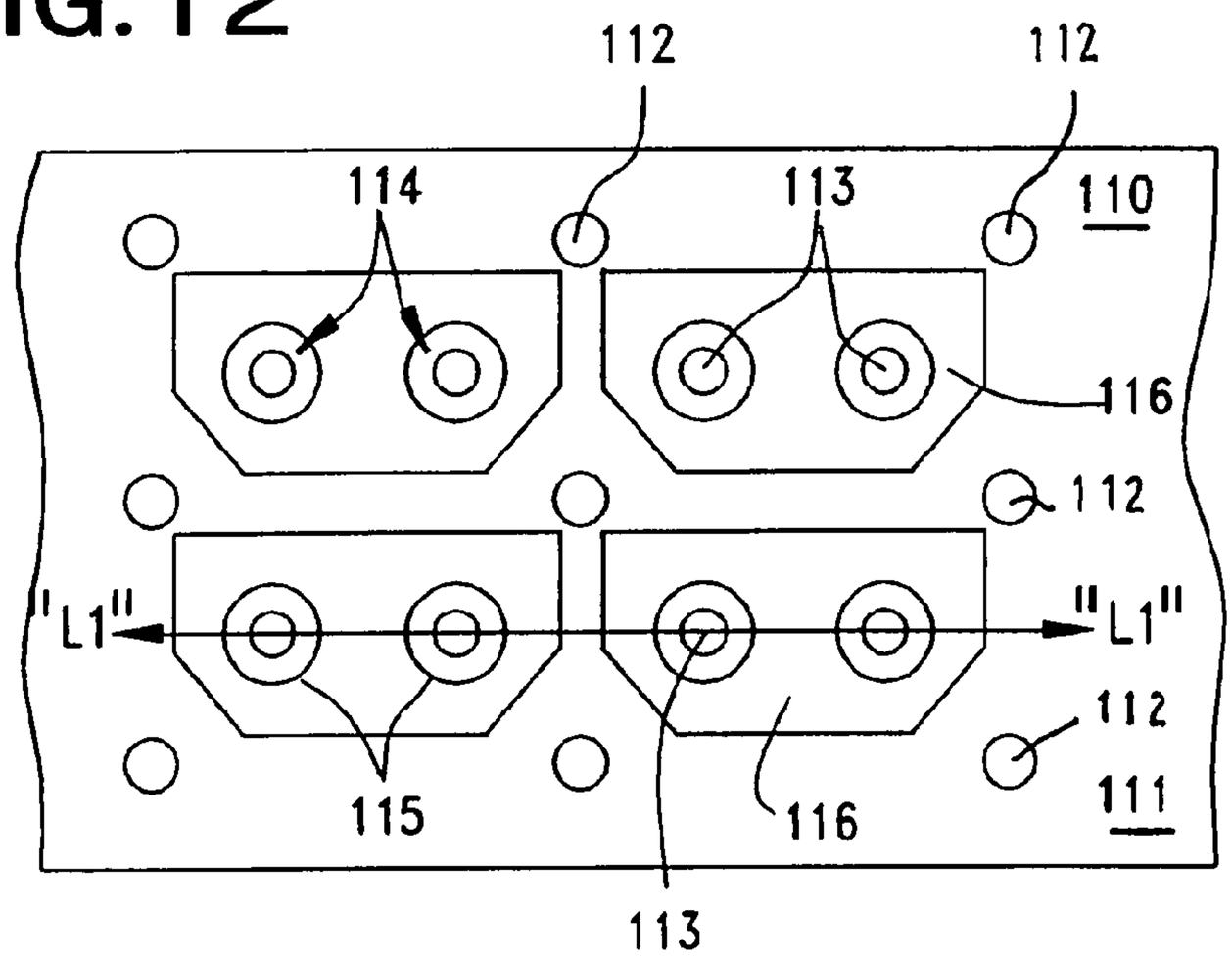
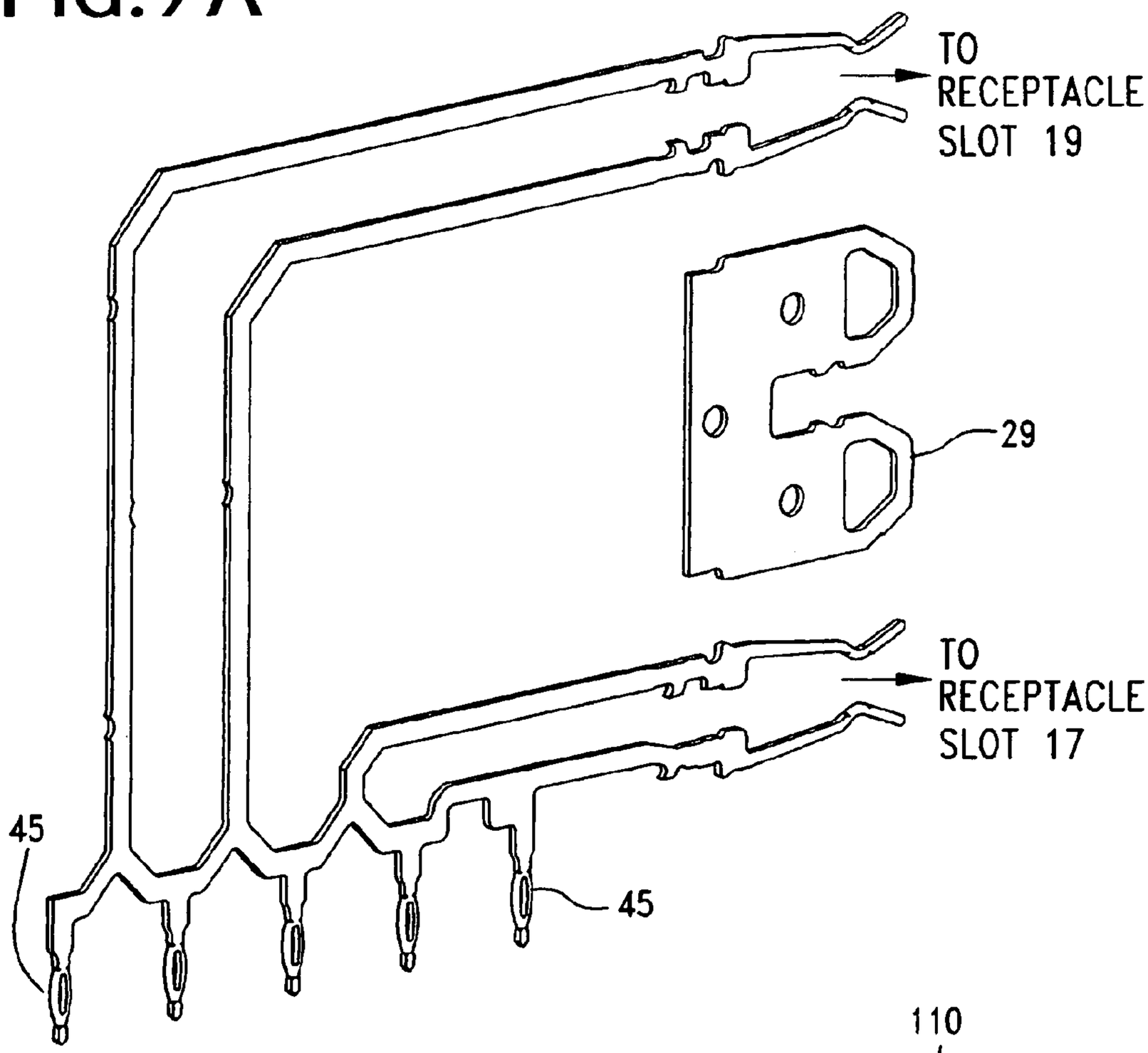

112
112
114
113
110
116
112
"L1"
"L1"
112
115
116
111
113

FIG.7A


TO
RECEPTACLE
SLOT 19
29
TO
RECEPTACLE
SLOT 17
45
45

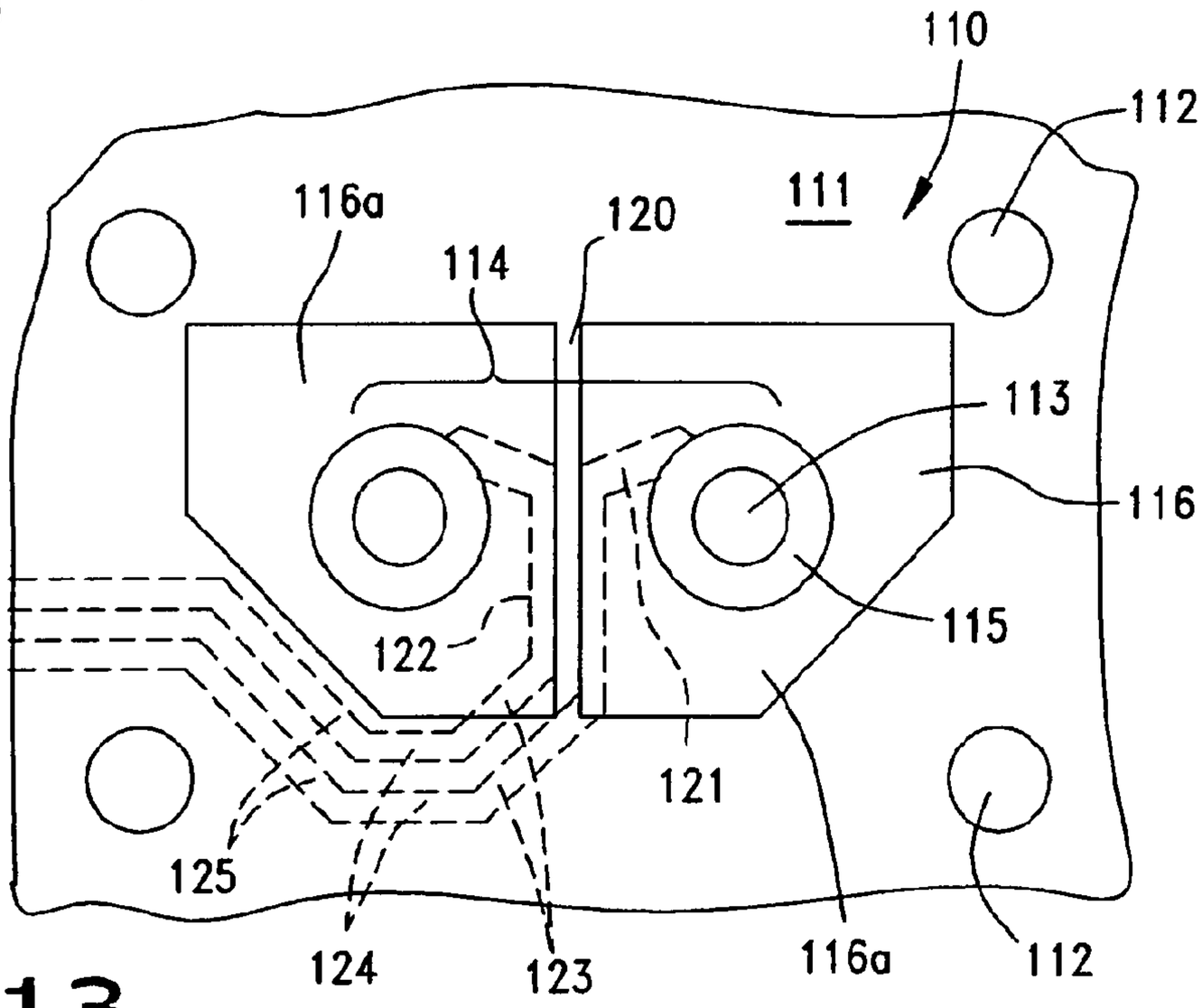

110
112
111
116a
120
114
113
116
115
122
121
125
124
123
116a
112

FIG.13

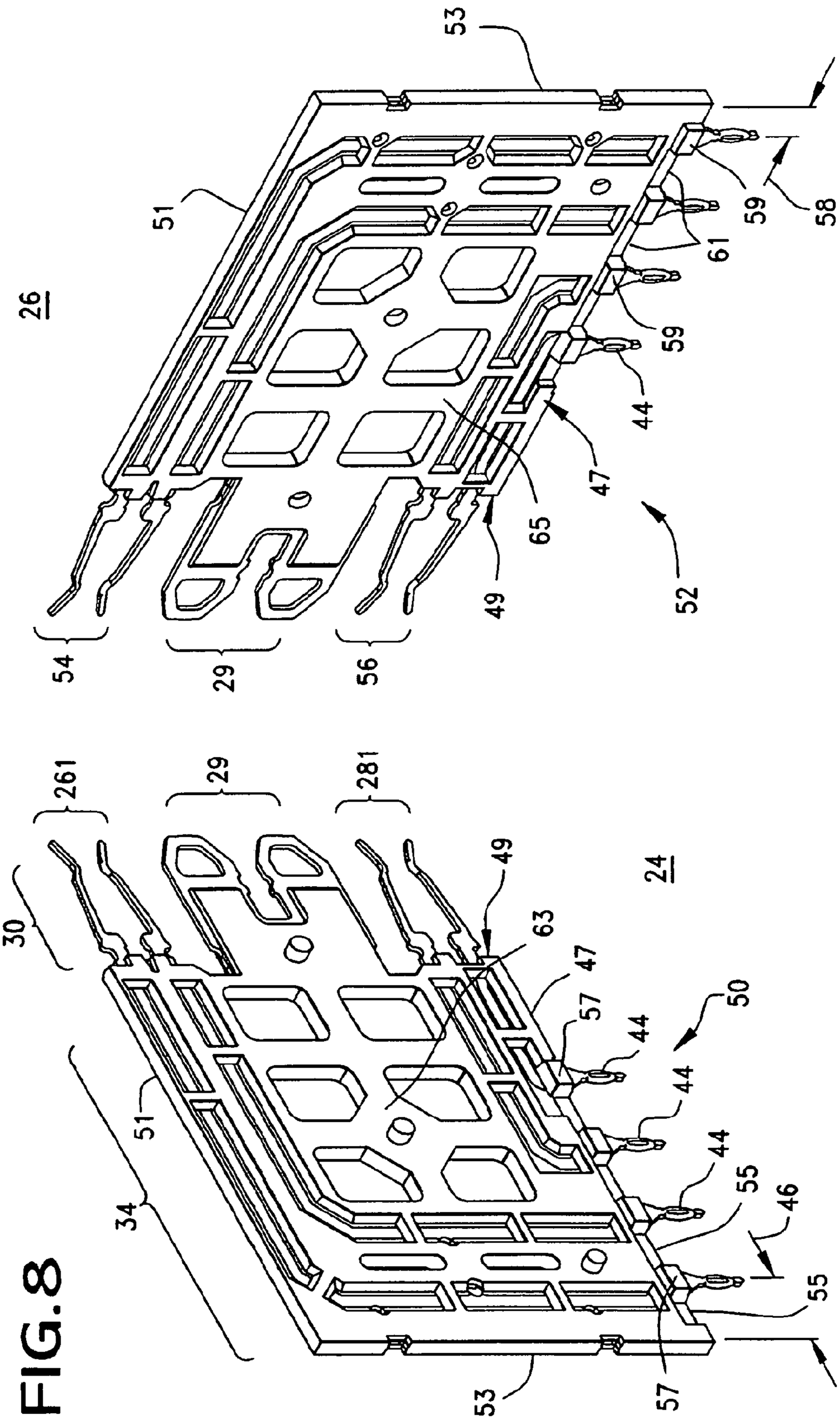

53
51
59
58
61
26
59
44
47
65
49
52
54
29
56
261
29
281
30
49
63
47
24
57
44
50
44
44
55
46
34
51
55
53
57

FIG.8

FIG.9A

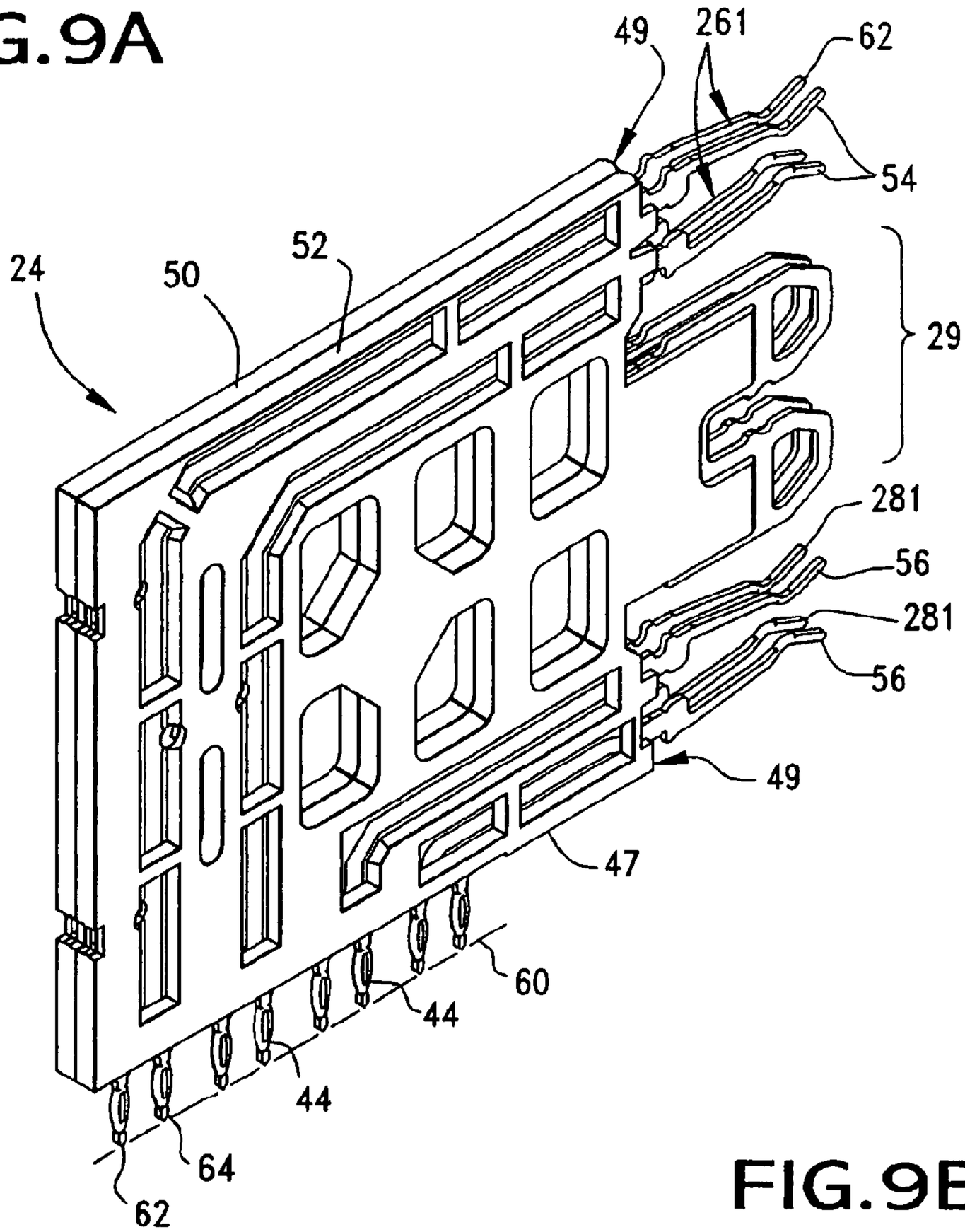
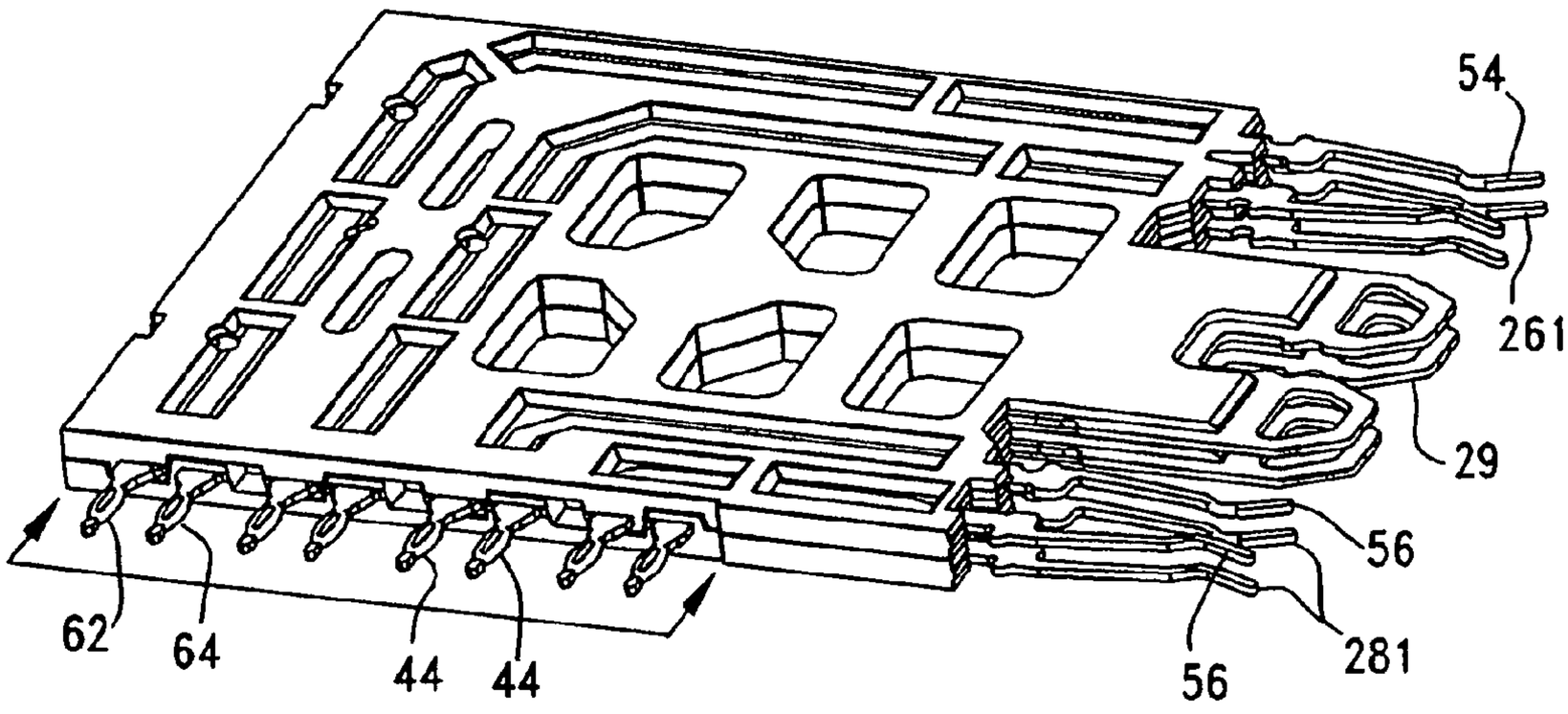

49
261
62
54
24
50
52
29
281
56
281
56
49
47
60
44
44
64
62

FIG.9B


54
261
29
56
281
56
62
64
44
44

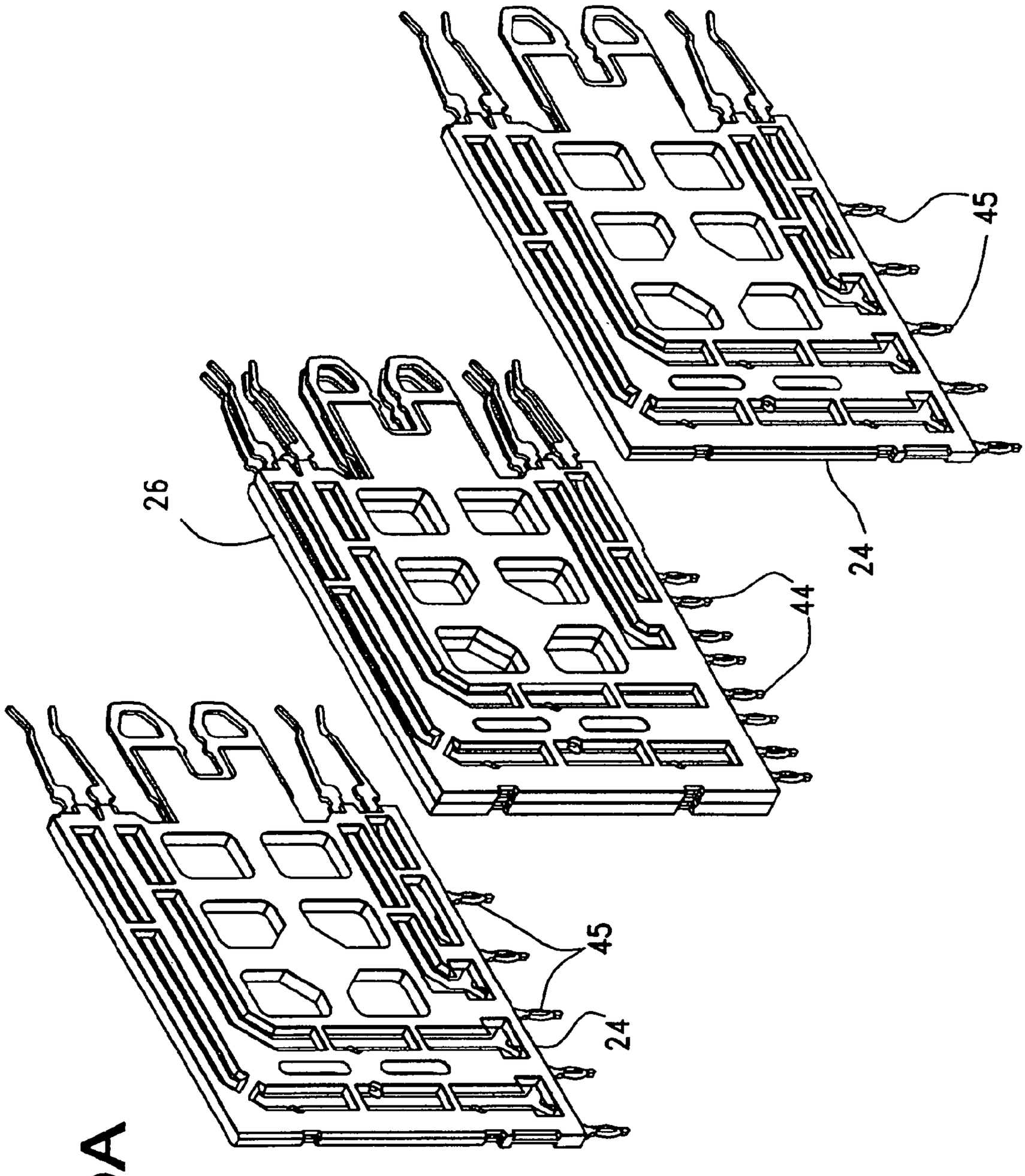


FIG. 10A

FIG. 10B

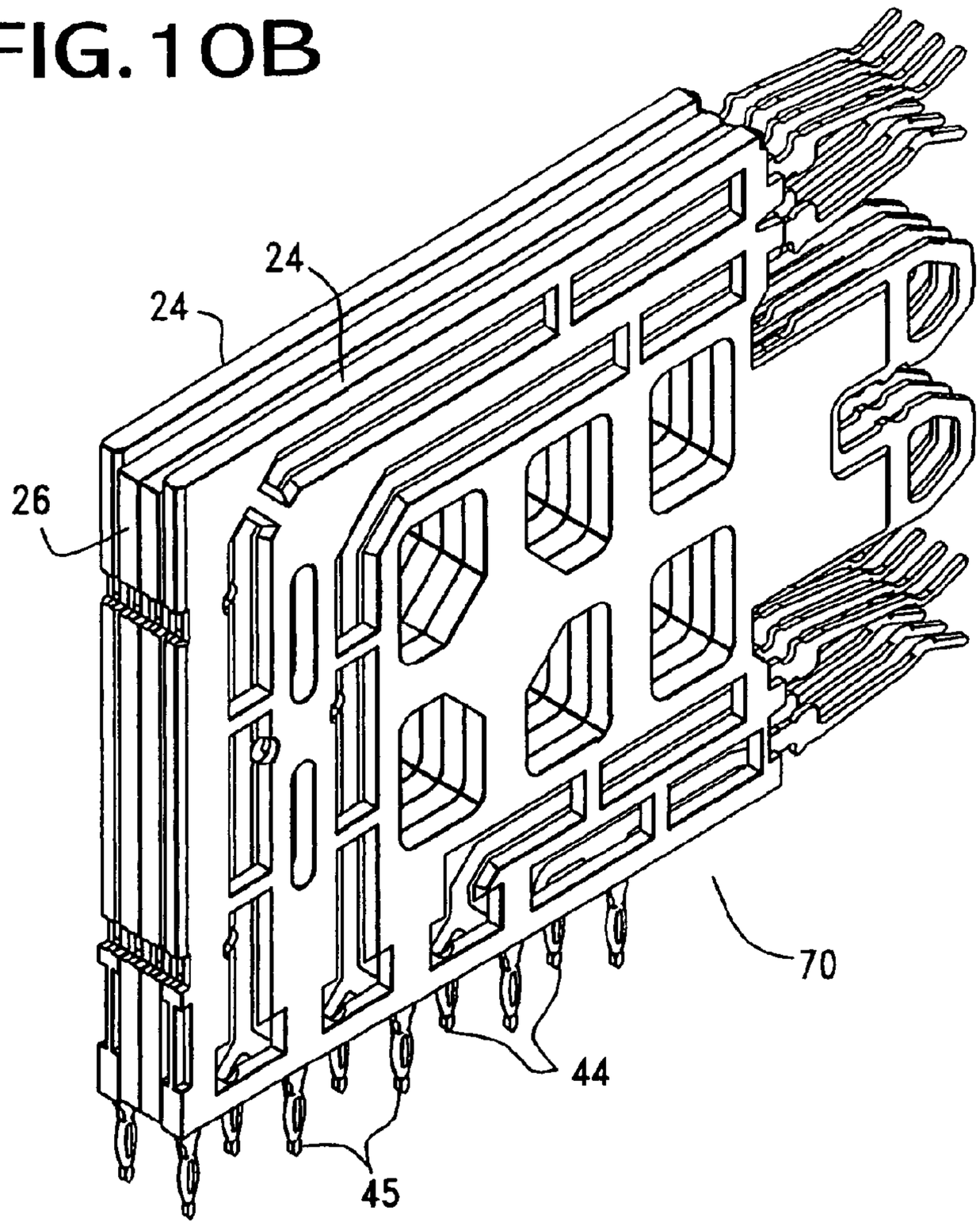


FIG. 11

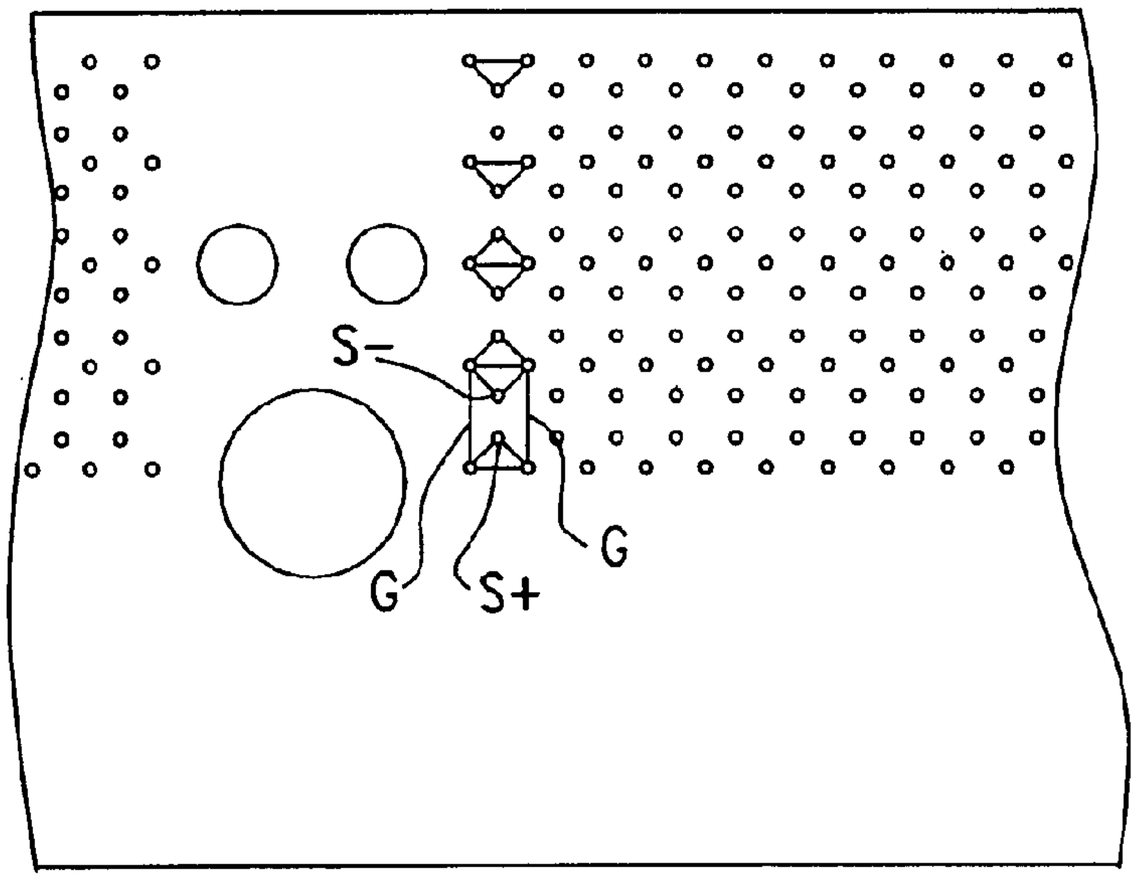
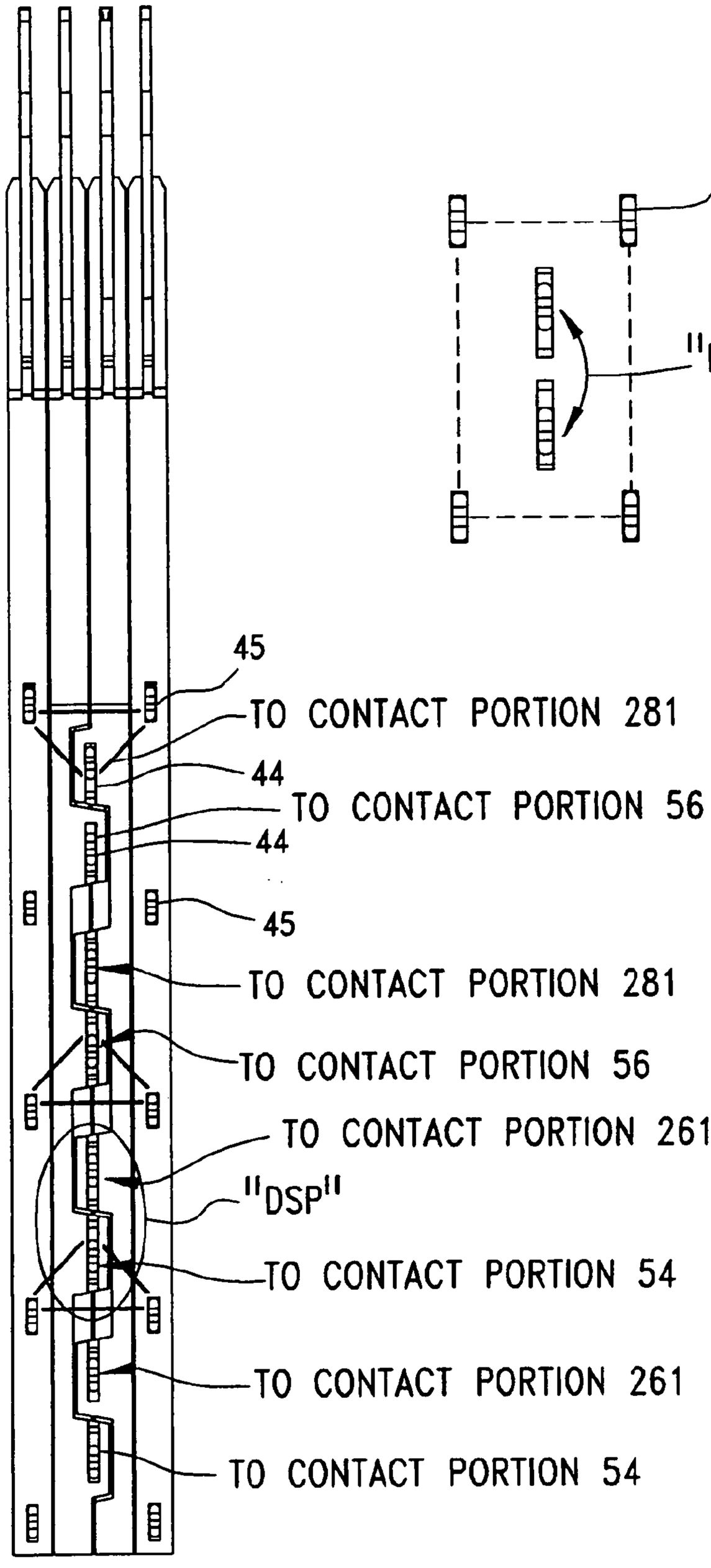


FIG. 10C


45
"DSP"
45
TO CONTACT PORTION 281
44
TO CONTACT PORTION 56
44
45
TO CONTACT PORTION 281
TO CONTACT PORTION 56
TO CONTACT PORTION 261
"DSP"
TO CONTACT PORTION 54
TO CONTACT PORTION 261
TO CONTACT PORTION 54

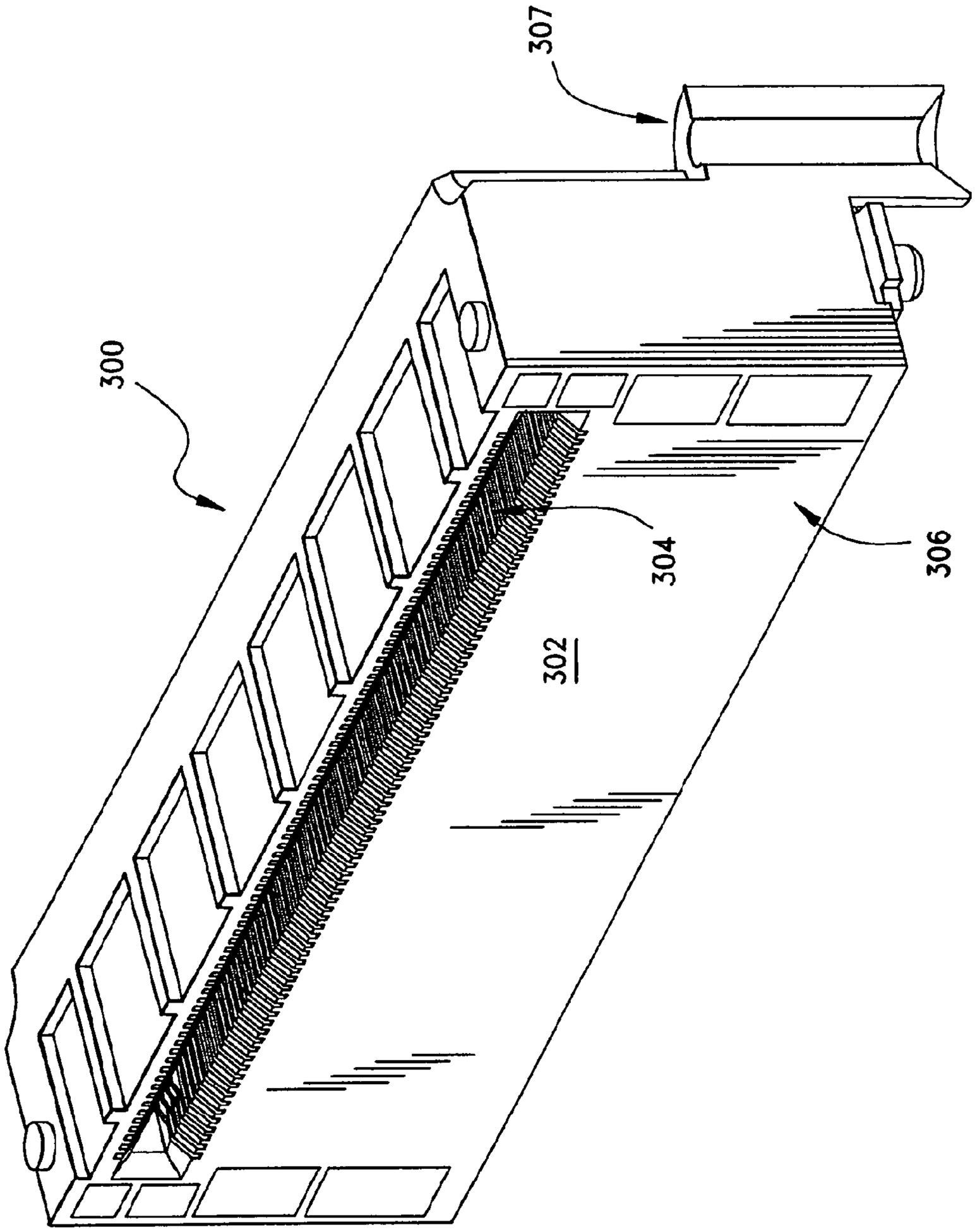


FIG. 14

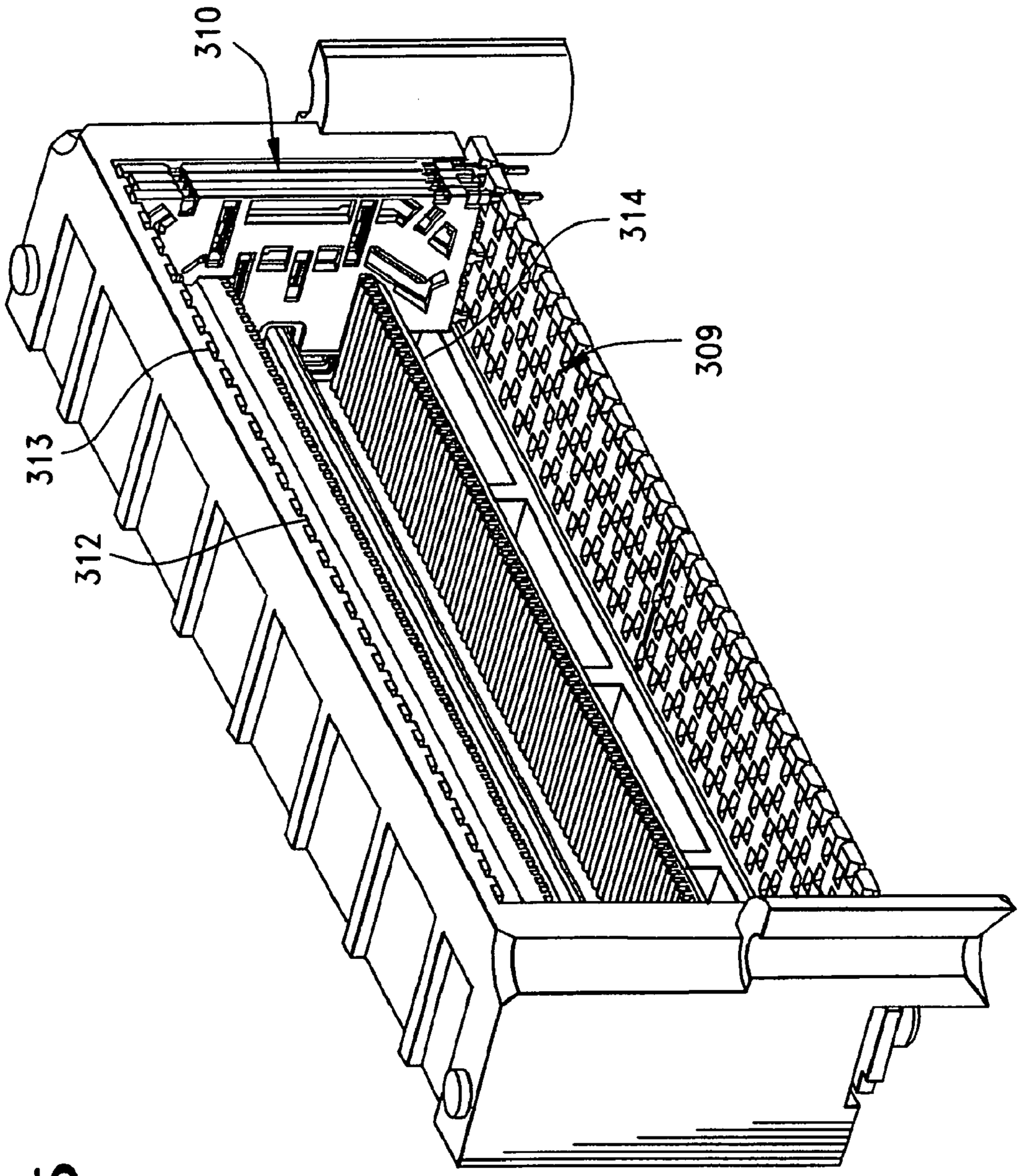


FIG. 15

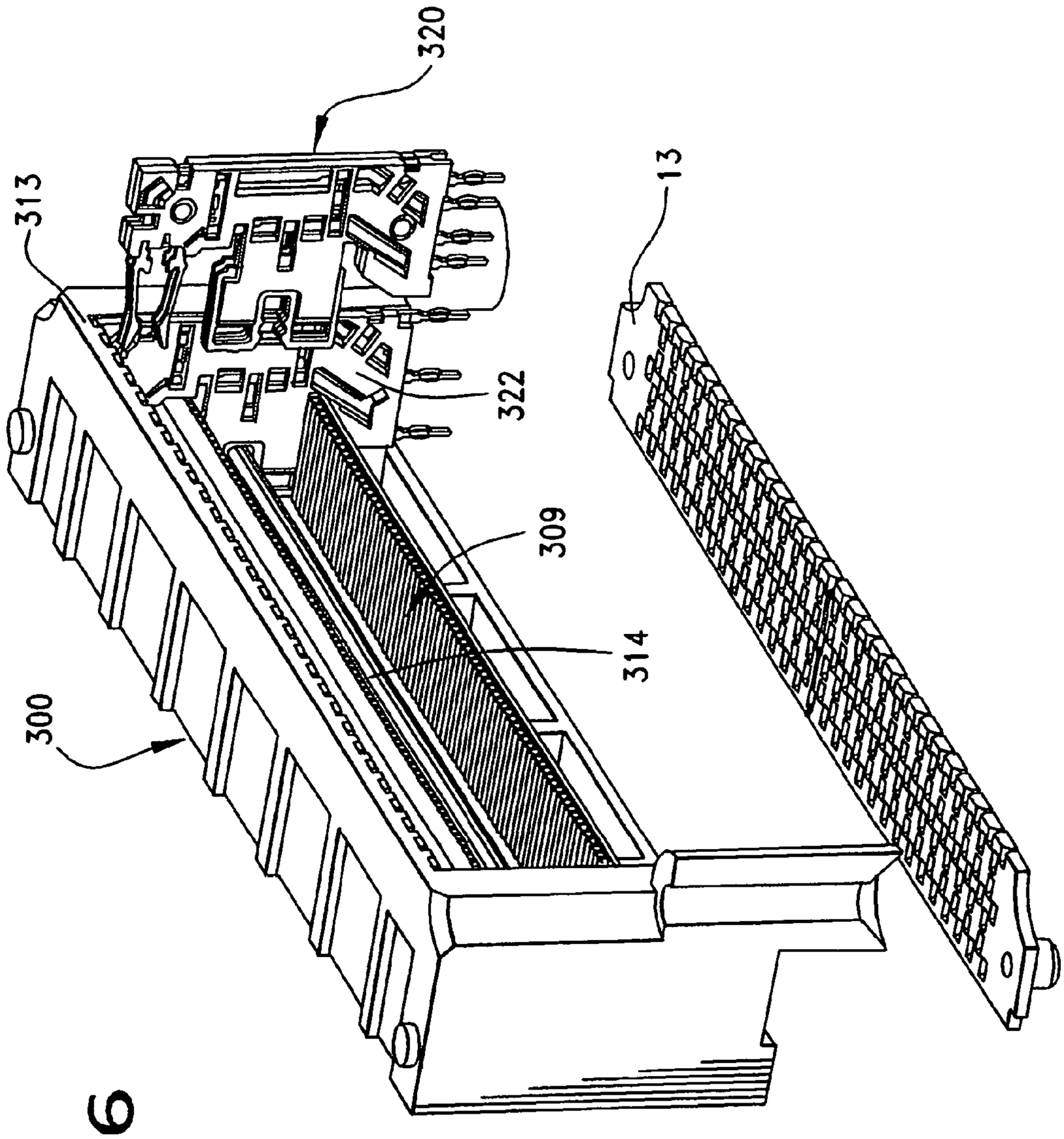
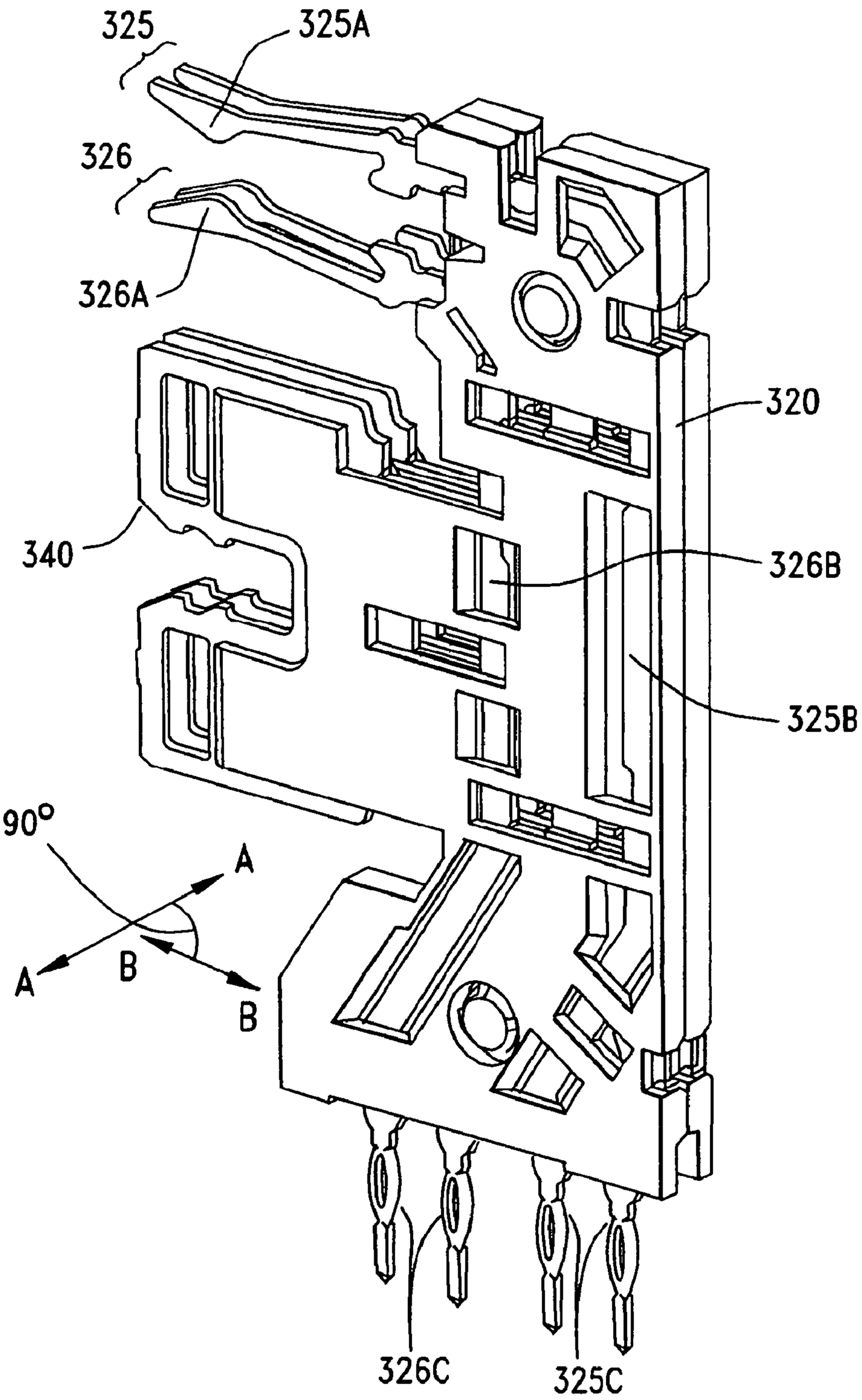


FIG. 16

FIG. 17



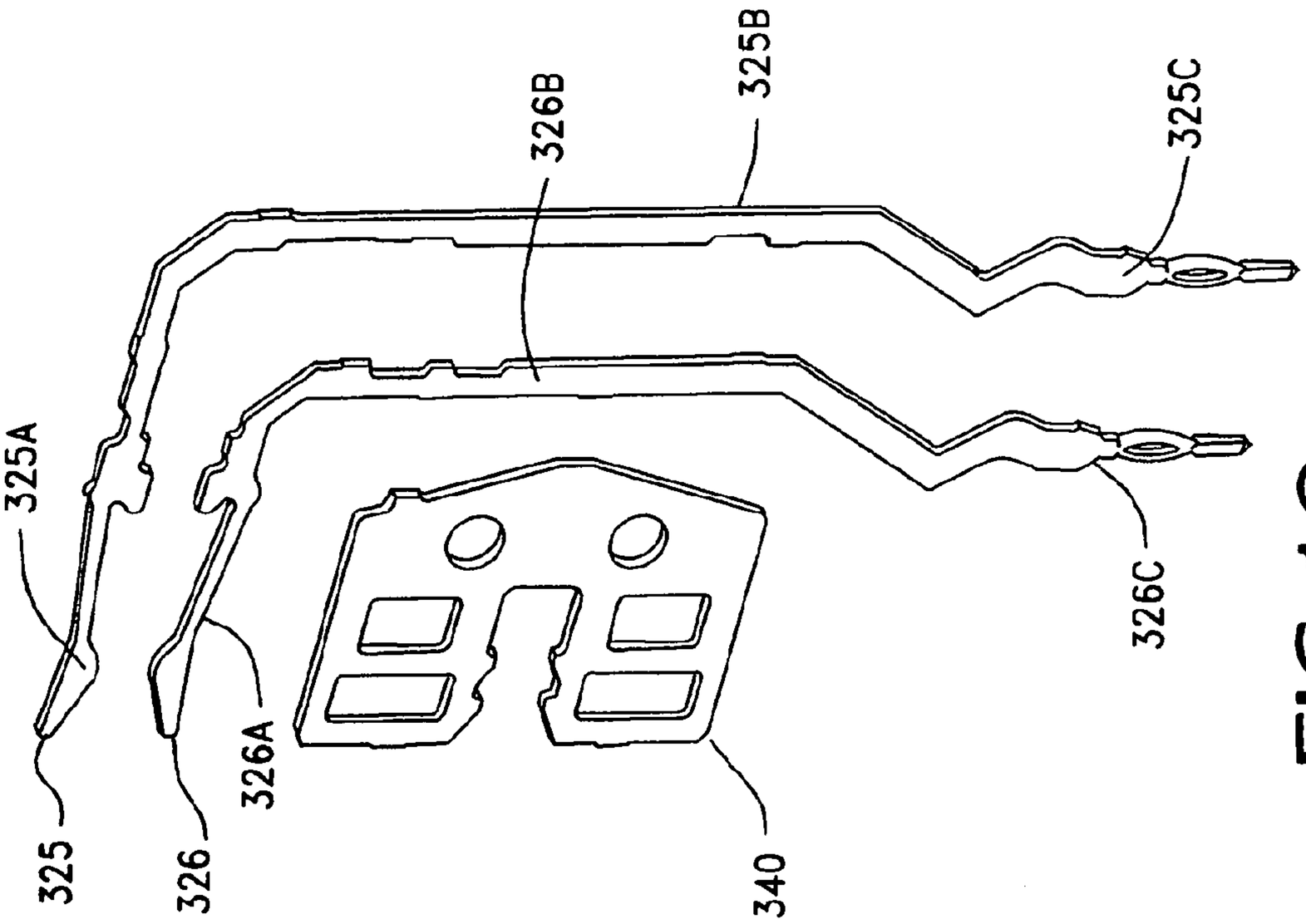


FIG. 19

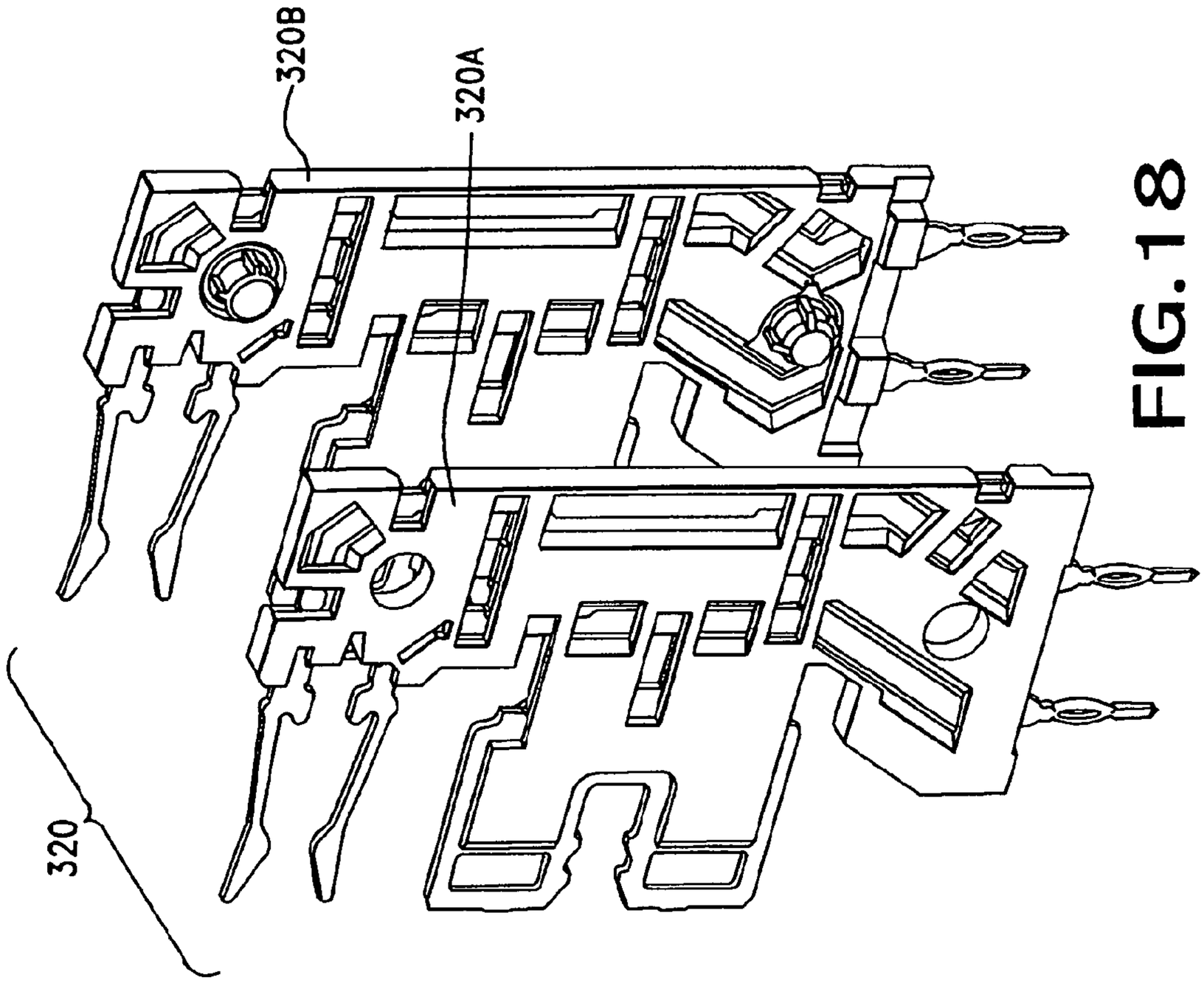


FIG. 18

CIRCUIT BOARD VIA ARRANGEMENT FOR DIFFERENTIAL SIGNAL CONNECTOR

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

REFERENCE TO RELATED APPLICATIONS

This application *is a divisional application of U.S. application Ser. No. 11/359,739, filed Feb. 22, 2006, now U.S. Pat. No. 7,422,483, which in turn* claims priority from U.S. Provisional Patent Application No. 60/655,051, filed Feb. 22, 2005.

BACKGROUND OF THE INVENTION

This invention relates generally to high speed connectors that are used as vertically stacked receptacle connectors, and more particularly, to connectors utilizing insert wafers that incorporate differential signal terminals which are positioned alongside each other where they appear in the connector receptacle portions and which are turned at their tail portions for joining to a printed circuit board.

Electrical connectors are well known to those of ordinary skill in the electronic arts as generally reliable devices by which electrical signal paths can be extended into and obtained from a printed circuit board. Over the last several years, however, electronic devices and systems have gotten both smaller and faster, making reliable connectors more difficult to design, manufacture and install onto printed circuit boards.

In a connector used in high-speed applications, crosstalk that is likely to occur between closely spaced, high-speed signal paths can be reduced by using differential-voltage signals. A differential signal pair is a pair of terminals or other conductors that together carry a signal but neither of the two conductors is at ground or reference potential. Rather, the voltage on one conductor of a differential pair is, at any given instant, the same magnitude, but opposite polarity as the voltage on the other conductor. A differential pair therefore is analogous to a transmission line, the conductors of which are capacitively and inductively coupled to each other. Crosstalk between two or more differential signal pairs as well as interference of one differential pair on another can be significantly reduced if a good ground plane (or other fixed-voltage reference plane) is provided between the conductors of one differential pair and the conductors of another differential pair as a sort of shield between them.

Each differential signal pair requires at least two capacitively coupled conductors, and it is important for a connector that links a differential signal pair between devices or circuit boards to maintain capacitive coupling. When a connector is used to provide an edge connection for a circuit board or is used as a plug connector, arranging differential signal pairs in a connector so that they are alongside each other and next to each other on the same side of a circuit board can cause the connector width to increase, but when the connector is installed onto a circuit board, connector width should be minimized.

SUMMARY OF THE INVENTION

It is therefore a general object of the present invention to provide a circuit board connector which provides one or more

receptacle connector, each of which will accept the edge connector of a circuit board or like device.

Another object of the present invention is to provide a stacked receptacle connector, each receptacle of which will accommodate differential signal pairs.

Yet another object of the present invention is to provide a stacked receptacle connector that enables differential signal pairs to be installed into a connector body using individual inserts in the form of wafers, each of which is relatively easy to manufacture and each of which also allows ground planes to be provided between each wafer insert in an encompassing connector housing.

Another object of the present invention is to provide a connector for use in high speed applications, the connector including an insulative housing with a hollow interior cavity, the cavity accommodating a plurality of terminal signal and ground terminal inserts in the form of thin wafers, each wafer supporting a plurality of conductive terminals, the terminals having contact portions, tail portions and body portions interconnecting the contact and tail portions together, the signal terminals being disposed so that most of the terminals are oriented with their wider sides arranged vertically for broadside capacitive coupling to adjacent corresponding terminals in adjacent wafers, and a small part of the signal terminal body and tail portions being bent and offset about 90 degrees so that the signal terminals are arranged in an edge-to-edge arrangement at the terminal tail portions.

Still another object of the present invention is to provide a connector for use with high speed differential signal applications in which terminals are held in assemblies that preferably take the form of insulative wafers, two wafers with conductive signal terminal being assembled together to form a signal terminal wafer assembly and two wafers that contain conductive ground terminals being arranged on opposite sides of the signal terminal assembly to provide reference ground terminal arrangements that flank the signal terminal assembly, the signal terminals having contact portion that are arranged in side-by-side order and termination portions that are arranged in edge-to-edge order.

A still further object of the present invention is to provide a unique circuit board layout for accommodating the tail portions of connectors of the structure described above, which circuit board layout facilities the high speed operation of connectors of the invention.

Yet another object of the present invention is to provide a circuit board with a particular arrangement of traces that enhance the high speed transmission abilities of the connectors of the invention, the circuit board having a plurality of conductive traces extending to mounting through holes disposed in a circuit board, the through holes being arranged in a pattern such that a plurality of ground traces encompass a pair of differential signal traces, and in which the ground traces are arranged at the corners of a four-sided figure, with the differential signal through holes arranged in line within a perimeter defined by the ground through holes.

These and other objects of the present invention are accomplished by way of the structure of the invention. A connector is provided with an insulative housing that has two or more receptacle portions, each of which is capable of accepting a card edge of other similar blade portion of an opposing electronic device, such as an electronic or opto-electronic module. The receptacle connectors of the invention include a plurality of pairs of differential signal terminals, and the terminals have a unique structure which permits them be broadside coupled in pairs along one extent of the connector, and subsequently edge coupled along a remaining extent of the connector.

Multiple inserts are provided which carry terminal that are intended to be designated as carrying differential signals. In this regard, multiple differential signal terminal pairs are supported in an insulative wafer that may be inserted into the connector housing. The signal terminal insert is preferably formed from two interengaging halves, and the terminals of each differential signal pair are spaced apart from each other in a parallel fashion. This is carried on from the terminal contact portions rearwardly in the terminal body portions to a location near the tail portions of the terminals.

The differential signal terminals conductors have their paths rotated in their supporting insert wafer so that they turn about 90 degrees near where the terminal body portions end and this turn extends into the terminal tail portions. Thus, the signal terminals are arranged in a line and are spaced apart along that line in an edge-to-edge arrangement. In this fashion, the terminals may engage in edge coupling along their tail portions and broadside coupling along their contact and body portions.

The halves of the signal terminal wafer inserts have serrated-style bases on which are formed alternating projections and recesses, with the projections of the first of the two insert wafer halves being received within the recesses of the second of the two signal insert wafer halves and vice-versa. In this manner the terminal tails portions are easily arranged in a line in the edge-to-edge fashion stated above.

Additional insert wafers are provided and are arranged in spaces provided between the signal terminal assemblies and these act as ground planes between adjoining signal terminal insert wafers to isolate signals carried through the signal wafers. The heights of the signal and ground terminal insert wafers are different so as to polarize the insert wafers and the connector housing so that ground terminal insert wafers cannot be inserted into a portion of the connector housing that is dedicated to receive a ground terminal insert wafer. Likewise, the connector housing is formed with different wafer-receiving slots, so that a ground wafer slot is capable of receiving only a ground terminal wafer and a signal terminal slot is capable of receiving only a signal terminal wafer assembly.

These and other objects, features and advantages of the present invention will be clearly understood through a consideration of the following detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

In the course of this description, references will be made to the drawings, in which:

FIG. **1** is a perspective view of a connector that is constructed in accordance with the principles of the present invention;

FIG. **2** is a perspective view of the connector of FIG. **1**, taken from the rear thereof, with all but three insert wafers removed from the interior of the connector for clarity;

FIG. **3** is a sectional view of the connector of FIG. **1**, taken from the rear and illustrating four ground terminal insert wafers in place within the interior of the connector housing;

FIG. **4** is the same sectional view as FIG. **3**, but illustrating three signal terminal insert wafers in place within the interior of the connector housing;

FIG. **5** is the same view as FIG. **4**, but illustrating one of the three signal terminal inserts partially in place in the connector housing between two adjoining ground terminal wafer inserts and illustrating two signal terminal insert wafers aligned with their respective openings in the connector housing;

FIG. **6** is the same view as FIG. **3**, with the ground terminal insert wafers removed to illustrate the interior of the connector housing;

FIG. **7** is a perspective view of a set of terminals used in a signal terminal insert wafer used in the connector of FIG. **1**;

FIG. **7**A is a perspective view of a set of terminals used in a ground terminal insert wafer used in the connector of FIG. **1**;

FIG. **8** is a perspective view of two sets of signal terminals with insulative body portions molded thereover, and facing in opposition to each other for subsequent assembly;

FIG. **9**A is the same view as FIG. **8**, but illustrating the two signal terminal insert wafer halves assembled together to form a single signal terminal insert wafer;

FIG. **9**B is the same view as FIG. **9**A but taken along the bottom of the signal terminal insert wafer to illustrate the alignment of the signal terminal tails along the bottom edges of the signal terminal insert wafer;

FIG. **10**A is a perspective view of the signal terminal wafer insert of FIG. **9** flanked by two ground terminal insert wafers;

FIG. **10**B is a perspective of all of the three (ground-signal-ground) insert wafers of FIG. **10**B assembled together to form a single signal transmission unit;

FIG. **10**C is a bottom plan view of the single signal terminal wafer insert of FIG. **10**A illustrating the orientation and layout of the tail portions of the terminals of the signal and ground terminal insert wafers;

FIG. **11** is a top plan view of a circuit board layout used in conjunction with the connectors of FIG. **1**;

FIG. **12** is an enlarged detail view of a portion of FIG. **11**, illustrating the use of an anti-pad style opening in a ground plane layer of the circuit board of FIG. **11**;

FIG. **13** is an enlarged detail view of a portion of the circuit board of FIG. **11**, illustrating another ground plane layer and signal trace route out construction suitable for use with connectors of the present invention.

FIG. **14** is a perspective view of an alternate embodiment of a connector constructed in accordance with the principles of the present invention, but having only a single card-receiving, or mating slot for mating with an opposing connector;

FIG. **15** is a view of the connector of FIG.**14**, taken from the rear;

FIG. **16** is the same view as FIG. **15**, but with the connector and its terminal assemblies removed from the circuit board and with a signal terminal assembly sown partially removed from the connector for clarity;

FIG. **17** is a perspective view of a signal terminal assembly used in the connector of FIG. **14**;

FIG. **18** is the same view as FIG. **17**, but with the signal terminal assembly halves removed for clarity; and,

FIG. **19** is a view of the terminal used in one of the signal terminal assembly halves of FIG. **17**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to FIG. **1**, there is shown a perspective view of a connector **10** that is constructed in accordance with the principles of the present invention. The connector **10** has a top surface **12**, a front face **14**, a bottom surface **16** and left and right side surfaces, or faces, **18** and **20**. As can be seen in FIG. **1**, the connector **10** front face has two receptacle portions **17** and **19** disposed thereon into which a circuit board, device or blade connector may be inserted and by which electrical signals can be carried to or extended from a circuit board **13** to which the base connector **10** is attached. The connector **10** of the present invention is a compressible attachment-style connector, meaning that it is attached to a circuit board by means of through hole pins, that as explained below, are shown in the embodiment depicted as compliant pins.

The connector also has a rear face **20**, which is shown more clearly in FIG. **2**, which is a perspective view of the connector **10** of FIG. **1**, but taken from the rear thereof and looking into at the rear face **22** of the connector and into the hollow interior cavity **25** of the connector **10**. At the left-hand side of the rear face **22** of the connector housing, there are shown three separate insert wafers, two of which are identified by reference numeral **24**, the other of which is identified by reference numeral **26**. As described more fully below, the insert wafers are of two types: a ground insert wafer **24** and a signal insert wafer **26** and the type is based upon the type of signals that are carried by the conductive terminals in each of the insert wafers. A signal insert wafer is intended to carry multiple signal signals, and particularly, pairs of differential signals. A ground insert wafer is intended to be connected to one or more ground planes on the circuit board and its terminals will carry ground signals as opposed to differential signals.

In the preferred embodiment of the connector **10** illustrated, each signal insert wafer **26** is installed between two ground insert wafers **24** as shown in FIG. **2**. In this manner, the differential signal terminals of each pair may be maintained and directed within the insert wafer **26**, but they are flanked by ground terminals that provide close ground paths that somewhat surround the signal pairs. This structure assists in providing maximum shielding of the signal insert wafer **26** and results in a reduction of EMI and signal cross talk and skew with or by other signal insert wafers that are present in the connector **10**.

FIG. **3** is a sectional view of the connector **10** of FIG. **1**, taken from the rear **22** of the connector **10** and illustrating four ground terminal insert wafers **24** installed within the interior of the connector housing and three signal-receiving slots interposed between the ground terminal insert wafers. FIG. **4**, illustrates the same view with the signal terminal insert wafers **26** inserted in place. As can be seen in FIG. **3**, each of the ground insert wafers **24** have compliant signal tail pins **45** that project from the bottom edge **47** of each ground insert wafer **24** and are co-linear along a longitudinal axis of the signal insert wafer. FIG. **4** is the same view of the rear face **22** of connector **10** as shown in FIG. **3**, but with three signal wafer inserts **26** installed into the connector **10**. Like the ground wafer inserts **24**, the signal insert wafers **26** also have compliant pin tails **44** that project from the bottom edge **47** of each signal insert wafer **24** along the same line and are also co-linear.

FIG. **5** is the same view as FIG. **4**, but it illustrates one of the three signal terminal insert wafers **26** partially in place in the connector **10** between two adjoining (or flanking) ground terminal insert wafers **24**. The signal insert wafers **26** and the ground insert wafers **24** have different heights so that they can be easily matched into their corresponding proper positions within the interior cavity **25** of the connector housing **10**. By making the signal wafer inserts **26** of one height and the ground insert wafers **24** a different height, and making the signal insert wafer slot and ground insert wafer slots of the connector **10** to be of similar corresponding heights, the possibility of incorrectly installing a ground insert wafer **24** (taller) into a signal insert wafer slot or of installing a signal terminal insert wafer into a position that is designated for a ground terminal insert wafer is eliminated. This speeds up assembly and repair of the connectors of the invention. The ground terminal insert wafers are fit into slots **100** (FIG. **3**) that are formed along at least one surface of the interior cavity **25** of the connector housing **10**, while the signal terminal insert wafers fit against the intervening land portions **101** that are arranged between the slots **100**. The heights of the signal and ground insert wafers may reversed, if desired, that is the signal insert wafers can be made taller than the ground insert wafers and the housing modified to accommodate this arrangement.

FIG. **6** is the same view as FIG. **3**, with the ground terminal insert wafers **24** removed for clarity in order to illustrate the interior cavity **25** of the connector **10** housing and clearly showing a insert wafer retention and alignment rib **27** that is formed as part of the connector **10** housing and which runs horizontally between the stacked receptacles **17** and **19** (FIG. **1**) into which a circuit board, device or connector can be inserted. This rib **27** is sized and structured so that the retention clip **29** that is formed as part of each insert wafer **24** and **26** engages the alignment rib **27** and holds the insert wafers **24** and **26** in the connector **10** as plug connectors (not shown) are inserted into and removed from the connector housing **10**. Additionally, the connector housing **10**, may, on opposite sides of the alignment rib **27**, include a plurality of secondary slots **102**, each of which receives edges of the retention clips **29** of the signal and the ground insert wafers **24**, **26**. The terminals, as explained below, may include retention barbs **104** that engage the inner surfaces of terminal-receiving cavities **105** of the connector housing **10**.

As set forth above, the use of differential signals on a circuit board or other device requires two conductors to carry one differential signal with each conductor carrying an equal but opposite polarity signal as its mate. When the stacked receptacles **17** and **19** are both used to provide differential signal connectors, the pairs of side-by-side differential signal conductors in each receptacle **17** and **19** need to be connected to a mating contact on a circuit board **13** to which the connector **10** is attached. Therefore, in order to accommodate the attachment of many differential signal pairs from the top receptacle **19** and those required of the bottom receptacle **17** in the width of the connector **10**, the differential signal pairs provided to each receptacle **17** and **19** needs to be "rotated" or somehow made offset so that the differential signal connections from the connector **10** to the circuit board **13** are aligned "front-to-back" or "edge-to-edge" as shown in FIG. **10**C, where the connector **10** meets a circuit board **13** instead of "side-to-side" where a circuit board would be inserted into one of the receptacles **17** and **19** and the terminals contact an opposing element, such as a circuit card edge.

FIG. **7** is a perspective view of a set of signal terminals **261**, **281** that are used in a signal terminal insert wafer **24** of the connectors of the present invention. FIG. **7** also shows the relative position of the aforementioned retention clip **29**. Because the sets of signal terminals **261** and **281** are identical except for their relative sizes, for brevity, only the top set of signal terminals **261** is described hereinafter. The signal terminal set **261** and **281** is comprised of a top or outside conductor **261**A and a lower or inside conductor **261**B. In one embodiment, conductive terminals **261**A, **261**B can be configured to be a differential signal pair. However, as is seen best in FIG. **8**, terminal **261**A is one terminal of one differential signal pair and terminal **261**B is one terminal of a second and distinct differential signal pair. These terminals have corresponding differential signal terminals **54** which cooperatively define the differential signal terminal pair.

Still referring to FIG. **7**, it can be seen that the terminals **261**A and **261**B each have a first, or contact, portion **30** which are mirror images of each other. Together, they form a contact beam pair that will slide over the edge of a plug connector mating blade (typically a circuit card) when it is inserted into one of the receptacles **17** and **19**. With respect to terminal **261**A, it includes a horizontal portion **34** that extends forward from a first point **32** away from an edge of the insulative wafer half into which it is molded. As can be seen in FIG. **8**, the first

point **32** is actually just beyond the front edge **49** of the first wafer half into which the terminals **261** and **281** are installed. The terminal **261**A horizontal portion **34** extends "inwardly" to a second point **36** where the terminal **261**A turns downwardly toward the bottom edge **47** of the signal insert wafer **26**. The vertical portion **38** extends downwardly to a third point **40** whereat the terminal is formed into an "offset" **42** that travels inwardly as shown (toward the viewer in FIG. **7**) in order to ensure that the tail portions are aligned along a line of action at the bottom of the signal terminal insert wafer. The compliant pin tails **44** extend from the bottom of the offset **42** and can be inserted into a circuit board through hole.

FIG. **7**A depicts a ground terminal for use in the aforementioned ground insert wafers. As can be seen, the ground terminal includes compliant tail pins **45** that are electrically and mechanically connected together as a single unit. The ground terminal set shown in FIG. **7**A extend from the tail pins **45** to where it would exit receptacle slots **17** and **19**. The ground terminal shown in FIG. **7**A provides an isolating ground plane between signal wafer inserts installed into the connector **10**.

FIG. **8** is a perspective view of the two halves that make up a signal wafer insert and in particular, a perspective view of two sets of signal terminals **261**, **281** with the insulative body portions of the insert wafer molded over the terminals (shown in FIG. **7**). As shown in the figure, the signal insert wafer **24** is comprised of a left half **50** and a right half **52**. With respect now to just the left half **50**, it can be seen that the terminals **26** and **28** have portions that extend beyond the front edge **49** of the wafer half to form the aforementioned clip and extend parallel to the bottom edge **47** and the top edge **51** toward the rear edge **53**. Near the rear edge **53**, the terminals turn downwardly toward the rear edge **47** and exit as the aforementioned compliant tails **44**. The signal terminal tail portions of the two wafer halves extend toward each other near the tail portions so that they may arrive at the in-line tail arrangement that is present at the bottom of the signal insert wafer.

Just above the bottom edge **47** of the left half **50** of the signal insert wafer **24** there are a series of notches **55** and teeth **57** (or "valleys" and "peaks") that run most of the length of the bottom edge **47**. In particular, however, a notch **55** is formed immediately in front of the rear edge **53** of the left half of the signal insert wafer. On the right half **52** of the signal wafer's **24** bottom edge **47**, a tooth **59** is formed that is immediately in front of the rear edge **53** of the right half **52** such that the tooth **59** on the right-hand half **52** of the insert wafer **24** will engage the notch **55** that is immediately in front of the rear edge **53** of the left half **50**. When the left and right halves **50** and **52** are joined together, the notches **55** and teeth **57** of the left half **52** engage the teeth **59** and notches **61** of the right half **52** in a sort of "sawtooth" engagement of each half to the other. This sawtooth, or serrated, arrangement permits the tail portions of the signal terminals to come out of plane and be aligned linearly along the bottom edge of the signal terminal insert wafer.

It can be seen in FIG. **8** that the signal insert wafer **24** includes a left half **50** and a right half **52**. The left half **52** includes a relatively flat or planar insulative body **63** that is, of course, made of a non-conductive material. The right half **52** is also comprised of a relatively flat or planar insulative body **65** that is sized and shaped to mate with the left body **63**. Both the spacer body **63** and the right body **65** have a "front" edge identified by reference numeral **49**. Both bodies have a "bottom" edge **47** as well as a "top" edge **51**. The rear edge **53** is considered to be "opposed" to the front edge **49**; the top edge **51** is considered to be opposite the bottom edge **47**.

The terminals depicted in FIG. **7** run through each of the left half **50** and the right half **52** and are identical except for one small but very important aspect. FIG. **9**A is the same view as FIG. **8**, but illustrates the two signal terminal wafer insert halves **50** and **52** assembled together to form a single signal terminal insert wafer **24**. As can be seen in FIG. **9**A, the compliant pin tails **44** that extend downwardly from the bottom edge **47** are co-linear because they lie in the same plane (not shown). Stated alternatively, the side-by-side positions of differential terminals **62** and **54** at the front edge **49** of the signal insert wafer **24** become front-to-back positions **62** and **54** when these same terminals exit the signal insert wafer **24** from its bottom edge **47**. The re-arrangement of the differential terminals is enabled by different and opposing offsets **42** in the left and right halves **50** and **52** of a signal insert wafer.

In FIG. **7** and FIG. **8**, the first signal terminals **261**A and **261**B are fixed into the planar left-side spacer body **63** such that they each have a horizontal portion **34** that extends to a vertical portion **38**. Both terminals **261**A and **261**B are substantially co-planar, meaning that they lie in a first plane and are adjacent to each other. The vertical portions **38** of each terminal **261**A and **261**B run to an offset section or segment **42**, which in the left side body **63** extends the terminals **261**A and **261**B upwardly from the plane in which they both lie, to a second plane that is parallel to but elevated from first plane in which the terminals **261**A and **261**B both lie. Both offsets **42** continue downwardly past the bottom edge **47** of the left side body **63** at where they become the compliant pin tail portions **44** of the terminal set.

In the right half **52** of the signal insert wafer **24**, there are terminals identical to terminals **261**A and **261**B except that in the right signal wafer half **52**, they lie in a third plane, which is parallel to and displaced or offset from the first plane in which terminals **261**A and **261**B lie and the second plane in which the pin tails lie. There are offsets in the right half, which are not shown, that extend the terminals in the third plane to the aforementioned second plane such that the pin tails **44** that extend from the bottom edge **47** of the right half **52** will be co-planar with the pin tails **44** that extend from the left half **50** when the two halves are assembled together. The halves **50**, **52** of the signal insert wafer may be assembled together with posts and holes as shown in FIG. **8** and they may be further connected such as a heat or ultrasonic welding.

In claim parlance, the signal terminals in the right side body **65** have a second offset that extends the terminals away from the third plane in a second direction to the aforementioned second plane from which they extend downwardly past the bottom edge of the wafer insert body. The extensions of the left side terminals and right side terminals are laterally displaced from each other, i.e., they are spaced apart from each other as shown in FIG. **9**A.

FIG. **9**B is the same view as FIG. **9**A but taken along the bottom of the signal terminal insert wafer **26** to illustrate the edge-to-edge alignment of the signal terminal tails **44** along the bottom edge **47** of the signal terminal insert wafer **24** halves **50** and **52**. FIG. **10**A is a perspective view of the signal terminal insert wafer **26** of FIG. **9** flanked by two ground terminal insert wafers **24**. As stated above, the ground terminal insert wafers **24** provide isolation for the signal insert wafers **26**. FIG. **10**B is a perspective of all of the three insert wafers **24** and **26** assembled together to form a single signal transmission unit **70**. As can be seen in the figure, the compliant pin tails **45** of the ground terminal insert wafer are co-planar and therefore lie alone the same line. Similarly for the compliant pin tails **44** of the signal insert wafer **25**, they are co-planar when they exit the bottom edge and lie along the same line.

FIG. **10**C is a bottom plan view of the single signal transmission unit **70**. As can be seen in this figure, each signal

terminal **44** forms the apex of a triangle, the other corners of which are two ground terminals **45**. Signal "leakage" from any one of the signal pin tails **44** is minimized because of the relatively close proximity of ground terminals **45** to which signals from the signal pin tails are capacitively shunted. Additionally, each differential signal pair "DSP" lies within a geometric figure that is formed by interconnecting the four ground terminals **45** by imaginary lines. This is illustrated in the inset to the right of FIG. **10**C. The geometric figure in the embodiments shown approximate a square or a rectangle and other figures may be used in their place, preferably four-sided figures. FIG. **10**C also explains the order of the terminals relative to the differential signal contact portions shown in FIG. **9**A. As shown, the tail portions are fully transitioned from the side-by-side arrangement in the contact portions thereof, where broadside capacitive coupling occurs, to and edge-to-edge arrangement in the tail portions where the terminals are connected to a circuit board.

FIGS. **14-19** show an alternate embodiment of the a connector **300** constructed in accordance with principles of the present invention, which utilizes a housing **302** with only one receptacle slot **304**. The housing **302** has a plurality of walls and the receptacle slot **304** is defined in the front wall **306**. Posts **307** that receive mounting screws are show sectioned in this embodiment which are used to mount the connector **300** to a circuit board **13**. As shown in FIG. **15**, the rear of the connector **300** includes a hollow cavity **309** that accommodates terminal inserts **310**. Similar to the embodiments explained above, the cavity **309** has a series of slots **312**, **313** of different heights, with the slot **312** really being a land as previously described. The difference in heights of the slots **312**, **313** matches the difference in height of the signal and ground insert wafers. The cavity also includes a retention rib **314** which the terminal insert wafers engage with retention clips.

FIG. **16** illustrates the connector **300** with one of the signal terminal insert wafers **320** partially removed from the cavity **309**, and the ground terminal insert wafer **322** left in place in the cavity. FIG. **17** illustrates the signal terminal insert wafer **320** as removed from the connector **300**. It can be seen that it includes two pairs of terminals **325**, **326** which are aligned with each other broadside, or widthwise, as shown in the other embodiments and with respect to the connector receptacle slot **304**. These terminal pairs have contact portions **325**A, **326**A, body portions **325**B, **326**B and tail portions **325**C, **326**C. The tail portions **325**C and **326**C are aligned lengthwise, or edge-to-edge with respect to each other. Whereas the contact portions **325**A, **3256**A are aligned horizontally along a line of action A-A shown in FIG. **17**, the tails portions **325**C, **326**C are aligned along a lengthwise line of action B-B as shown in FIG. **17**, which is offset from line of action A-A, and preferably at an angle of 90 degrees thereto, hence the reason why we refer to the tail portions being 90 degrees offset from the contact portions.

As shown in FIG. **18**, the signal terminal insert wafer **320** is formed from two engaging halves **320**A and **320**B. FIG. **19** illustrates one set of the terminals that make of the terminal pairs in FIG. **17**.

FIG. **11** is a top plan view of a circuit board layout used in conjunction with the connectors of FIG. **1**. As can be seen in FIG. **11**, each through hole for a signal pin is closely bounded by at least two ground leads or through holes that are intended to receive ground pins therein. That the closest pins to a signal lead are ground pins tends to shunt signals from a signal pin to ground potential thus reducing the likelihood that a signal on one set of differential pairs will be coupled to another differential signal pair. This circuit board arrangement minimizes cross talk between differential signal pairs in that at the circuit board level, there are four ground terminals extending into the circuit board that encompass each differential signal pair. Additionally, the ground terminals of the connectors of the invention are commoned together near the circuit board level and this commoning bar also provide a short path from a differential signal terminal to the nearest reference ground terminal set. Each differential signal tail portion hole is at the apex of an imaginary triangle in which the other two apices are formed by intersecting lines drawn through the two closest ground terminal tail portion holes. This arrangement is shown to the left of FIG. **11**, where "S+" represents a positive differential signal through hole of a signal pair and "S−" represents a negative differential signal through hole of that signal pair and "G" represents ground signal through holes of the circuit board.

FIG. **12** is an enlarged detail view of a portion of FIG. **1**, illustrating the use of an anti-pad style opening in a ground plane layer of the circuit board **110** of FIG. **11**. This is a top plane view and it illustrates signal through holes, or vias **113** and ground through holes, or vias **112**. The signal vias are arranged in line with each other along an axis L**1**. Two of the signal vias **113** are closely spaced to each other to form a pair of differential signal vias **114** and so accommodate the tail portions of the signal terminal insert wafer. The remaining vias **112** are connected tot he ground plane **111** and these vias are also arranged in rows that flank the signal via pairs. An anti-pad **116**, may be included and this "anti-pad" refers to an area in which the conductive material that forms the ground plane **11** has been removed. Remaining in these open areas are annular conductive rings **115**. The openings shown in FIG. **12** are five-sided and take a polygonal shape, and are oriented as illustrated so that one line of ground vias (that shown above the top row of signal vias in FIG. **12**) is proximate to the sharp corners (90 degrees) of the openings **116**, while the other and opposite line of ground vias, those shown below the top row of signal vias in FIG. **12** are spaced further away from the angled edges of the openings **116**. If the anti-pad structure of the circuit board were square, rather than a pentagon, the ground vias would be located proximate the corners of the anti-pad. These ground vias may be considered as defining an imaginary four-sided figure, the perimeter of which encloses the anti-pad structures.

FIG. **13** is an enlarged detail view of a portion of the circuit board of FIG. **11**, illustrating another ground plane layer and signal trace route out construction suitable for use with connectors of the present invention. In this arrangement, the pentagon-like opening **116** has been spilt into two openings, **116**a, each of which encompasses a single signal via **113** of a pair **114** of differential signal vias **113**. The two openings **116**a are spilt by a thin extension strip **120** of the ground plane that cuts across, and preferably bisects, the opening **116** into two substantially equal openings **116**a.

The circuit traces that exit the signal vias **113** are shown in phantom in FIG. **13**. They include flag portions or the like **121** that extend toward each other from the vias **113**. Those flag portions are joined to first strip portions **122** that run in a circuit board layer underneath (or above) the ground plane layer **111**. These first portions, as shown, extend beneath the center bisecting trip **120** and they are preferably aligned with the strip **120** so that the outer edges of the first portions **122** align themselves with the outer edges of the strip **120** (or the inner edges of the two openings **116**a on opposite sides of the strip **120**. Second conductive portions **123** are shown joined to the first portions **122** and are shown extending at an angle thereto. Third and fourth portions **124**, **125** are also joined to the second and third portions, respectively, at angles so that

the circuit traces tend to follow the outer configuration of the opening **116**a on the left of the strip **120** in FIG. **13**. This is to give these circuit traces a ground plane or strip of particular configuration to couple with.

While the preferred embodiments of the invention have been shown and described, it will be appreciated by those skilled in the art that changes and modifications may be made to these embodiments without departing from the spirit of the invention, the scope of which is defined by the appended claims.

What is claimed is:

1. A circuit board for use with a connector carrying differential signals, comprising:

a substrate, the substrate including a plurality of openings formed therein, the openings including plated portions so as to make electrical contact with conductive terminal tail portions inserted therein, the openings being divided into first and second groups of openings, the first group of openings receiving differential signal terminal tails therein when a connector is mounted to said circuit board and the second group of openings receiving ground terminal tails therein when a connector is mounted to said circuit board;

the first group of openings having a plurality of first opening and the second of group of openings having a plurality of second opening,

each *of said* first opening having a pair of *said* second openings associated therewith, the first opening and said associated second opening pair being arranged at apexes of an imaginary triangle, two of said first openings being spaced apart from each other and aligned with each other such that said two first openings are contained within a perimeter defined by imaginary lines intersecting said two pairs of associated second openings.

2. The circuit board of claim **1**, wherein said two pairs of associated second openings are arranged to define a four-sided figure.

3. The circuit board of claim **1**, wherein said substrate includes a conductive layer having at least one opening therein devoid of conductive material, the conductive layer opening encompassing said two first openings.

4. The circuit board of claim **3**, wherein said conductive layer opening encompasses said two first openings and said two pairs of associated second openings define an imaginary perimeter that encompasses said conductive layer opening.

5. The circuit board of claim **4**, wherein said conductive layer opening is a five-sided figure.

6. The circuit board of claim **4**, wherein said conductive layer opening is divided into two separate conductive layer sub-openings by a thin conductive strip which bisects said conductive layer opening and which extends between said two first openings.

7. A circuit board for use with a connector carrying differential signals, comprising:

a substrate, the substrate including a plurality of vias formed therein, the vias including plated portions so as to make electrical contact with a conductive terminal tail portion inserted therein, said vias being divided into first and second groups of vias, the first group of vias receiving differential signal terminal tails therein when a connector is mounted to said circuit board and the second group of vias receiving ground terminal tails therein when a connector is mounted to said circuit board;

said first group of vias being arranged in a first line of vias and said second group of vias being arranged in second and third lines of vias, the second and third lines of vias being disposed on opposite side of said first line of vias;

the first group of vias having a plurality of first via and the second of group of vias having a plurality of second via, and,

each of said first vias having a pair of *said* second vias associated therewith, such that pairs of said first vias disposed in said first line of vias are contained within a perimeter defined by imaginary lines intersecting said two pairs of associated second vias disposed in said second and third lines of vias.

8. The circuit board of claims **7**, wherein said each of first vias and said associated pair of second vias therewith are arranged at apexes of an imaginary triangle.

9. The circuit board of claim **7**, wherein said imaginary lines intersecting said two pairs of associated second vias define a four-sided figure.

10. The circuit board of claim **7**, wherein said substrate includes a conductive layer having at least one opening therein devoid of conductive material, the conductive layer opening encompassing a pair of said first vias.

11. The circuit board of claim **10**, wherein said conductive layer opening encompasses the pair of first vias and said two pairs of associated second vias define an imaginary perimeter that encompasses said conductive layer opening.

12. The circuit board of claim **11**, wherein said conductive layer opening is a five-sided figure.

13. The circuit board of claim **11**, wherein said conductive layer opening is divided into two separate conductive layer sub-openings by a thin conductive strip which bisects said conductive layer opening and which extends between each via of said pair of first vias.

14. A circuit board for use with a connector carrying differential signals, comprising:

a substrate, the substrate including a plurality of openings formed therein, the openings including plated portions so as to make electrical contact with conductive terminal tail portions inserted therein, the openings being divided into first and second groups of openings, the first group of openings receiving differential signal terminal tails therein when a connector is mounted to the circuit board and the second group of openings receiving ground terminal tails therein when a connector is mounted to the circuit board;

the first group of openings having a plurality of first opening and the second of group of openings having a plurality of second opening, and

each *of said* first opening having a pair of *said* second openings associated therewith, the first opening and the associated second opening pair being arranged at apexes of an imaginary triangle, two of the first openings being spaced apart from each other and aligned with each other such that the two first openings are contained within a perimeter defined by imaginary lines intersecting the two pairs of associated second openings, wherein the substrate including a conductive layer having at least one opening therein devoid of conductive material, the conductive layer opening encompassing the two first openings.

15. The circuit board of claim **14**, wherein the two pairs of associated second openings are arranged to define a four-sided figure.

16. The circuit board of claim **14**, wherein the conductive layer opening encompasses the two first openings and the two pairs of associated second openings define an imaginary perimeter that encompasses the conductive layer opening.

17. The circuit board of claim **16**, wherein the conductive layer opening is a five-sided figure.

18. The circuit board of claim **14**, wherein the conductive layer opening is divided into two separate conductive layer sub-openings by a thin conductive strip which bisects the conductive layer opening and which extends between the two first openings.

19. The circuit board of claim **14**, wherein the conductive layer opening is divided into two separate conductive layer sub-openings by a thin conductive strip which bisects the conductive layer opening and which extends between each via of the pair of first vias.

* * * * *