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(54) **SEMICONDUCTOR LIGHT EMITTING DEVICE**

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**Related U.S. Patent Documents**

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Filed: **Mar. 10, 2006**

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**H01L 33/00** (2010.01)

(52) **U.S. Cl.** ..... 257/94; 257/617

(58) **Field of Classification Search** ..... 257/11,  
257/13, 23, 79-97, 103, E33.001, 617

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,984,242	A	1/1991	Scifres et al.
5,019,874	A	5/1991	Inoue et al.
5,153,889	A	10/1992	Sugawara et al.
5,164,798	A	11/1992	Huang
5,233,204	A	8/1993	Fletcher et al.
7,038,243	B1 *	5/2006	Kamakura ..... 257/94
7,432,535	B2 *	10/2008	Kamakura ..... 257/94

FOREIGN PATENT DOCUMENTS

JP	1-243482	9/1989
JP	4-296075	10/1992
JP	6-61525	3/1994

OTHER PUBLICATIONS

Journal of Electronic Materials, vol. 20, No. 12, 1991, The Growth and Properties of High Performance AlGaInP Emitters Using a Lattice Mismatched GaP Window Layer, pp. 1125-1130, R.M. Fletcher, C.P. Kuo, T.D. Osentowski, K.H. Huang and M.G. Craford.

\* cited by examiner

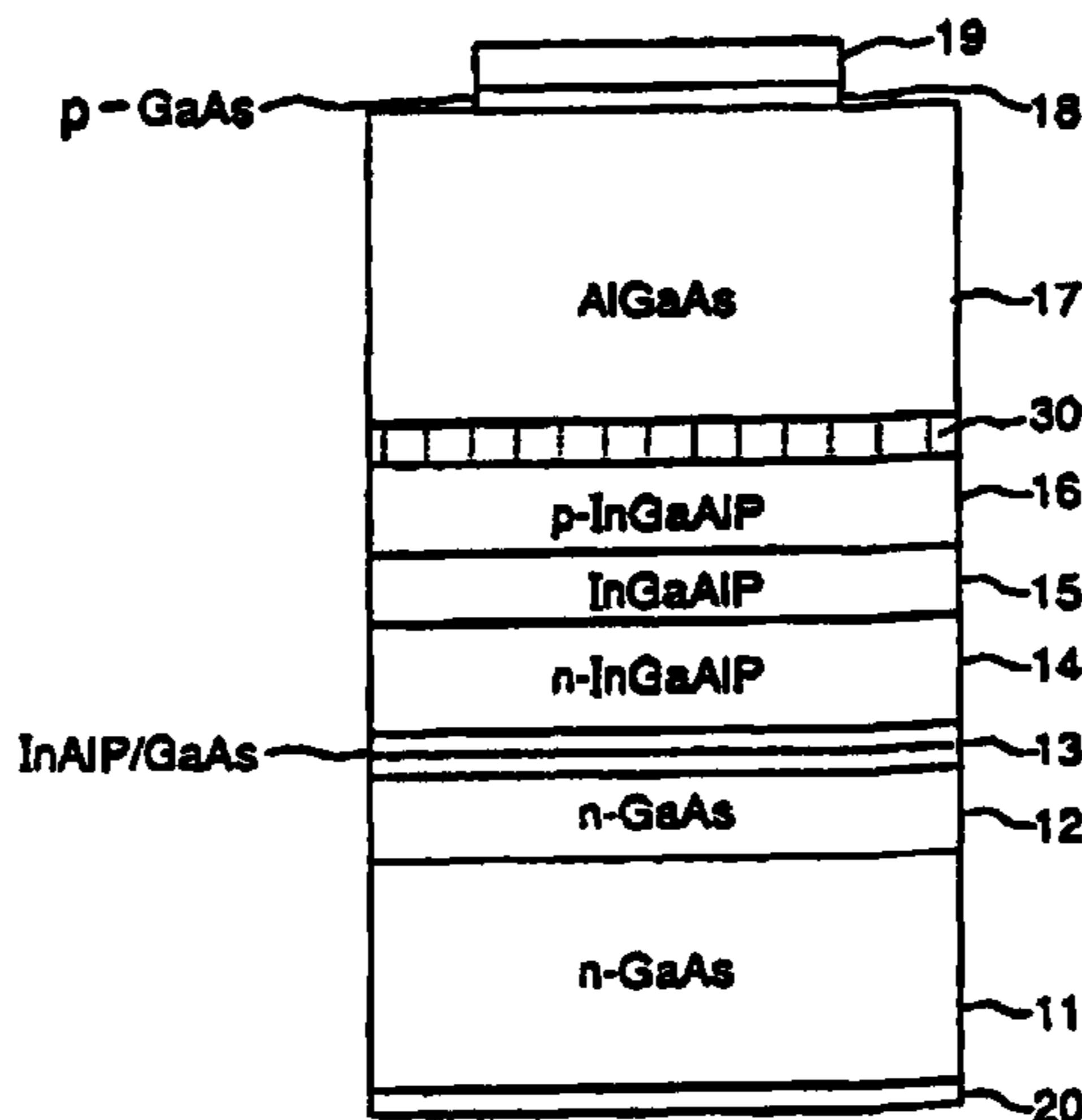
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(57) **ABSTRACT**

A semiconductor light emitting device includes a hetero-configuration having an active layer, a first clad layer, and a second clad layer, the active layer being interposed between the clad layers. The active layer emits light when charge carriers are injected. The first and second clad layers keep the injected charge carriers in the active layer. The hetero-configuration is interposed between a first and a second electrode. The semiconductor light emitting device further includes a dense defect-injected layer. This layer is provided between the first electrode and the hetero-configuration. The dense defect-injected layer is made of material more fragile than the hetero-configuration. The dense defect-injected layer prevents defects injected into the hetero-configuration.

**76 Claims, 4 Drawing Sheets**



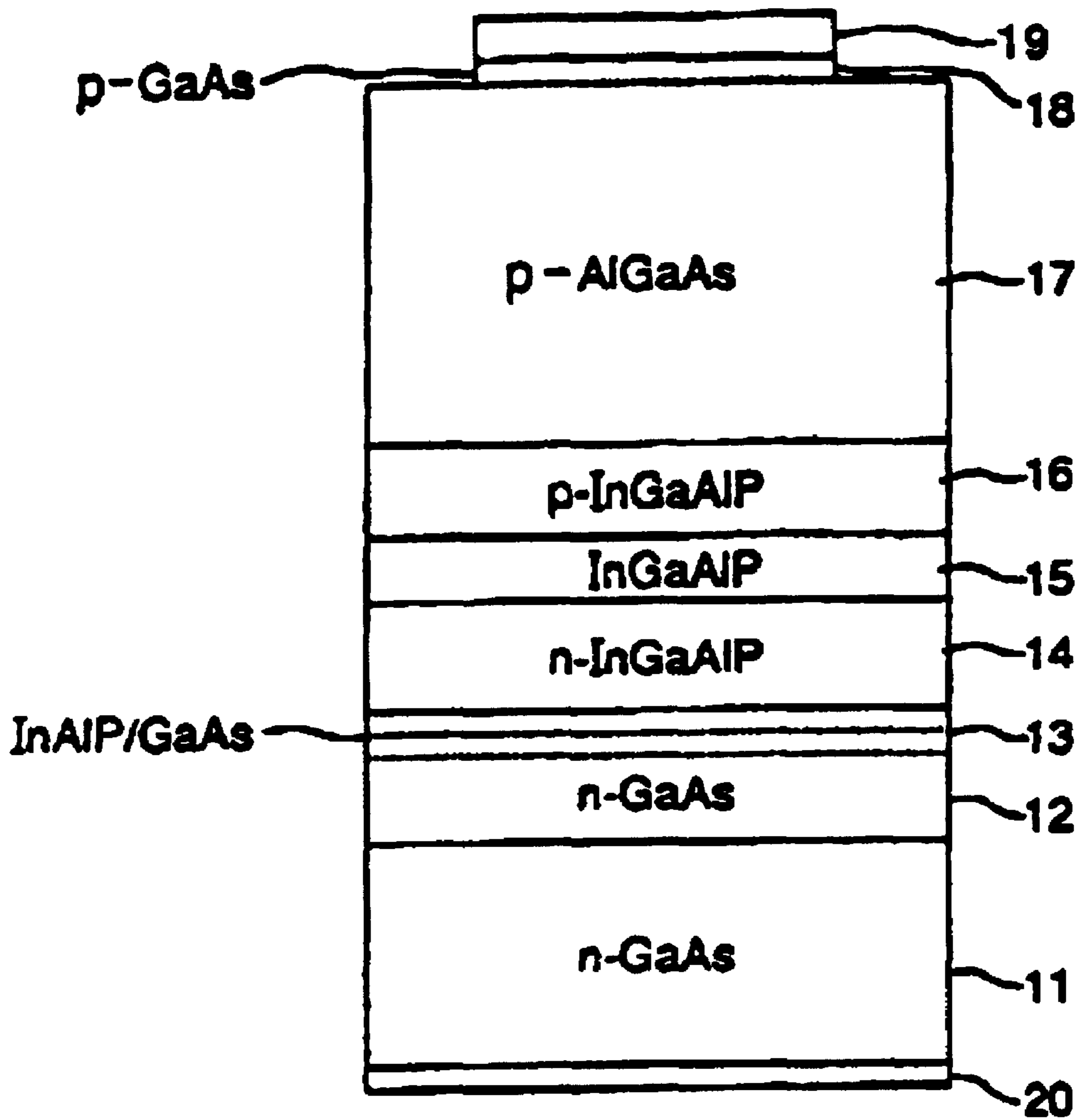


FIG. 1 PRIOR ART

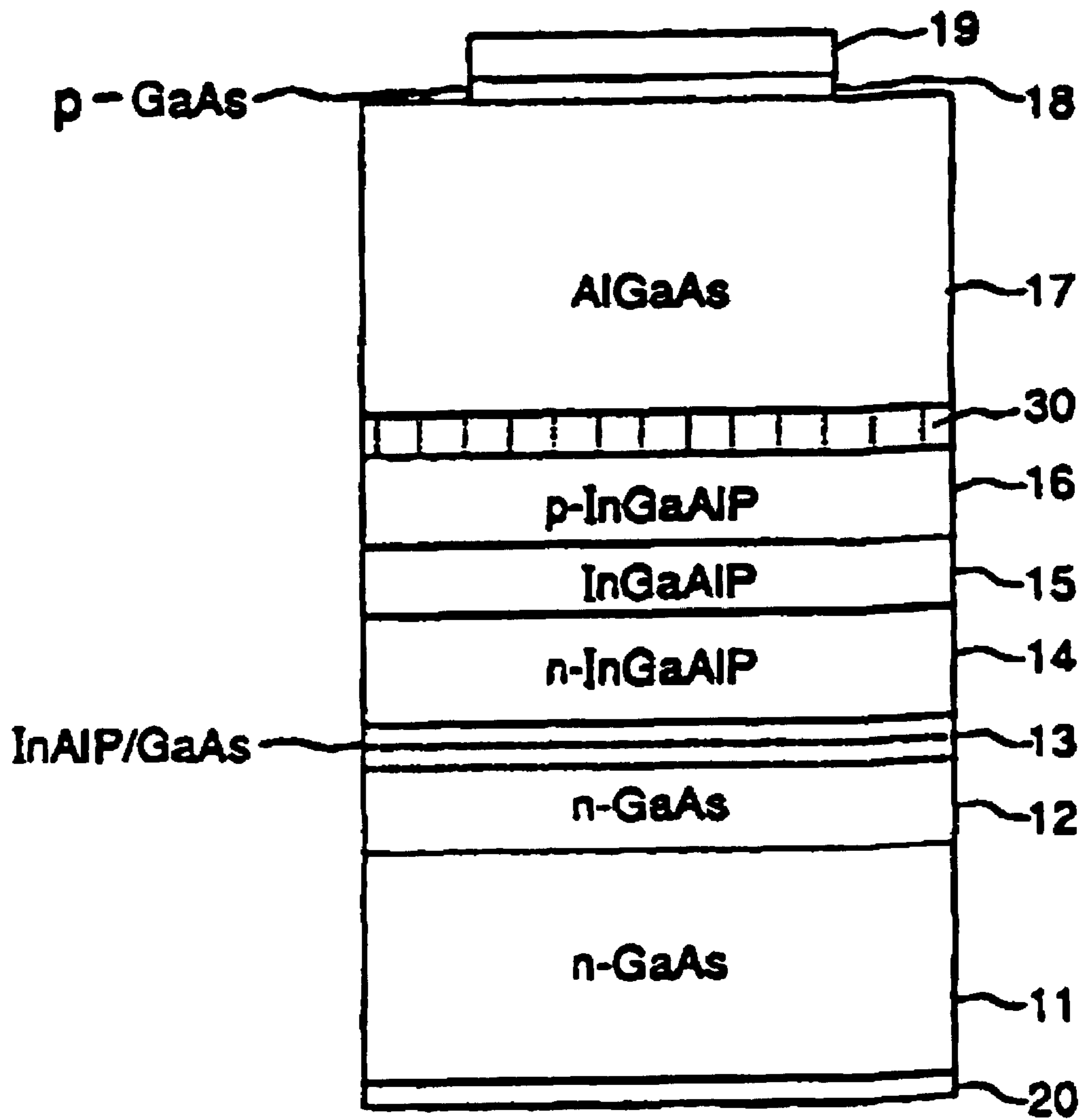


FIG. 2

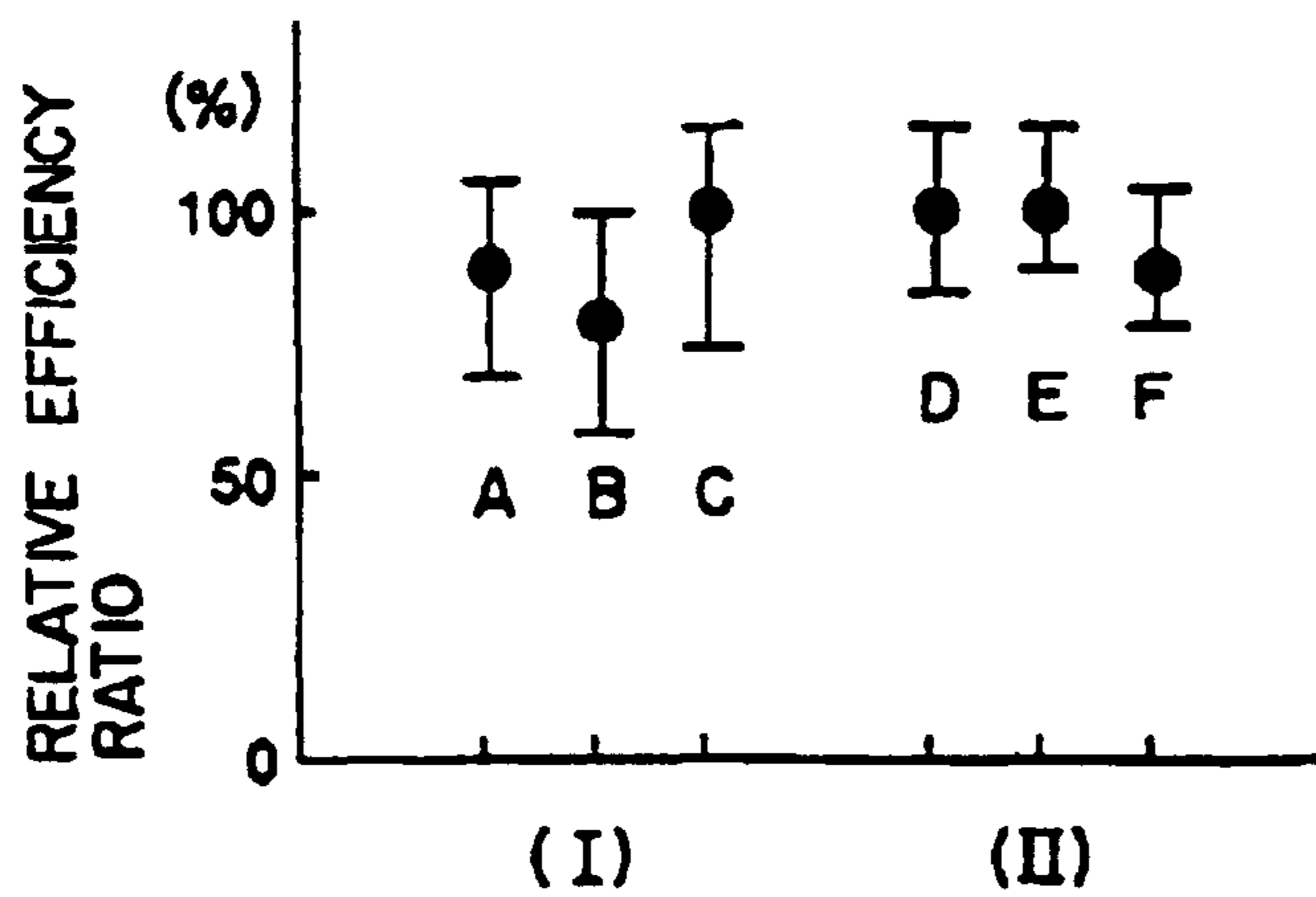


FIG. 3

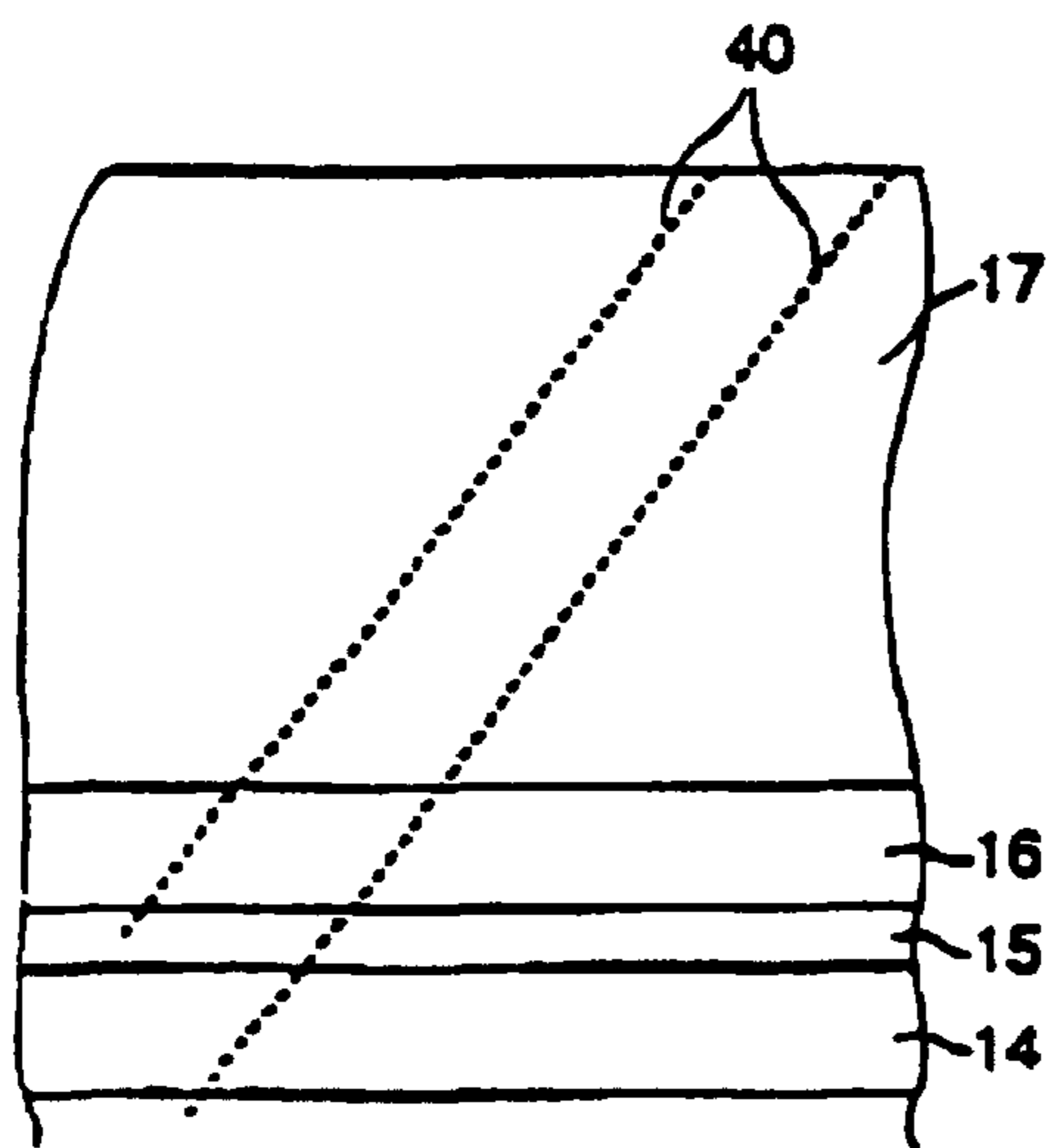


FIG. 4A

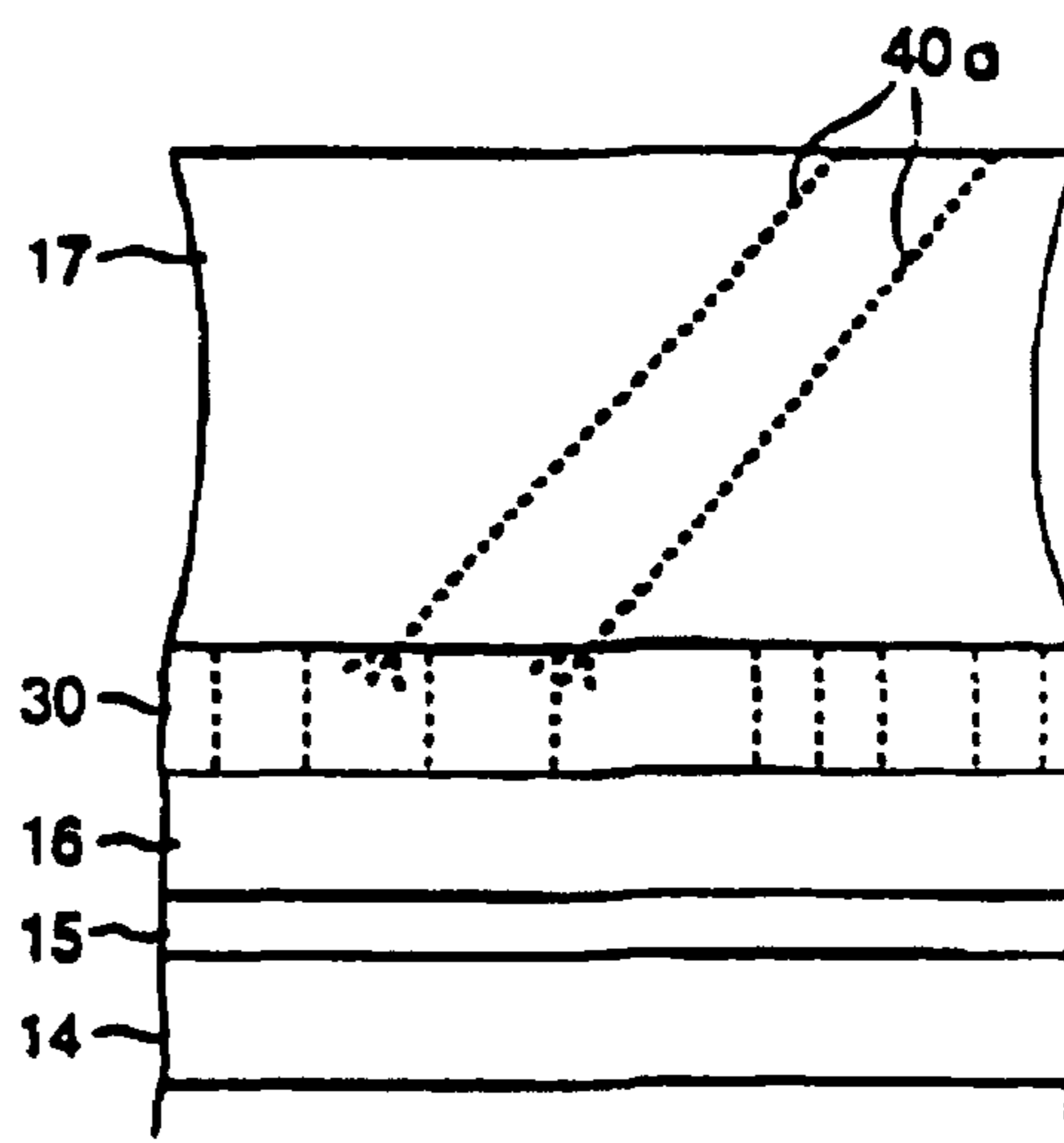


FIG. 4B

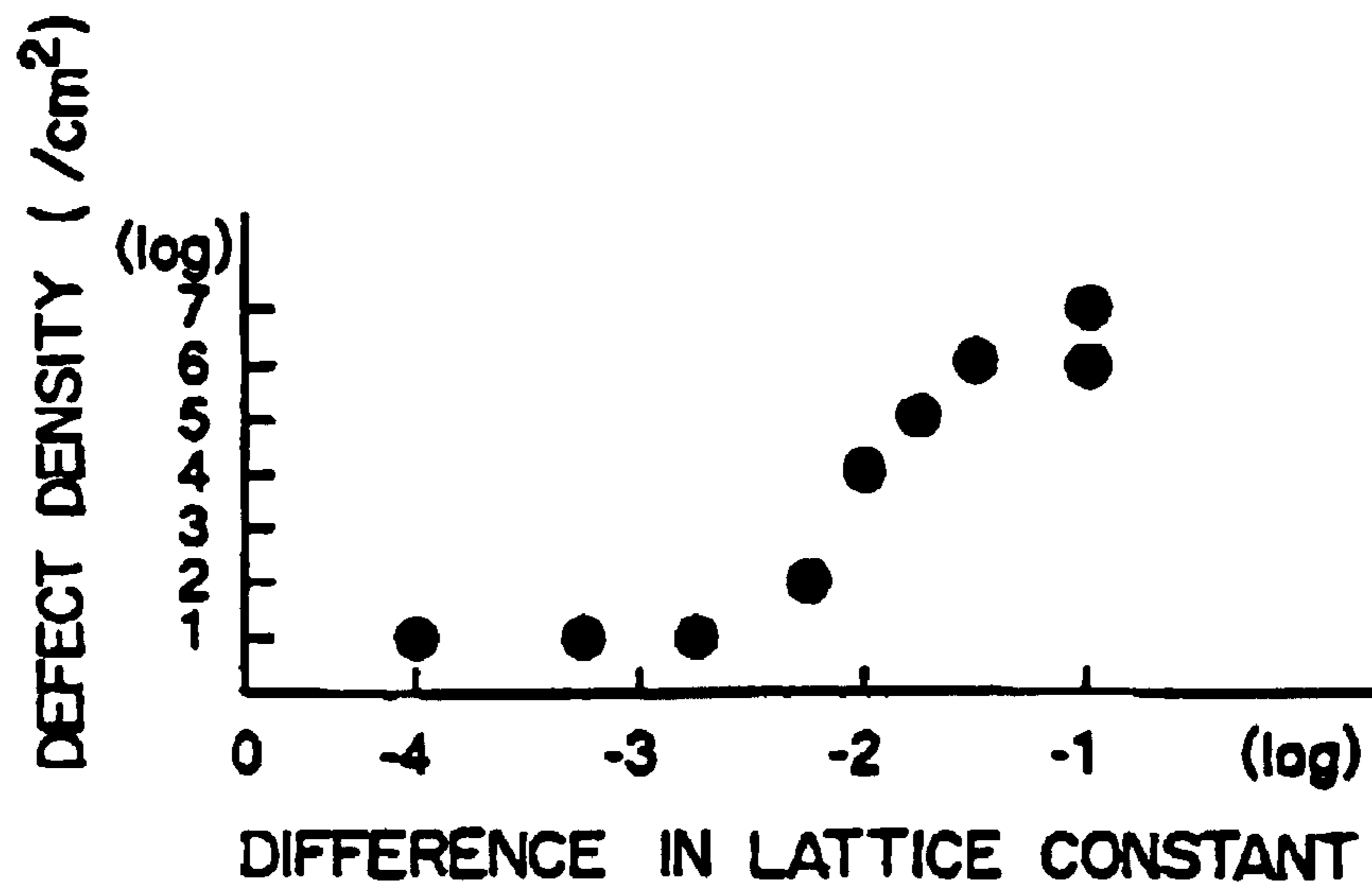


FIG. 5

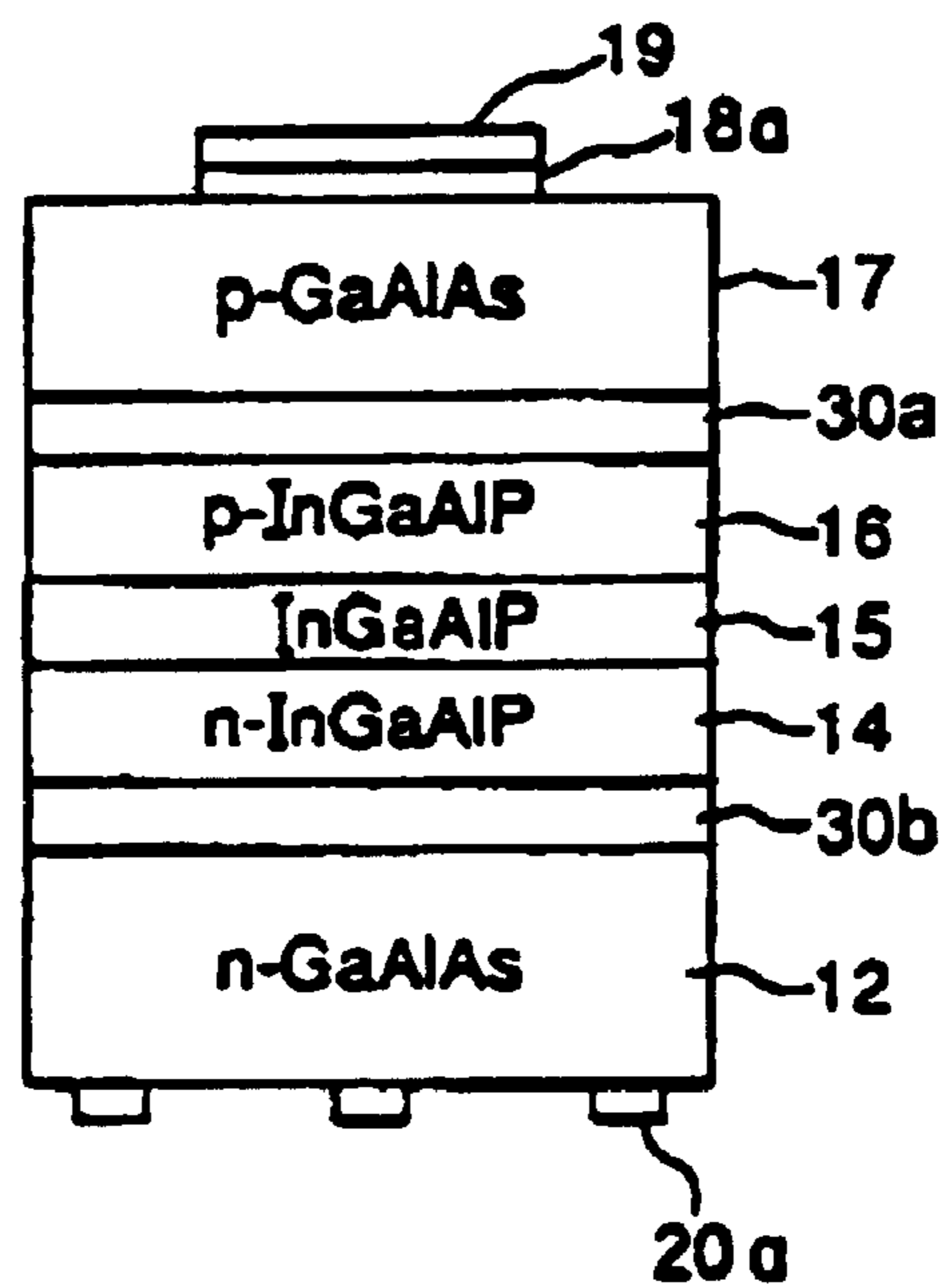


FIG. 6

## SEMICONDUCTOR LIGHT EMITTING DEVICE

**Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.**

This application is a Continuation Application of Ser. No. 08/578,980 filed Dec. 27, 1995, now U.S. Pat. No. 7,038,243, issued May 2, 2006, the entire contents of which are incorporated herein by reference and claims the benefit of priority from the prior Japanese Application No. 6-325713 filed Dec. 27, 1994.

### BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor light emitting device. Particularly, this invention relates to a semiconductor light emitting device with low crystal defects and higher performance.

FIG. 1 shows a conventional semiconductor light emitting device at its cross section. This semiconductor light emitting device consists of: a semiconductor substrate **11** of n-type gallium arsenide (GaAs); a transparent buffer layer **12** of n-type GaAs; a reflective layer **13** consisting of laminated two layers of indium aluminum phosphate (InAlP)/GaAs (InAlP on GaAs); a lower clad layer **14** of n-type InGaAlP; an active layer **15** of undoped InGaAlP; an upper clad layer **16** of p-type InGaAlP; a transparent current diffusing layer **17** of p-type AlGaAs; a contact layer **18** of p-type GaAs; an upper electrode **19** and a lower electrode **20**.

The buffer layer **12** prevents faults from being produced due to contamination of the surface of the semiconductor substrate **11** and also prevents the active layer **15** from being infected with the defects.

The reflective layer **13** reflects light emitted by the active layer **15** so that the emitted light does not enter the buffer layer **12** and the semiconductor substrate **11** made of light absorbent material. For this reason, the reflective layer **13** consists of semiconductor layers of InAlP and GaAs laminated with each other in a predetermined thickness. The layers of InAlP and GaAs have different refractive indices to the emitted light. The lower and upper clad layers **14** and **16** keep charge carriers injected into the active layer **15** to achieve high luminous efficiency.

The active layer **15** consists of  $\text{In}_{1-y}(\text{Ga}_{1-x}\text{Al}_x)\text{P}_y$ . The components "a" and "y" and the layer construction determine energy gap. The active layer **15** emits light of wavelength corresponding to the energy gap when the injected carriers recombine with each other.

The current diffusing layer **17** diffuses current thereacross to take out the emitted light through whole region of the layer **17** not only directly below the upper electrode **19**.

The current diffusing layer **17** is made of transparent material (p-type AlGaAs) that has a small absorbing coefficient to the emitted light wavelength.

The contact layer **18** makes better ohmic contact between the current diffusing layer **17** and the upper electrode **19**.

The upper electrode **19** is a p-type electrode of Au layer which contains zinc. Through the upper electrode **19**, a current is injected into a chip of the semiconductor light emitting device. The upper electrode **19** spreads the current over entire region of the semiconductor chip. Further, the upper electrode

**19** is formed so as not to scatter the emitted light. The upper electrode **19** also acts as a bonding pad.

The lower electrode **20** is an n-type electrode of Au formed as a layer which contains germanium. The lower electrode **20** drains the current.

Another conventional semiconductor light emitting device is disclosed by Japanese Patent Laid-Open NO: 4 (1992)-212479. The conventional device is a light emitting diode with double hetero-configuration. In this device, an InGaAlP active layer is interposed between two clad layers.

Such a device with the InGaAlP active layer has required advanced epitaxy aiming at epitaxial growth with better crystallization, or fewer crystal defects. This epitaxial growth achieves higher device reliability. Further, such a light emitting device is fabricated with a molding material of low resin stress. The low-resin stress material reduces decrease in luminescence after the light emitting device is driven.

However, it is very hard to keep crystal defects to a minimum in all layers grown by epitaxy. Device selection for quality in accordance with the number of crystal defects in all epitaxy-grown layers lowers device production yields. Further, low- and high-temperature degradation tests, after packaging the devices with molding resin, tend to produce much degradation in the resin packaged devices.

### SUMMARY OF THE INVENTION

A purpose of the present invention is to provide a semiconductor light emitting device with high reliability and production yields.

The present invention provides a semiconductor light emitting device including: a hetero-configuration having an active layer that emits light when charge carriers are injected, a first clad layer, and a second clad layer, the active layer being interposed between the clad layers, the first and second clad layers keeping the injected charge carriers in the active layer; a first and a second electrode, the hetero-configuration being inter-posed between the electrodes; and a first dense, defect layer, provided between the first electrode and the hetero-configuration, the first dense defect layer being made of material more able to absorb crystal defects and prevent defect extension and migration than the hetero-configuration, the first dense defect layer preventing defects from extending or migrating into the hetero-configuration.

The device may further include a second dense defect layer, provided between the second electrode and the hetero-configuration. The second dense defect layer is made of material more able to absorb crystal defects and prevent defect extension and migration than the hetero-configuration. The second dense defect layer prevents defects from extending or migrating into the hetero-configuration.

The hetero-configuration may be a double hetero-configuration in which the active layer is undoped, and the first and second clad layers are doped for a specific conductivity type.

The device may further include a current diffusion layer, provided between the first electrode and the first dense defect layer. The current diffusion layer diffuses current applied through the first electrode.

The device may further include a semiconductor substrate provided between the second electrode and the hetero-configuration and a buffer layer provided on the semiconductor substrate. The buffer layer prevents defects from being generated in the semiconductor substrate and the expansion of the defects into the active layer.

The present invention further provides a semiconductor light emitting device including: a hetero-configuration having an active layer that emits light when charge carriers are

injected, a first-clad layer, and a second clad layer, the active layer being interposed between the clad layers, the first and second clad layers keeping the injected charge carriers in the active layer; a first and a second electrode, the hetero-configuration being interposed between the electrodes; and a dense defect layer, provided between the first electrode and the hetero-configuration, the dense defect layer being made of material more able to absorb crystal defects and prevent defect extension and migration than the hetero-configuration, the dense defect layer preventing defects from extending or migrating into the hetero-configuration; a current diffusion layer, provided between the first electrode and the dense defect layer, the current diffusion layer diffusing current applied through the first electrode; a contact layer, provided between the first electrode and the current diffusion layer, the contact layer making ohmic contact between the first electrode and the current diffusion layer; a semiconductor substrate, provided between the second electrode and the hetero-configuration; a buffer layer, provided on the semiconductor substrate, the buffer layer preventing defects from being generated in the semiconductor substrate and the expansion of defects into the active layer; and a reflective layer, provided on the buffer layer, the reflective layer reflecting light emitted by the active layer so that the emitted light does not enter the buffer layer and semiconductor substrate.

The present invention further provides a semiconductor light emitting device including: a hetero-configuration having an active layer that emits light when charge carriers are injected, a first clad layer and a second clad layer, the active layer being interposed between the clad layers, the first and second clad layers keeping the injected charge carriers in the active layer; a first and a second electrode, the hetero-configuration being interposed between the electrodes; a first dense defect layer, provided between the first electrode and the hetero-configuration, the first dense defect layer being made of material more able to absorb crystal defects and prevent defect extension and migration than the hetero-configuration, the first dense defect layer preventing defects from extending or migrating into the hetero-configuration; a current diffusion layer, provided between the first electrode and the first dense defect layer, the current diffusion layer diffusing current applied through the first electrode; a contact layer, provided between the first electrode and the current diffusion layer, the contact layer making ohmic contact between the first electrode and the current diffusion layer; a second dense defect layer, provided between the second electrode and the hetero-configuration, the second dense defect layer made of material being more able to absorb crystal defects and prevent defect extension and migration than the hetero-configuration, the second dense defect layer preventing defects from extending or migrating into the hetero-configuration; and a buffer layer, provided on the second electrode, the buffer layer preventing defects from being generated in the semiconductor substrate and the expansion of defects into the active layer.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross sectional schematic illustration of a conventional semiconductor light emitting device;

FIG. 2 is a cross sectional schematic illustration of a preferred embodiment of a semiconductor light emitting device according to the present invention;

FIG. 3 is a graphical representation of variation of luminescence efficiency;

FIGS. 4A and 4B show fragmentary sectional views of the conventional sample chip and that of the present invention;

FIG. 5 is a graphical representation of comparison to device characteristics of the conventional sample chip and that of the present invention; and

FIG. 6 is a cross sectional schematic illustration of another preferred embodiment of a semiconductor light emitting device according to the present invention.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments will be described with reference to the attached drawings.

FIG. 2 shows a cross sectional schematic illustration of an embodiment of the semiconductor light emitting device according to the present invention. The layers of the same reference numerals as the layers shown in FIG. 1 function the same as those conventional device layers.

This semiconductor light emitting device includes a buffer layer **12** of n-type GaAs; a reflective layer **13** consisting of laminated two layers of indium aluminum phosphate (InAlP)/GaAs (InAlP on GaAs); a lower clad layer **14** of n-type InGaAlP; an active layer, **15** of undoped InGaAlP; an upper clad layer **16** of p-type InGaAlP; a dense defect layer **30**; a current diffusing layer **17** of p-type AlGaAs; and a contact layer **18** of p-type GaAs. These layers are formed in order on a semiconductor substrate **11** of n-type gallium arsenide (GaAs). A double hetero-configuration consists of the lower clad layer **14**, the active layer **15** and the upper clad layer **16**. An upper electrode **19** is formed the contact layer **18**. A lower electrode **20** is formed beneath the substrate **11**.

Either of the buffer layer **12** and the current diffusing layer **17** may be omitted. The reflective layer **13** and the contact layer **18** may also be omitted.

Compared to the conventional device of FIG. 1, the added feature of the embodiment of FIG. 2 is the dense defect layer **30** interposed between the p-type InGaAlP upper clad layer **16** and the p-type AlGaAs current diffusing layer **17**. The dense defect-injected layer **30** is made of 50 nm-thick InP mixed crystal that is more able to absorb crystal defects and prevent defect extension and migration than the p-type InGaAlP upper clad layer **16**.

The semiconductor light emitting device is fabricated as follows:

The layers described above are grown epitaxially one by one on the n-type GaAs substrate **11** formed on a semiconductor wafer as describe below. These epitaxial growths are performed in a chemical vapor deposition (CVD) reaction chamber. A carrier gas (hydrogen) flows into the CVD reaction chamber at a gas flow rate of 10l/min. The semiconductor substrate **11** is annealed at a temperature in the range of 720° to 870° C.

(1) Trimethylgallium (TMG) and arsenic hydride (AsH<sub>3</sub>) flow into the chamber at a gas flow rate in the range of 20 to 400 ccm and 500 to 800 ccm, respectively. Further, silicon hydride (SiH<sub>4</sub>) flows at a gas velocity in the range of 10 to 15 ccm for doping to form the n-type GaAs buffer layer **12** on the substrate **11**.

(2) Trimethylgallium and AsH<sub>3</sub> flow again at the same gas flow rates in step (1) to form a GaAs layer on the buffer layer **12**. Further, trimethylindium (TMI), trimethylaluminum (TMA) and phosphorus hydride (PH<sub>3</sub>) flow at a gas velocity in the range of 0.5 to 0.8 ccm, 10 to 300 ccm and 250 to 400 ccm, respectively, to form an InAlP layer on the GaAs layer to form the InAlP/GaAs reflective layer **13**.

(3) Trimethylindium, TMG, TMA and PH<sub>3</sub> flow at the same gas flow rates in the above steps. Further, SiH<sub>4</sub> flows at

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the same gas flow rate in step (1) to form the n-type InGaAlP lower clad layer **14** on the reflective layer **13**.

(4) Trimethylgallium, TMG, TAM and PH<sub>3</sub> flow at the same gas flow rates in the above steps to form the undoped InGaAlP active layer **15** on the lower clad layer **14**.

(5) Trimethylgallium, TMG, TAM and PH<sub>3</sub> flow at the same gas flow rates in the above steps. Further, dimethylzinc (DMZ) flows at a gas velocity in the range of 0.3 to 0.5 ccm for doping to form the p-type InGaAlP upper clad layer **16** on the active layer **15**.

(6) The susceptor temperature is decreased by 100° C. Trimethylaluminum and PH<sub>3</sub> flow at the same gas flow rates in the above steps to form the dense defect layer **30** of 50 nm-thick InP mixed crystal on the upper clad layer **16**.

(7) The chamber temperature decreased by 100° C. in step (6) is increased to the original temperature at which the process is executed in steps (1) to (5). At this temperature, TMA, TMG and AsH<sub>3</sub> flow at the same gas flow rates in the above steps. Further, DMZ flows at the same gas flow rate in step (5) for doping to form the p-type AlGaAs current diffusing layer **17** on the dense defect layer **30**.

(8) Trimethylgallium and AsH<sub>3</sub> flow at the same gas flow rates in the above steps. Further, DMZ flows at the same gas flow rate in step (5) for doping to form the p type GaAs contact layer **18** on the current diffusing layer **17**. And,

(9) A reverse-sided lapping operation thins the substrate **11**. The upper and lower electrodes **19** and **20** are deposited on the contact layer **18** and the thinned substrate **11**, respectively. The semiconductor wafer on which the above multiple layers were laminated was diced and molded to obtain many chips of semiconductor light emitting devices (FIG. 2). Each chip was of 400×400 μm<sup>2</sup> in area and 200 μm in height. Also produced were the chips of the conventional semiconductor light emitting devices (FIG. 1) of the same size as the present invention.

These semiconductor light emitting devices were tested for luminance efficiency. A forward current of 20 mA of 5 volts was supplied to each device to find out initial luminance efficiency and luminance efficiency after 500 hours have elapsed. These tests were conducted for determining the degradation rate of the semiconductor light emitting devices of the present invention and the conventional devices.

Fifty sample chips were selected per sample lot from the semiconductor light emitting devices of the present invention and also from the conventional devices to determine the initial luminance efficiency and luminance efficiency after 500-hour elapsing. The dense defect layer **30** of 50 nm-thick InP mixed crystal was grown for the devices of the present invention.

FIG. 3 is a graphical representation of variation of the luminance efficiency after 500 hours have elapsed indicated by the relative efficiency ratio (ratio of initial luminance efficiency/luminance efficiency after 500 have elapsed). Each dot depicts an average survival rate for 50 samples per lot (A, B, C, D, E, and F). The upper and lower ends of each bar depict the maximum and minimum survival rates, respectively. FIG. 3 teaches that the sample chips of the present invention (II) have a higher survival rate than the conventional sample chips (I). Further, FIG. 3 teaches that the sample chips of the present invention have nearly the survival rate for the lots D, E, and F.

The conventional sample chips (lot B) that had the worst survival rates were analyzed by cathode luminescence technique.

This technique revealed an un-luminous crystallization fault **40** called a dark line as shown in FIG. 4A. FIG. 4A shows a fragmentary cross sectional view of the conventional sample device chip of FIG. 1. The dark line crossed the current diffusing layer **17** from the device surface. Further,

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the dark line penetrated into the upper clad layer **16**, active layer **15**, and lower upper clad layer **14**.

The destruction of the active (light emitting) layer **15** by the un-luminous crystallization fault **40** was deemed to cause the low survival rates, and corresponding high levels of degradation. The dark line (fault **40**) extended towards the active layer **15** from directly below a bonding wire (not shown) fixed on the upper electrode **19** of FIG. 1. It is believed that: wire bonding caused damage to the device surface; the damage expanded due to heat and resin stress; and the expanded damage penetrated into the device as the un-luminous crystallization fault **40** that damaged the active layer **15**.

The sample device chips of the present invention were also analyzed by the cathode luminescence technique. This technique revealed an un-luminous crystallization fault **40a** as shown in FIG. 4B. FIG. 4B shows a fragmentary cross sectional view of the sample device chip of the present invention of FIG. 2. The un-luminous crystallization fault **40a** produced due to wire bonding crossed the current diffusing layer **17**.

However, contrary to the conventional sample device chip of FIG. 4A, the un-luminous crystallization fault **40a** stopped in the 50 nm-thick dense defect InP layer **30** that is the feature of the present invention. The un-luminous crystallization fault **40a** did not reach the active layer **15** and upper clad layer **16**. The faults **40a** are absorbed or impeded in the dense defect layer **30** is believed to be the reason for the higher luminance efficiency of the device chips of the present invention. More precisely, the dense defect layer **30** was deemed to prevent the un-luminous crystallization fault **40a** from or migrating into the cladding layer **14** or active layer **15** due to heat and resin stress. The device chips of the present invention were thus protected from defect migration or extension from external areas into the clad and active layers of the device.

FIG. 4B, the fragmentary cross sectional view of FIG. 2, further schematically depicts prevention of secondary generated defects from extending or migrating into the active layer **15** and upper clad layer **16** by the dense defect-injected layer **30**.

This advantage was provided by the use of the Inp mixed crystal layer for the dense defect layer **30**. Besides Inp mixed crystal, use of GaP, InGaP, InAlP, AlP, and AlAs mixed crystals as the dense defect layer **30** is also contemplated.

However, InGaAs mixed crystal did not work well for the dense defect layer **30**. This was noted by observing the boundary of the InGaAs dense defect layer and InGaAlP layers as the active and clad layers with cross section Transmission Electron Microscopy (TEM).

The observation revealed that: enough defects were not provided in the InGaAs layer acting as the dense defect layer **30**; the InGaAs layer could not sufficiently disperse the secondary defects traveling or migrating into this layer and due to bonding damage; and a part of the secondary defects were injected into the InGaAlP upper clad layer **16**.

The observation further revealed that reduces the effects of a un-luminous crystallization fault **40a** can be achieved by providing defects in the dense defect-injected material and not in the InGaAlP layer.

Moreover, the observation revealed as shown in FIG. 5 that: the desired reduction in defect effects can be achieved when the defect density (the number of defects) of the dense defect injected layer **30** is 10<sup>4</sup>/cm<sup>2</sup> or more; the difference in lattice constant is 10<sup>-2</sup> or more between the dense defect layer **30** and InGaAlP upper clad layer **16**; and the dense defect layer **30** is preferably 10 nm or more in thickness.

FIG. 6 shows a cross sectional schematic illustration of another embodiment of the semiconductor light emitting device according to the present invention. The layers of the



same reference numerals as the layers shown in FIG. 2 function the same as those conventional device layers. And hence explanation of those are omitted here.

This embodiment does not require the semiconductor substrate **11** of FIG. 2. An upper dense defect layer **30a** is formed between the transparent current diffusion layer **17** and the upper clad layer **16**. Further, a lower dense defect layer **30b** is formed between the transparent buffer layer **12** and the lower clad layer **16**.

These upper and lower layers **30a** and **30b** restrict crystal defect damage to the active region of the double hetero-configuration that consists of the n-InGaAlP lower clad layer **14**, InGaAlP active layer **15** and p-InGaAlP upper clad layer **16**. . . Further, the layers **30a** and **30b** restrict crystallization faults being passed into the current diffusion layer **17** and buffer layer **12**, respectively. The crystallization faults are generated mostly due to internal stress caused by thermal expansion and shrink-age when the devices are molded. The lower dense defect layer **30b** can restrict generation of crystallization faults.

The semiconductor devices of the two embodiments include the double hetero-configuration. This configuration consists of the n-type InGaAlP lower clad layer **14**, p-type InGaAlP upper clad layer **16**, and undoped InGaAlP active layer **15** interposed between the two clad layers.

According to the preferred embodiments of the invention, semiconductor devices, particularly light emitting devices, can be obtained with high reliability, long lifetime, high yield rates, and of reasonable price. The light emitting device includes a double or single hetero-configuration that consists of a pair of clad layers and an InGaAlP active layer interposed between the clad layers. During epitaxial growth of this device, a dense defect layer is formed on or beneath the hetero-configuration. Or, two dense defect-injected layers are formed on and beneath the hetero-configuration. The dense defect layer is made of material of two or three mixed crystals. The mixed crystals are a combination of elements selected from the group consisting of In, Ga, Al, P, and As. The elements for the combination are different in lattice constant of  $10^{-2}$  or more. Further, the dense defect layer includes defects of  $10^4/\text{cm}^2$  or more. Such a dense defect layer prevents secondarily generated defects from migrating or extending as un-luminance crystallization faults into the important InGaAlP active (light emitting) layer.

As described above, the present invention provides a semiconductor device configuration including at least a first layer with a first function, a second layer with a second function, and a third layer interposed between the first and second layers. The third layer is a dense defect-injected layer made of material that is more able to absorb crystal defects and prevent defect migration and extension than the second layer. The third layer disperses or absorbs a dark line (the un-luminous crystallization fault in the embodiments) that would otherwise cross the first layer and reach the second layer. The third layer thus restricts the extension or migration of crystallization faults. The present invention is therefore useful for any semiconductor devices with a layer of specific function that should be protected from crystallization faults.

What is claimed is:

1. A semiconductor light emitting device, comprising:
  - a first defect layer;
  - a first clad layer of a first conductive type formed on the first defect layer;
  - an active layer formed on the first clad layer;
  - a second clad layer of a second conductive type formed on the active layer;
  - a second defect layer formed on the second clad layer;

- a first electrode electrically connected to the first clad layer; and
- a second electrode electrically connected to the second clad layer.

2. A semiconductor light emitting device of claim 1, wherein the first defect layer has a higher defect density than the first clad layer.

3. A semiconductor light emitting device of claim 1, wherein the second defect layer has a higher defect density than the second clad layer.

4. A semiconductor light emitting device of claim 1, wherein the first defect layer is  $10^{-2}$  or more different in lattice constant from the first clad layer.

5. A semiconductor light emitting device of claim 1, wherein the second defect layer is  $10^{-2}$  or more different in lattice constant from the second clad layer.

6. A semiconductor light emitting device of claim 1, wherein the first defect layer is 10 nm or more in thickness.

7. A semiconductor light emitting device of claim 1, wherein the second defect layer is 10 nm or more in thickness.

8. A semiconductor light device of claim 1, further comprising, a current diffusion layer provided between the second defect layer and the second electrode.

9. A semiconductor light emitting device, comprising:

- a first layer having a first defect region;
- a [first] first clad layer of a first conductive type formed on [the defect region of] the first [defect region] layer;
- an active layer formed on the first clad layer;
- a second clad layer of a second conductive type formed on the active layer;
- a second layer having a second defect region, the second [defect regions] layer formed on the second clad layer;
- a first electrode electrically connected to the first clad layer; and
- a second electrode electrically connected to the second clad layer.

10. A semiconductor light emitting device of claim 9, wherein the first defect region has a higher defect density than the first clad layer.

11. A semiconductor light emitting device of claim 9, wherein the second defect region has a higher defect density than the second clad layer.

12. A semiconductor light emitting device of claim 9, wherein the first defect region is  $10^{-2}$  or more different in lattice constant from the first clad layer.

13. A semiconductor light emitting device of claim 9, wherein the second defect region is  $10^{-2}$  or more different in lattice constant from the second clad layer.

14. A semiconductor light emitting device of claim 9, wherein the first defect region is 10 nm or more in thickness.

15. A semiconductor light emitting device of claim 9, wherein the second defect region is 10 nm or more in thickness.

16. A semiconductor light emitting device of claim 9, further comprising, a current diffusion layer provided between the second defect layer and the second electrode.

17. A semiconductor light emitting device of claim 16, wherein the current diffusion layer is transparent to light from the active layer.

18. A semiconductor light emitting device of claim 8, wherein the current diffusion layer is transparent to light from the active layer.

19. A semiconductor light emitting device, comprising:

- a first defect layer;
- a first clad layer of a first conductivity type formed above the first defect layer;
- an active layer formed on the first clad layer;

a second clad layer of a second conductivity type formed on the active layer;  
 a second defect layer formed above the second clad layer;  
 a first electrode electrically connected to the first clad layer; and  
 a second electrode electrically connected to the second clad layer.

20. A semiconductor light emitting device of claim 19, wherein the first defect layer has a higher defect density than the first clad layer.

21. A semiconductor light emitting device of claim 19, wherein the second defect layer has a higher defect density than the second clad layer.

22. A semiconductor light emitting device of claim 19, wherein the first defect layer is  $10^{-2}$  or more different in lattice constant from the first clad layer.

23. A semiconductor light emitting device of claim 19, wherein the second defect layer is  $10^{-2}$  or more different in lattice constant from the second clad layer.

24. A semiconductor light emitting device of claim 19, wherein the first defect layer is 10 nm or more in thickness.

25. A semiconductor light emitting device of claim 19, wherein the second defect layer is 10 nm or more in thickness.

26. A semiconductor light device of claim 19, further comprising, a current diffusion layer provided between the second defect layer and the second electrode.

27. A semiconductor light emitting device, comprising  
 a first layer having a first defect region;  
 a first clad layer of a first conductivity type formed above the first layer;  
 an active layer formed on the first clad layer;  
 a second clad layer of a second conductivity type formed on the active layer;  
 a second layer having a second defect region, the second layer formed above the second clad layer;  
 a first electrode electrically connected to the first clad layer; and  
 a second electrode electrically connected to the second clad layer.

28. A semiconductor light emitting device of claim 27, wherein the first defect region has a higher defect density than the first clad layer.

29. A semiconductor light emitting device of claim 27, wherein the second defect region has a higher defect density than the second clad layer.

30. A semiconductor light emitting device of claim 27, wherein the first defect region is  $10^{-2}$  or more different in lattice constant from the first clad layer.

31. A semiconductor light emitting device of claim 27, wherein the second defect region is  $10^{-2}$  or more different in lattice constant from the second clad layer.

32. A semiconductor light emitting device of claim 27, wherein the first defect region is 10 nm or more in thickness.

33. A semiconductor light emitting device of claim 27, wherein the second defect region is 10 nm or more in thickness.

34. A semiconductor light emitting device of claim 27, further comprising, a current diffusion layer provided between the second defect layer and the second electrode.

35. A semiconductor light emitting device of claim 34, wherein the current diffusion layer is transparent to light from the active layer.

36. A semiconductor light emitting device of claim 27, wherein the current diffusion layer is transparent to light from the active layer.

37. A semiconductor light emitting device, comprising:  
 a substrate;  
 a first clad layer of a first conductive type on the substrate;  
 an active layer formed on the first clad layer;  
 a second clad layer of a second conductive type formed on the active layer;  
 a defect layer formed above the second clad layer;  
 a first electrode electrically connected to the first clad layer; and  
 a second electrode electrically connected to the second clad layer.

38. A semiconductor light emitting device of claim 37, wherein the defect layer has a higher defect density than the second clad layer.

39. A semiconductor light emitting device of claim 38, wherein the defect layer is  $10^{-2}$  or more different in lattice constant from the second clad layer.

40. A semiconductor light emitting device of claim 37, wherein the defect layer is  $10^{-2}$  or more different in lattice constant from the second clad layer.

41. A semiconductor light emitting device of claim 37, wherein the defect layer is 10 nm or more in thickness.

42. A semiconductor light emitting device of claim 38, wherein the defect layer is 10 nm or more in thickness.

43. A semiconductor light emitting device of claim 39, wherein the defect layer is 10 nm or more in thickness.

44. A semiconductor light emitting device of claim 40, wherein the defect layer is 10 nm or more in thickness.

45. A semiconductor light emitting device of claim 37, the first conductivity type is N type and the second conductivity type is P type, and the defect layer is P type.

46. A semiconductor light emitting device, comprising:  
 a substrate;  
 a first clad layer of a first conductive type on the substrate;  
 an active layer formed on the first clad layer;  
 a second clad layer of a second conductive type formed on the active layer;  
 a semiconductor layer of a second conductive type formed above the second clad layer;  
 a first electrode electrically connected to the first clad layer;  
 a second electrode electrically connected to the semiconductor layer; and  
 a defect layer formed above the second clad layer and below the semiconductor layer.

47. A semiconductor light emitting device of claim 46, wherein the defect layer has a higher defect density than the second clad layer.

48. A semiconductor light emitting device of claim 47, wherein the defect layer is  $10^{-2}$  or more different in lattice constant from the second clad layer.

49. A semiconductor light emitting device of claim 46, wherein the defect layer is  $10^{-2}$  or more different in lattice constant from the second clad layer.

50. A semiconductor light emitting device of claim 46, wherein the defect layer is 10 nm or more in thickness.

51. A semiconductor light emitting device of claim 47, wherein the defect layer is 10 nm or more in thickness.

52. A semiconductor light emitting device of claim 46, the first conductive type is N type and the second conductive type is P type, and the defect layer has a P type conductive type.

53. A semiconductor light emitting device of claim 46, wherein the semiconductor layer of the second conductive type is transparent to a light emitted from the active layer.

54. A semiconductor light emitting device of claim 46, wherein the semiconductor layer of the second conductive type is made of different material to the defect layer.

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55. A semiconductor light emitting device of claim 53, wherein the semiconductor layer of the second conductive type is made of different material to the defect layer.

56. A semiconductor light emitting device of claim 46, wherein the defect layer includes InGaP.

57. A semiconductor light emitting device of claim 53, wherein the defect layer includes InGaP.

58. A semiconductor light emitting device of claim 54, wherein the defect layer includes InGaP.

59. A semiconductor light emitting device of claim 55, wherein the defect layer includes InGaP.

60. A semiconductor light emitting device, comprising:  
a first semiconductor layer of a first conductive type;  
a first clad layer of the first conductive type formed above  
the first semiconductor layer;

an active layer formed on the first clad layer;

a second clad layer of a second conductive type formed on  
the active layer;

a second semiconductor layer of a second conductive type  
formed above the second clad layer;

a first electrode electrically connected to the first clad  
layer;

a second electrode electrically connected to the second  
clad layer; and

a defect layer formed above the second clad layer and  
below the second semiconductor layer,

wherein the first semiconductor layer and the second semi-  
conductor layer are transparent to a light emitted from  
the active layer.

61. A semiconductor light emitting device of claim 60, wherein the first semiconductor layer, the first clad layer, the active layer, the second clad layer, the defect layer and the second semiconductor layer are grown on a semiconductor substrate, a portion of the substrate is removed after the first semiconductor layer, the first clad layer, the active layer, the second clad layer and the second semiconductor layer are grown.

62. A semiconductor light emitting device of claim 60, wherein the defect layer has a higher defect density than the second clad layer.

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63. A semiconductor light emitting device of claim 60, wherein the defect layer is  $10^{-2}$  or more different in lattice constant from the second clad layer.

64. A semiconductor light emitting device of claim 60, wherein the defect layer is 10 nm or more in thickness.

65. A semiconductor light emitting device of claim 60, wherein the first conductive type is N type and the second conductive type is P type.

66. A semiconductor light emitting device of claim 60, wherein the defect layer is directly formed on the second clad layer.

67. A semiconductor light emitting device of claim 60, wherein the defect layer is directly formed on the second clad layer, and the second semiconductor layer is directly formed on the defect layer.

68. A semiconductor light emitting device of claim 61, wherein the semiconductor substrate is GaAs substrate.

69. A semiconductor light emitting device of claim 61, wherein the defect layer has a higher defect density than the second clad layer.

70. A semiconductor light emitting device of claim 61, wherein the defect layer is  $10^{-2}$  or more different in lattice constant from the second clad layer.

71. A semiconductor light emitting device of claim 61, wherein the defect layer is 10 nm or more in thickness.

72. A semiconductor light emitting device of claim 61, wherein the first conductive type is N type and the second conductive type is P type.

73. A semiconductor light emitting device of claim 61, wherein the substrate is N type GaAs substrate.

74. A semiconductor light emitting device of claim 61, wherein the defect layer is directly formed on the second clad layer.

75. A semiconductor light emitting device of claim 61, wherein the defect layer is directly formed on the second clad layer, and the second semiconductor layer is directly formed on the defect layer.

76. A semiconductor light emitting device of claim 61, wherein the first semiconductor layer, the first clad layer, the active layer, the second clad layer, the defect layer and the second semiconductor layer are grown in this order.

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