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(54) **PACKET ACQUISITION AND CHANNEL TRACKING FOR A WIRELESS COMMUNICATION DEVICE CONFIGURED IN A ZERO INTERMEDIATE FREQUENCY ARCHITECTURE**

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(58) **Field of Classification Search** **455/232.1, 455/234.1, 239.1, 343.2; 375/346**

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,828,249 A 8/1974 Alber et al.
3,953,805 A 4/1976 Couvillon
4,028,626 A 6/1977 Motley et al.
4,101,841 A 7/1978 Okada et al.
4,134,078 A 1/1979 Arai et al.

(Continued)

FOREIGN PATENT DOCUMENTS

EP 0 719 013 6/1996

(Continued)

OTHER PUBLICATIONS

Abidi A., "Direct-Conversion Radio Transceivers for Digital Communications," IEEE Journal of Solid-State Circuits, vol. 30, No. 12, Dec. 1995, pp. 1399-1410.

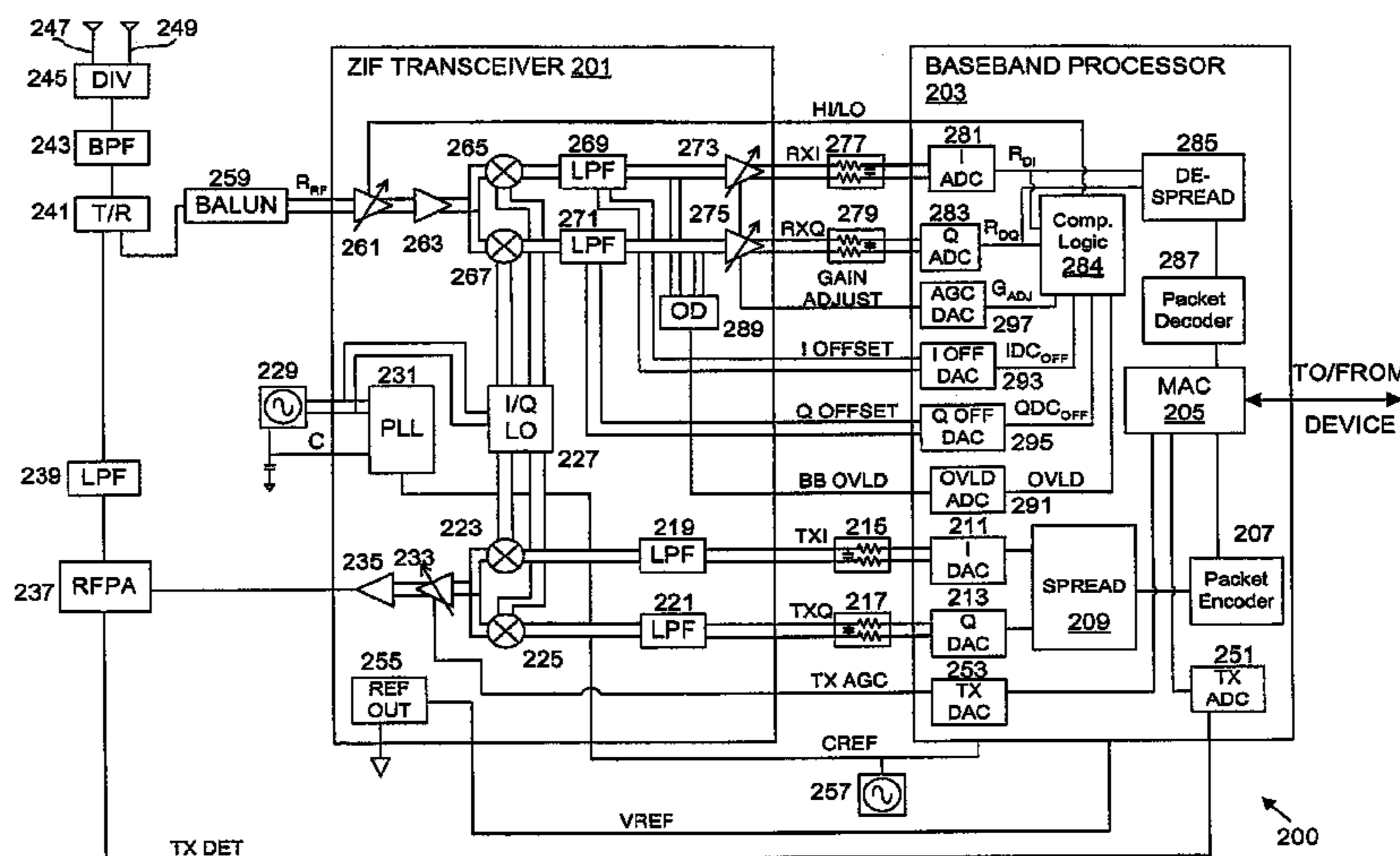
(Continued)

Primary Examiner — Thjuan K Addy

(57) **ABSTRACT**

A method of controlling operation of a wireless device configured in a zero intermediate frequency architecture including a DC loop and a gain loop. The method includes processing energy in a wireless medium to generate a corresponding receive signal, monitoring the receive signal via a predetermined measurement window, detecting a changed condition in the channel, holding the gain feedback control loop at a constant gain level, and operating the DC loop in an attempt to search a stable DC value for the receive signal while the gain loop is held constant. A first case is DC saturation, where the gain is held constant until DC is controlled. A second case is clear channel assessment, where a prior stored gain setting is applied to the gain loop after detecting the end of the packet. A third case is preparation for receiving an expected acknowledgement packet after transmitting a packet, where again a prior stored gain setting is applied to the gain loop and DC is searched.

60 Claims, 13 Drawing Sheets



U.S. PATENT DOCUMENTS

4,164,036	A	8/1979	Wax	
4,458,210	A	7/1984	Horl	
4,502,021	A	2/1985	Hill et al.	
4,514,702	A	4/1985	Zogg	
4,823,129	A	4/1989	Nelson	
4,951,000	A	8/1990	Dautriche	
5,009,126	A	4/1991	Meisinger et al.	
5,077,541	A	12/1991	Gilbert	
5,157,350	A	10/1992	Rubens	
5,175,749	A	12/1992	Ficht et al.	
5,212,826	A	5/1993	Rabe et al.	
5,212,827	A	5/1993	Meszko et al.	
5,241,702	A	8/1993	Dent	
5,264,798	A	11/1993	Bey et al.	
5,400,366	A	3/1995	Iwamatsu	
5,471,665	A *	11/1995	Pace et al.	455/343.2
5,483,691	A	1/1996	Heck et al.	
5,573,001	A	11/1996	Petrofsky et al.	
5,574,755	A	11/1996	Persico	
5,575,001	A	11/1996	Ku	
5,608,796	A	3/1997	Banu et al.	
5,617,060	A *	4/1997	Wilson et al.	330/129
5,644,308	A	7/1997	Kerth et al.	
5,659,263	A	8/1997	Dow et al.	
5,661,761	A	8/1997	Iwamatsu	
5,684,431	A	11/1997	Gilbert et al.	
5,712,203	A	1/1998	Hsu	
5,712,594	A	1/1998	Kimura	
5,715,281	A	2/1998	Bly et al.	
5,724,653	A	3/1998	Baker et al.	
5,732,341	A *	3/1998	Wheatley, III	455/234.1
5,742,203	A	4/1998	Van De Plassche et al.	
5,742,622	A	4/1998	Claydon et al.	
5,872,810	A	2/1999	Philips et al.	
5,880,631	A	3/1999	Sahota	
5,896,053	A	4/1999	Prentice	
5,901,347	A	5/1999	Chambers et al.	
6,009,126	A	12/1999	Van Bezooijen	
6,016,422	A	1/2000	Bartusiak	
6,029,059	A	2/2000	Bojer	
6,078,219	A	6/2000	Hadjichristos et al.	
6,108,529	A	8/2000	Vice et al.	
6,111,529	A	8/2000	Maulik et al.	
6,111,592	A	8/2000	Yagi	
6,141,169	A	10/2000	Pietruszynski et al.	
6,157,235	A	12/2000	Bautista et al.	
6,172,543	B1	1/2001	Kurusu	
6,321,073	B1 *	11/2001	Luz et al.	455/239.1
6,324,389	B1	11/2001	Vaisanen	
6,327,313	B1	12/2001	Traylor et al.	
6,356,131	B1	3/2002	Kuwano	
6,370,205	B1	4/2002	Lindoff et al.	
6,442,380	B1	8/2002	Mohindra	
6,459,889	B1	10/2002	Ruelke	
6,473,471	B2	10/2002	Lindquist et al.	
6,498,927	B2	12/2002	Kang et al.	
6,498,929	B1	12/2002	Tsurumi et al.	
6,504,498	B1	1/2003	O'Brien	
6,504,884	B1	1/2003	Zvonar	
6,507,241	B1	1/2003	Ritter	
6,507,732	B1	1/2003	Dajer et al.	
6,509,777	B2	1/2003	Razavi et al.	
6,516,183	B1	2/2003	Hellmark	
6,516,185	B1	2/2003	MacNally	
6,516,187	B1	2/2003	Williams et al.	
6,766,153	B2 *	7/2004	Kozak et al.	455/232.1
2002/0042256	A1	4/2002	Baldwin et al.	
2002/0123319	A1	9/2002	Peterzell	
2004/0071238	A1 *	4/2004	Khlat et al.	375/346

FOREIGN PATENT DOCUMENTS

EP	0 719 013	A2	6/1996
EP	0 729 230		8/1996
EP	0 729 230	A1	8/1996
EP	0 767 544		4/1997
EP	0 767 544	A	4/1997
EP	0 948 128		10/1999
EP	0 948 128	A1	10/1999
EP	0 964 557		12/1999
EP	0 964 557	A1	12/1999
EP	1 172 928		1/2002
EP	1 172 928	A2	1/2002
WO	WO-92/11704		7/1992
WO	WO-95/30275		11/1995
WO	WO 95/30275	A	11/1995
WO	WO-97/06604		2/1997
WO	WO 97/06604	A	2/1997
WO	WO-98/38799		9/1998
WO	WO 98/38799	A	9/1998
WO	WO-02/29985		4/2002

OTHER PUBLICATIONS

Bateman A., et al., "Direct Conversion Transceiver Design for Compact Low-Cost Portable Mobile Radio Terminals," IEEE Veh. Tech. Conf., 1989, pp. 57-62.

Cavers J., et al., "Adaptive Compensation for Imbalance and Offset Losses in Direct Conversion Transceivers," IEEE Transactions on Vehicular Technology, vol. 42, No. 4, Nov. 1993, pp. 581-588.

International Preliminary Examination Report on PCT/US01/49748, completed Jan. 14, 2003.

International Preliminary Report on Patentability for PCT/US2004/007408, issued Sep. 16, 2005.

International Search Report for PCT/US01/49748, mailed Aug. 5, 2002.

International Search Report for PCT/US01/49751, mailed May 7, 2002.

International Search Report for PCT/US01/50599, mailed Mar. 17, 2003.

International Search Report on PCT/US2004/007408, mailed Aug. 12, 2004.

PCT Notification of Transmittal of the International Search Report or the Declaration for PCT/US2001/050268 dated Apr. 2, 2002, 7 pages.

PCT Notification of Transmittal of the International Search Report or the Declaration for PCT/US2001/050268, dated Apr. 2, 2003, 5 pages.

PCT Notification of Transmittal of the International Search Report or the Declaration for PCT/US01/30807, dated Oct. 2, 2002, 8 pages.

Razvi B. "Design Considerations for Direct-Conversion Receivers," IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, vol. 44, No. 6, Jun. 1997, pp. 428-435.

Sampei S., et al., "Adaptive DC-Offset Compensation Algorithm for Burst Mode Operated Direct Conversion Receivers," IEEE Veh. Tech. Conf., 1992, pp. 93-96.

Tsukahara T., et al., "A 2-V 2-GHZ SI-Bipolar Direct-Conversion Quadrature Modulator," IEEE Journal of Solid State Circuits, vol. 31, No. 2, Feb. 1, 1996, pp. 263-267.

Tsurumi H., et al., "System-Level Compensation Approach to Overcome Signal Saturation, DC Offset, and 2nd-Order Nonlinear Distortion in Linear Direct Conversion Receiver," IEICE Transactions on Electronics, Institute of Electronics Information and Comm. Eng. Tokyo, JP, vol. E82-C, No. 5, May 1999.

PCT Notification of Transmittal of the International Preliminary Examination Report dated May 5, 2003, 6 pages.

* cited by examiner

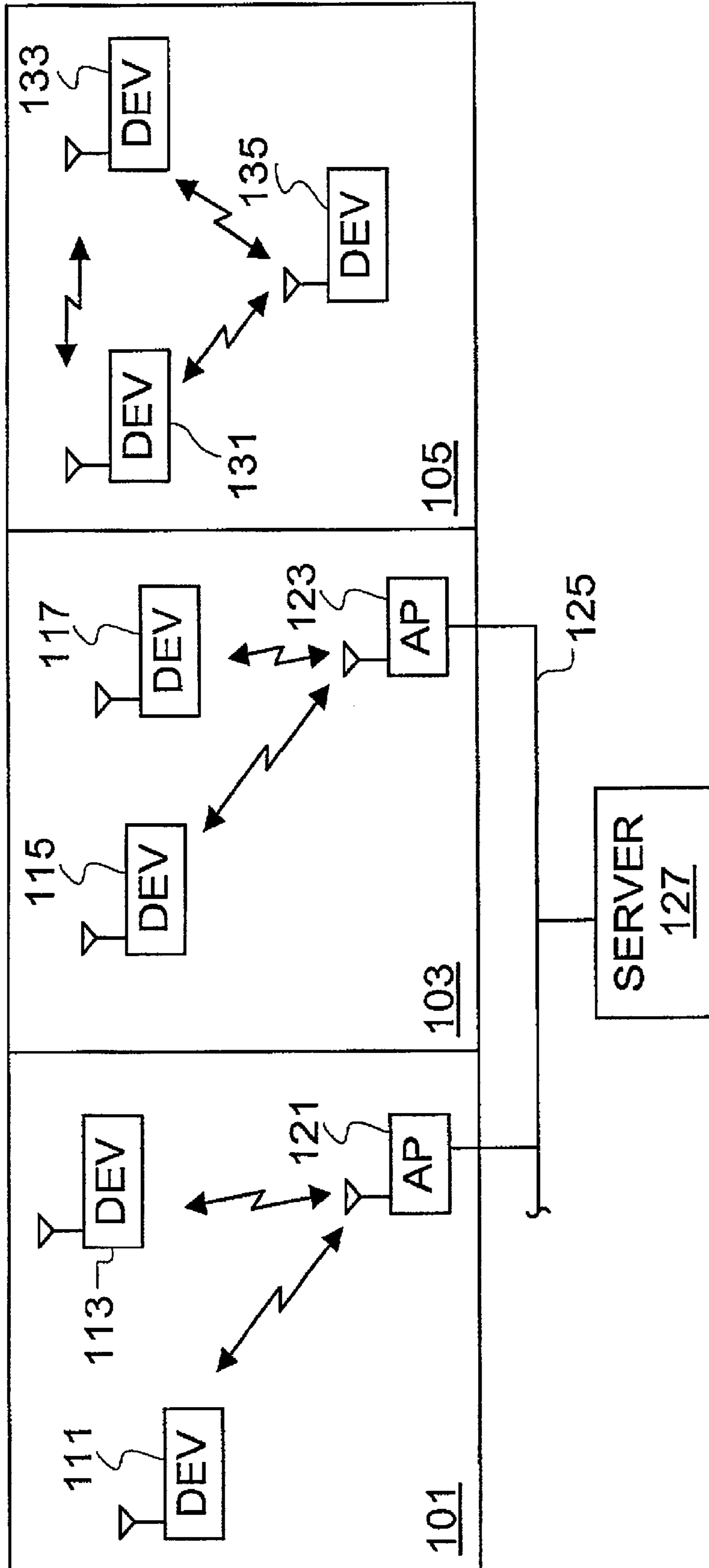


FIG. 1

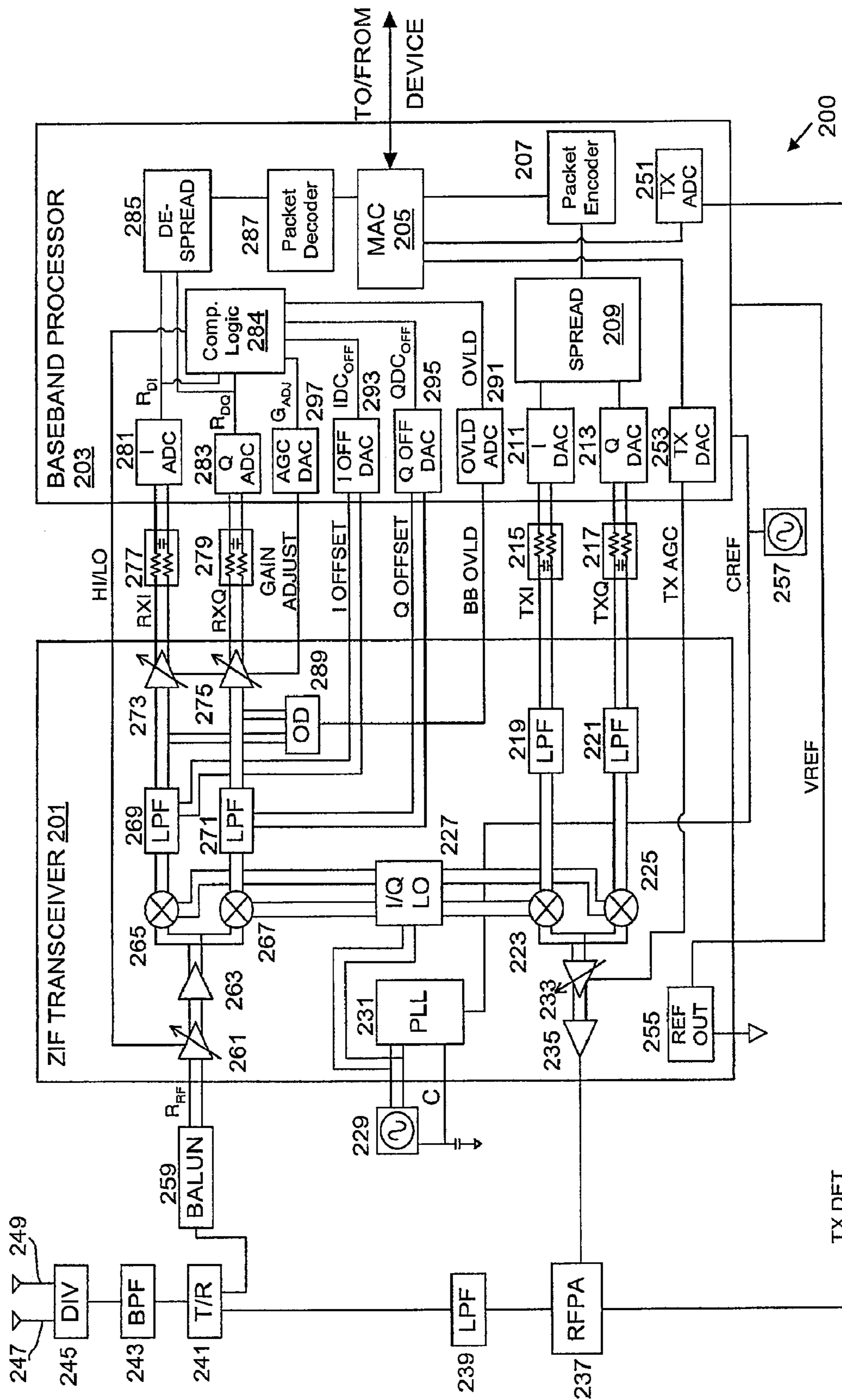


FIG. 2

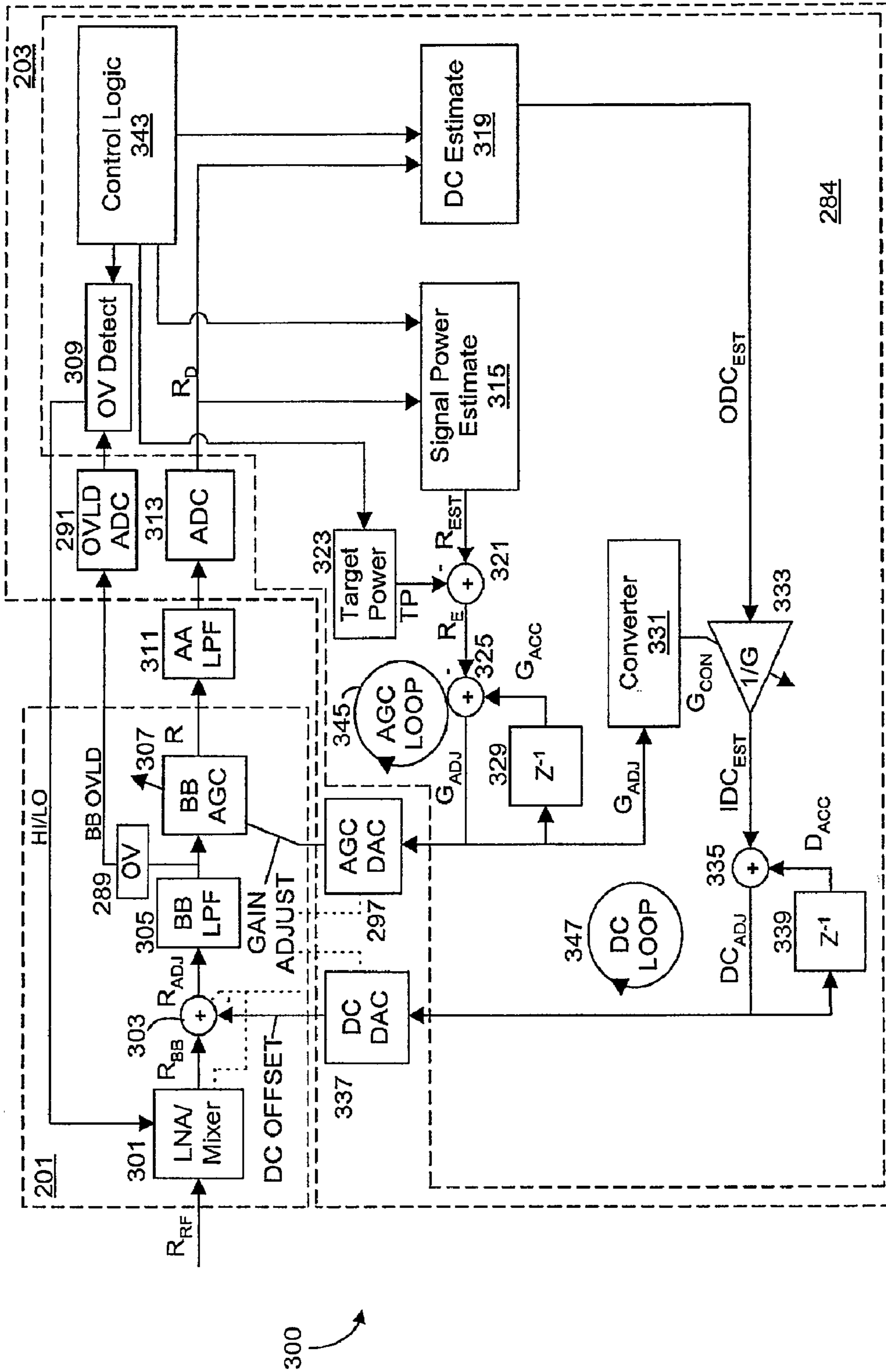


FIG. 3

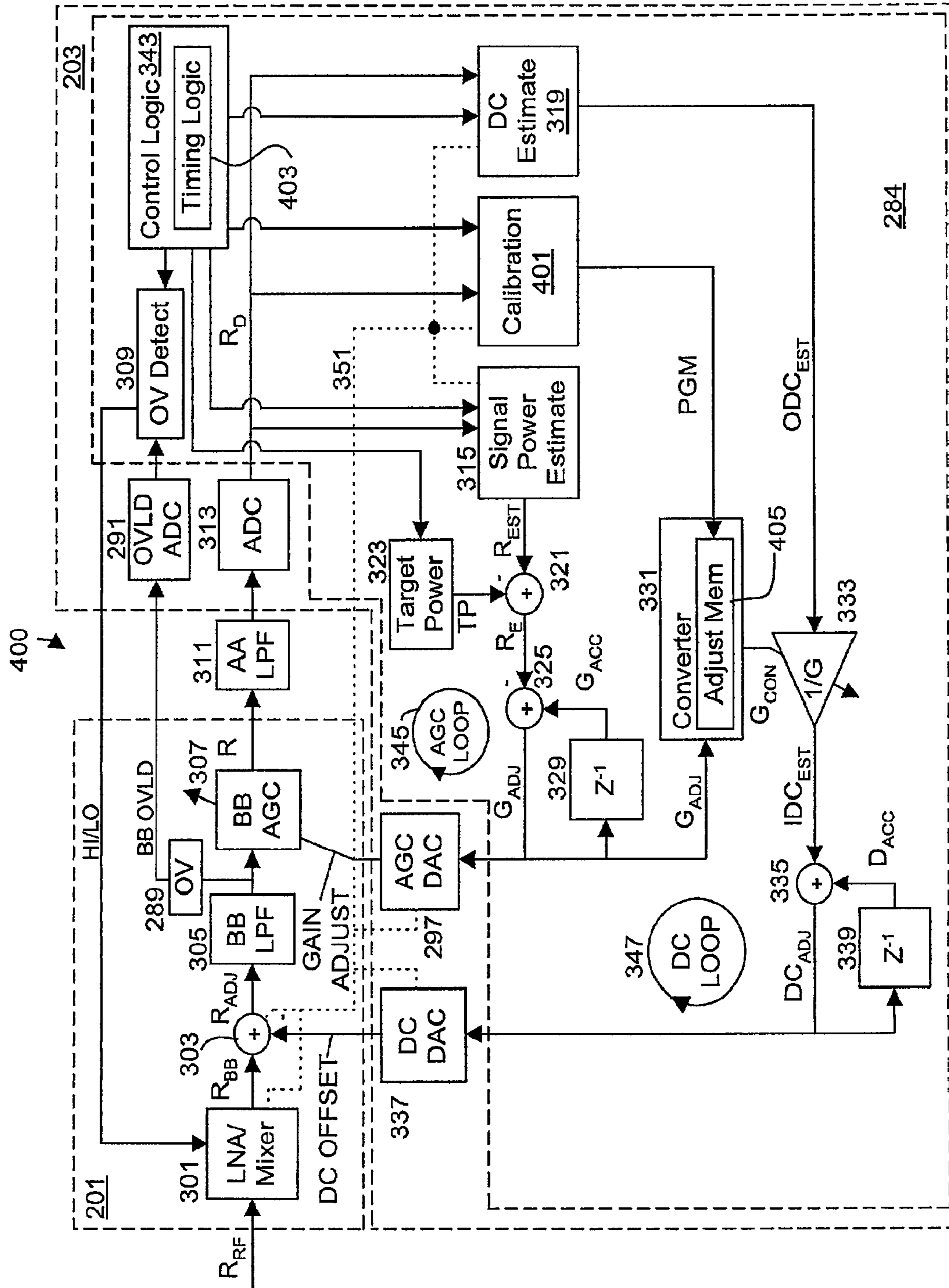


FIG. 4

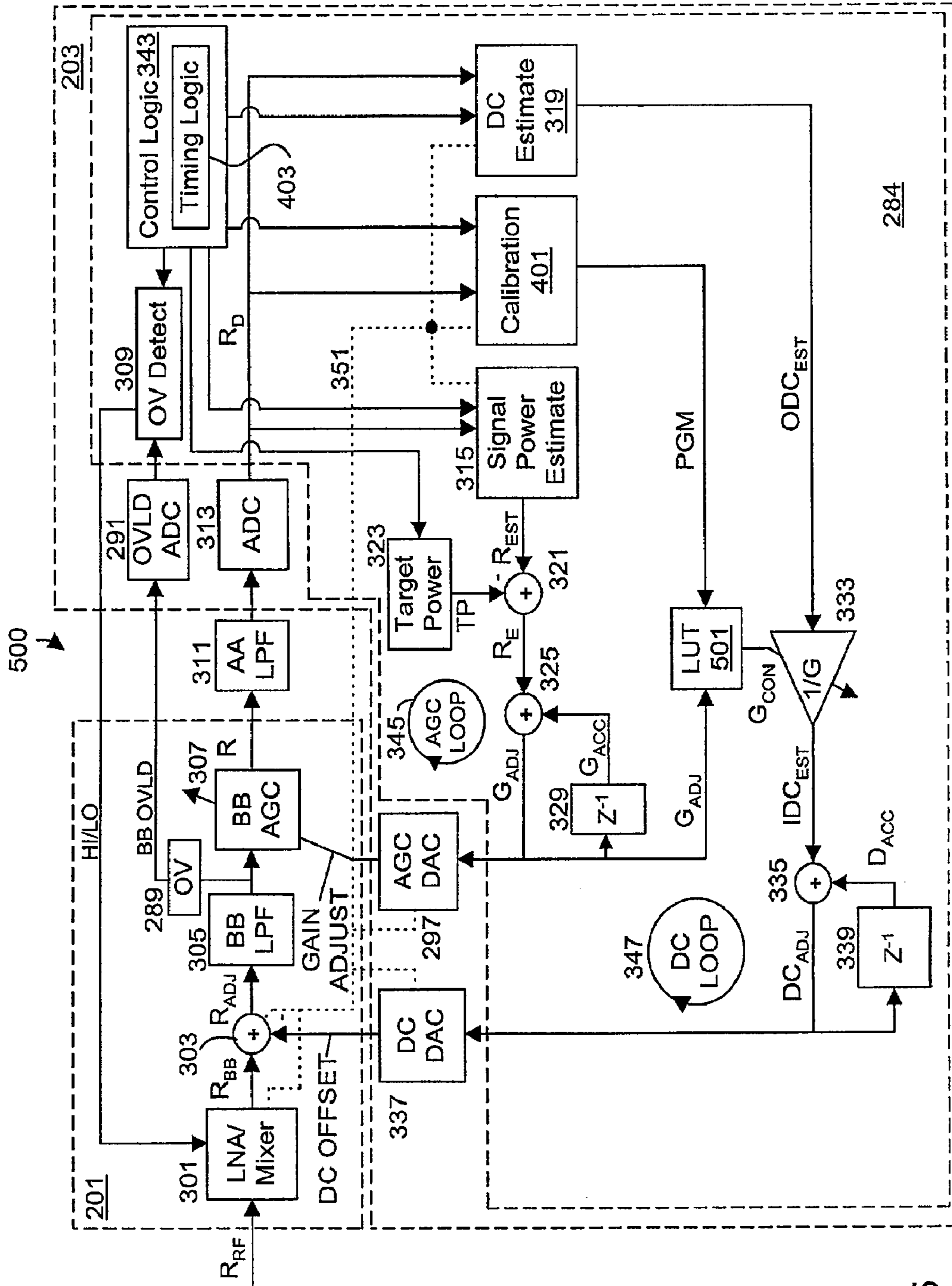


FIG. 5

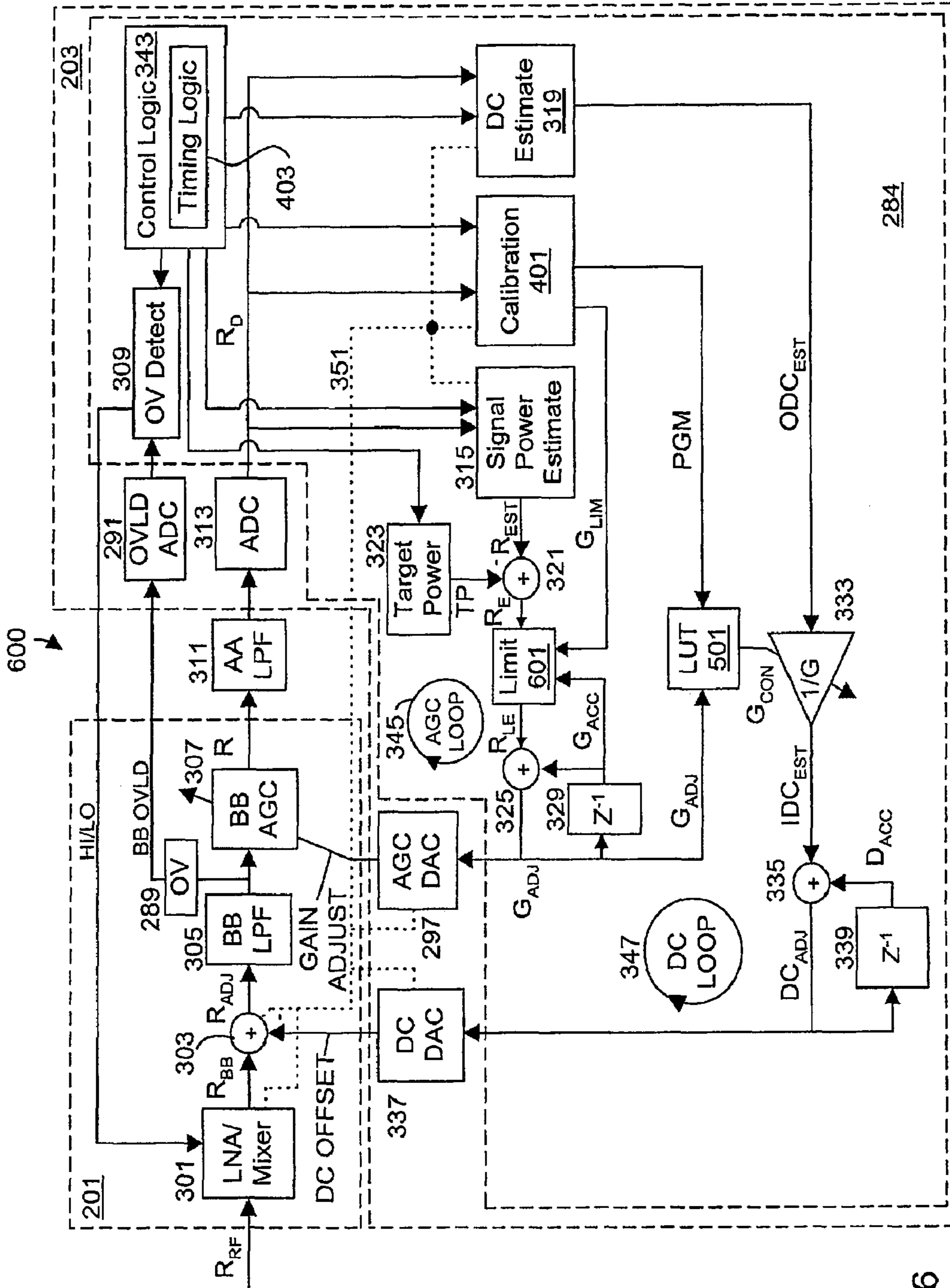


FIG. 6

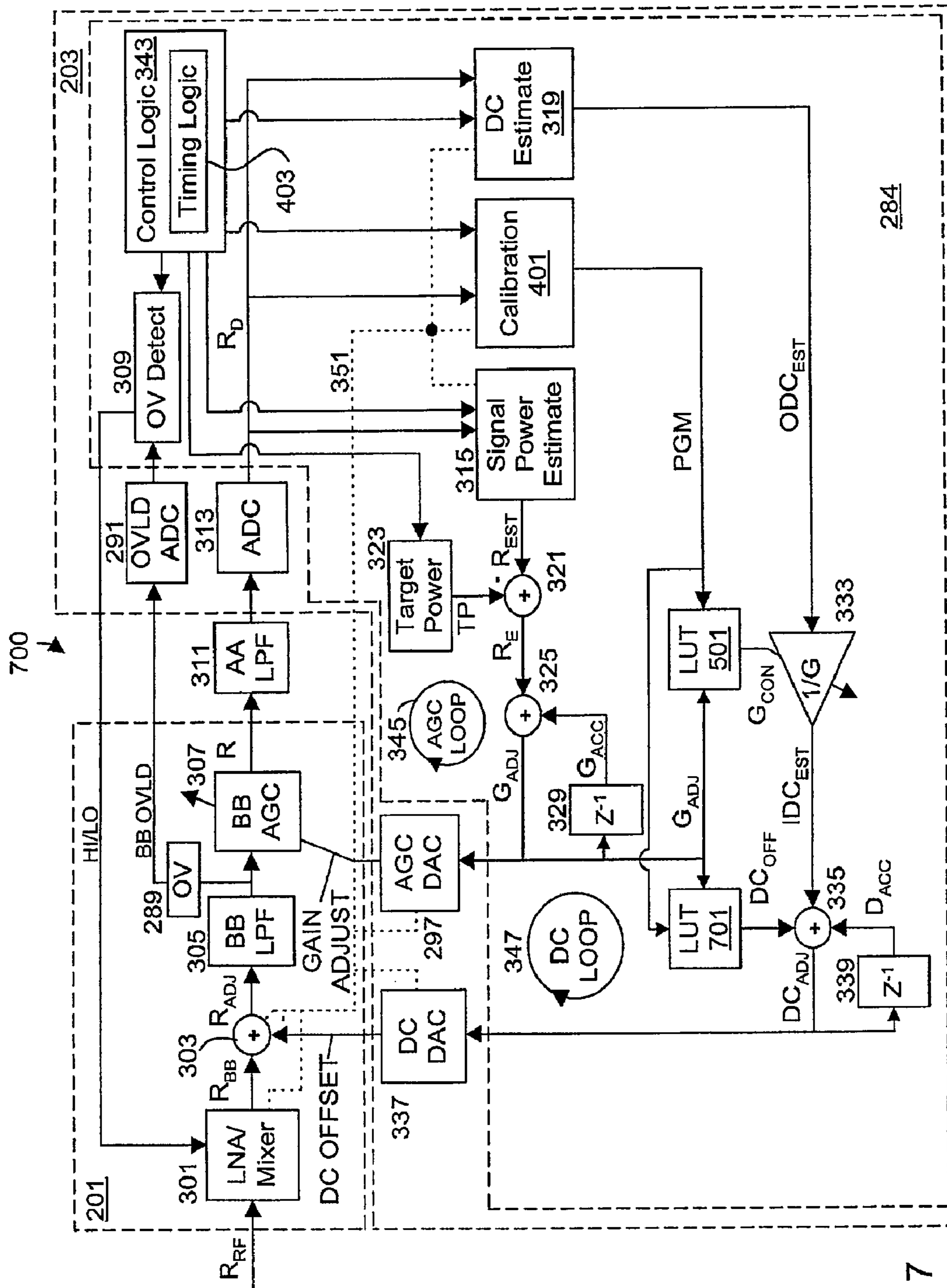
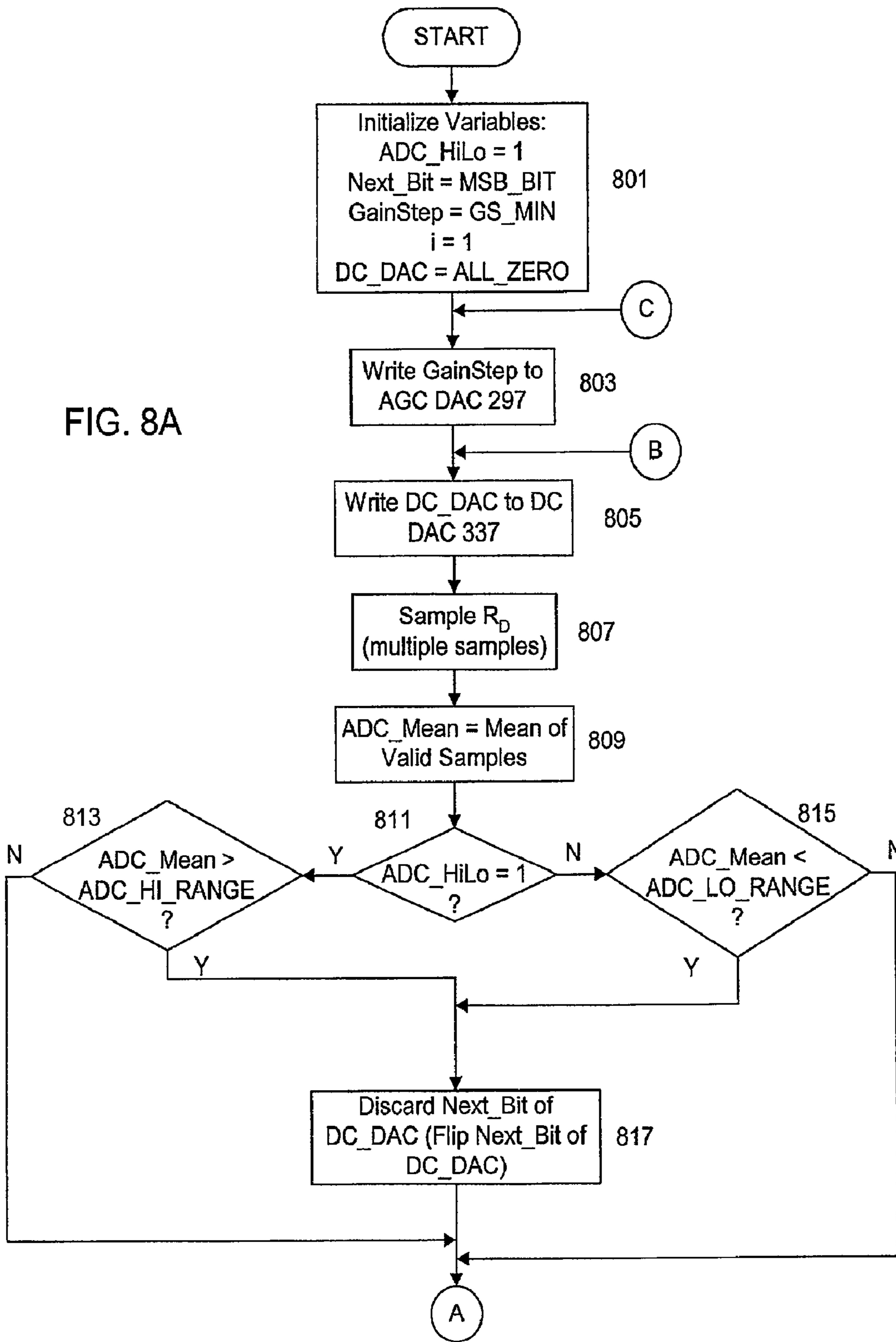


FIG. 7

FIG. 8A



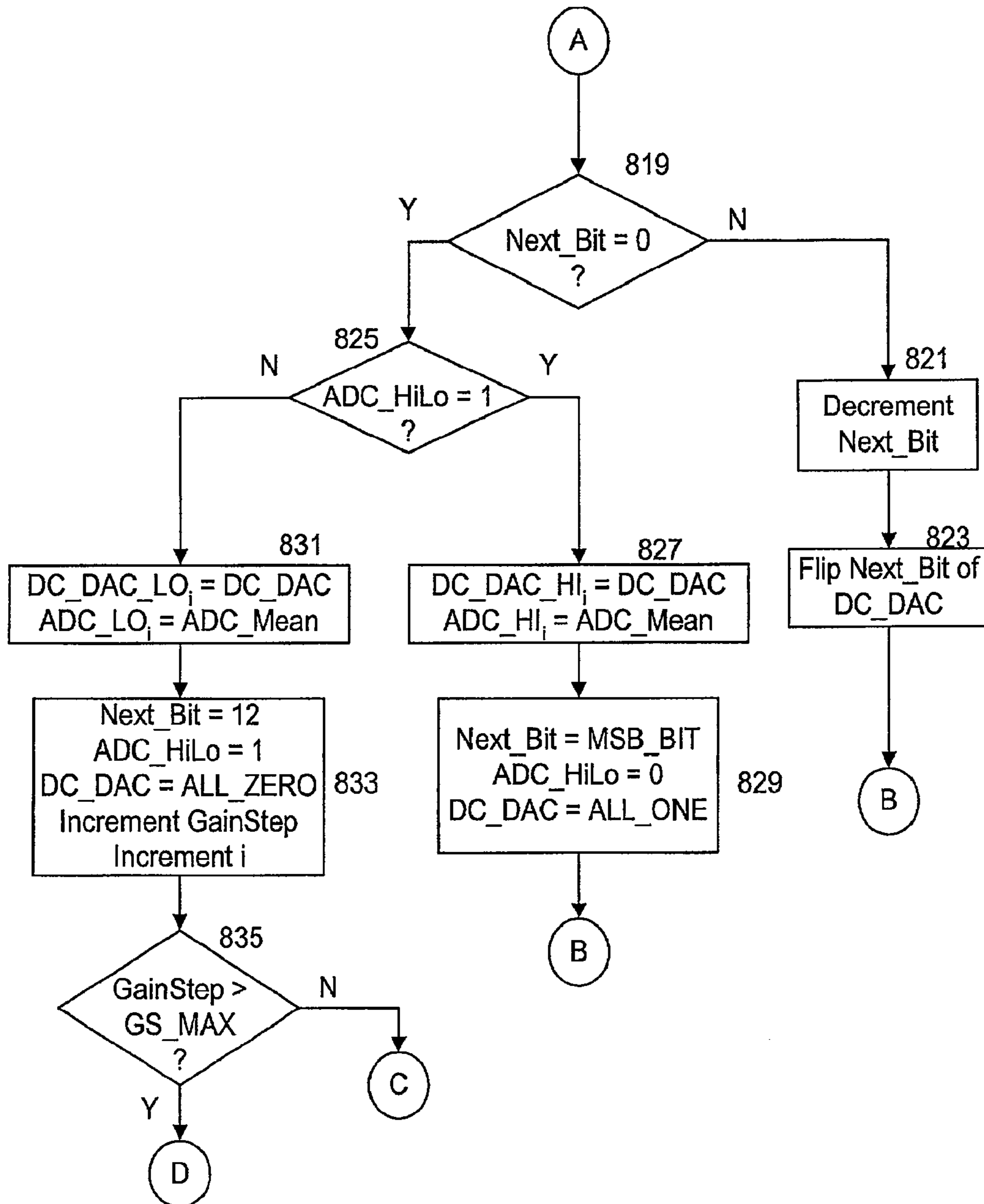


FIG. 8B

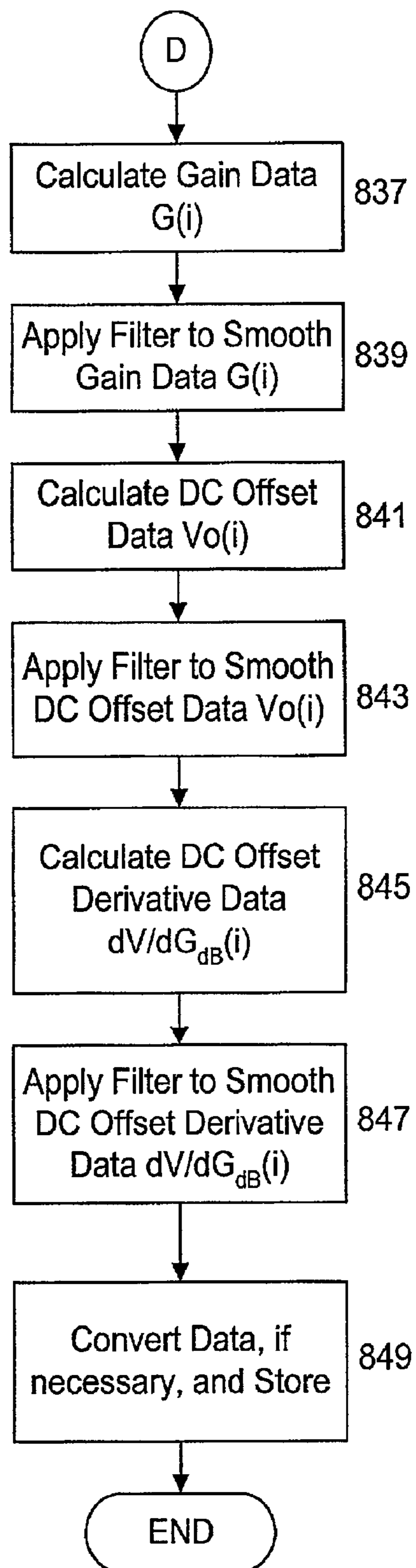


FIG. 8C

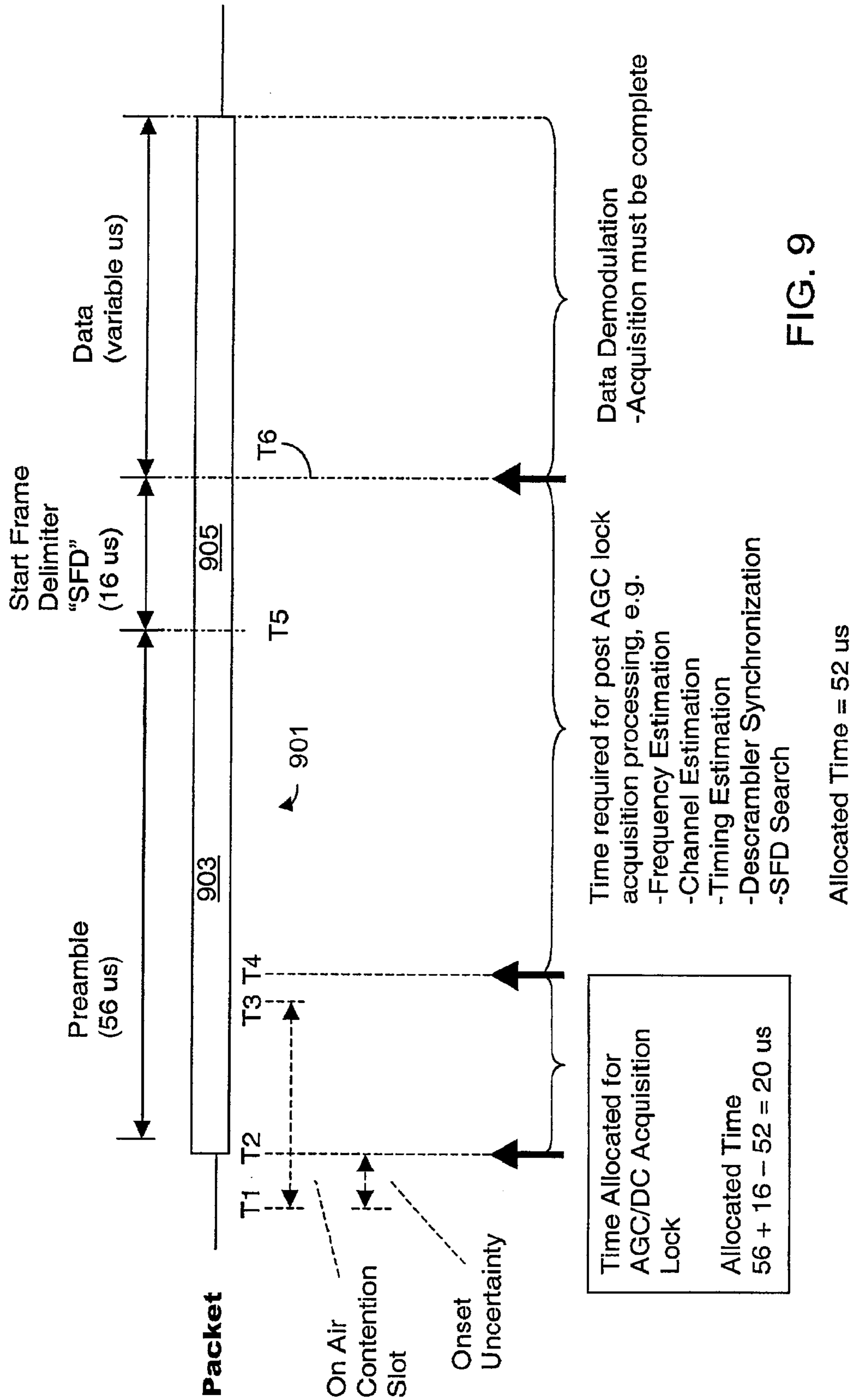


FIG. 9

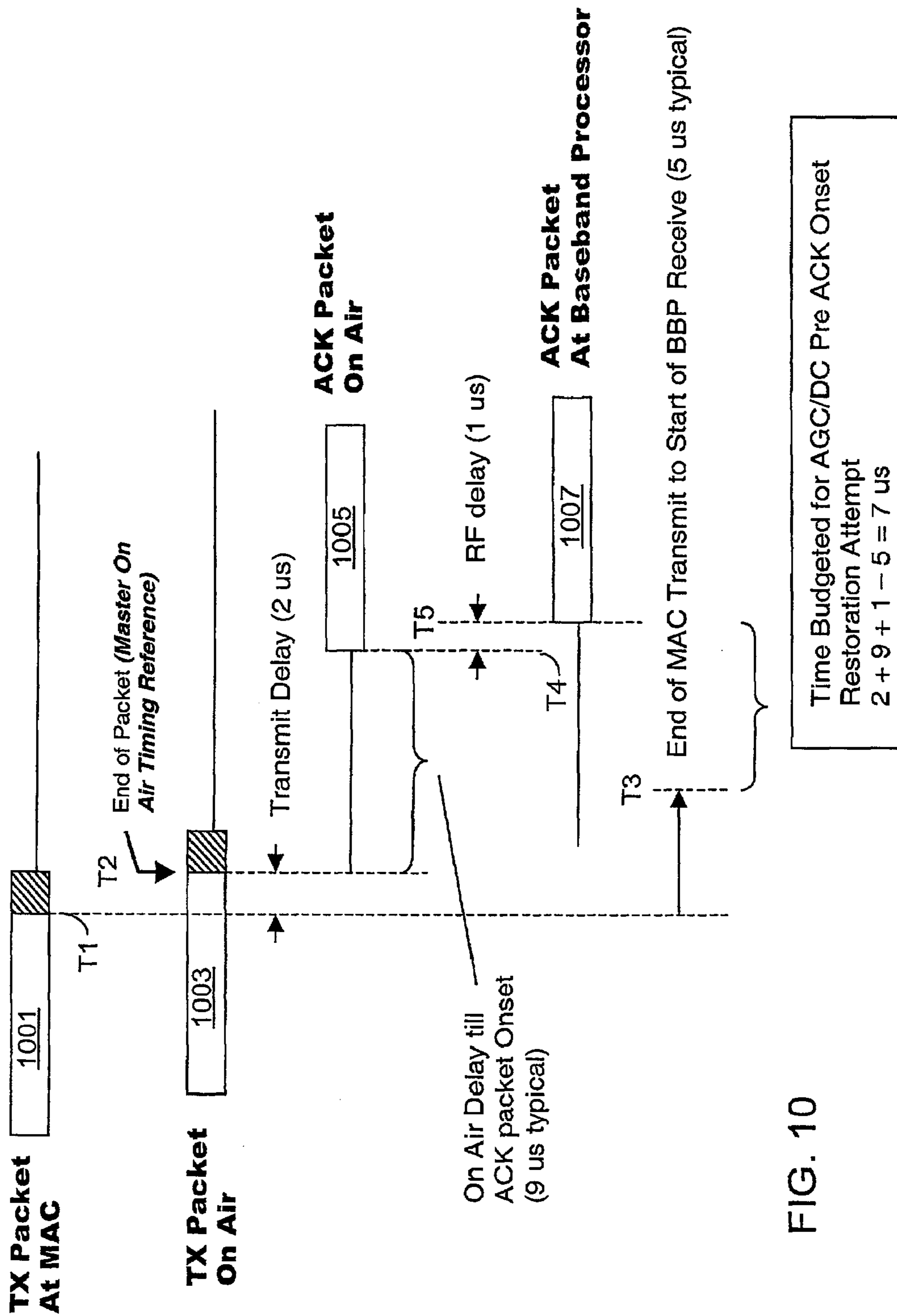


FIG. 10

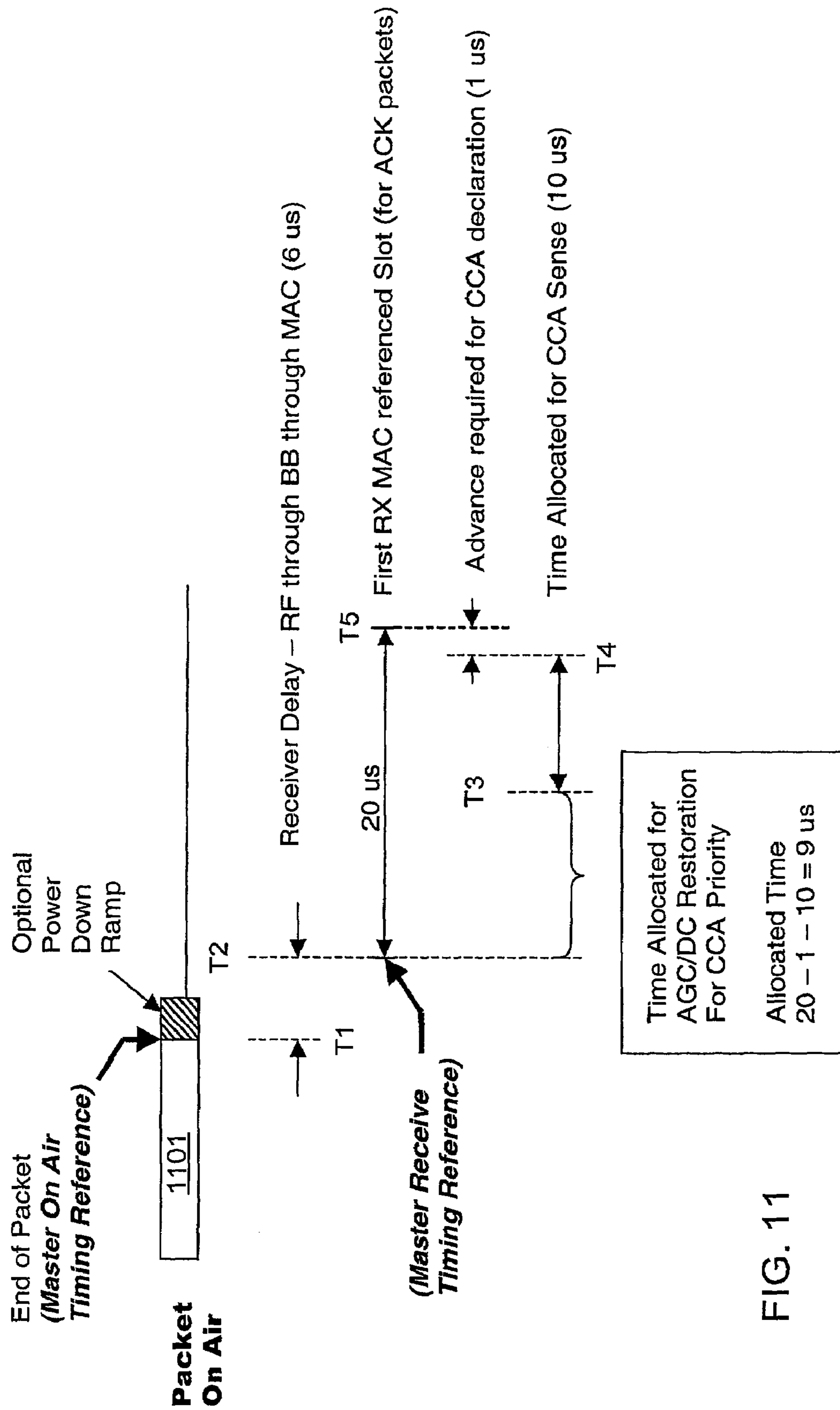


FIG. 11

**PACKET ACQUISITION AND CHANNEL
TRACKING FOR A WIRELESS
COMMUNICATION DEVICE CONFIGURED
IN A ZERO INTERMEDIATE FREQUENCY
ARCHITECTURE**

Matter enclosed in heavy brackets [] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

CROSS-REFERENCE TO RELATED
APPLICATION(S)

The present application is based on U.S. Provisional Patent Application entitled "Packet Acquisition and Channel Tracking For A Wireless Communication Device Configured In A Zero Intermediate Frequency Architecture", Ser. No. 60/259,731, filed Jan. 4, 2001, which is hereby incorporated by reference in its entirety. The present application is also a continuation-in-part (CIP) of U.S. Patent Application entitled "A Calibrated DC Compensation System For A Wireless Communication Device Configured In A Zero Intermediate Frequency Architecture", Ser. No. 09/677,975, filed Oct. 2, 2000, which is hereby incorporated by reference in its entirety.

FIELD OF THE INVENTION

The present invention relates to wireless communications, and more particularly to packet acquisition and channel tracking for a wireless communication device configured in a zero intermediate frequency (ZIF) architecture that utilizes a DC control loop to enable direct conversion of radio frequency signals to baseband frequency and a calibration procedure that more accurately determines and controls DC voltage levels.

DESCRIPTION OF RELATED ART

Network communication is a growing area of technology both for business and home applications. A network system enhances communication and provides a suitable environment for enhanced productivity and capabilities both at home and in the workplace. The Internet for example, is a global, mostly wired, communication network that couples devices together on a world-wide basis that enables world-wide communication between any devices coupled to the Internet. The Internet enables access to a plurality of services, such as file sharing, faxing, chat, email and information access via web-sites to files, libraries, databases, computer programs, etc.

Many businesses and commercial entities include a relatively established and sophisticated network environment for enhanced productivity and communication. For example, Extranets or Intranets provide enhanced yet protected or secure communication to a selected group of people on the Internet. Many small businesses and homes are coupled to the Internet via some variation of local area network (LAN) or the like. It is becoming more advantageous and common for small businesses and home environments to include LAN capabilities to connect to the Internet or to access other services, such as file sharing, printing, faxing, etc. and to further enable communication such as via chat and email services, and the like and to provide access to common databases and libraries, etc. Many such small networks are connected through a set of wires. For example, a network may be estab-

lished in a small office or home through standard phone wires. Phone wires are already available in each office of a business and in several rooms of a typical home. Technology also exists to establish network communications via power lines which are typically available in every room of a house. Many small offices and homes may alternatively be wired with network wires, such as a twisted-pair telephone wires with corresponding RJ-45 connectors utilized by various Ethernet embodiments.

Wired networks provide a certain level of convenience but have many limitations. Each device coupled to the network must be attached to a corresponding wire through which the network is established. The location of each device, therefore, is limited to enable access to the network wires. Cable management is also a significant issue, since devices must be placed to enable proper routing of wires. It is desired that the wires be conveniently placed and for aesthetic reasons, out of sight. Wires should be located in such a manner as to reduce or eliminate any chance of accidental interference or disconnect or hazards such as tripping. Once wired devices are properly placed, movement of the devices is very limited or otherwise not practical without substantial re-configuration or re-routing of the wires. Maintenance of wired network devices can be inconvenient and often requires that the wires be removed during service and then reconnected properly.

Certain wireless technologies are known, such as infrared technology. Infrared technology works well for certain applications, such as remote control systems or the like. For network applications, infrared technology is a relatively inexpensive option but has certain limitations, including limited bandwidth, range limitations, and line-of-sight issues. Infrared technology has been utilized in certain applications, such as access points (APs) and point to point relay nodes to extend a network down hallways and the like. For example, infrared devices are known for use in hospitals, hotels and other relatively large structures. The APs or nodes, however, are usually fixed and located in such a manner, such as on the ceiling, to avoid potential interference with physical objects. Due to line of sight issues, infrared technology is not particularly convenient for network communications at the end points of the network where human interaction is necessary.

Radio frequency (RF) technology appears to be the technology of choice for establishing a viable wireless local area network (WLAN). RF technology for LAN systems, however, is not particularly optimized for small office or home use. Wireless technology is established for industrial and commercial uses and applications such as courier services, vehicle rentals, warehouse operations and inventories, etc. The wireless embodiments for commercial and industrial applications are too expensive or otherwise specialized and thus are not suited for direct use in the small office or home environment.

The Bluetooth technology is being developed for application in the home or office. Bluetooth technology offers relatively limited bandwidth at very low cost to enable connectivity and network communications between certain communication devices, such as cellular phones, computer systems including notebook, laptop and desktop computers and further including other hand-held devices such as personal digital assistants (PDAs) or the like. The Bluetooth technology, however, has limited bandwidth and therefore relatively low data throughput capability. The consumer market demands higher data throughput and reliability such as is necessary for DVD and other multimedia applications.

The typical environment for a WLAN is very noisy and not optimal for wireless communications. For example, most homes include many electronic devices resulting in an elec-

tronically noisy environment that may interfere with WLAN communications, such as microwave ovens, garage door openers, radios, television sets, computer systems, etc. Further, the communication medium between wireless devices constantly changes. For example, most environments or rooms include multiple reflective surfaces creating multipath noise in the wireless environment. Furthermore, movement of items or devices or the like such as hands, bodies, jewelry, mouse pointers, etc. or activation of electronic devices, such as cooling fans or the like, affects the overall wireless communication path and potentially degrades wireless communication performance.

Low cost and low power wireless communication devices for enabling a WLAN system or the like for use at home or in the small business is desirable. It is further desired to provide low cost and low power wireless communication devices for any type of wireless system for any type of application. The system must be relatively robust with significant performance and be capable of significant data throughput.

SUMMARY OF THE INVENTION

A method of controlling operation of a wireless communication device configured in a zero intermediate frequency (ZIF) architecture including a DC feedback control loop and a gain feedback control loop according to embodiments of the present invention includes processing energy in a wireless medium to generate a corresponding receive signal, monitoring the receive signal via a predetermined measurement window, detecting a changed condition in the wireless medium, holding the gain feedback control loop at a constant gain level after detecting the changed condition, and operating the DC feedback control loop in an attempt to search a stable DC value for the receive signal while the gain loop is held constant. There are several changed conditions contemplated herein, including onset of a new packet causing DC saturation, completion of transmission of a packet for preparation of clear channel assessment (CCA), and completion of transmission of a packet and preparation for an expected acknowledgement (ACK) packet.

The processing of energy may involve processing the noise energy in the wireless medium while no packets are being transmitted. In this manner, the wireless communication device tracks the noise floor of the channel prior to the changed condition. The changed condition may include detecting DC saturation of the measurement window, which typically indicates or is otherwise caused by operation during onset of a new packet. In one embodiment, DC saturation is detected when the sampled receive signal "rails" to one side of a digital measurement window. In normal operation, the DC feedback control loop is operated in an attempt control the DC level of the receive signal to within a predetermined maximum DC threshold level so that the gain loop may lock on the signal. However, DC saturation calls for a different procedure to quickly change the DC level of the receive signal so that the incoming signal is not obscured and is observable in the limited measurement window. Upon DC saturation, the gain feedback control loop is held and the DC feedback control loop is operated to add opposite polarity DC to the receive signal to remove the DC saturated condition. When the DC saturation condition is removed, the gain feedback control loop is released to control the power level of the receive signal to a predetermined target power level.

The method may further include detecting gain saturation in which the measurement window is clipped at both of predetermined minimum and maximum values above a predetermined clip rate and in which clipping is relatively balanced

between the predetermined minimum and maximum values. In the event of gain saturation, the method may further include operating the gain feedback control loop to perform a clip-step procedure to reduce the gain of the receive signal. In one embodiment, the clip-step procedure includes using a graduated clip gain adjustment in which gain is adjusted based on an amount of clipping of the receive signal.

The method may further include processing noise energy in the wireless medium while no packets are being transmitted, operating the gain feedback control loop until a noise floor gain value is determined, and storing the noise floor gain value. For expected ACK packet acquisition, the method may further include detecting an end of transmission of a packet in the wireless medium (such as by indication of a local MAC), retrieving and applying the stored noise floor gain value in the gain feedback control loop, holding the gain at the retrieved noise floor gain value during a predetermined quiet period, and releasing the gain feedback control loop to operate in normal mode after expiration of the quiet period. In this case, it is expected that the wireless medium has not changed significantly after transmission of only one packet, so that the gain is retrieved as soon as possible after the device transmits a packet in order to facilitate re-establishing control the gain loop as soon as possible. The method may further include determining a DC noise value of the DC feedback control loop prior to transmission of the packet (while tracking the noise floor of the wireless medium), storing the DC noise value, and retrieving and applying the DC noise value to the DC feedback control loop after detecting the end of transmission of the packet. In this case, the gain of the DC loop is also restored to the same level it was prior to packet transmission in order to facilitate re-establishing control the DC loop as soon as possible after packet transmission.

In order to perform CCA, the method may further include detecting an end of transmission of a packet being transmitted in the wireless medium, retrieving and applying the stored noise floor gain value in the gain feedback control loop for a predetermined period of time, and determining whether the DC feedback control loop converges to a stable DC level within the predetermined period of time. In this case, it may be determined that the wireless medium is busy if the DC feedback control loop does not converge to a stable DC level within the predetermined period of time. This may occur if another device is transmitting a packet, such as an ACK packet in response to the original packet detected in the channel, or if some other channel phenomenon is preventing convergence of the DC loop. In either case, the wireless device backs off and does not attempt packet transmission until after CCA is determined.

A method of operating a wireless communication device (including gain and DC loops) to perform initial acquisition of a packet being transmitted in a wireless medium includes processing radio frequency (RF) energy in the wireless medium to generate a corresponding receive signal, determining if a DC threshold condition of the receive signal is exceeded, and if so, holding the gain feedback control loop at a constant gain level and operating the DC feedback control loop to reduce DC of the receive signal until the DC threshold condition of the receive signal is met, and, when the DC threshold condition of the receive signal is met, operating the DC feedback control loop to control the DC level of the receive signal and operating the gain feedback control loop to control a power level of the receive signal to a predetermined target power level.

This latter method is more particular to onset of a new packet in the wireless medium. In one embodiment in which the receive signal is an analog signal, the method may include

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sampling the receive signal with an analog to digital converter (ADC) to generate corresponding digital samples, where the ADC has a sufficient range to maintain signal integrity without covering a total potential signal range of the receive signal. In this case, DC saturation is determined when a DC threshold condition is exceeded. The digital samples may range between a minimum value and a maximum value, where the DC threshold condition is exceeded when a percentage of digital samples at the minimum value or a percentage of digital samples at the maximum value exceeds a predetermined threshold percentage of a total number of digital samples. For example, this may occur when the number of clipped signals at one rail exceeds a predetermined clipping rate. The predetermined clipping rate is arbitrarily determined depending upon the particular configuration, but is typically a relatively high percentage, such as 90% or the like.

When the DC threshold condition is exceeded, the method includes operating the DC feedback control loop by adding DC to the receive signal. Several methods are contemplated, including conducting a step search procedure by repeatedly adding a predetermined DC amount until the DC threshold condition is met. The predetermined DC amount may be any arbitrary value, but should be selected to avoid overshooting the gain window and thus may be related to the relative size of the measurement window. In an alternative embodiment, the method includes performing a successive approximation DC search procedure until the DC threshold condition is met. In this case, a binary search or the like is performed to converge on the applicable DC level. The step search procedure may take longer than the successive approximation technique in many cases, but is sufficient, simple, and relatively easy to implement.

The method may further include detecting a gain saturation state in which clipped digital samples occur at both of the minimum and maximum levels at a rate greater than a predetermined clip ratio threshold and in which a number of digital samples at the minimum level is relatively balanced with a number of digital samples at the maximum level. The balance may be as rough or accurate as desired, such as 3:1, 2:1 or as close to 1:1 as desired. When the gain saturation state is detected, the method includes operating the gain feedback control loop in a clipping mode while in the gain saturation state. The clipping mode may involve adjusting the gain level of the gain feedback control loop based on an amount of clipping using a graduated clip gain adjustment. The graduated clip gain adjustment may include a corresponding one of a predetermined plurality of gain level adjustments for each of a plurality of predetermined clip ratio ranges. The graduated clip gain adjustment may be graduated between a high gain adjustment for a high clip ratio and a low gain adjustment for a low clip ratio.

A method of operating a wireless transceiver device in preparation for an expected ACK packet includes holding a gain level of the gain feedback control loop constant after a packet is transmitted and during a predetermined quiet period, operating the DC feedback control loop during the predetermined quiet period in an attempt to resolve DC level while the gain feedback control loop is held, and releasing the gain feedback control loop to operate in a normal packet acquisition mode after the quiet period. In this case, the method may include storing a gain level value of the gain feedback loop before the packet was transmitted and retrieving the stored gain level value and holding the gain feedback control loop at the retrieved gain level value during the predetermined quiet period after transmission of the packet. Also, the method may include storing a DC value of the DC feedback control loop before transmission of the packet and

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applying the stored DC value after packet transmission. In this method, the wireless transceiver device may be the device that transmits the packet and expects to receive the ACK packet, or the wireless transceiver device may be a different device operating in ACK priority mode, such as network monitor or analyzer operating in a "sniffer" mode or the like to analyze protocol.

A method of operating a wireless communication device to determine CCA of a wireless medium includes storing a gain level value of the gain feedback control loop, detecting a packet being transmitted, retrieving the stored gain level value and holding the gain feedback control loop at the retrieved gain level value after transmission of the packet is completed, operating the DC feedback control loop to search a stable DC level, and determining whether the DC loop converges to a stable DC level. Again, the gain level value may be determined and stored while tracking the wireless medium with no packets being transmitted. Also, the method may include storing a DC value of the DC feedback control loop before detecting a packet being transmitted, and applying the stored DC gain setting after packet transmission. Further, the method may include holding the gain level of the gain feedback control loop constant during a predetermined quiet period, and releasing the gain feedback control loop after the predetermined quiet period to operate in a normal mode. In this case, the method may include determining if the DC feedback control loop converges to a stable DC level within a predetermined period, and if so, operating the DC feedback control loop and the gain feedback control loop in a normal mode. The wireless medium is determined to be busy if the DC feedback control loop does not converge to a stable DC level within a predetermined period of time.

BRIEF DESCRIPTION OF THE DRAWINGS

A better understanding of the present invention can be obtained when the following detailed description of one or more embodiment(s) of the invention is considered in conjunction with the following drawings, in which:

FIG. 1 is a block diagram of one or more wireless LANs generally illustrating operation of wireless devices implemented according to one or more embodiments of the present invention.

FIG. 2 is a simplified schematic and block diagram of a wireless transceiver in a Zero Intermediate Frequency (ZIF) architecture and implemented according to an embodiment of the present invention that may be incorporated within any of the devices or access points of FIG. 1.

FIG. 3 is a block diagram of a compensation system utilized to control the gain of the received signal and to reduce or eliminate DC offsets in the wireless transceiver of FIG. 2.

FIG. 4 is a block diagram of a calibrated DC compensation system similar to the compensation system of FIG. 3 that further includes a calibrator that periodically performs a calibration procedure and a programmable adjust memory provided in the gain interface between the gain loop and the DC loop to more accurately determine and control DC.

FIG. 5 is a block diagram of a calibrated compensation system similar to the compensation system of FIG. 4 that uses a lookup table as the gain interface between the gain loop and the DC loop.

FIG. 6 is a block diagram of a calibrated compensation system similar to the compensation system of FIG. 5 with the inclusion of a limit block in the gain loop to limit gain change.

FIG. 7 is a block diagram of a calibrated compensation system similar to the compensation system of FIG. 5 with the

inclusion of an additional lookup table that stores and provides one or more DC adjust values to further adjust the DC loop.

FIGS. 8A-8C are flowchart diagrams illustrating a calibration procedure that determines gain, DC offset and derivative data.

FIG. 9 is a timeline diagram illustrating gain and DC loop timing for normal packet onset of a short preamble packet, indicative of timing necessary for all packets.

FIG. 10 is a timeline diagram illustrating timing of ACK packet priority acquisition at end of packet transmission.

FIG. 11 is a timeline diagram illustrating CCA priority acquisition end of packet timing for the wireless transceiver of FIG. 2.

DETAILED DESCRIPTION OF EMBODIMENT(S) OF THE INVENTION

FIG. 1 is a block diagram of one or more WLANs generally illustrating operation of wireless devices implemented according to one or more embodiments of the present invention. Although the present invention is illustrated for use with WLANs in exemplary embodiments, it is understood that the present invention applies for any radio or wireless communications and is not limited to WLAN applications. A first area **101** and a second area **103** represent separate compartments or divisions of a location such as offices within an office building or rooms within a house. The areas **101** and **103** may each include wireless access points (APs) **121** and **123** for controlling communications within the respective areas **101** and **103**. As shown, the APs **121**, **123** are coupled to a wired network such as a LAN **125**, which is further coupled to a common server computer **127**.

Within the area **101**, wireless devices **111** and **113** are able to communicate with each other via the AP **121**, and within the area **103**, wireless devices **115** and **117** are able to communicate with each other via the AP **123**. The AP **121** enables the devices **111** and **113** to communicate to the server **127** via the LAN **125** and the AP **123** also enables the devices **115** and **117** to communicate to the server **127** via the LAN **125**. It is further noted that the LAN **125** enables the devices **111**, **113**, **115** and **117** to communicate with each other and with any other device coupled thereto.

APs, if used, are usually connected to a wired LAN, such as the LAN **125**, although they need not be. The number and location of APs usually depends on the particular configuration and needs, such as the number of users served, range of coverage, and/or adjacent channel interference. It is noted that a single AP can serve a whole floor of rooms subject to user density and interference. Multiple APs are used much like cells in cellular communication. Adjacent APs may operate on adjacent channels to prevent interference. Roaming capability may be enabled to allow devices to move from one area to another, such as from area **101** to **103** and vice versa. Generally, each AP has additional software and has access to house or building main power.

An alternative embodiment is shown by area **105** including devices **131**, **133** and **135**. The devices **131**, **133** and **135** communicate directly with one another rather than via any APs. Networks without APs are ad hoc in nature and typically contain fewer clients. The primary difference between the devices **111**, **113**, **115** and **117** from the devices **131**, **133** and **135** is the mode of operation. Each of the wireless devices **111**, **113**, **115**, **117** and **131**, **133**, **135** includes a wireless transceiver that may be implemented according to an embodiment of the present invention for enabling wireless communications.

The devices **111**, **113**, **115**, **117**, **131**, **133**, and **135** may be any type of device that includes wireless communication capabilities. In an office or home environment for example, the devices may each comprise any one or more personal computers, laptop computers, desktop computers, etc., printing devices including any type of printer technology, personal digital assistants (PDAs) or the like, scanners, fax machines, etc. The use of wireless technology enables any of the devices to be located anywhere within a given area to communicate with, and transfer data and information between, other devices within the same communication area. For example, the device **111** may be a computer that wirelessly communicates to the device **113** which may be a printer. Further, the device **111**, as a computer, may send and receive files to the server **127**. The device **111** may be moved to the area **103** from area **101** and still maintain communication with the LAN **125** and the server **127** via the AP **121**. The LAN **125** may comprise any type of wire technology, such as telephone wires, power wires, twisted-pair, coaxial cables, etc., and may be implemented according to any type of suitable architecture, such as any type of Ethernet configuration or the like. It is further noted that a wireless LAN **125** is contemplated, where the APs **121**, **123** include corresponding wireless transceivers and are mobile or portable devices. Within the area **105**, the devices **131-135** themselves establish a wireless LAN (WLAN) for communicating to each other in a similar fashion.

FIG. 2 is a simplified schematic and block diagram of a wireless transceiver **200** implemented according to an embodiment of the present invention that may be incorporated within any of the devices **111**, **113**, **115**, **117**, **131-135** and in either or both of the APs **121**, **123**. It is understood, however, that the wireless transceiver **200** is not limited to WLAN configurations, which are exemplary only, but instead may be employed in other types of radio or wireless communications for other types of applications. The wireless transceiver **200** is implemented as a zero intermediate frequency (ZIF) architecture including a ZIF transceiver **201** and a baseband processor **203**. As described more fully below, the ZIF architecture enables a simplified configuration by entirely eliminating intermediate frequency (IF) logic and associated circuitry. In this manner, only two primary modules, chips, or ICs (transceiver and processor) are utilized in the ZIF architecture to enable wireless communications. This, in turn, significantly reduces the number of components, reduces cost and further reduces power consumption of the wireless transceiver **200** as compared to similar transceivers including IF circuitry and logic.

A problematic characteristic of traditional ZIF architectures is the introduction of substantial DC offset voltages in the receiver that must be compensated for or otherwise eliminated to capture incoming signals and allow communications. The wireless transceiver **200** is configured with an automatic gain control (AGC) loop **345** (FIG. 3) combined with a DC loop **347** to measure and reduce or otherwise eliminate undesired DC in the receiver. As described further below, the AGC loop **345** includes gain control logic that receives an amplified input signal, that estimates input signal power and that asserts a gain adjust signal in an attempt to keep the input signal power at a target power level. The DC loop **347** includes DC control logic that estimates an amount of DC in the amplified input signal and that provides a DC offset in an attempt to reduce DC in the amplified input signal. Also, a gain interface is provided that converts gain levels between the gain control logic and the DC control logic.

The wireless transceiver **200** may utilize any desired carrier frequency and modulation technique to achieve any of several corresponding data throughputs. For example, the wireless transceiver **200** may be configured to operate according to the Institute of Electrical and Electronics Engineers (IEEE) 802.11b with a carrier frequency of approximately 2.4 gigahertz (GHz) and with data throughputs of 1, 2, 5.5 or 11 Megabits per second (Mbps). Alternatively, the wireless transceiver **200** may be configured according to IEEE 802.11a with a carrier frequency of approximately 5 GHz for data throughputs of 6, 12, 18, 24, 36 or 54 Mbps. In the embodiment shown, the wireless transceiver **200** operates in accordance with IEEE 802.11b at a carrier frequency of 2.4 GHz with data throughput rates of 1, 2, 5.5 or 11 Mbps. The direct sequence spread spectrum (DSSS) modulation technique is used in the embodiment shown, although it is understood that the present invention is not limited to any particular communication or modulation technique or standard.

Any of the devices **111-117** or **131-133** or the APs **121, 123** may be configured according to the wireless transceiver **200**. The particular configuration depends upon the type of device and communication interface. The wireless transceiver **200** may be configured as a plug-in peripheral or expansion card that plugs into an appropriate slot or interface of a computer system. For example, for portables and laptop computers and the like, the wireless transceiver **200** may be implemented as a Personal Computer Memory Card International Association (PCMCIA) card or PC Card that plugs into a PC Card slot of the computer. The antenna may be incorporated on the PC Card itself, or provided externally or on the computer and interfaced to the PC Card in any appropriate manner. For desktop computers and the like, the wireless transceiver **200** may be implemented according to any type of expansion or peripheral standard, such as according to the peripheral component interconnect (PCI), the Industry Standard Architecture (ISA), the Extended-ISA (EISA) standard, etc. For example, the wireless transceiver **200** may be implemented on a PCI card that plugs into a PCI slot. Again, the antenna may be integrated or coupled externally. Mini PCI cards with antennas embedded in displays are also contemplated. Self-contained or standalone packaging with appropriate communication interface(s) is also contemplated, which is particularly advantageous for APs. For example, the wireless transceiver **200** may be implemented as a separate unit with serial or parallel connections, such as a Universal Serial Bus (USB) connection or an Ethernet interface (twisted-pair, coaxial cable, etc.), or any other suitable interface to the device.

Digital data sent from or received by the wireless transceiver **200** is processed through a medium access control (MAC) device **205**. For transmission, the MAC device **205** asserts digital data signals to a packet encoder **207**, which formulates the data into packets for transmission. In packet encoder **207**, a packet is formed by the concatenation of three serial bit streams. The first serial bit stream, referred to as the preamble, is a 1 Mbps stream of ones or zeroes followed by a synchronization (sync) pattern. The second serial bit stream, referred to as the header, is a 1 or 2 Mbps stream of packet information, such as packet length and the data rate of the data portion of the packet. The third serial bit stream, referred to as the data portion or payload, is any selected one of 1, 2, 5.5, or 11 Mbps streams of data.

The packet encoder **207** provides baseband encoded packets to a spreading encoder (SPREAD) **209**. In the embodiment shown, the 1 and 2 Mbps bit rates are encoded according to Barker word encoding spreading, whereas the 5.5 and 11 Mbps bit rates are encoded according to Complementary

Code Keying (CCK) encoding. The spreading encoder **209** uses a quadrature generation technique and provides in phase (I) and quadrature (Q) signals on respective I and Q channels. For 1 Mbps, every bit in 11 chips of a Barker word are output identically on the I and Q channels. If the input bit is zero, then the sense of the 11 chips is inverted, and if the input bit is one, the sense of the 11 chips is not inverted. The data is thus spread by the Barker code. For 2 Mbps, for every two bits input, 11 chips are output on each of the I and Q channels. One bit is used to invert or not the I channel and the other bit is used for the Q channel. For 5.5 Mbps, 4 bits are mapped to 8 complex (I and Q channel) chips. 8 chip complex code words are chosen and then rotated according to specific rules defined in the standard. 11 Mbps is similar to 5.5 Mbps, except that 8 bits are mapped to 8 complex chips.

The I channel signal is provided to an I digital-to-analog converter (I DAC) **211** and the Q channel signal is provided to a Q DAC **213**, where the I DAC **211** and the Q DAC **213** also receive a clock signal CREF from a clock source **257**. In one embodiment, the CREF signal is 44 MHz based on the 22 MHz fundamental for IEEE 802.11b. The I DAC **211** and the Q DAC **213** up-sample and digitally filter the I and Q channel signals, respectively. For 11 Mbps, the I and Q DACs convert each chip to four samples. The I DAC **211** asserts an I channel analog output signal to an anti-aliasing low-pass filter (AA LPF) **215**, which provides an I channel transmit signal TX1 to an LPF **219** within the ZIF transceiver **201**. The Q DAC **213** asserts a Q channel analog output signal to another AA LPF **217**, which provides a Q channel transmit signal TXQ to the input of another LPF **221** within the ZIF transceiver **201**.

An external voltage controlled oscillator (VCO) **229** provides an output local oscillator (LO) signal at approximately 4.8 GHz to a phase lock loop (PLL) **231** and an input of an I/Q LO generator **227**. In one embodiment, a reference crystal is used to tune the VCO **229** by a voltage control to generate the 4.8 GHz LO signal. The PLL **231** receives the CREF clock signal which is divided down to an appropriate low frequency signal. The PLL **231** also divides down the VCO 4.8 GHz signal to the same appropriate low frequency signal. A phase detector circuit (not shown) within the PLL **231** compares these two low frequency signals—one being the CREF signal and the other from the VCO **229**, and generates a correction (C) signal which after filtering is input to the VCO **229**. This phase locked loop system reduces jitter on the VCO output LO signal. The I/Q LO **227** divides the 4.8 GHz carrier signal from the PLL **231** by two and generates two separate 2.4 GHz carrier signals, including an in-phase (I) carrier signal, and a quadrature (Q) carrier signal. The I and Q carrier signals are 90 degrees out of phase with respect to each other. The I carrier signal is provided to one input of an I channel mixer **223**, and the Q carrier signal is provided to one input of a Q channel mixer **225**. The other input of the I channel mixer **223** receives the output of the LPF **219** and the other input of the Q channel mixer **225** receives the output of the LPF **221**. The I channel mixer **223** combines the I carrier signal with the I channel transmit signal to up-convert the I channel from baseband to 2.4 GHz radio frequency (RF). The Q channel mixer **225** combines the Q carrier signal with the Q channel transmit signal to up-convert the Q channel from baseband to 2.4 GHz RF. The outputs of the I/Q channel mixers **223, 225** are combined at the input of a variable gain amplifier (VGA) **233**. The VGA **233** asserts an amplified transmit signal to the input of a fixed-gain amplifier **235**, which provides its output to a radio frequency power amplifier (RFPA) **237**. The RFPA **237** asserts an amplified RF signal to an RF LPF **239**, which provides a filtered RF output signal to one input of a transmit/receive (T/R) switch **241**. For transmission, the T/R switch

241 provides the RF output of the LPF 239 to a bi-directional band pass filter (BPF) 243, which provides a filtered RF output to a diversity switch 245. The diversity switch 245 asserts the RF transmit signal on a selected one of two antennas 247, 249.

The RFPA 237 asserts a transmit detect (TX DET) signal back to a transmit analog-to-digital converter (ADC) 251 within the baseband processor 203, which provides a corresponding digital feedback signal to the MAC 205. The MAC 205 includes a power control algorithm that detects the transmitted output signal via the ADC 251 and provides a feed forward signal to the input of a transmit (TX) DAC 253, which asserts a transmit automatic gain control (TX AGC) signal to control the gain of the VGA 233. Further, the ZIF transceiver 201 includes a voltage reference source 255 to provide a voltage reference (VREF) signal for the ZIF transceiver 201 and for the baseband processor 203. The VREF signal may be any convenient voltage, such as 1.2 volts or the like. The clock source 257 provides the CREF signal to the PLL 231 within the ZIF transceiver 201.

The T/R switch 241 is selected to receive signals from either of the antennas 247, 249 and provides a filtered signal (through BPF 243) to the input of a balanced/unbalanced (BALUN) impedance matching network 259. The BALUN 259 provides a received RF input signal R_{RF} to the input of a variable LNA 261. The LNA 261 asserts its output to the input of a fixed-gain LNA 263. The LNA 263 asserts the amplified RF receive signal to respective inputs of an I channel mixer 265 and a Q channel mixer 267. The I/Q LO 227 asserts the I carrier signal to another input of the I channel mixer 265 and the Q carrier signal to another input of the Q channel mixer 267. The I channel mixer 265 splits the I carrier frequency from the I channel output signal in the RF receive signal and provides the I channel output signal to an LPF 269. In a similar manner, the Q channel mixer 267 splits the Q carrier frequency from the Q channel output signal in the RF receive signal and provides the Q channel output signal to an LPF 271.

The output of the LPF 269 is provided to the input of a variable baseband automatic gain control (BB AGC) amplifier 273. In a similar manner, the LPF 271 asserts its output to the input of another BB AGC amplifier 275. The BB AGC amplifier 273 asserts an amplified I channel analog receive signal (RXI) to the input of an I channel receiver AA LPF 277, which asserts its output to the input of an I channel ADC (I ADC) 281 within the baseband processor 203. The BB AGC amplifier 275 asserts an amplified Q channel analog receive signal (RXQ) to the input of a Q channel AA LPF 279, which provides its output to an input of a Q channel ADC (Q ADC) 283 within the baseband processor 203. The I ADC 281 and the Q ADC 283 assert respective I and Q channel digital receive signals R_{DI} , R_{DQ} to a spreading decoder (DESPREAD) 285, which performs the opposite process as the spreading encoder 209 to retrieve received baseband encoded packets. The spreading decoder 285 provides the received baseband packets to a packet decoder 287, which, among other functions, retrieves the packet payloads and generates a stream of received data signals. The R_{DI} and R_{DQ} signals are also provided to compensation logic 284, further described below. The data signals from the packet decoder 287 are provided to a receive input of the MAC device 205, which provides received signals to the corresponding device across the implemented interface. The MAC interface may be incorporated internally within a device, such as on a PC CARD or the like, or may be external with appropriate external connectors, such as according to USB or the like.

An overload detector (OD) 289 within the ZIF transceiver 201 has first and second inputs coupled to the respective outputs of the LPF 269 and LPF 271 to detect an overload in the received input signal. The overload detector 289 asserts a baseband overload (BB OVLD) signal to an OVLD ADC 291 within the baseband processor 203, which provides a corresponding digital overload signal OVLD to the compensation logic 284. In this manner, the compensation logic 284 detects an overload of the received signal and asserts a HI/LO signal to control the variable LNA 261 of the ZIF transceiver 201. In the embodiment shown, the variable LNA 261 has an approximate 33 decibel (dB) step differential between a high gain (HI) and a low gain (LO). The gain is initially set high to detect weak signals and is switched to low gain upon certain conditions if the receive signal causes an overload condition as detected by the overload detector 289.

As more fully described below, the compensation logic 284 controls the gain of the received signal to a target power level by asserting a gain adjust signal G_{ADJ} to a gain DAC referred to as the AGC DAC 297. The AGC DAC 297 asserts a corresponding analog feedback gain control signal GAIN ADJUST to control the gain of both of the BB AGC amplifiers 273, 275. A single gain control signal is provided to both of the BB AGC amplifiers 273, 275 so that the gain of the I and Q channels of the receive signal appropriately track one another. The compensation logic 284 further asserts respective digital I and Q channel DC offset signals IDC_{OFF} , QDC_{OFF} to an I channel offset (I OFF) DAC 293 and a Q channel offset (Q OFF) DAC 295, respectively. The I OFF DAC 293 asserts an I channel DC offset analog signal (I OFFSET) to the LPF 269 and the Q OFF DAC 295 asserts a Q channel DC offset analog signal (Q OFFSET) to the LPF 271. In this manner, the compensation logic 284 attempts to measure and reduce or otherwise eliminate DC offsets in both the I and Q channels of the receive signal within the ZIF transceiver 201.

A ZIF architecture is utilized to obtain sufficient performance and higher data throughput at lower cost and power consumption. This is particularly advantageous to the consumer market which demands multimedia and DVD applications requiring relatively good performance. The consumer market also demands a lower cost. The ZIF architecture is one way to achieve lower cost with sufficient performance by eliminating IF components and external filters. The target carrier frequencies are in the GHz range such as 2-5 GHz ranges and higher, although the present invention is not limited to any particular frequency range. The 2-5 GHz bands are relatively noisy with significant amounts of interference. The ZIF architecture is utilized to maintain a level of performance in a noisy environment.

A particular problem with the ZIF architecture is the development of DC offsets at baseband that degrade signal-to-noise (SNR) ratio, which is directly related to performance of the system. The IF stage, which may be utilized to combat a significant level of DC offset, is not provided in the ZIF architecture. A number of sources of DC offset are due to temperature change, such as die self-heating of integrated circuits. The receive mixers 265, 267 internally inject DC offset from the carrier frequencies generated by the I/Q LO 227. This LO DC offset varies with RF frequency or channel selection as well as a selected level of gain of the variable LNA 261. This change occurs very quickly with changes of channel or gain. A slow DC drift with temperature also occurs. Externally, the LO carrier frequencies from the I/Q LO 227 leaks to the antenna input port causing DC offset. This external DC offset varies with changes in the external environment, such as movement of hands, bodies, jewelry,

mouse pointers, activation of electronic devices such as cooling fans or the like and re-radiation from nearby reflectors around the antenna. Movement of the wireless devices or changes in antenna direction also causes significant changes of the propagation characteristics of the channel or area. Such environmental changes induce impedance changes that dynamically change LO leakage magnitude and phase.

The receive mixers **265**, **267** also exhibit DC offsets at their outputs. This DC offset is primarily a function of circuit matching, such as bipolar and Metal Oxide Semiconductor (MOS) device matching and resistor matching. This DC offset also drifts due to temperature variations and self-heating. The I and Q channel LPFs **269**, **271** also exhibit offset at their outputs. This DC offset is also primarily a function of circuit matching. The I and Q channel baseband AGC amplifiers **273**, **275** also exhibit DC offset at their inputs. This DC offset is also primarily a function of circuit matching. Due to the analog control circuitry associated with this function, the impact of matching variation is more severe than the DC offset experienced by the receive mixers **265**, **267** and the LPFs **269**, **271**. This DC offset also changes non-linearly with gain setting, and drifts due to temperature variation and self-heating. The control voltage versus gain characteristic may also vary slowly with time. The main reason for drift is slower package temperature variations. A certain level of DC offset due to internal radio jamming from harmonics of digitally generated signals also occurs. As radio jamming is injected into the antenna and/or RF front end, this DC offset is a function of channel and LNA gain as well as a strong function of the particular digital circuit that is creating the spurious signal. Below a certain frequency (f) such as 1 kilohertz (kHz), $1/f$ noise appears as an impairment similar in effect to DC offsets.

It is noted that one possible solution of removing DC offset is through AC coupling, such as using coupling capacitors or the like. However, AC coupling results in filtering that tends to filter out low frequency content. The amount of data thrown away becomes significant above 1 kHz, so that AC coupling must only filter below 1 kHz. Within this range, however, the settling time is too long, such as on the order of approximately 100 microseconds (μ s), which is not practical in a bursty environment such as packet-based communications. The settling time is limited due to the bursty nature of communication. Short preamble time lines of IEEE 802.11a and IEEE 802.11b standards have little room for accurate DC estimation.

All of the sources of DC offsets are referenced to the inputs of the BB AGC amplifiers **273**, **275**. The gain range of the BB AGC amplifiers **273**, **275** must be sufficient to guarantee acceptable performance in a variety of environments. In the embodiment shown, the gain range of each of the BB AGC amplifiers **273**, **275** is approximately -6 dB to 60 dB, or 0.5 V/V to 1000 V/V to obtain the desired operation range of approximately 0.7 V/V to 800 V/V. It has been determined that the DC offset range can be on the order of ± 50 - 100 millivolts (mV). It is desired that the DC correction occur before the baseband amplifiers **273**, **275** because of its significant gain range.

FIG. 3 is a block diagram of a compensation system **300** utilized to control the gain of the received signal and to reduce or eliminate DC offsets in the ZIF architecture. The compensation system **300** illustrates operation of the receive portion of the wireless transceiver **200** for purposes of gain and DC compensation. The compensation system **300** includes various blocks representative of the elements within the wireless transceiver **200**, including circuitry from the ZIF transceiver **201** and the baseband processor **203**, with a focus on the

operations of the compensation logic **284**. The block diagram of the compensation system **300** is simplified in that the separate I and Q channel signals are illustrated by single communication path, which represents operation of both I and Q channels. Thus, it is noted that the same techniques are applied for both the I and Q channels and thus are applicable for use in the wireless transceiver **200**.

The received RF input signal R_{RF} from the antennas **247**, **249** through the BALUN **259** is provided to an RF mixer circuit referred to as the LNA/mixer **301**, which represents the LNAs **261**, **263** and the receive mixers **265**, **267**. The LNA/mixer **301** provides a baseband receive input signal R_{BB} to one input of a combiner **303**, which provides a DC-adjusted receive input signal R_{ADJ} to the input of a baseband BB LPF **305** representing the LPFs **269**, **271**. The other input of the combiner **303** receives a DC OFFSET signal. The combiner **303** operates as a combiner that combines the DC OFFSET signal with the R_{BB} receive signal to provide the DC-adjusted R_{ADJ} signal. In one embodiment, the combiner **303** is a summing junction that subtracts the DC OFFSET signal from the R_{BB} receive signal to provide the DC-adjusted R_{ADJ} signal. It is noted that the combiner **303** may alternatively operate as a summing junction that adds an inverted DC OFFSET signal. The invention is not limited to any particular implementation or design configuration.

The output of the BB LPF **305** is provided to the input of a baseband gain amplifier BB AGC amplifier **307**, representing operation of the BB AGC amplifiers **273**, **275**. The output of the BB LPF **305** is also provided to the overload detector **289**, which asserts the baseband overload signal BB OVLD to the OVLD ADC **291** within the baseband processor **203**, which provides the OVLD signal to an overload (OV) detect block **309** of the compensation logic **284**. The OV detect block **309** asserts the HI/LO signal to the LNA/mixer **301** to switch the variable LNA **261** between high and low gains. The BB AGC amplifier **307** asserts the amplified input signal R to the input of an AA LPF **311** representing the AA LPFs **277**, **279**. The output of the AA LPF **311** is provided to an ADC **313** representing the ADCs **281**, **283**. The ADC **313** provides a digital version R_D of the amplified receive input signal R at its output, where the R_D signal represents the I and Q digital receive signals R_{DI} and R_{DQ} . The R_D signal from the ADC **313** is provided to the spreading decoder **285**.

The R_D signal is provided to a signal power estimate block **315** and a DC estimate block **319** of the compensation logic **284**. The signal power estimate block **315** provides a input signal power estimate signal R_{EST} to one input of a combiner **321**. The combiner **321** receives a target power (TP) signal from a target power block **323** and combines the TP signal with the R_{EST} signal to provide a receive error signal R_E , which is provided to an input of another combiner **325**. In one embodiment, the combiner **321** operates as a summing junction that subtracts the TP signal from the R_{EST} signal to provide a receive error signal R_E to an input of the combiner **325**. The combiner **325** combines the R_E signal with a gain accumulation signal G_{ACC} from an accumulator **329** to provide the gain adjust signal G_{ADJ} at its output. In one embodiment, the combiner **325** also operates as a summing junction that subtracts the R_E signal from the gain accumulation signal G_{ACC} from an accumulator **329** to provide the gain adjust signal G_{ADJ} at its output. The G_{ADJ} signal is provided to the respective inputs of the AGC DAC **297**, the accumulator **329** and a gain converter **331**. The AGC DAC **297** converts the digital G_{ADJ} signal to the analog GAIN ADJUST signal, which controls the gain of the BB AGC amplifier **307**. The accumulator **329** continuously or periodically adjusts the G_{ACC} signal to track changes of the G_{ADJ} signal.

The DC estimate block **319** provides an output DC estimate digital signal ODC_{EST} to the input of a DC amplifier **333**, which is adjusted by a gain conversion signal G_{CON} from an output of the converter **331**. The DC amplifier **333** amplifies or attenuates ($1/G$) the ODC_{EST} signal by an amount determined by the G_{CON} signal from the converter **331**, and provides an input DC estimate signal IDC_{EST} to one input of a combiner **335**, which receives a DC offset accumulation signal D_{ACC} from an accumulator **339** at its other input. The combiner **335** combines the IDC_{EST} signal with the D_{ACC} signal to provide a DC offset signal DC_{ADJ} , which is provided to the input of a DC DAC **337** and to the input of the DC accumulator **339**. In one embodiment, the combiner **335** operates as a summing junction that adds the IDC_{EST} signal to the D_{ACC} signal to provide the DC offset signal DC_{ADJ} . The accumulator **339** continuously adjusts the D_{ACC} signal to the level of the DC_{ADJ} signal to maintain an accumulated DC value. The DC DAC **337** converts the digital DC_{ADJ} signal to the analog DC OFFSET signal provided to the combiner **303**. The DC_{ADJ} signal represents operation of the IDC_{OFF} and QDC_{OFF} signals and the DC OFFSET signal represents operation of the I OFFSET and Q OFFSET signals.

It is noted that many alternatives and variations are contemplated. For example, the combiner **303** may be implemented as a simple summing junction, where the DC amplifier **333** or the DC DAC **337** performs negation or inversion to generate a negative DC OFFSET signal, which is then added to the R_{BB} signal by the combiner **303**.

Control logic **343** is coupled to the OV detect block **309**, the target power block **323** and the DC estimate block **319** for controlling operations, setting parameters, etc. For example, the control block **343** may be used to enable a manufacturer or user to set a target power level used by the target power block **323** to control the TP signal.

In operation, the R_{RF} signal from the antennas **247**, **249** is converted to the R_{BB} signal at baseband frequency by the LNA/mixer **301**. The OV detect block **309** initially sets the gain of the LNA portion of the LNA/mixer **301** high by asserting the HI/LO signal to HI in order to ensure detection of a valid but weak RF signal received by either of the antennas **247**, **249**. The R_{BB} signal is DC adjusted by the combiner **303**, which combines or otherwise subtracts the DC OFFSET signal and provides the R_{ADJ} signal to the BB LPF **305**. The BB LPF **305** provides a filtered version of the R_{ADJ} signal to the BB AGC amplifier **307**. The DC OFFSET signal is based on an estimate of the amount of undesired DC at the input of the BB AGC amplifier **307**. The overload detector **289** detects whether an overload condition of the received input signal at the output of the BB LPF **305** exists, and if so, asserts the BB OVLN signal. If an overload condition is detected, the OV detect block **309** asserts the HI/LO signal to LO to reduce the input gain of the LNA/mixer **301** to bring the received input signal R_{BB} closer to a target power level.

The BB AGC amplifier **307** amplifies the R_{ADJ} signal to provide the R signal to the AA LPF **311** and then to the ADC **313** of the baseband processor **203**. The ADC **313** converts the analog R signal to the digital receive signal R_D , which is provided to the spreading decoder **285** (as the R_{DI} and R_{DQ} signals). The signal power estimate block **315**, the combiners **321** and **325**, the target power block **323**, the accumulator **329** and the AGC DAC **297**, in combination with the signal path devices including the BB AGC amplifier **307**, the AA LPF **311** and the ADC **313**, form the AGC loop **345**, which is a gain feedback circuit centered around the BB AGC amplifier **307**. The AGC loop **345** includes gain control logic that receives the amplified input signal, that estimates input signal power and that asserts the gain adjust signal in an attempt to keep the

input signal power at a target power level. In particular, the signal power estimate block **315** estimates the power of the baseband input signal within the R_D signal and asserts the R_{EST} signal indicative thereof. In one embodiment, this power estimate excludes any DC level of the R_D signal. The combiner **321** compares the R_{EST} signal with the TP signal to generate the R_E signal, which identifies an amount of power error of the R_D signal relative to the target power level represented by the TP signal. The combiner **325** adjusts the present value of the G_{ADJ} signal in an attempt to compensate for any power error that exists. The AGC DAC **297** converts the G_{ADJ} signal to the analog GAIN ADJUST signal, which is provided to the gain control input of the BB AGC amplifier **307** to control the power level of baseband input signal within the R_D signal. Thus, the AGC loop **345** attempts to maintain or otherwise regulate the power level of the input baseband signal within the R_D signal to the target power level.

In the embodiment shown, the BB AGC amplifier **307**, representing either of the BB AGC amplifiers **273**, **275**, uses a logarithmic gain scale, such as measured in dB, that ranges between -6 and 60 dB. The R_D signal is in digital format, so the signal power estimate block **315**, the target power block **323**, the accumulator **329** and the combiners **321**, **325** are digital devices and the R_{EST} , TP, R_E , G_{ACC} and G_{ADJ} signals are digital signals. The AGC DAC **297** is a 7-bit DAC with 128 steps that outputs an analog current signal with a control current range of approximately ± 1 mA to achieve the desired gain range for the BB AGC amplifier **307**. The current output of the AGC DAC **297** is converted to a voltage signal, such as by a resistive network or the like (not shown), to obtain the GAIN ADJUST signal.

The DC estimate block **319**, the gain converter **331**, the DC amplifier **333**, the combiner **335**, the accumulator **339**, the DC DAC **337** and the combiner **303**, in combination with the receive signal path between the combiner **303** and the ADC **313**, form the DC loop **347** that operates to attempt to reduce or otherwise remove DC from the R_D signal in the input signal path. The DC loop **347** includes DC control logic that estimates an amount of DC in the amplified input signal and provides a DC offset in an attempt to reduce DC in the amplified input signal. In particular, the DC estimate block **319** estimates the DC offset of the R_D signal, and provides the ODC_{EST} signal indicative of the amount of DC at the output of the BB AGC amplifier **307**. Since the DC OFFSET signal is applied at the combiner **303** at the input of the BB AGC amplifier **307**, and since any remaining DC of the R_{ADJ} signal is effectively amplified by the BB AGC amplifier **307**, the DC amplifier **333** operates to compensate for the gain of the BB AGC amplifier **307**. The gain converter **331**, receiving the G_{ADJ} signal and generating the G_{CON} signal that controls the gain of the DC amplifier **333**, operates as a gain interface that converts gain levels between the gain control logic and the DC control logic. In one embodiment, the gain converter **331** inverts the gain ($1/G$). The gain converter **331** may further compensate for different gain ranges and/or different gain scales between the BB AGC amplifier **307** and the DC amplifier **333**. In this manner, the IDC_{EST} signal, asserted by the DC amplifier **333**, represents an error of the DC OFFSET signal. The combiner **335** adjusts the DC_{ADJ} signal, maintained by the accumulator **339** as the D_{ACC} signal, by the IDC_{EST} signal to compensate for errors in the DC OFFSET signal.

In the embodiment shown, the R_D signal is in digital format, so the DC estimate block **319**, the DC amplifier **333**, the accumulator **339** and the combiner **335** are digital devices and the ODC_{EST} , IDC_{EST} , D_{ACC} and DC_{ADJ} signals are digital. Also, the DC DAC **337**, representing either of the I, Q OFF DACs **293**, **295**, is a 12-bit, current-based DAC operated in

2's-complement format that outputs an analog current with an approximate range of ± 5 milliamps (mA). The DAC output current is converted to the DC OFFSET voltage signal having a range of approximately ± 75 mV to compensate for an expected DC offset range of approximately ± 64 mV. The gain converter **331** may operate entirely as a digital device to convert the digital G_{ADJ} signal to a digital G_{CON} signal. Alternatively, it is contemplated that the G_{CON} signal may be an analog signal depending upon the configuration of the DC amplifier **333**. In the embodiment shown, the DC amplifier **333** is a linear gain amplifier. In general, the BB AGC amplifier **307** amplifies the input signal including any DC, so that the DC amplifier **333** operates as an amplifier that amplifies the ODC_{EST} signal to maintain control of the DC loop **347**. The amount of amplification by the DC amplifier **333** is controlled by the gain converter **331** via the G_{CON} signal. The gain converter **331** receives the G_{ADJ} signal and adjusts the G_{CON} signal accordingly.

As described previously, the gain converter **331** operates as a gain interface that converts gain levels between the gain control logic and the DC control logic. In one embodiment, the gain converter **331** inverts the gain between the BB AGC amplifier **307** and the DC amplifier **333**. The gain converter **331** may further convert between the corresponding ranges or units along with any bit weighting of the G_{ADJ} and G_{CON} signals so that the amplification of the ODC_{EST} signal corresponds to the gain of the R_{ADJ} signal. In the alternative or in addition, the gain converter **331** further converts between gain scales, such as between logarithmic and linear scales. In particular for the embodiment shown, since the BB AGC amplifier **307** is a logarithmic gain amplifier measured in decibels (dBs) and since the DC amplifier **333** is a linear gain amplifier, the gain converter **331** converts from the G_{ADJ} signal in dBs to the linear gain G_{CON} signal. For embodiments in which the BB AGC amplifier **307** and the DC amplifier **333** are both linear amplifiers, the gain converter **331** converts between the corresponding ranges or units along with any bit weighting of the G_{ADJ} and G_{CON} signals without need of logarithmic conversion.

FIG. 4 is a block diagram of a calibrated DC compensation system **400** similar to the compensation **300** except utilizing calibration to more accurately determine and control DC. In particular, a calibration block **401** includes calibration logic that receives the R_D signal and provides one or more calibration programming signals, collectively referred to as PGM signals, to the gain converter **331**. The gain converter **331** includes an optional adjust memory **405** for storing adjust values as further described below. The PGM signals may be implemented in any suitable manner, such as multiple bus signals or the like to program the adjust memory **405**. The control block **343** may also be used to control a calibration procedure or calibration function or to control if and when a calibration procedure is performed by the calibration block **401**. For example, the control logic **343** optionally includes timing logic **403** or the like that determines a time interval for performing a calibration procedure, as further described below. The time interval between consecutive calibration operations depends upon the particular configuration or implementation. In the embodiment shown, the calibration time interval is on the order of seconds or minutes, such as approximately 30 seconds or 1 minute or the like.

As previously described, there are many sources of DC, and the DC level changes over time. The BB AGC amplifier **307** itself introduces DC offset that may change significantly from one gain step to another. In the embodiment shown, the calibration block **401** is a digital device that operates as a calibrator, which monitors the digital R_D signal, makes

appropriate measurements and calculations, and programs the adjust memory **405** accordingly. The converter **331** receives the G_{ADJ} signal, determines a corresponding initial value for the G_{CON} signal, and makes any necessary adjustments utilizing adjust values in the adjust memory **405** if provided. The adjust value may be incorporated in any one of several manners. In one configuration, the adjust value is a multiplier value which is multiplied by the initial conversion value determined by the gain converter **331** and the result is used as the G_{CON} signal to control the DC amplifier **333**. Alternatively, the adjust value is an offset or additive value that is added to or subtracted from the initial conversion value determined by the gain converter **331** and the sum is used as the G_{CON} signal to control the DC amplifier **333**. In alternative embodiments, the calibration block **401** may simply assert a calibration signal that is used for adjusting the G_{CON} signal. The calibration signal is maintained at a current adjust level as controlled by the calibration block **401**, and utilized by the gain converter **331** in a similar manner as a single adjust value. It is noted, however, that due to the unpredictable and often non-linear nature of DC voltage in ZIF architecture embodiments in many environments, a single-valued calibration signal may not be sufficient to compensate for DC.

Any suitable number of adjust values are contemplated to achieve any desired level of accuracy. In one configuration, a low gain adjust value and a high gain adjust value are used. The particular G_{ADJ} value that is used as the threshold to switch between the low and high adjust values may be determined arbitrarily or experimentally. A half-way point is contemplated, although any suitable threshold point is contemplated depending upon the particular configuration and design. Alternatively, any number of adjust values could be used for each of a corresponding number of gain steps or levels of the G_{ADJ} signal. If the AGC DAC **297** is a 7-bit DAC with 128 corresponding discrete gain steps, for example, then the number gain adjust values programmed into the adjust memory **405** may range from 2 to 128 different adjust values. The embodiment of a different adjust value for each discrete gain step of the G_{ADJ} signal provides relatively high accuracy.

Upon timeout of the timing logic **403**, the control logic **343** determines whether the wireless transceiver **200** is performing any communication functions, such as sending or receiving any packets of information. If not busy, or after the wireless transceiver **200** has performed its functions and becomes idle, the control logic **343** indicates to the calibration block **401** to conduct a calibration procedure. The calibration block **401** is coupled to control certain functions of the wireless transceiver **200**, as indicated by dotted line **351**, to conduct calibration. During calibration, the calibration block **401** may control the LNA/mixer **301** and/or the combiner **303** to temporarily remove the input signal R_{BB} from the compensation system **300**. For example, the input of the combiner **303** that receives the R_{BB} signal is temporarily disconnected from the LNA/mixer **301** and grounded or otherwise left floating. It is noted, however, that control of the LNA/mixer **301** and/or the combiner **303** may require a more complicated interface between the ZIF transceiver **201** and the baseband amplifier **203**. Alternatively, the calibration procedure and functions may be wholly contained within the baseband processor **203**. In either case, the calibration block **401** controls the DC DAC **337** and the AGC DAC **297** to temporarily disable the AGC loop **345** and the DC loop **347** to conduct the calibration procedure.

During the calibration procedure, the calibration block **401** controls the DC DAC **337** to inject a predetermined or arbitrary DC level or setting into the compensation system **300**, such as a DC value of zero volts or any other predetermined or

suitable voltage. The calibration block **401** controls the AGC DAC **297** to a predetermined gain step or level, or otherwise to consecutively step through one or more gain steps. The calibration block **401** then samples the R_D signal one or more times for each gain step. From this data, the calibration block determines one or more gain values or otherwise determines one or more DC offset values corresponding DC levels of the R_D signal. In some embodiments, the calibration block **401** makes any necessary calculations based on measured parameters, such as DC levels of the R_D signal and/or gain of the BB AGC amplifier **307**, and programs the adjust memory **405** with one or more adjust values accordingly.

In one embodiment, the calibration block **401** controls the DC DAC **337** to assert an arbitrary and known DC voltage to the combiner **303** and controls the AGC DAC **297** to a particular gain level. The calibration block **401** then samples the R_D signal. The calibration block **401** may use an assumed or theoretical gain of the BB AGC amplifier **307**, calculate the theoretical value of the R_D signal based on the gain level, and compare with the actual value of measured R_D signal. The difference between the theoretical gain value and the measured value is a DC differential value that is utilized to determine the necessary DC offset at that gain level. Alternatively, the calibration block **401** determines one or more gain values representing measured gain of the BB AGC amplifier **307** in any appropriate manner, and uses the determined gain values rather than theoretical gain in the calculation. For example, the calibration block **401** may determine first and second DC offset values programmed into the DC DAC **337** that result in the R_D signal reaching corresponding first and second range values, such as 75% upper and lower range values, respectively. As described further below, the first and second DC offset values are utilized to calculate a gain value of the BB AGC amplifier **307** at the particular gain step of the AGC DAC **297**.

The calibration block **401** repeats the process for one or more gain steps of the AGC DAC **297** resulting in a plurality of gain values and DC differential values that are used to determine the adjust values programmed into the adjust memory **405**. The calibration block **401** may incorporate any differences in gain ranges or gain scales between the BB AGC amplifier **307** and the DC amplifier **333** to convert each DC differential value to the appropriate adjust value. For example, conversion from logarithmic to linear scales is contemplated. Alternatively, the adjust memory **405** is programmed with the DC differential values, where the gain converter **331** performs any necessary conversions during operation. Although the calibration block **401** and the adjust memory **405** are additional components that further complicate the circuitry and logic, the DC loop **347** converges and eliminates the DC offset more quickly. The calibration procedure is repeated on a periodic basis since the operating environment is dynamic and unpredictable.

FIG. **5** is a block diagram of a calibrated compensation system **500** similar to the compensation system **400**, except that the gain converter **331** is replaced by a lookup table (LUT) **501** as the gain interface between the AGC loop **345** and the DC loop **347**. The LUT **501** is a memory device that operates in a similar manner as the gain converter **331** and adjust memory **403**, except that gain conversion values programmed in the LUT **501** are asserted directly as the G_{CON} signal to control the gain of the DC amplifier **333**. In particular, the G_{ADJ} signal is used as an address to access a gain conversion value within the LUT **501**, which is then asserted as the G_{CON} signal to the DC amplifier **333**. The calibration block **401** performs the calibration procedure in a similar

manner as previously described to determine one or more gain values or DC offset values via the R_D signal.

The calibration block **401** performs any necessary calculations on the measured gain values and/or DC offset values to convert between the AGC loop **345** and the DC loop **347** to program the gain conversion values within the LUT **501**. In particular, the calibration block **401** converts between corresponding ranges or units along with any bit weighting of the G_{ADJ} and G_{CON} signals as previously described. In the alternative or in addition, the calibration block **401** further converts between different scales, if any, between the BB AGC amplifier **307** and the DC amplifier **333**, such as between logarithmic and linear scales as previously described. The calibration block **401** programs a separate gain conversion value within the LUT **501** that corresponds to at least one gain level or step of the AGC DAC **297**. A separate gain conversion value for each gain step is contemplated, which provides an advantage during operation in that no conversion is necessary so that the LUT **501** supplies an appropriate G_{CON} value for every G_{ADJ} value.

FIG. **6** is a block diagram of a calibrated compensation system **600**, which is similar to the compensation system **500**, but that further includes a limit block **601** that operates as a gain adjust limiter to limit change of the G_{ADJ} signal during operation. The R_E signal from the combiner **321** is provided to the limit block **601**, which also receives the G_{ACC} signal from the accumulator **329**. The limit block **601** asserts a limited receive error signal, referred to as R_{LE} , to the accumulator **325** rather than the R_E signal. In this manner, the R_{LE} signal is a limited version of the R_E signal as determined by the limit block **601** using the R_E signal and the G_{ACC} signal. The G_{ACC} signal is the current gain level of the AGC DAC **297** (via the G_{ADJ} signal) and the R_E signal is the desired error differential or change to determine a new level of the G_{ADJ} signal. The accumulator **329** updates the G_{ACC} signal with the new value of the G_{ADJ} signal after being changed.

Instead of directly applying the R_E signal, the limit block **601** provides a way of limiting the amount of change of the G_{ADJ} signal to prevent loss of loop control, as further described below. Many different embodiments are contemplated. In one embodiment, the limit block **601** is preprogrammed with a predetermined gain change limit that always applies, such as a 90% factor applied to the R_E signal or the like, or a constant maximum gain change limit that is not exceeded during operation of the wireless transceiver **200**. Alternatively, the limit block **601** is programmed by the calibration block **401** via one or more G_{LIM} signals or the like, in a similar manner described above for the LUT **501**.

It is possible that the ADC **313** include as many bits as necessary to capture most, substantially all, or all possible ranges of the receive signal R asserted by the BB AGC amplifier **307**. In a particular embodiment, the BB AGC amplifier **307** has a gain range of approximately 66 dB (-6 dB to 60 dB) to provide a sufficient dynamic gain range to enable appropriate operation in the anticipated environments. The AGC DAC **297** includes a sufficient number of bits to achieve the desired accuracy over the entire gain range of the BB AGC amplifier **307**. For example, in one embodiment, the AGC DAC **297** is 7 bits. Such configuration would require that the ADC **313** has a significantly large number of bits to track the receive signal R regardless of the gain level of the BB AGC amplifier **307**. It is further noted that the ADC **313** could further include additional bits to further incorporate the entire range of DC offsets incorporated within the receive signal that might not yet be completely compensated for by the DC loop **347**. Again, this is a substantially large number of bits that would require a large ADC **313**. Further, the baseband pro-

cessor 203 could be designed to appropriately handle the significantly large number of bits of the ADC 313.

In a more practical embodiment, the ADC 313 includes only as many bits as necessary to maintain signal integrity with sufficient head and foot room (collectively, head room). In one embodiment, for example, the ADC 313 is a 6-bit converter with a 36 dB of range resulting in approximately 6 dB per bit. In this manner, the ADC 313 does not attempt to handle the entire operating range of the BB AGC amplifier 307, but instead is sufficient to maintain signal integrity with sufficient head room. The target power block 323 asserts the TP signal at the appropriate target power in an attempt to maintain the receive signal R with reduced or eliminated DC offset to within the operating range of the ADC 313. It is noted that the target power is less than the full scale of the ADC 313 and in one embodiment is set to approximately ± 75 percent of the full scale power observable with the ADC 313.

The ZIF transceiver 201, therefore, may provide a received R signal that is beyond the range of the ADC 313 of the baseband processor 203. This may be particularly true during initial packet acquisition. For example, an excessive DC level may cause the ADC 313 to rail to either its maximum or minimum limits. An overpowered input receive signal may cause clipping at either or both rails depending upon corresponding DC level. The AGC loop 297 and the DC loop 347 are provided to compensate for signal power and DC level to control the level of the R_D signal to within the desired target power and operating range of the baseband processor 203. Furthermore, even after the R_D signal converges to the desired operating range, the environmental conditions may suddenly change causing a change of signal power and/or DC level. Since the BB AGC amplifier 307 has unpredictable DC at its input that may change significantly with gain level changes, significant gain changes requested by the signal power estimate block 315 may otherwise cause a substantial change of the DC level of the R_D signal causing a rail condition of the ADC 313 and/or loss of DC loop 347 control. This is particularly problematic at high gain levels, since any new DC level is substantially amplified at high gain by the BB AGC amplifier 307 potentially causing quick loss of loop control.

The limit block 601 is provided in the compensation system 600 to reduce or eliminate over-correction by the signal power estimate block 315. At higher level gain steps of the AGC DAC 297 corresponding to higher gain levels of the BB AGC amplifier 307, a certain level of the R_{EST} signal may correspond to a significant amount of differential of the G_{ADJ} signal and the AGC DAC 297, which could introduce too much DC offset for control by the DC loop 347. Alternatively, a significant change in the G_{ADJ} signal may substantially reduce DC offset otherwise supplied by the BB AGC amplifier 307, such that the accumulated DC offset signal itself over-compensates and thus introduces too much DC voltage that may not be controllable. Thus, the limit block 601 reduces the amount of correction of the R_E signal at higher gain steps. The limit block 601 compares the R_E signal with the G_{ACC} signal and determines the level of the R_{LE} signal to maintain a controllable modification of the G_{ADJ} signal to maintain proper control loop operation.

Many different embodiments and variations of the limit block 601 are contemplated. In one embodiment, the limit block 601 is pre-programmed with a single maximum gain differential value that is applicable for all operating gain levels. Alternatively, the limit block 601 is programmed by the calibration block 401 via the G_{LIM} signals during calibration with one or more gain limit values. A single maximum gain change limit G_M is contemplated as determined and programmed by the calibration block 401. One or more gain

change limits may also be determined and programmed depending upon particular gain steps. The limit block 601 may be programmed with a different gain change limit for each gain step of the G_{ADJ} signal, operable in a similar manner as the LUT 501. Alternatively, the limit block 601 may be programmed with gain change limit values only at higher gain levels, such as the higher 30 dB gain levels. Alternatively, the limit block 601 may be implemented with any combination of gain limitations, including a maximum gain change limit operative across the entire gain range and particular gain change limits at particular gain levels, such as the higher gain levels.

As mentioned previously and as further described below, in one embodiment, the calibration block 401 measures or otherwise determines a gain value representing the gain of the BB AGC amplifier 307 for each gain step of the G_{ADJ} signal (or gain step of the AGC DAC 297) during each calibration procedure. The calibration block 401 may then use an upper bound method that further utilizes an assumed DC offset model or characteristic of the BB AGC amplifier 307. In the assumed model, the change of DC offset (dV) is linear with linear gain change (dG), so that it is assumed that the rate of change of the DC offset is constant with respect to voltage gain, or $dV/dG=k$, where prefix “d” denotes a derivative or delta value. Using the model, it is assumed that the rate of change of DC offset with respect to voltage gain is the constant value “k”. Although this may not be true for particular configurations of the BB AGC amplifier 307, this model is sufficiently accurate from an upper bounding perspective. The linear DC offset change model, when converted to the decibel range (dV/dG_{dB}), is no longer linear and changes more rapidly with increasing gain dB. However, over small ranges of gain, the linear approximation is a relatively accurate estimation of the change of DC offset at any given gain point. The rate of change is relatively small at lower gain points but begins to increase rapidly at the mid range point of approximately 30 dB. Thus, correction may be applied over the entire gain range or at the higher gain levels.

To achieve a relatively accurate slope for dV/dG_{dB} , it is desired to find the differences in DC and gain at two relatively close points. For convenience, the two points are the current operating gain $G1_{dB}$ and the gain at one (1) dB greater, or $G2_{dB}=G1_{dB}+1$. In this manner, $dG_{dB}=1$ dB, which is simpler for implementation purposes and sufficiently accurate. To find dV (or delta DC), the linear curve with constant “k” is utilized at two gain points by converting between the linear model and dB scales. First, the linear gain $G1=invlog G1_{dB}=10^{(G1_{dB}/20)}$, where the “^” symbol denotes a power factor or “raised to the power of”. The first DC offset $DC1=k*G1$, where an asterisk “*” represents multiplication. If $G2_{dB}=G1_{dB}+1$, then the second DC offset $DC2=k(G2)=k10^{[(G1_{dB}+1)/20]}$. Thus, $dV=DC2-DC1=dV/dG_{dB}$.

The gain change limit, referred to as MaxGainStep, is the step in gain from an initial operating point that results in extra DC that is the largest observable at the ADC 313. If DC is initially fairly well compensated, then the largest tolerable extra DC is half the range of the ADC 313, referred to as MaxDCStep. In this manner, $MaxGainStep=MaxDCStep/(dV/dG_{dB})$. The ADC 313 has a range of approximately ± 500 mV, so that $MaxDCStep=500$ mV is an acceptable limit value for the embodiment shown. In one embodiment, a separate dV_i , denoted with index “i”, is measured for each gain level or gain step (i) of the BB AGC amplifier 307, or each gain step of the G_{ADJ} signal. A corresponding $MaxGainStep_i$ value is then determined for each gain step (i). In one embodiment, all of the $MaxGainStep_i$ values are stored within the limit block 601

by the calibration block **401**. For an ADC DAC **297** of 7 bits, 128 different MaxGainStep_{*i*} values are calculated and stored. Alternatively, a subset of MaxGainStep_{*i*} values are calculated and stored, such as the gain steps corresponding to the upper 30 dB gain range of the BB AGC amplifier **307**. In operation, the current gain as determined by the G_{ACC} signal is used to access the corresponding MaxGainStep_{*i*} value, if any, stored within the limit block **601** in a similar manner as a lookup table embodiment. The R_{LE} signal is asserted by the limit block **601** as the lesser of the current R_E signal and the corresponding MaxGainStep_{*i*} value. In another alternative embodiment, each dV_{*i*} is calculated, but only the maximum value is stored, or dV_{*M*}. Then, a maximum gain change limit, or G_{*M*}, is calculated using dV_{*M*} and stored in the limit block **601** and used over the entire gain range.

In another alternative embodiment, the linear model is not used in favor of actual DC offset measurements. In the embodiment shown, the AGC DAC **297** is a current-based, 7-bit DAC with GD_{lsb}≈approximately 2/128 mA per step or click for a full-scale range of 2 mA, where GD_{lsb} represents the least significant bit (lsb) conversion value for the AGC DAC **297**. If “*i*” is an index representing the gain steps of the G_{ADJ} signal corresponding to the AGC DAC **297**, if Vo(*i*) represents a measured DC offset at a particular gain level at operating point (*i*), and if dG_{*mA*} is the gain change in milliamps, then dV/dG_{*mA*}(*i*) for each gain step (*i*) is determined according to the following equation (1):

$$dV/dG_{mA}(i) = \frac{Vo(i+1) - Vo(i-1)}{2 * GD_{lsb}} \quad (1)$$

where the quantity Vo(*i*+1)–Vo(*i*–1) is a local DC offset change over two gain steps as would be observed after the BB AGC amplifier **307** at the input to the ADC **313**. The conversion from mA to dB is nearly linear, where dV/dG_{*dB*}(*i*) for each gain step is determined by conversion of dV/dG_{*mA*}(*i*) according to the following equation (2):

$$dV/dG_{dB}(i) = \frac{2 * (dV/dG_{mA}(i))}{\max G_{dB}(i) - \min G_{dB}(i)} \quad (2)$$

where maxG_{*dB*}(*i*) and minG_{*dB*}(*i*) are the maximum and minimum measured gain values in decibels, respectively. Then dV/dG_{*dB*}(*i*) is determined according to the following equation (3):

$$dV/dG_{dB}(i) = \frac{Vo(i+1) - Vo(i-1)}{\max G_{dB}(i) - \min G_{dB}(i)} \quad (3)$$

FIG. 7 is a block diagram of a calibrated compensation system **700** that is similar to the compensation system **500** with the inclusion of an additional lookup table (LUT) **701**. The LUT **701** is another memory device that stores and asserts measured DC adjust values on a signal DC_{ADJ} to another input of the combiner **335**. The G_{ADJ} signal is provided to an input of the LUT **701**, which is programmed by the calibration block **401** with the DC adjust values via the PGM signals. The DC adjust values represent measured DC offsets for corresponding gain steps (*i*) of the G_{ADJ} signal. In the calibrated compensation systems **500** and **600**, the IDC_{EST} signal asserted by the DC amplifier **333** is a gain compensated DC signal that does not account for measured DC levels. The

LUT **701** provides additional correction based on measured DC levels. For example, gain changes by the G_{ADJ} signal are handled by the LUT **501** and measured DC offsets at the gain steps are handled by the LUT **701**. Although an additional combiner could be added, the LUT **701** conveniently provides direct DC offset correction to the combiner **335** for more directly controlling the DC_{ADJ} signal and the DC OFFSET signal via the DC DAC **337**. The limit block **601** could also be added, but is deemed unnecessary since measured DC offsets are compensated via the LUT **701** in the compensation system **700**.

FIGS. 8A-8C are flowchart diagrams illustrating a calibration procedure according to an embodiment of the present invention. This particular calibration procedure measures both the gain of the BB AGC amplifier **307** at each of the gain steps (*i*) of the AGC DAC **297** and further measures the corresponding DC offset of the R_D signal. Further, the change in DC offsets and/or DC offset derivatives are determined for use by the limit block **601**, if desired.

Prior to discussing specific operation, a brief discussion of the overall operation is provided. As described before, the calibration block **401** controls the AGC DAC **297** and the DC DAC **337** to perform measurements while the wireless transceiver **200** is idle and not communicating. A successive approximation algorithm is utilized to establish a voltage difference at the BB AGC amplifier **307** input that corresponds to a desired voltage difference of the R_D signal. During the calibration procedure, the AGC DAC **297** is stepped through each gain step (*i*) beginning from lowest to highest. Then, for each gain step, the DC DAC **337** is adjusted to obtain a target level of the R_D signal output by the ADC **313**. In the particular embodiment described, high and low values of the R_D signal are determined by successive approximation and stored for each gain step of the AGC DAC **297**. The use of two separate target levels of the R_D signal enables calculation of the gain using differences in which the DC offsets are common mode and cancel out. Also, utilizing summation in conjunction with the previously calculated gain, the actual DC offset voltage may be calculated.

For the successive approximation, the value of the DC DAC **337** is initially started low and successively increased until the R_D signal is sampled at a predetermined high value. Then, the DC DAC **337** is initially started high and successively decreased until the low value of the R_D signal is sampled at a predetermined low value. A successive approximation or binary search method is used in order to converge on the desired value very quickly. In particular, each bit beginning with the most significant bit (MSB) to the least significant bit (LSB) is flipped and examined independently until the R_D signal is less than or equal to the high value or greater than or equal to the low value.

Referring to FIG. 8A, several variables used in the calibration procedure are initialized at a first block **801**. For each gain step, a binary variable ADC_HiLo is used to distinguish between the high and low target values. It is initially set equal to 1. A Next_Bit variable is utilized to step through each bit of the DC DAC **337** in the successive approximation algorithm. The Next_Bit variable is initially set equal to MSB_BIT to point to the most significant bit of the DC DAC **337**. In the embodiment shown for the compensation systems **300-700**, the DC DAC **337** is 12 bits so that MSB_BIT is set equal to 12. A GainStep variable is utilized to track each gain step of the AGC DAC **297** for controlling the BB AGC amplifier **307**. The GainStep variable is initially set equal to GS_MIN or the lowest setting of the AGC DAC **297**. In the embodiment shown, GS_MIN is –64 and is incremented to the highest gain step or GS_MAX, which is 63 in the embodiment shown. The

index variable “i” is used as an index for storing variables for calculations performed after each calibration procedure and tracks the GainStep variable. A DC_DAC variable is utilized to track the value programmed into the DC DAC 337 for successive iterations. In the embodiment shown, DC_DAC is a 12-bit variable represented in signed 2’s complement form that ranges from 100000000000b to 011111111111b, where “b” represents a binary value. The binary range represents a decimal range of -2048 to +2047.

At block 801, DC_DAC is initially set equal to ALL_ZERO which means that all 12 bits of DC_DAC are set equal to binary zero. In signed 2’s complement form, this also represents a binary and a decimal value of zero (0). In the first iteration of the calibration procedure, the DC DAC 337 is increased from the lowest value of -2048 and successively increased until the R_D signal becomes equal to a ADC_HI_RANGE constant, which in the embodiment shown is +24. If the DC DAC 337 is to increase from -2048 towards the maximum value of +2047 in the successive approximation, then it is first set approximately equal to the mid-range value of zero. At next block 803, the GainStep variable is written to the AGC DAC 297 to set the gain of the BB AGC amplifier 307 at its lowest level. At next block 805, the DC_DAC variable is written to the DC DAC 337. In this manner, in the first iteration, the AGC DAC 297 is at the lowest gain step and the DC DAC 337 is set equal to zero or at its mid-range level.

At next block 807, the R_D signal is sampled one or more times by the calibration block 401. At next block 809, the arithmetic mean value of valid samples taken at block 807 is stored in a variable ADC_Mean. In the embodiment shown, 48 samples are taken at block 807 and the first 16 are discarded, so that the last 32 samples are considered valid. Thus, the mean value of the last 32 samples is determined and ADC_Mean is set equal to the determined mean value.

At next block 811, it is queried whether ADC_HiLo is equal to 1. Since ADC_HiLo was set equal to one at block 801 during the first iteration, operation proceeds to next block 813, in which it is queried whether the ADC_Mean variable is greater than the ADC_HI_RANGE constant. As described previously, each bit of the DC DAC 337 using the DC_DAC variable is successively tested for each gain step, which in the first iteration is the minimum gain step of GS_MIN, until the R_D signal reaches the ADC_HI_RANGE constant. If the ADC_Mean value has increased beyond ADC_HI_RANGE as determined at block 813, then operation proceeds to next block 817 in which the Next_Bit of the DC_DAC variable is discarded. To discard a bit, its value is changed or “flipped”, where if it is 0, it is changed to 1 and vice-versa. In effect, the bit is discarded if the mean value has overshoot the target value of ADC_HI_RANGE constant. For example, in the first iteration where Next_Bit is equal to 12 in the embodiment shown and initially set to 0, if the mean value ADC_Mean is greater than the ADC_HI_RANGE constant (+24), then the 12th or most significant bit of the DC_DAC variable is flipped “back” to 1 to discard the bit. If this occurs, then DC_DAC becomes equal to 100000000000b or the minimum value of -2048. Otherwise, if the ADC_Mean value is not greater than the ADC_HI_RANGE constant, then block 817 is skipped so that the Next_Bit or bit 12 remains at 0.

Referring to FIG. 8B, if ADC_Mean is not greater than the ADC_HI_RANGE constant as determined at block 813 or after the Next_Bit is discarded at block 817, operation proceeds to block 819 in which it is queried whether Next_Bit is equal to zero. If not, operation proceeds to next block 821 in which Next_Bit is decremented. In the first iteration, Next_Bit is decremented to 11 to test the next bit of DC_DAC in the

successive approximation. In this manner, each bit of the DC DAC 337 is tested until the Next_Bit becomes equal to 0 as determined at block 819. At next block 823, the Next_Bit of DC_DAC is flipped for evaluation. In the first iteration, the Next_Bit or bit 11 of DC_DAC is set equal to 1 so that the DC_DAC variable is increased in value according to the successive approximation algorithm. In particular, had the 12th bit been discarded at block 817 so that DC_DAC became equal to 100000000000b or -2048, then DC_DAC is set equal to 110000000000b or -1024 at block 823. Otherwise, had the 12th bit not been discarded as determined at block 813 so that DC_DAC remained at zero, then DC_DAC is set equal to 010000000000b or +1024 at block 823.

After the Next_Bit of DC_DAC is flipped at block 823, operation proceeds back to block 805 to write the new value of DC_DAC to the DC DAC 337. Operation loops in this manner between blocks 805-823 via block 813 for each bit of the DC_DAC variable until Next_Bit is decremented to zero as determined at block 819. When this occurs, the DC_DAC variable, when programmed into the DC DAC 337 at the lowest gain step of the AGC DAC 297 provides the R_D signal as close as possible to, and less than or equal to, the predetermined ADC_HI_RANGE constant. Operation then proceeds to block 825 where the ADC_HiLo variable is queried. Since ADC_HiLo is still 1 in the first iteration, operation proceeds to next block 827 in which an indexed variable DC_DAC_HI_i is set equal to the DC_DAC variable for storage and/or calculation. Also at block 827, a mean value variable ADC_HI_i is set equal to the current value of ADC_Mean. It is noted that although ADC_Mean should be equal to the ADC_HI_RANGE constant, it may vary somewhat and any variation is stored for use in calculations.

Operation proceeds to block 829 from block 827 to reset variables for the second half of the first iteration of the successive approximation for the current gain step (i). In particular, Next_Bit is set back equal to MSD_BIT, ADC_HiLo is set equal to 0 and the DC_DAC variable is set equal to a binary variable ALL_ONE meaning that all bits of DC_DAC are set equal to one. This initializes the variables for the second half of the calculation for the current gain step in which the DC DAC 337 is started at the maximum value or +2047 and successively decreased according to the successive approximation algorithm until a predetermined ADC_LO_RANGE constant is achieved as determined at block 815. It is noted that DC_DAC is effectively set equal to -1 since 111111111111b in sign 2’s complement form represents -1 which is approximately half way between the maximum DAC value of +2047 and the minimum DAC value of -2048.

From block 829, operation proceeds back to block 805 where the new DC_DAC value is written into the DC DAC 337. Again, one or more samples of the R_D signal are taken at block 807 and the mean value of valid samples are determined and stored into the ADC_Mean variable at block 809. At next block 811, since ADC_HiLo is equal to 0, operation proceeds to block 815 in which it is determined whether ADC_Mean is less than the ADC_LO_RANGE constant. If not, operation proceeds directly to 819 and if so, operation proceeds to next block 817 where the Next_Bit is discarded in a similar manner as previously described. If the Next_Bit is not discarded during the first iteration, then operation proceeds with a DC_DAC value of -1 or 111111111111b. If the Next_Bit is discarded at block 817, then the DC_DAC value is set equal to +2047 or 011111111111b, which is the maximum DAC value.

At next block 819, it is queried whether Next_Bit is equal to 0 and if not, operation proceeds to blocks 821 and 823 where, as before, Next_Bit is decremented and the corre-

sponding bit of the DC_DAC variable is flipped for evaluation. In a similar manner as before, if DC_DAC is equal to -1 or 1111111111b, then at block **823** DC_DAC is next set equal to -1025 or 0111111111b. Alternatively, if DC_DAC was +2047 or 0111111111b, then at block **823** DC_DAC is set equal to +1023 or 0011111111b.

Operation loops in a similar manner for the low to high successive approximation between blocks **805-823** via block **815** until Next_Bit is decremented to zero as determined at block **819**. At this point, the ADC_Mean should be close to, and greater than or equal to, the ADC_LO_RANGE constant as determined at block **815**. After all bits have been examined, operation proceeds to next block **825** in which the value of ADC_HiLo is queried. Since this is the second half of the first iteration at the current gain step, where ADC_HiLo is 0, operation proceeds to next block **831** where the DC_DAC variable is stored into an index variable DC_DAC_LO_i for the current gain step. Also, the current value of ADC_Mean is stored into an index value ADC_LO_i at block **831**. At next block **833**, the variables are initialized for the first half of the next iteration of the successive approximation procedure, as tracked by the GainStep variable. In particular, Next_Bit is set equal to 12, ADC_HiLo is set back equal to 1, and DC_DAC is set back equal to ALL_ZERO. Furthermore, GainStep and the index "i" are both incremented. As described previously, GainStep is initially set to GS_MIN or -64 in the embodiment shown. Thus, at the first occurrence of block **833**, GainStep is set equal to -63 and "i" is incremented to 2. At next block **835**, it is queried whether GainStep has become greater than the GS_MAX constant to determine if calculations have been completed for all gain steps. In the first iteration of block **835**, operation proceeds back to block **803** where the new GainStep value is written into AGC DAC **297**. The entire first and second halves of the successive approximation utilizing the DC_DAC variable is repeated for the next GainStep. In this manner, for each GainStep, the indexed variables DC_DAC_HI_i, ADC_HI_i, DC_DAC_LO_i and ADC_LO_i are determined and locally stored if necessary.

After all calculations for each GainStep have been determined in which GainStep is incremented at block **833** to be greater than GS_MAX as determined at block **835**, then operation proceeds to block **837** as shown in FIG. **8C** in which calculations are initiated using the stored indexed variables. At block **837**, the gain data, referred to as G(i), is determined for each gain step (i). In the embodiment shown, "i" is the index value varying from 1 to 128 representing GainStep values of -64 to +63, respectively. The following equation (4) is used at block **837** to calculate the gain data G(i):

$$G(i) = \frac{(ADC_lsb)}{(DC_DAC_lsb)} * \frac{(ADC_HI_i - ADC_LO_i)}{(DC_DAC_HI_i - DC_DAC_LO_i)} \quad (4)$$

where ADC_lsb is the step value conversion of the ADC **313**, DC_DAC_lsb is the step value conversion of the DC DAC **337** and where ADC_HI_i, ADC_LO_i, DC_DAC_HI_i and DC_DAC_LO_i are the indexed variables previously determined at block **827** and **831**. In the embodiment shown, ADC_lsb is approximately equal to 1 Vpp/64 or 15.625×10⁻⁰³ volts per step and DC_DAC_lsb is approximately equal to 150 mV/4096 or 36.62×10⁻⁰³ mV per step. 128 gain data values G(i) are determined in the embodiment shown. At next block **839**, a filter is applied to smooth the gain data G(i). In one embodiment, a five-wide moving average filter is applied across the gain data G(i) to smooth out the curve. A three-wide filter is used at the end points for the second and second

to last values and the end point values are not changed. In particular, the first three values are averaged and the second value is set equal to the average. Then, the first five values are averaged and the third value is set equal to the average. Then, the second through fifth values are averaged and the fourth value is set equal to the average. Operation of the five-wide moving average continues in this manner until the last five values are averaged and the third to the last value is set equal to the average. Then, the last three values are averaged and the second to last value is set equal to the average, and the filter operation is completed. A filter is utilized since the measured gain values may be calculated in a very noisy environment where substantial variations and inaccuracies would otherwise result.

Operation proceeds from block **839** to block **841** in which a calculated DC offset value Voffset(i) is determined for each gain step (i), where Voffset refers to the calculated DC offset at the input to the BB AGC amplifier **307**. A simplified version of the DC offset value, denoted Voffset(i)_s, is determined according to the following equation (5):

$$Voffset(i)_s = -DC_DAC_lsb * \frac{DC_DAC_LO_i + DC_DAC_HI_i - 4096}{2} \quad (5)$$

The simplified version assumes that the ADC_HI_i and ADC_LO_i variables are set to the ADC_HI_RANGE and ADC_LO_RANGE constants, respectively. In operation, however, the ADC_HI_i and ADC_LO_i variables may vary by a step or two, so that an adjust value ADJ_i is calculated for each gain step (i) according to the following equation (6):

$$ADJ_i = \frac{(ADC_HI_i + ADC_LO_i) * (DC_DAC_HI_i - DC_DAC_LO_i)}{2 * (ADC_HI_i - ADC_LO_i)} \quad (6)$$

The adjust value is utilized to calculate more accurate DC offset values Vo(i) according to the following equation (7):

$$Voffset(i)_s = DC_DAC_lsb * \left[ADJ_i - \frac{DC_DAC_LO_i + DC_DAC_HI_i - 4096}{2} \right] \quad (7)$$

It is noted that for each case in which ADC_HI_i is equal to ADC_HI_RANGE and where ADC_LO_i is equal to ADC_LO_RANGE, that the adjust value ADJ_i cancels and becomes zero. Otherwise, the adjust value is utilized to improve accuracy. Operation proceeds to block **843** to smooth out the DC offset data Voffset(i) in a similar manner as described above for block **839**, such as the five-wide moving average filter with the three-wide filter at both ends.

At next block **845**, DC offset derivative data dV/dG_{dB}(i) is determined for each gain step (i) by first calculating the DC offset value at the output of the BB AGC amplifier **307** according to the equation Vo(i)=Voffset(i)*G(i), and then plugging each Vo(i) value into equation (3) previously described. At next block **847**, the DC offset derivative data dV/dG_{dB}(i) is smoothed in a similar manner as previously described, such as with the five-wide moving average filter with a three-wide filter used at either end points. At next block **849**, the measured and/or calculated data is converted and/or otherwise stored depending upon the particular configura-

tion. For example, for the compensation systems **500-700**, the gain data $G(i)$ is stored in the LUT **501**, for the compensation system **700**, the DC offset data $V_o(i)$ is stored in the LUT **701**, and for the compensation system **600**, the derivative data $dV/dG_{dB}(i)$ is used to determine the maximum gain change limit G_M or one or more gain change limits for one or more gain steps. The determined gain change limit value(s) are stored in the limit block **601**.

It is appreciated that removal of the IF portion of a high performance wireless transceiver, with proper DC compensation and DC calibration, results in a relatively high performance, low cost wireless ZIF transceiver with reduced power requirements. The use of a calibrated DC compensation loop interfaced to the gain loop achieves these goals. Estimation of DC at the output of the baseband gain amplifier and amplification of the DC estimate based on a gain conversion linked with the gain loop provides a DC offset at the input to effectively control DC provided to the baseband processor decoder devices. The calibration procedure provides additional accuracy by periodically measuring actual gain and DC offset and storing one or more gain adjust values or DC offset adjust values. The adjust values are utilized during operation to modify the gain conversion signal or to limit gain change to maintain loop control. Such capability enables a WLAN system to be designed for use at home or in the small business that is relatively robust and that has significant performance with relatively high data throughput operation. A ZIF design in accordance with embodiments of the present invention provides high sensitivity and allows for fast settling of the gain and DC offset loops. Fast settling is desirable because of the bursty and packetized nature of communications. The design also contends well with large amounts of inherent noise which is averaged out or otherwise eliminated in order to compensate for DC offsets.

As described above, a calibration procedure is initially conducted upon power up to measure and store parameters to prepare the wireless transceiver **200** for packet acquisition. Changes in the wireless medium may result in the need for gain changes. Although DC is not transmitted over the wireless medium, changes in the receive radio front end may result in the need for both gain and DC changes. Because the wireless medium is dynamic and unpredictable and because changes may occur in the receive radio front end, the calibration procedure is repeated periodically.

Even though the calibration procedure, if employed, facilitates stability, the conditions of the wireless medium are constantly changing and the wireless transceiver **200** must detect the changes and operate the AGC loop **345** (gain feedback control loop) and the DC loop **347** (DC feedback control loop) to track the changing conditions of the wireless medium. The wireless transceiver **200** detects several contemplated condition changes and performs procedures, such as by the control logic **343**, the signal estimate power block **315**, the DC estimate block **319** and other control logic, to identify the changed condition and take the appropriate response. The contemplated changed conditions include onset of a new packet in the wireless medium causing DC saturation of the ADC measurement window, completion of transmission of a packet in which the wireless device **200** must perform clear channel assessment (CCA), and completion of transmission of a packet by the wireless device **200** itself, in which case the wireless transceiver **200** must prepare to acquire an acknowledgement (ACK) packet if transmitted by the receiving device. As described further below, the wireless transceiver **200** has a limited amount of time to detect each condition change, to determine whether an appropriate response is necessary, and to take the appropriate response.

For each changed condition situation described herein, the wireless transceiver **200** holds the gain feedback control loop at a constant gain level and operates the DC feedback control loop in an attempt to search a stable DC value for the receive signal. The ZIF transceiver **201** continuously processes energy in the wireless medium to generate and provide a receive signal to the baseband processor **203**. Such processing is performed even when there are no packets being transmitted on the wireless medium, so that the gain and DC feedback control loops effectively track the noise floor of the wireless medium. Onset of a new packet usually causes the gain loop to make gain adjustments in an attempt to achieve the target power level for packet acquisition, which could lead to gain saturation. Several gain iterations may be required since the range of the ADC **313** is limited as compared to the total possible signal range. Such changes in gain may cause DC saturation in which the sampled signal rails to maximum or minimum levels of the ADC measurement window. Thus, a very limited amount of information is initially available to the control logic **343**, the signal power estimate block **315** and the DC estimate block **319**.

An attempt to continue operating both the gain and DC loops to acquire the new packet may result in instability since gain change also causes a DC level change. Instead, upon DC saturation, the AGC loop **345** is held constant and the DC level is searched during initial packet onset. Since the noise floor level is not expected to change appreciably after transmission of the packet, the noise floor gain setting, and optionally the DC noise setting, are stored prior to onset of the packet. As soon as packet transmission is completed, the noise gain setting is retrieved and applied to the gain loop and the gain loop is once again held while DC is searched. Optionally, the DC noise setting, if stored, may also be retrieved and applied to the DC loop as a starting point.

FIG. **9** is a timeline diagram illustrating gain and DC loop timing for normal packet onset of short preamble packets. A time T_1 indicates the start of a new slot for transmission of a packet, which begins an on air contention period of time that lasts for about 20 microseconds (μs) and ends at a time T_3 while one or more devices are contending for the slot. A first portion of the contention period is an onset uncertainty time that ends at a time T_2 upon transmission of a new packet **901** in the slot. The new packet **901** starts with a known preamble **903**, which initiates a packet acquisition time period that begins at time T_2 . In this case, the preamble **903** has a duration of approximately 56 μs followed by a start frame delimiter (SFD) **905** having a duration of approximately 16 μs beginning at a time T_5 and ending at a time T_6 . The packet acquisition time is between times T_2 and T_6 , during which time the wireless transceiver **200** must stabilize and lock the DC and gain feedback control loops **345**, **347** on the incoming signal, perform frequency, channel and timing estimation, perform descrambler synchronization, and search and identify the SFD **905** to determine whether the packet is intended for the wireless transceiver **200**. In this case, the AGC/DC acquisition time begins at time T_2 at the onset of the packet **901** and must be completed approximately 20 μs later at a time T_4 . A packet may be transmitted by any one of multiple devices, so that acquisition conditions may be different even if the wireless medium is relatively stable. For example, one device may send a weak signal whereas the next may send a very strong signal and vice-versa.

The gain of the variable LNA **261** is initially set high to detect weak signals and is switched to low gain upon certain conditions if the received signal causes an overload condition as detected by the overload detector **289**, for example. If an overload condition is detected and the LNA **261** is "tripped"

and switched to low gain, this low gain condition is initially held until it is determined whether a packet is being transmitted. If a packet is not detected, a noise spike or the like may have caused the overload condition and the LNA 261 is allowed to switch back to high gain mode if and when the noise condition disappears. If a packet is detected, the state of the LNA 261 may be allowed to change during the preamble of the packet. The LNA 261 may not trip initially upon detection of a packet, but is allowed to trip during the preamble in the event of a strong packet signal. After the preamble portion of the packet is completed, the state of the LNA 261 is held and not allowed to change during the payload portion of the incoming packet.

As described above, in one embodiment the ADC 313 includes only as many bits as necessary to maintain signal integrity with sufficient head room. For example, the ADC 313 may be only a 6-bit converter with a 36 dB of range resulting in approximately 6 dB per bit. The BB AGC amplifier 307, on the other hand, has a significantly greater gain range (e.g., -6 dB to 60 dB) to provide a sufficient dynamic gain range to enable appropriate operation in anticipated environments. In this manner, regardless of the actual signal strength at the receiving device, the existence of DC may cause the signal to initially appear outside the limited 36 dB ADC measurement window range. It is desired to control the AGC loop 345 and the DC loop 347 to resolve the incoming signal as quickly as possible to within the target power range (e.g., 75 percent of the full scale power) of the ADC 313. The signal power estimate block 315 and the DC estimate block 319 monitor the R_D signal output from the ADC 313 to determine whether conditions have changed and/or a packet is being received.

Assuming initial DC conditions are correct and that DC conditions do not substantially change, the signal power estimate block 315 controls the LNA 261 and the AGC loop 345 to bring the signal within target power level. The DC estimate block 319 remains operative to control any DC level changes. Regardless of signal strength, a substantial change in DC level, for whatever reason, may saturate the ADC 313. DC saturation, by itself, does not necessarily cause an overload condition to trip the LNA 261 to low gain since the AC power of the signal itself may be weak. The DC saturation causes a rail condition of the ADC 313, which completely obscures the incoming signal. A DC saturation or rail condition means that all or substantially all of the digital samples are at one "rail" or the other, although not at both rails (which may indicate a gain saturation condition, described below). Two rails are defined including a maximum digital value and minimum digital value at either end of the ADC measurement window. It is desired to reduce or otherwise eliminate DC and set gain so that the signal is at a target power level in which all or substantially all of the digital samples occur within the rails with sufficient headroom to enable correction for signal fluctuations. A DC threshold condition is defined in which a percentage of digital samples that occur at one rail is at or below a predetermined threshold percentage. In one embodiment, the threshold percentage is 90%, so that the DC threshold condition is exceeded when more than 90% of the samples occur at one rail and met when 90% or less of the samples occur at one rail. Since the signal strength is initially unknown and since gain changes affect DC, the AGC loop 345 is initially held at the existing gain setting while the DC loop 347 compensates for DC during the rail condition. The DC saturation or rail condition is corrected by adding a sufficient level of DC offset of the opposite polarity. For example, if the ADC 313 rails positive (or negative), then a sufficient level of

negative (or positive) DC offset is applied at the combiner 303 to substantially center the R_D signal within the range of the ADC 313.

There are several methods that may be employed to eliminate the DC saturation condition. A first method is a step search procedure in which a predetermined DC step amount is repeatedly added until the DC threshold condition is met, or when the percentage of clipped samples drops below the threshold percentage, such as 90% or any other arbitrarily determined threshold percentage. The predetermined DC step amount may also be arbitrarily determined, but should be selected in such a manner to avoid the possibility of overstepping or completely bypassing the ADC measurement window, causing an opposite rail condition. In one embodiment, the predetermined DC step amount is related to the size of the ADC measurement window, so that the added DC does not move the signal by more than the relative size of the ADC measurement window. For example, if the DC step amount is chosen to move the signal by an amount approximately equal to the size of the ADC measurement window, then if the signal is just above an upper rail of the ADC measurement window, the added DC step moves the signal to just above the lower rail of the ADC measurement window. In alternative embodiments, the DC step amount corresponds to any other portion of the ADC measurement window size, such as half size or quarter size, etc.

The step search procedure is advantageous in that it is relatively simple to implement, is relatively well-behaved and converges on the incoming signal in a reasonably sufficient amount of time. Another technique is successive approximation or a binary search method in which the DC range between the existing ADC measurement window and the maximum level range is searched in a binary fashion. For example, the rail condition indicates a positive or negative direction, and the successive approximation approach determines the maximum possible signal range in that direction and then tries full range, half range, quarter range, etc. The direction of each successive binary step is indicated by the rail condition until the signal is detected within the ADC measurement window. The successive approximation approach is bounded in that no more than a predetermined maximum amount of time is consumed no matter how much error exists upon packet onset.

The step search method may be faster than successive approximation in certain instances, such as for small signal onset cases with a modest DC change resulting from a small gain change. The step search method, however, may also take significantly longer for large signal onsets with large gain changes that may produce larger DC offsets. The binary search algorithm of the successive approximation approach, on the other hand, is bounded and will converge to a specified limit within a known uncertainty. The use of one method over the other depends on the expected nature of the input conditions and the consequences when the input is not as expected. For initial packet onset, it may be preferable to use the step search because the critical small packets are acquired faster, which leaves more time for post AGC/DC processing. Since there is adequate time to ensure convergence, the consequence for large packet onsets is acceptable. For the end of packet scenarios, less time is available and bounded convergence time is most important. Trading longer acquisition times to gain rapid acquisition of smaller packets may not be desired.

Eventually, the rail condition of the R_D signal is removed by DC compensation and the signal is either within range or changes to a clipping condition that meets the DC threshold condition previously described, such as clipping at one end or both ends but still less than or equal to the threshold percent-

age (e.g., 90%). If an unbalanced clip condition still remains in which clipping at one rail is still present at or below the specified DC threshold condition, then the gain feedback control loop is released and both the DC and gain loops are operated in a normal mode using the unbalanced clipped signal to eventually lock onto the incoming signal. The DC estimate block **319** controlling the DC loop **347** remains operative to control DC as before. In this case, even though the clipped signal may not be an accurate representation of the actual signal, the estimated gain and DC are close enough so that the actual signal should be acquired sufficiently fast enough with normal loop operations. If the power level of the incoming signal is high or otherwise if the peak-to-peak levels are beyond the range of the ADC **313**, then the clipping condition may be reduced but may not be resolved solely by operation of the DC loop **347**. As long as the percentage of clipped digital signals (at both ends of the gain range) is at or below a predetermined clip rate threshold, then the gain feedback control loop is released and both loops operate in a normal mode to acquire the incoming signal. Again, even though the clipped signal may not be an accurate representation of the actual signal, the estimated gain and DC are close enough so that the actual signal should be acquired sufficiently fast enough with normal loop operations. The clip rate threshold is any suitable arbitrary value, such as 50% or the like. In various embodiments, the AGC loop **345** is unlocked when the clipping condition is substantially balanced when the DC condition has been corrected or when the ratio of clipping between the positive and negative rails of the ADC **313** is below or within the predetermined clip rate threshold.

If, on the other hand, the percentage of clipped digital signals (at both ends of the ADC measurement window range) is above the predetermined clip rate threshold and if clipped samples at both rails is relatively balanced (e.g., if the number of digital samples at the maximum level is roughly equivalent with the number of digital samples at the minimum level), then a gain saturation state or condition is detected and the signal power estimate block **315** enters a clipping mode employing a clip-step procedure to reduce the power level of the received signal to eliminate clipping. The gain saturation condition indicates a significantly high amount of clipping occurring at both rails. The balance condition is any suitable and arbitrary ratio between the minimum and maximum clipped samples, such as 3:1 or 2:1 or the like. If the balance condition is defined as a 3:1 clip ratio, for example, 75% of the clip samples occur at one rail while the remaining 25% at the opposite rail, which would still qualify as "balanced" even though the 3:1 ratio is a relatively rough balance criterion. In the clipping mode, the signal power estimate block **315** samples the R_D signal and determines the amount of clipping present. In one embodiment, the signal power estimate block **315** determines the number of values or samples at maximum range (positive or negative rail) compared to the number of samples less than maximum range for a given total number of samples to estimate the power level based on the clipping information. The signal power estimate block **315** then adjusts gain to reduce the power level. Thus, the signal power estimate block **315** determines the number of rail (or clip) samples for a total number of samples to estimate power level.

A graduated set of thresholds may be employed during the gain saturation condition. If the relative number of clip samples is high, then a higher gain adjustment is used whereas if the relative number of clip samples is low, then a lower gain adjustment is used to resolve the power level of the received signal. For example, a graduated clip gain adjustment may be employed based on clip sample ratios, such as 7/8 (high clipping, high gain adjust), 3/4, 5/8, 1/2, 3/8, 1/8

(low clipping, low gain adjust), etc. Any number of thresholds or break points may be defined or utilized. The amount of clip gain adjust values may depend upon the particular configuration. For example, larger gain adjustments may be used for the calibrated compensation system **700** as compared to other calibrated compensation embodiments since the compensation system **700** more accurately compensates DC in response to gain changes. During the clipping mode, the DC estimate block **319** and the DC loop **347** remain operative to control the DC level. When the clipping condition is eliminated, the AGC loop **345** and the DC loop **347** are both operated as normal to obtain and maintain the R_D signal at the target power level.

It is noted that once the wireless transceiver **200** enters the clipping mode to eliminate the gain saturation condition, there are several options as to when to exit the clipping mode in favor of the normal mode to complete gain and DC lock on the signal. In one embodiment, as soon as the clip rate is below the clip rate threshold, such as, for example, when the total clipping rate drops below 50%, then the gain saturation conditions are no longer met and the normal mode is entered from the clipping mode. In an alternative embodiment, the wireless transceiver **200** may remain in the clipping mode until the clipping condition is substantially removed even after one or more of the gain saturation conditions are no longer true.

A next mode of operation is end of packet re-acquisition (of the wireless medium) which includes two sub-modes including clear channel assessment (CCA) and receive (RX) priority for reception of an expected acknowledge (ACK) packet. An ACK packet is often transmitted by a "receiving device" that has just received a packet from a "transmitting device". ACK packets are highly recommended for most types of information transfer in wireless systems but are not always necessary or even desired. If an ACK packet is expected to be sent, the receiving device, after successfully receiving a packet, transmits the ACK packet. If an ACK packet is expected by the original transmitting device, it attempts to acquire the ACK packet if sent. The transmitting device may resend the packet if an ACK packet is expected but not received from the receiving device. Thus, a transmitting device expecting an ACK packet must detect and acquire the ACK packet if sent. The other devices in the network, if any, need only detect the presence of, but do not need to acquire, the ACK packet in the wireless medium.

FIG. **10** is a timeline diagram illustrating timing of ACK packet priority acquisition at end of packet transmission. A packet **1001**, transmitted by the wireless device **200**, is illustrated ending at a time T_1 at the MAC **205**. The same packet is shown at **1003** while being transmitted in the wireless medium after a delay through the transmitter portion of the ZIF transceiver **201**. In this manner, the transmitted packet **1003** ends at a time T_2 defining a Master On Air Timing Reference for all wireless devices communicating in the wireless medium (ignoring minor RF delays during transmission). The transmit delay through the ZIF transceiver **201**, or $T_2 - T_1$, is approximately $2 \mu\text{s}$ in the embodiment shown. In this manner, the MAC **205** has a $2 \mu\text{s}$ head start to shut down the transmitter and activate the receiver portion of the wireless transceiver **200** to receive an expected ACK packet from the receiving device. The MAC **205** indicates the start of baseband processor **203** receive at a time T_3 , which, in the embodiment shown, is approximately $5 \mu\text{s}$ from the time T_1 when the packet originally left the baseband processor **203**. The time T_3 represents a change condition upon which the wireless transceiver **200** must respond and enter the ACK receive priority mode in an attempt to acquire an ACK packet if sent.

ACK packets are given preferential treatment in that there is a predetermined reserved period of time for ACK transmission immediately after a packet has been sent. In particular, after a packet is received successfully, the receiving device is provided a certain amount of time to send the ACK packet. The device transmitting the ACK packet need not perform CCA but simply transmits the ACK packet as soon as possible and within the reserved period of time for ACK transmission. A device expecting the ACK packet, such as the wireless transceiver **200**, enters the ACK receive priority mode as soon as possible after transmitting a packet. As shown in FIG. **10**, this occurs at time **T3**, which is approximately 5 μ s after the time **T1** when the packet **1001** left the baseband processor. The receiving device transmits an ACK packet **1005** in the wireless medium in response to the transmitted packet **1003**. It is assumed that the receiving device experiences a certain amount of "on air delay" and transmits the ACK packet **1005** in the wireless medium beginning at a time **T4**. In the embodiment shown, the on air delay is assumed to be no less than approximately 9 μ s from the Master On Air Timing Reference time **T2**. An RF delay occurs through the receiver portion of the ZIF transceiver **201**, so that the ACK packet **1005** arrives at the baseband processor **203**, shown as ACK packet **1007**, at a time **T5**. In the embodiment shown, the RF delay through the receiver portion of the ZIF transceiver **201** is approximately 1 μ s. In this manner, the baseband processor **203** of the wireless transceiver **200** has a time from **T3** to **T5** to prepare for the onset of the ACK packet, which is approximately 7 μ s in the embodiment shown.

During the ACK receive priority mode, the expecting device holds its noise floor gain setting during the quiet period between indication of the end of the original packet **1003**, occurring at time **T5**, and the detected onset of the ACK packet **1007** at the baseband processor, occurring at time **T5**. For wireless Ethernet configurations, this period is approximately 7-9 μ s at a minimum. In one embodiment, the gain and DC settings prior to transmission of the original packet are stored by the transmitting device. As described previously, in one embodiment, prior to transmission of the packet **1001**, the wireless transceiver **200** tracks the noise floor of the wireless medium while no packets are being transmitted and determines and stores a noise floor gain setting, and optionally a DC noise setting.

To enter the ACK receive priority mode after transmission of the packet, the transmitting device immediately retrieves and resets the stored gain and DC settings, such as the noise floor gain and DC noise settings. While the gain setting is frozen and held constant, the ACK-expecting device searches the DC level until the quiet period is over. Much of the DC uncertainty can be determined during the quiet period. In other words, the stored gain is retrieved and applied to the AGC loop **345**, which is held at the retrieved gain value during interim period while DC is searched. Then, when the quiet period is over, the AGC loop **345** is released and both loops are operated in the normal packet acquisition mode, described previously, to acquire the ACK packet. It is noted that the DC loop **347** may or may not converge during the quiet period. Regardless of whether it has converged or not, both loops are operated together after the quiet period in normal mode so that the ACK-expecting device can receive and acquire the expected ACK packet if it has been sent. In the Ethernet embodiments, the ACK packet should be initiated within a 20 μ s period. If the ACK packet is not received, the device may or may not re-send the original packet depending upon higher-level operations. It is noted that a receiver of a device other than the device that transmitted the packet may

also desire to operate in ACK priority mode, such as a network monitor that operates in "sniffer" mode or the like used to analyze protocol.

After a packet has been transmitted from the transmitting device to the receiving device, any remaining devices (third party devices) in the same wireless medium enter the CCA mode to determine when the channel is clear to transmit if they have a packet to send. If any packet, including an ACK packet, is transmitted in the wireless medium during CCA, then the remaining devices must back off until the end of the packet to conduct CCA once again. FIG. **11** is a timeline diagram illustrating CCA priority acquisition end of packet timing for the wireless transceiver **200**. A packet **1101** transmitted by another device is shown in the wireless medium and ending at a Master On Air Timing Reference at a time **T1**. A receiver delay is incurred through the ZIF transceiver **201** and the baseband processor **203** until the MAC **205** is able to identify and indicate the end of packet at a time **T2**, which defines a Master Receive Timing Reference for the wireless transceiver **200**. In the embodiment shown, the receiver delay is approximately 6 μ s. Beginning at the Master Receive Timing Reference at time **T2**, the wireless transceiver **200** has a predetermined time allocated to conduct CCA and determine whether the channel is clear, and if so, to declare that the channel is clear, which ends at a time **T5**. A quiet period of approximately 20 μ s is allocated for this purpose. The wireless transceiver **200** also experiences a slight delay to declare CCA to begin preparation of transmitting a packet, which delay begins at a time **T4** prior to the time **T5**. In the embodiment shown, this CCA declaration time is approximately 1 μ s, so that the time from **T2** to **T4** is approximately 19 μ s.

The gain and DC loops of the wireless transceiver **200** must lock onto the energy in the wireless medium at a time **T3** in order to have sufficient time to complete the CCA determination by the time **T4**. In the embodiment shown, the time **T3** is placed at approximately 10 μ s before the time **T4** in order to complete the CCA assessment, so that the wireless transceiver **200** has approximately 9 μ s between times **T2** and **T3** to lock. As described previously, the wireless transceiver **200** determines and stores a noise floor gain setting prior to transmission of the packet **1101**. In the CCA mode, the noise floor gain setting is retrieved and applied in the gain feedback control loop as soon as possible following transmission of the packet **1101**, such as at time **T2** after the receiver delay. The noise power level of the medium may change somewhat, but is not expected to change appreciably after only one packet. The retrieved noise floor gain setting is then held, and the DC level is searched by the DC feedback control loop. In effect, the AGC loop **345** is jammed and held, while a step procedure or binary search or successive approximation or the like is conducted by the DC loop **347** during the CCA mode.

If there is no packet signal in the channel, then the channel is clear and the DC loop should converge to a stable value by the time **T3**. If, however, the DC loop does not converge by the time **T3**, then there is either a packet and channel is not clear or the wireless transceiver **200** is otherwise unable to make the CCA assessment and declaration in time. If a signal is not present, the DC loop **347** typically converges relatively quickly. In one embodiment, the AGC loop **345** is unlocked after approximately 9 μ s and packet acquisition is conducted normally. Although an ACK packet, if present, may not be acquired by a third party device, it is of no consequence since third party devices need not acquire the ACK packet. If the DC loop **347** does not converge at the time **T3**, even after the AGC loop **345** is released, then the channel is deemed to be busy.

A tracking mode is also contemplated, which is a slower, higher level and longer term mode as compared to the modes described above. The tracking mode is a steady state operation and is employed to track the channel over time. A significant amount of data is reviewed over a substantial amount of time and finer, more precise adjustments are made in the operation. In general, steady state conditions are monitored and longer term trends are tracked and adjustments made to follow the channel conditions. Updates to the steady state operating conditions are made more slowly at longer time intervals, such as 10 μ s or the like. Short-term trends may be tracked, but adjustments are made more slowly to avoid over-compensation.

It is noted that data is stored over several successive short cycles and then evaluated. If the error between current settings, such as gain and DC settings or the like, is relatively small, then any such error is stored, but an adjustment is not necessarily made at the next update interval. In this manner, a predetermined "null zone" or threshold error level is employed, so that updates and changes are not made unless and until the measured error exceeds the predetermined null mode values. In other words, updates are made only when a significant amount of error exists to avoid overcompensation and chattering during operation. The null zone operation is even more significant at higher gain settings, because even small gain changes at high gain levels may have a significant impact on operation. In one embodiment, gain adjustments are not made at all if the gain is above a certain threshold level.

Although a system and method according to the present invention has been described in connection with one or more embodiments, it is not intended to be limited to the specific form set forth herein, but on the contrary, it is intended to cover such alternatives, modifications, and equivalents, as can be reasonably included within the spirit and scope of the invention.

The invention claimed is:

1. A method of controlling operation of a wireless communication device configured in a zero intermediate frequency (ZIF) architecture including a DC feedback control loop and a gain feedback control loop, *the method* comprising:

processing energy in a wireless medium to generate a [corresponding] receive signal;
 monitoring the receive signal via a predetermined measurement window;
 detecting a changed condition in the wireless medium;
 holding the gain feedback control loop at a constant gain level after detecting the changed condition; and
 operating the DC feedback control loop [in an attempt] to search a stable DC value for the receive signal while the gain feedback control loop is held *at the constant gain level*.

2. The method of claim 1, [further comprising] *wherein*:
 said processing [comprising] *comprises* processing noise energy in the wireless medium while no packets are being transmitted;

said detecting a changed condition [comprising] *comprises* detecting DC saturation of the measurement window;
 said operating the DC feedback control loop [comprising] *comprises* adding opposite polarity DC to the receive signal to reduce DC level of the receive signal until the measurement window is no longer DC saturated; and

wherein the method further comprises, when the measurement window is no longer DC saturated, operating the DC feedback control loop to control the DC level of the receive signal and releasing the gain feedback control loop to control power level of the receive signal to a predetermined target power level.

3. The method of claim 2, further comprising:
 detecting gain saturation in which the measurement window is clipped at both of predetermined minimum and maximum values above a predetermined clip rate and relatively balanced between the predetermined minimum and maximum values; and

operating the gain feedback control loop to perform a clip-step procedure to reduce gain of the receive signal.

4. The method of claim 3, wherein said clip-step procedure includes using a graduated clip gain adjustment in which gain is adjusted based on an amount of clipping of the receive signal.

5. The method of claim 1, [further comprising:] *wherein* said processing [comprising] *comprises* processing noise energy in the wireless medium while no packets are being transmitted[:], *the method further comprising*:

operating the gain feedback control loop until a noise floor gain value is determined; and
 storing the noise floor gain value.

6. The method of claim 5, [further comprising:] *wherein* said detecting a changed condition in the wireless medium [comprising] *comprises* detecting an end of transmission of a packet in the wireless medium; *wherein said holding the gain feedback control loop at a constant gain level comprises holding the gain at the retrieved noise floor gain value during a predetermined quiet period; the method further comprising*:

retrieving and applying the stored noise floor gain value in the gain feedback control loop;

[said holding the gain feedback control loop at a constant gain level comprising holding the gain at the retrieved noise floor gain value during a predetermined quiet period;] and

after expiration of the quiet period, releasing the gain feedback control loop.

7. The method of claim 6, further comprising:
 prior to transmission of the packet, determining a DC noise value of the DC feedback control loop;
 storing the DC noise value; and

after detecting an end of transmission of the packet in the wireless medium, retrieving and applying the DC noise value to the DC feedback control loop.

8. The method of claim 5, [further comprising:] *wherein* said detecting a changed condition in the wireless medium [comprising] *comprises* detecting an end of transmission of a packet being transmitted in the wireless medium; *and wherein* said holding the gain feedback control loop at a constant gain level [comprising] *comprises* retrieving and applying the stored noise floor gain value in the gain feedback control loop for a predetermined period of time; [and] *the method further comprising* determining whether the DC feedback control loop converges to a stable DC level within the predetermined period of time.

9. The method of claim 8, further comprising[:]
 determining that the wireless medium is busy if the DC feedback control loop does not converge to a stable DC level within the predetermined period of time.

10. A method of operating a wireless communication device to perform initial acquisition of a packet being transmitted in a wireless medium, the wireless communication device configured in a zero intermediate frequency (ZIF) architecture including a DC feedback control loop and a gain feedback control loop, [said] *the method* comprising:

processing radio frequency (RF) energy in the wireless medium to generate a corresponding receive signal;
 determining if a DC threshold condition of the receive signal is exceeded;

if the DC threshold condition is exceeded, holding the gain feedback control loop at a constant gain level and operating the DC feedback control loop to reduce DC of the receive signal until the DC threshold condition of the receive signal is met; and

when the DC threshold condition of the receive signal is met, operating the DC feedback control loop to control the DC level of the receive signal and operating the gain feedback control loop to control a power level of the receive signal to a predetermined target power level.

11. The method of claim 10, wherein said operating the DC feedback control loop to control the DC level of the receive signal comprises controlling the DC level to within a predetermined maximum DC level.

12. The method of claim 10, wherein the receive signal [comprising] comprises an analog signal, the method further comprising[:] sampling the receive signal with an analog to digital converter (ADC) to generate corresponding digital samples, the ADC having a sufficient range to maintain signal integrity without covering a total potential signal range of the receive signal.

13. The method of claim 12, the digital samples ranging between a minimum value and a maximum value, wherein the DC threshold condition is exceeded when a percentage of digital samples at the minimum value or a percentage of digital samples at the maximum value exceed a predetermined threshold percentage of a total number of digital samples.

14. The method of claim 13, wherein the predetermined threshold percentage is 90 percent.

15. The method of claim 13, wherein said operating the DC feedback control loop to reduce the DC level of the receive signal comprises adding a DC offset to the receive signal in an attempt to meet the DC threshold condition.

16. The method of claim 15, wherein said adding a DC offset comprises conducting a step search procedure by repeatedly adding a predetermined DC offset voltage amount until the DC threshold condition is met.

17. The method of claim 15, wherein said adding a DC offset comprises performing a successive approximation DC offset voltage search procedure until the DC threshold condition is met.

18. The method of claim 12, the digital samples ranging between a minimum value and a maximum value, the method further comprising:

detecting a gain saturation state in which clipped digital samples occur at both of the minimum and maximum levels at a rate greater than a predetermined clip ratio threshold and in which a number of digital samples at the minimum level is relatively balanced with a number of digital samples at the maximum level; and

operating the gain feedback control loop in a clipping mode while in the gain saturation state.

19. The method of claim 18, further comprising[:] adjusting the gain level of the gain feedback control loop based on an amount of clipping using a graduated clip gain adjustment.

20. The method of claim 19, wherein said graduated clip gain adjustment includes a corresponding one of a predetermined plurality of gain level adjustments for each of a plurality of predetermined clip ratio ranges.

21. The method of claim 20, wherein said graduated clip gain adjustment is graduated between a high gain adjustment for a high clip ratio and a low gain adjustment for a low clip ratio.

22. A method of operating a wireless transceiver device in preparation for an expected acknowledgment packet, the wireless transceiver device configured in a zero intermediate

frequency (ZIF) architecture and including a DC feedback control loop and a gain feedback control loop, the method comprising:

holding a gain level of the gain feedback control loop constant during a predetermined quiet period after transmission of a packet;

operating the DC feedback control loop during the predetermined quiet period [in an attempt] to resolve DC level while the gain feedback control loop is held constant; and

after the quiet period, releasing the gain feedback control loop to operate in a normal packet acquisition mode.

23. The method of claim 22, further comprising: prior to transmission of the packet, storing a gain level value of the gain feedback loop; and

after transmission of the packet, retrieving the stored gain level value and holding the gain feedback control loop at the retrieved gain level value during the predetermined quiet period.

24. The method of claim 22, further comprising: prior to said transmitting a packet, storing a DC value of the DC feedback control loop; and applying the stored DC value after transmitting the packet.

25. A method of operating a wireless communication device to determine clear channel assessment of a wireless medium, the wireless communication device configured in a zero intermediate frequency (ZIF) architecture and including a DC feedback control loop and a gain feedback control loop, the method [of] comprising:

storing a gain level value of the gain feedback control loop; detecting a packet being transmitted;

after transmission of the packet is completed, retrieving the stored gain level value and holding the gain feedback control loop at the retrieved gain level value;

operating the DC feedback control loop to search a stable DC level; and determining whether the DC loop converges to a stable DC level.

26. The method of claim 25, wherein said storing a gain level value is performed while no packets are being transmitted via the wireless medium.

27. The method of claim 25, further comprising: storing a DC value of the DC feedback control loop prior to said detecting a packet being transmitted; and

applying the stored DC gain setting after packet transmission.

28. The method of claim 25, further comprising: holding the gain level of the gain feedback control loop constant during a predetermined quiet period; and releasing the gain feedback control loop after the predetermined quiet period to operate in a normal mode.

29. The method of claim 25, further comprising: determining if the DC feedback control loop converges to a stable DC level within a predetermined period; and if the DC feedback control loop converges within the predetermined period, operating the DC feedback control loop and the gain feedback control loop in a normal mode.

30. The method of claim 25, further comprising[:] determining that the wireless medium is busy if the DC feedback control loop does not converge to a stable DC level within a predetermined period of time.

31. An apparatus for controlling DC offset voltage comprising:

an automatic gain control (AGC) amplifier having a gain control input configured to set a gain of the AGC amplifier;

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a gain feedback control loop connected to the gain control input configured to set the gain of the AGC amplifier, wherein the gain feedback control loop is configured to detect a changed condition in a wireless medium and to responsively hold the gain of the AGC amplifier constant;

a DC feedback control loop configured to generate a DC offset correction signal to reduce a DC offset voltage while the gain feedback control loop is held constant.

32. The apparatus of claim 31, wherein the DC feedback control loop includes a DC digital to analog converter (DAC) configured to generate the DC offset correction signal.

33. The apparatus of claim 31, wherein the gain feedback control loop includes an AGC digital to analog converter (DAC) configured to generate the DC offset correction signal.

34. The apparatus of claim 31, further comprising an analog to digital converter (ADC) coupled to the AGC amplifier, wherein the changed condition is a rail condition of the ADC.

35. The apparatus of claim 31, wherein the DC control loop includes a DC offset estimator configured to generate a DC estimate signal.

36. The apparatus of claim 35, further comprising a gain converter circuit configured to use the AGC gain to alter the DC estimate signal.

37. The apparatus of claim 36, wherein the gain converter circuit is a look up table.

38. The apparatus of claim 36, wherein the gain converter circuit includes an adjust memory.

39. The apparatus of claim 31, wherein the DC control loop includes a look up table.

40. The apparatus of claim 31, further comprising a calibration circuit configured to inject a predetermined or arbitrary DC level.

41. An apparatus for controlling DC offset voltage comprising:

an automatic gain control (AGC) amplifier;

an AGC gain signal generator connected to the AGC amplifier;

a DC offset signal generator configured to generate a DC offset correction signal,

compensation logic circuitry connected to the AGC gain signal generator and the DC offset signal generator, and configured to detect a changed condition in a wireless medium and to responsively hold the gain of the AGC amplifier constant while controlling the DC offset signal generator to reduce a DC offset.

42. The apparatus of claim 41, wherein the DC offset signal generator is a DC digital to analog converter (DAC).

43. The apparatus of claim 42, wherein the DC DAC is configured to generate a DC offset correction signal for an in phase channel and for a quadrature channel.

44. An apparatus comprising:

a zero intermediate frequency (ZIF) transceiver; and

a baseband processor configured to detect a changed condition in the wireless medium, wherein the baseband processor further comprises:

a gain feedback control loop configured to maintain a constant gain level after detection of the changed condition; and

a DC feedback control loop configured to search for a stable DC value for the receive signal while the gain feedback control loop is maintained at the constant gain level.

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45. The apparatus of claim 44, wherein the baseband processor is further configured to process energy in a wireless medium to generate a receive signal and monitor the receive signal via a predetermined measurement window to detect the changed condition.

46. The apparatus of claim 45, wherein the baseband processor is configured to process noise energy in the wireless medium while no packets are being transmitted and detect DC saturation of the measurement window, and wherein the DC feedback control loop is configured to add opposite polarity DC to the receive signal to reduce a direct current level of the receive signal until the measure window is no longer DC saturated.

47. The apparatus of claim 45, wherein the baseband processor is configured to process noise energy in the wireless medium while no packets are being transmitted, and wherein the gain feedback control loop is configured to operate until a noise floor gain value is determined, and wherein the baseband processor is further configured to store the noise floor gain value.

48. The apparatus of claim 47, wherein the gain feedback control loop is configured to maintain a constant gain level at the retrieved noise floor gain value during a predetermined quiet period associated with a packet, and after expiration of the predetermined quiet period, operate normally.

49. The apparatus of claim 48, wherein the baseband processor is further configured to determine a DC noise value of the DC feedback control loop prior to transmission of the packet, store the DC noise value, and after detection of the transmission of the packet in the wireless medium, retrieve and apply the DC noise value to the DC feedback control loop.

50. An apparatus comprising:

a processor configured to determine if a DC threshold condition of a receive signal is exceeded; wherein the processor further comprises:

a gain feedback control loop configured to maintain a constant gain level in response to a determination that the DC threshold condition of the receive signal is exceeded and control a power level of the receive signal at a predetermined target power level in response to a determination that the DC threshold condition of the receive signal is not exceeded; and

a DC feedback control loop configured to reduce a direct current level of the receive signal until the DC threshold condition of the receive signal is met in response to the determination that the DC threshold condition of the receive signal is exceeded and control the direct current level of the receive signal in response to the determination that the DC threshold condition of the receive signal is not exceeded.

51. The apparatus of claim 50, wherein the processor further comprising an analog to digital converter (ADC) configured to sample the receive signal to generate digital samples.

52. The apparatus of claim 51, wherein the digital samples range between a minimum value and a maximum value, and wherein the DC threshold condition is exceeded when a percentage of the digital samples at the minimum value or a percentage of the digital samples at the maximum value exceed a predetermined threshold percentage of a total number of the digital samples.

53. The apparatus of claim 52, wherein the DC feedback control loop is configured to reduce the direct current level of the receive signal by adding a DC offset to the receive signal.

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54. The apparatus of claim 53, wherein the DC feedback control loop is configured to conduct a step search procedure by repeatedly adding a predetermined DC offset voltage amount until the DC threshold condition is met.

55. The apparatus of claim 51, wherein the digital samples 5 range between a minimum value and a maximum value, wherein the processor is configured to detect a gain saturation state in which clipped digital samples occur at both of the minimum and maximum levels at a rate greater than a pre-determined clip ratio threshold, and wherein the gain feed- 10 back control loop is configured to operate in a clipping mode while in the gain saturation state.

56. The apparatus of claim 55, wherein the gain feedback control loop is further configured to adjust the gain level 15 based on an amount of clipping using a graduated clip gain adjustment.

57. An apparatus comprising:
a processor including:

20 a gain feedback control loop configured to maintain a gain level constant during a predetermined quiet

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period after transmission of a packet and operate in a normal packet acquisition mode after the quiet period; and

a DC feedback control loop configured to resolve a direct current level while the gain feedback control loop maintains the constant gain level.

58. The apparatus of claim 57, wherein the quiet period corresponds to a period during an ACK receive priority mode between an indication of an end of an original packet and a detected onset of an ACK packet.

59. The apparatus of claim 57, wherein the processor is configured to store a gain level value of the gain feedback loop prior to transmission of a packet and, after transmission of the packet, retrieve the stored gain level value and maintain 15 the gain feedback control loop at the retrieved gain level value during the predetermined quiet period.

60. The apparatus of claim 57, wherein the processor is configured to store a DC value of the DC feedback control loop prior to transmission of a packet and apply the stored DC value after transmission of the packet.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : RE42,799 E
APPLICATION NO. : 12/147975
DATED : October 4, 2011
INVENTOR(S) : Baldwin et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page 2, item (56), under "Other Publications", in Column 2, Line 25, delete "Delcaration" and insert -- Declaration --.

Signed and Sealed this
Tenth Day of April, 2012

A handwritten signature in black ink that reads "David J. Kappos". The signature is written in a cursive style with a large initial 'D' and 'K'.

David J. Kappos
Director of the United States Patent and Trademark Office