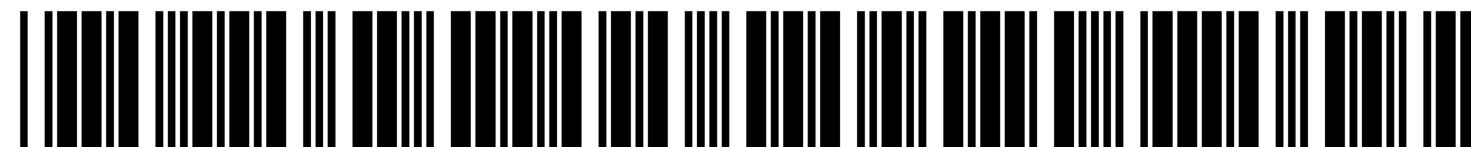

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(54) **METHODS OF PACKAGING AN INTEGRATED CIRCUIT AND METHODS OF FORMING AN INTEGRATED CIRCUIT PACKAGE**

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H01L 21/44	(2006.01)
H01L 21/48	(2006.01)
H01L 21/50	(2006.01)

(52) **U.S. Cl.** **438/112**; 438/612; 438/613

(58) **Field of Classification Search** 438/112, 438/119, 612, 613

See application file for complete search history.

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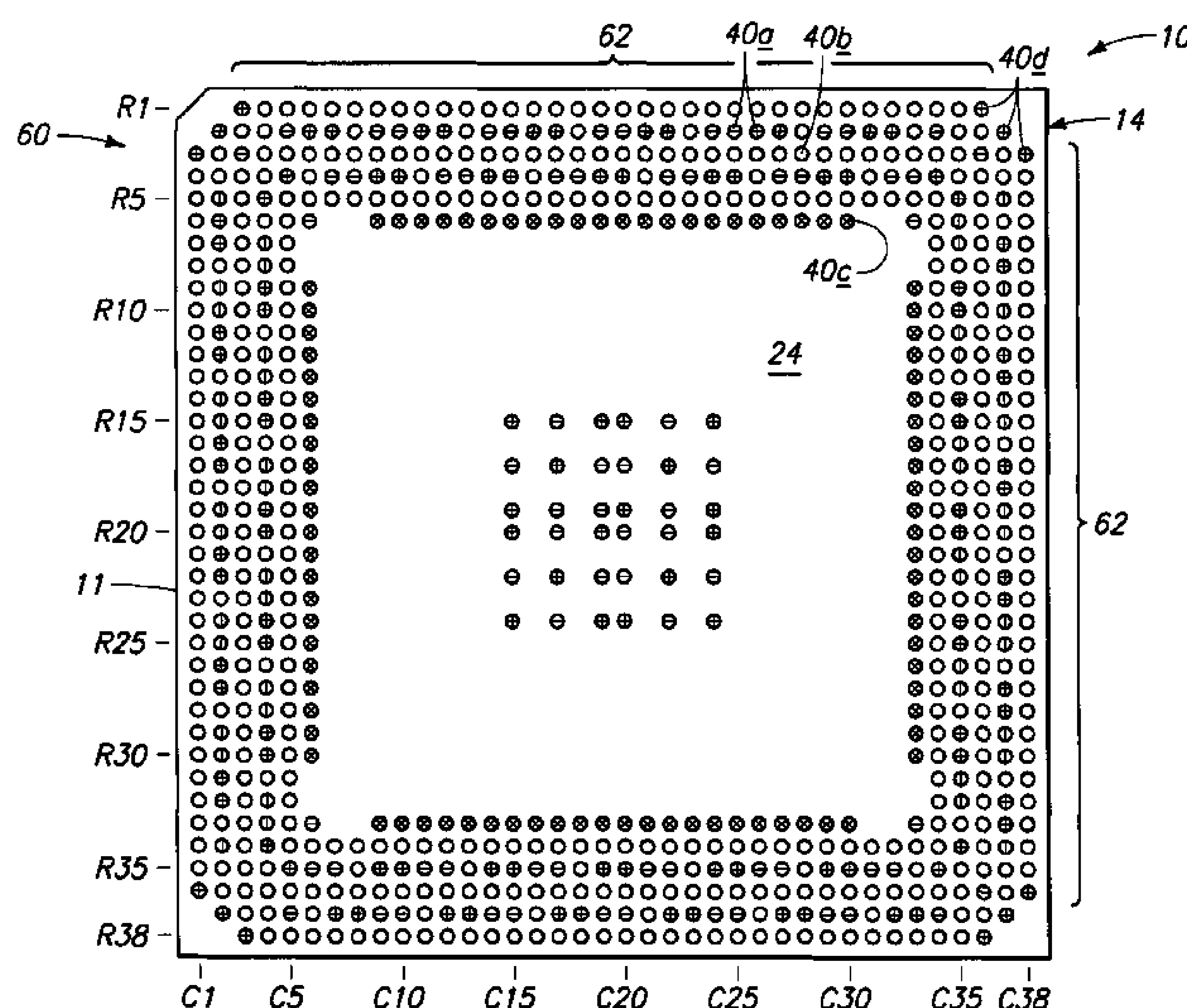
(57) **ABSTRACT**

The present invention includes an integrated circuit package, a ball-grid array integrated circuit package, a method of packaging an integrated circuit, and a method of forming an integrated circuit package. According to one aspect, the present invention provides an integrated circuit package including a substrate including a first surface, a second surface and a plurality of conductors, the first surface includes a plurality of conductive pads adapted to couple with a plurality of corresponding bond pads of a semiconductor die, and the conductors being configured to couple the conductive pads with the second surface; and a plurality of conductive bumps coupled with the second surface of the substrate and electrically coupled with respective conductors, the conductive bumps being formed in an array including a plurality of power bumps and signal bumps, and the signal bumps being individually positioned immediately adjacent at least one power bump. One method of packaging an integrated circuit includes providing a semiconductor die including a plurality of bond pads; providing a package substrate including a plurality of conductive bumps including plural power bumps and plural signal bumps; arranging individual signal bumps to be immediately adjacent at least one power bump; and electrically coupling the bond pads of the semiconductor die with respective conductive bumps.

36 Claims, 4 Drawing Sheets



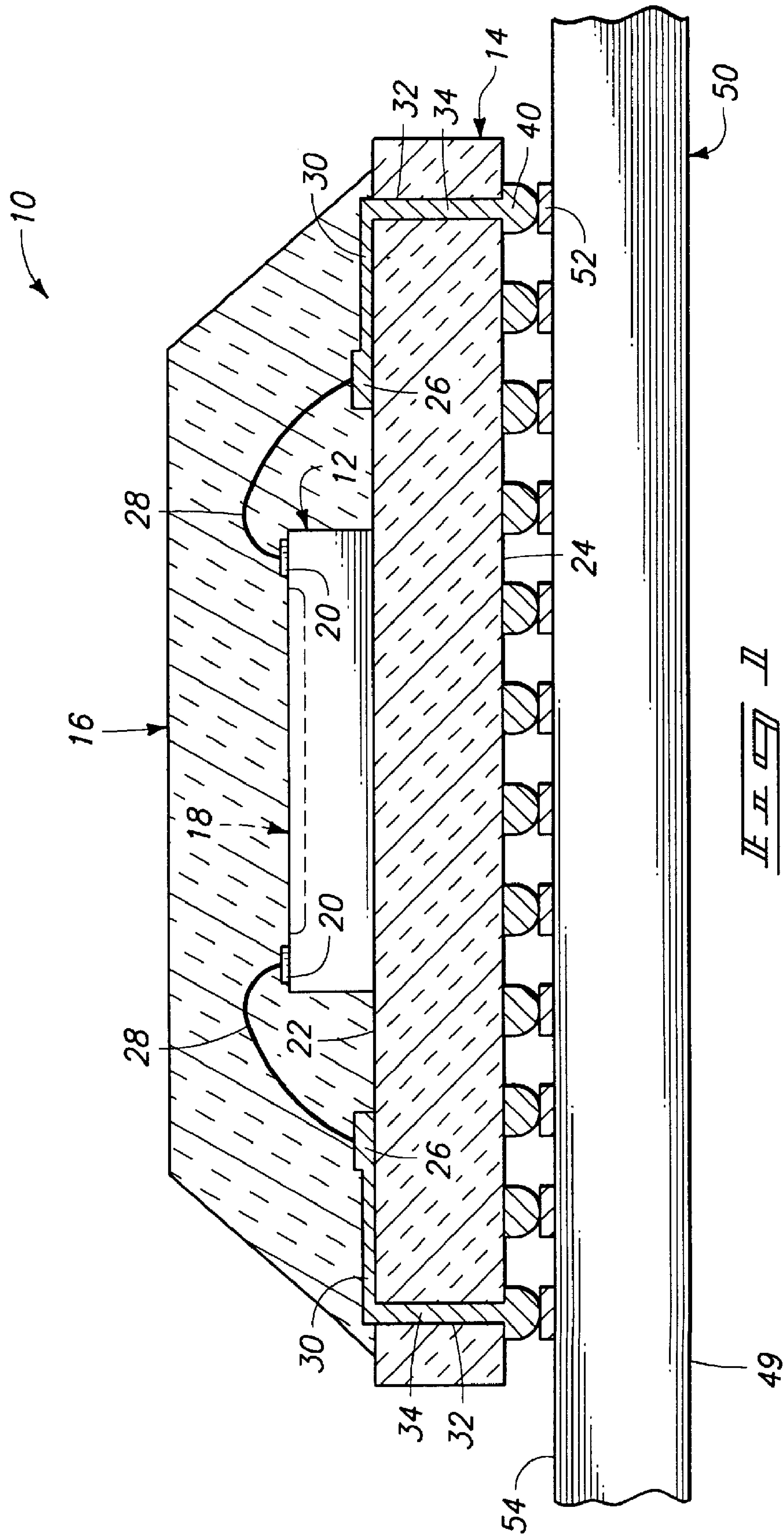
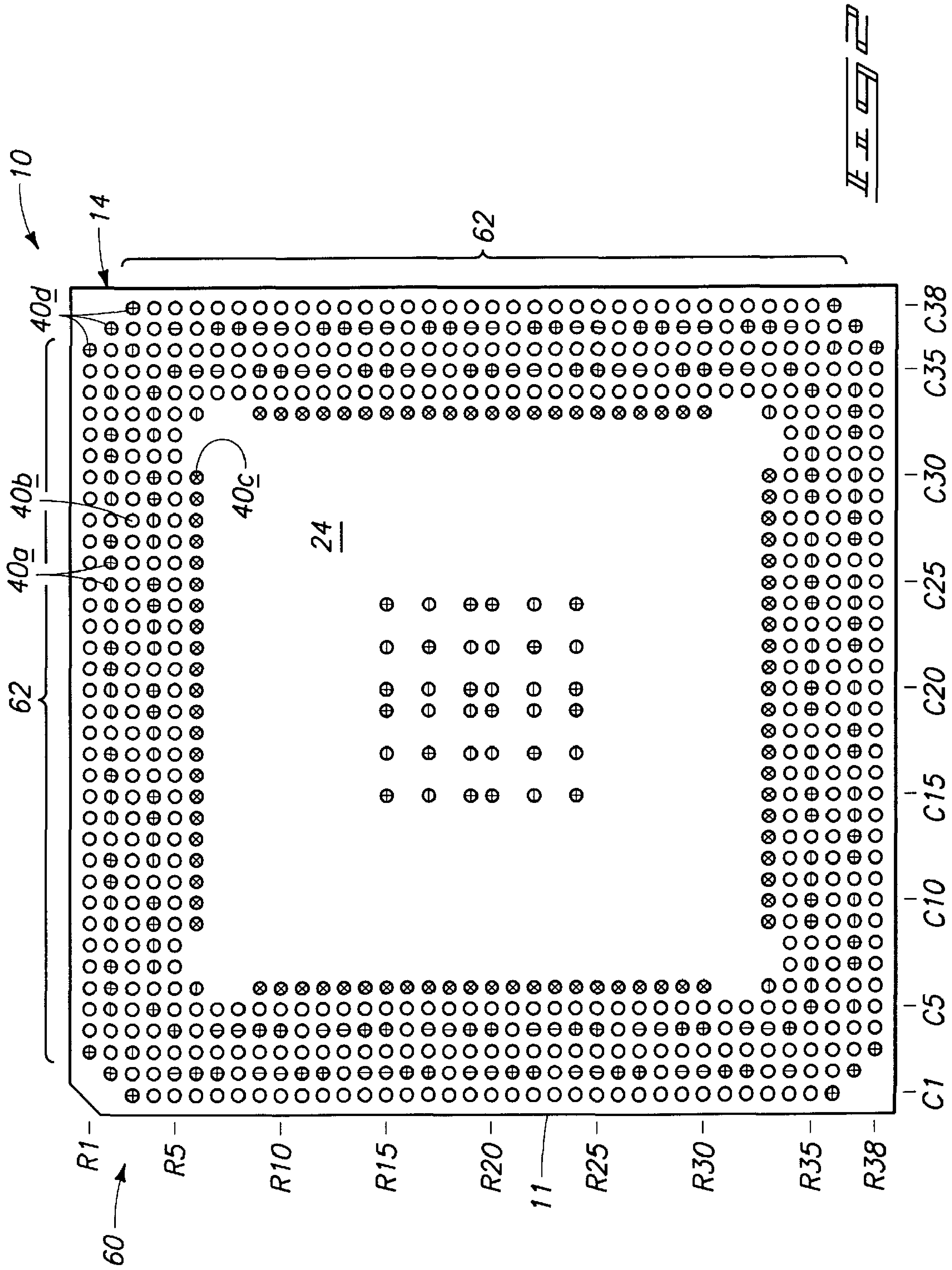
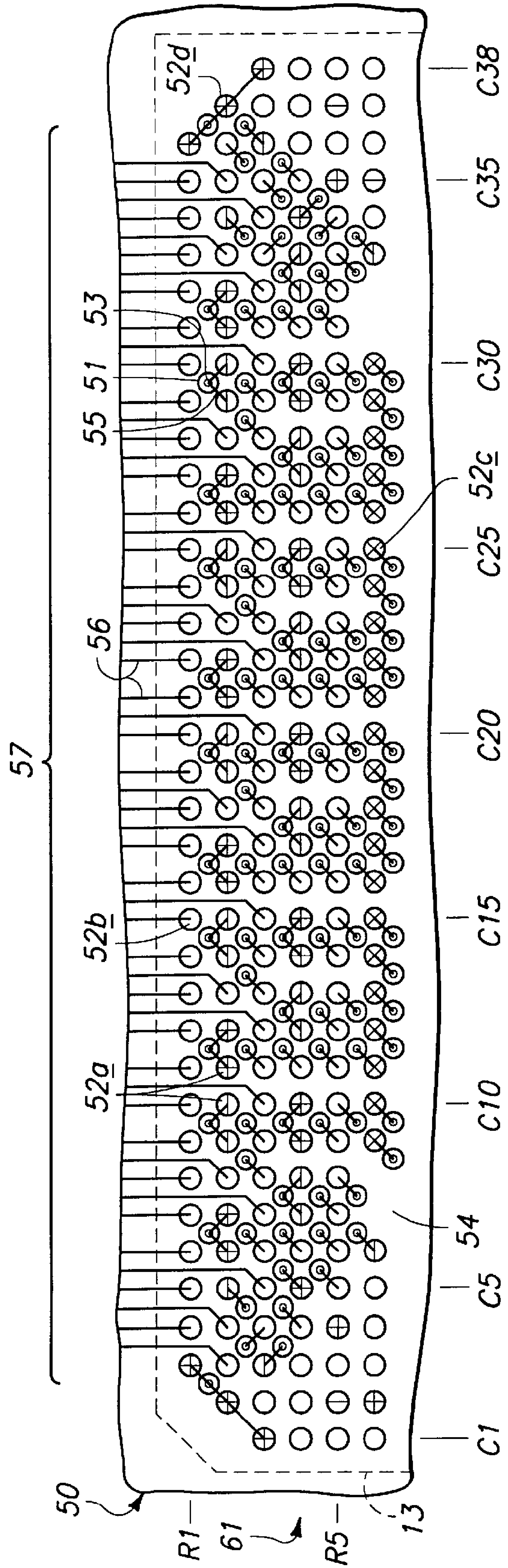
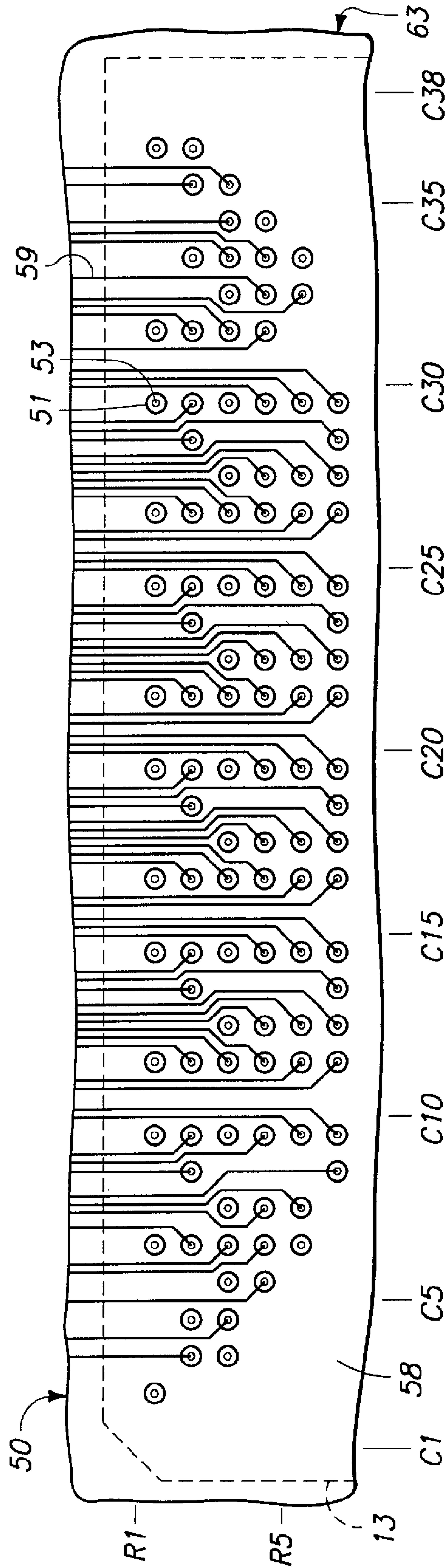


Fig. 1


10
14
62
40d
40b
40c
40a
24
62
11
60
R1
R5
R10
R15
R20
R25
R30
R35
R38
C1
C5
C10
C15
C20
C25
C30
C35
C38
Fig 2


52d
C38
C35
53
51
55
C30
52c
C25
56
57
C20
C15
52b
52a
C10
54
C5
C1
50
R1
61
R5
13


63
C38
C35
59
53
51
C30
C25
C20
C15
C10
C5
58
50
C1
R1
R5
13
Fig 4

METHODS OF PACKAGING AN INTEGRATED CIRCUIT AND METHODS OF FORMING AN INTEGRATED CIRCUIT PACKAGE

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

TECHNICAL FIELD

The present invention relates to integrated circuit packages, ball-grid array integrated circuit packages, and methods of packaging an integrated circuit.

BACKGROUND OF THE INVENTION

Integrated circuit devices are utilized in an ever-increasing number of applications. Exemplary integrated circuit devices include processing devices for manipulating data and memory devices for storing data. Numerous packaging technologies have emerged for housing integrated circuit devices.

Integrated circuit devices are typically mechanically and electrically coupled with an associated substrate. Initially, dual in-line packages (DIPs) were utilized to mount integrated circuits. Dual in-line packages typically include a flat rectangular body and a plurality of leads. The leads are provided in parallel rows at right angles to the body. Plastic dual in-line packages were fabricated by molding epoxy resin on a stamped leadframe which included the integrated circuit device.

Improved mounting and packaging technologies have been developed to provide integrated circuit devices which offer improved operational characteristics. Further, recently introduced device packaging configurations provide an increased number of connections to meet modern semiconductor device demands. For example, the lower surfaces of integrated circuit packages have been utilized to increase the number of connections which can be made to a particular device.

One exemplary packaging technology which provides the aforementioned benefits are ball-grid array (BGA) packages. Ball-grid array devices individually include a flat package utilized for surface mounting a large-scale integrated circuit upon a circuit board or other substrate. Ball-grid array packages have a plurality of solder bumps (balls) which are utilized in place of pins to provide electrical and mechanical connection of the integrated circuit package to a circuit board. Such packages are referred to as fine pitch ball-grid array (FBGA) packages for applications wherein the pitch of the balls is 1 mm or less.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

FIG. **1** is a side cross-sectional view of an integrated circuit package.

FIG. **2** is a plan view of a lower surface of the integrated circuit package of FIG. **1**.

FIG. **3** is a plan view of a surface portion of an exemplary printed circuit board configured to couple with the integrated circuit package of FIG. **1**.

FIG. **4** is a plan view of an intermediate layer of the printed circuit board of FIG. **3**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

One aspect of the present invention provides an integrated circuit package comprising: a substrate including a first surface, a second surface and a plurality of conductors, the first surface includes a plurality of conductive pads adapted to couple with a plurality of corresponding bond pads of a semiconductor die, and the conductors being configured to couple the conductive pads with the second surface; and a plurality of conductive bumps coupled with the second surface of the substrate and electrically coupled with respective conductors, the conductive bumps being formed in an array including a plurality of power bumps and signal bumps, and the signal bumps being individually positioned immediately adjacent at least one power bump.

A second aspect of the present invention provides an integrated circuit package comprising: a substrate including a first surface, a second surface and a plurality of conductors, the first surface includes a plurality of conductive pads adapted to couple with a plurality of corresponding bond pads of a semiconductor die, and the conductors being configured to couple the conductive pads with the second surface; and a plurality of conductive bumps coupled with the second surface and electrically coupled with respective conductors of the substrate, the conductive bumps including a plurality of power bumps and signal bumps formed in an array having plural sides individually comprising at least a majority of signal bumps.

According to another aspect, the present invention provides a ballgrid array integrated circuit package comprising: a semiconductor die having a plurality of bond pads; a substrate including a first surface including a plurality of conductive pads, a second surface, and a plurality of conductors to electrically couple the conductive pads of the first surface with the second surface, the semiconductor die being coupled with the first surface and the bond pads being electrically coupled with the conductive pads and the conductors; a plurality of conductive balls coupled with the second surface and electrically coupled with respective ones of the conductors, conductive pads and bond pads, the conductive balls including a plurality of power balls and signal balls formed in an array having plural sides; and wherein individual signal balls are positioned immediately adjacent at least one power ball, and the sides of the array individually comprise at least a majority of signal balls.

Another aspect of the present invention provides a ball-grid array integrated circuit package comprising: a semiconductor die including integrated circuitry electrically coupled with a plurality of bond pads; a substrate including a first surface including a plurality of conductive pads, a second surface, and a plurality of vias including respective via conductors to electrically couple the conductive pads of the first surface with the second surface, the semiconductor die being coupled with the first surface; plural wire bonding connections configured to electrically couple the bond pads with the conductive pads and the via conductors; a plurality of conductive balls coupled with the second surface and adapted to electrically couple ones of the conductors, conductive pads and bond pads with external circuitry, and including a plurality of

power balls and signal balls formed in an array having plural sides; and wherein individual signal balls are positioned immediately adjacent at least one power ball, and the sides of the array individually comprise signal balls.

Another aspect provides a method of packaging an integrated circuit comprising: providing a semiconductor die including a plurality of bond pads; providing a package substrate including a plurality of conductive bumps including plural power bumps and plural signal bumps; arranging individual signal bumps to be immediately adjacent at least one power bump; and electrically coupling the bond pads of the semiconductor die with respective conductive bumps.

Another aspect of the present invention provides a method of packaging an integrated circuit comprising: providing a semiconductor die including a plurality of pads; providing a package substrate including a plurality of conductive bumps arranged in an array including plural power bumps and plural signal bumps; arranging plural sides of the array to individually include at least a majority of signal bumps; and electrically coupling the pads of the semiconductor die with respective conductive bumps.

According to another aspect, the present invention provides a method of forming an integrated circuit package comprising: providing a package substrate including a plurality of conductive bumps including plural power bumps and plural signal bumps; and arranging individual signal bumps to be immediately adjacent at least one power bump.

According to yet another aspect, the present invention provides a method of packaging an integrated circuit comprising: providing a package substrate including a plurality of conductive bumps arranged in an array including plural power bumps and plural signal bumps; and arranging plural sides of the array to individually include a majority of signal bumps.

Referring to FIG. **1**, an integrated circuit package **10** is illustrated. Integrated circuit package **10** comprises a ball-grid array (BGA) package or fine pitch ball-grid array (FBGA) package in the described embodiment. However, the present invention is applicable to other integrated circuitry packaging technologies.

The depicted integrated circuit package **10** includes a semiconductor die **12** and a package substrate **14**. Package substrate **14** comprises a printed circuit board (PCB) in an exemplary embodiment. Package substrate **14** includes a first surface **22** and an opposing second surface **24**. Semiconductor die **12** is attached to surface **22** of package substrate **14** using an adhesive (not shown) or other attachment technique. Integrated circuit package **10** additionally includes a housing **16** defined by an encapsulant, such as epoxy.

Semiconductor die **12** includes integrated circuitry **18** coupled with a plurality of bond pads **20**. Integrated circuitry **18** of semiconductor die **12** includes processing circuitry or memory circuitry in exemplary configurations.

Surface **22** of package substrate **14** supports a plurality of conductive pads **26** coupled with respective conductive traces **30**. Conductive pads **26** are provided to electrically couple with bond pads **20** of semiconductor die **12**. Wire bonding connections **28** are utilized in the described embodiment to electrically couple bond pads **20** with conductive pads **26**. Other electrical connection configurations can be utilized to couple bond pads **20** with conductive pads **26**.

Package substrate **14** includes a plurality of vias **32** formed intermediate first surface **22** and second surface **24**. Plural via conductors **34** are provided within respective vias **32**. Via conductors **34** can electrically couple conductive pads **26** upon first surface **22** with second surface **24**. Only two exemplary vias **32** are illustrated in FIG. **1**. Typically, substrate **14** includes hundreds of vias **32** and via conductors **34** to provide appropriate electrical connections intermediate integrated circuitry **18** and external circuitry or power sources (not shown). Package substrate **14** can include power and ground connections for coupling with selected conductive pads **26** and bond pads **20** of semiconductor die **18**. Although not depicted in FIG. **1**, such power and ground connections can comprise conductive planes extending substantially throughout the length of package substrate **14**.

As depicted in FIG. **1**, a plurality of conductive bumps **40** are provided upon second surface **24** of package substrate **14**. Conductive bumps **40** individually comprise a conductive material, such as solder. Conductive bumps **40** are coupled with respective via conductors **34**. Although only two of conductive bumps **40** are illustrated coupled with via conductors **34** in the illustrated configuration of FIG. **1**, typically all of the conductive bumps **40** are coupled with respective ones of via conductors **34**.

Conductive bumps **40** are electrically coupled with respective via conductors **34**, conductive pads **26**, traces **30**, wire bonding connections **28**, and bond pads **20** of semiconductor die **18**. Conductive bumps **40** are configured to couple respective bond pads **20** of semiconductor die **18** with external circuitry.

In the depicted configuration, conductive bumps **40** of integrated circuit package **10** are coupled with external circuitry comprising an external substrate **50** in the depicted arrangement. An exemplary external substrate **50** comprises a motherboard. External substrate **50** includes opposing surfaces **49**, **54**. A plurality of conductive pads **52** configured to couple with respective conductive bumps **40** are provided upon upper surface **54** of external substrate **50**. Plural conductive traces (shown in FIG. **3** and FIG. **4**) can be coupled with individual conductive pads **52** to provide electrical coupling of respective conductive bumps **40** with circuitry external of integrated circuit package **10**.

Although not distinguished as such in FIG. **1**, conductive bumps **40** define either a power conductor or an input/output (I/O) signal conductor. Exemplary power conductors are configured to provide coupling with voltage references such as first and second different voltage values VDD and VSS. I/O signal conductors are configured to pass input/output signals intermediate semiconductor die **12** and integrated circuitry **18**. In an exemplary embodiment, data is inputted to and outputted from semiconductor die **12** via such I/O signaling conductors.

As mentioned above, the depicted integrated circuit package **10** comprises a ball-grid array (BGA) package wherein conductive bumps **40** comprise solder balls. In one embodiment, integrated circuit package **10** comprises a fine pitch ball-grid array (FBGA) where the pitch of solder ball conductive bumps **40** is one millimeter or less.

Referring to FIG. **2**, a plurality of conductive bumps **40** upon surface **24** of package substrate **14** are illustrated. Conductive bumps **40** are arranged in an array **60** upon substrate surface **24**. The depicted array is exemplary and conductive bumps **40** can be arranged in other desired configurations in accordance with the present invention.

The depicted conductive bumps **40** include plural power bumps **40**a, signal bumps **40**b, differential bumps **40**c, and corner bumps **40**d. Power bumps **40**a can comprise VSS bumps represented by a minus sign and VDD power bumps represented by a plus sign. Signal bumps **40**b are preferably individually positioned immediately adjacent at least one power bump **40**a and can be individually configured to communicate one of input signals and output signals. Positioning

of signal bump **40**b adjacent at least one power bump **40**a reduces noise within the signals communicated within the individual signal bumps **40**b.

Differential signaling bumps **40**c communicate differential signals and typically may be spaced from power bumps **40**a without adverse performance results. Alternatively, differential signaling bumps **40**c may be individually placed immediately adjacent at least one power bump **40**a in another arrangement. Corner bumps **40**d are diagonally arranged intermediate adjacent sides in the depicted arrangement.

The depicted conductive bump array **60** includes a plurality of sides **62**. Sides **62** in the present description individually include conductive bumps **40** within row R**1** and columns C**3**-C**36**, column C**1** and rows R**3**-R**36**, column C**38** and rows R**3**-R**36**, and row R**38** and columns C**3**-C**36**, respectively. Array sides **62** preferably individually comprise signal bumps **40**b adjacent a periphery **11** defined by package substrate **14** of integrated circuit package **10** as shown. Alternatively, array sides **62** individually comprise a majority of signal bumps **40**b. Such enables improved routing with external circuitry coupled with integrated circuit package **10** as described below.

Referring to FIG. **3** and FIG. **4**, traces formed upon and within a motherboard substrate **50** are shown. FIG. **3** illustrates a plurality of conductive pads **52** and respective traces formed over surface **54** of external substrate **50**. FIG. **4** illustrates a plurality of vias and traces at an intermediate level within external substrate **50**. A footprint **13** corresponding to periphery **11** of integrated circuit device **10** is illustrated in FIG. **3** and FIG. **4**.

Referring specifically to FIG. **3**, a portion of an array **61** of conductive pads **52** configured to couple with conductive bumps **40** of integrated circuit package **10** is depicted. Array **61** includes a plurality of sides **57** although only one such side is illustrated. Sides **57** in the present description include conductive pads **52** corresponding to conductive bumps **40** within row R**1** and columns C**3**-C**36**, column C**1** and rows R**4**-R**36**, column C**38** and rows R**3**-R**36**, and row R**3** and columns C**3**-**36**, respectively. Although only one portion including one side **57** of array **61** is shown, the illustrated pattern of conductive pads **52** is preferably repeated for the remaining portions and sides **57** of array **61**.

The conductive pads **52** illustrated in FIG. **3** are configured to couple directly with corresponding conductive bumps **40** of package substrate **14**. Conductive pads **52** include power conductive pads **52**a configured to couple with power conductive bumps **40**a, signal conductive pads **52**b configured to couple with conductive bumps **40**b, differential conductive pads **52**c configured to couple with differential conductive bumps **40**c, and corner conductive pads **52**d configured to couple with corner conductive bumps **40**d.

A plurality of traces **55**, **56** are formed upon surface **54** to provide electrical coupling of conductive pads **52** with other circuit components either provided upon substrate **50** or external to the substrate **50**. As illustrated, a plurality of vias **51** are also provided within external substrate **50**. Via conductors **53** are provided within respective vias **51**. Via conductors **53** are operable to elevationally electrically couple various layers of external substrate **50**.

For example, via conductors **53** operate to couple the upper surface shown in FIG. **3** with an intermediate layer of external substrate **50** depicted in FIG. **4**. Referring to FIG. **3**, a plurality of conductive traces **55** are formed upon surface **54** to couple via conductors **53** with corresponding conductive pads **52**. Power conductive pads **52**a, differential conductive pads **52**c and corner conductive pads **52**d are individually coupled with respective traces **55** and via conductors **53** in the depicted arrangement.

The depicted traces **56** upon surface **54** couple conductive pads **52** with circuitry outside of footprint **13** of integrated circuit package **10**. As shown in FIG. **4**, a plurality of traces **59** operate to couple via conductors **53** with circuitry outside of footprint **13** of integrated circuit package **10** at an intermediate level of substrate **50**. Although not shown, other intermediate levels within substrate **50** may be provided.

In the preferred configuration, sides **62** of array **60** include at least a majority of signal conductive bumps **40**b. Accordingly, corresponding sides **57** of array **61** include at least a majority of I/O signal conductive pads **52** which correspond to the pattern of conductive bumps **40**.

In the depicted configuration, signal conductive pads **52**b of sides **57** are coupled with traces **56** which extend across surface **54** of external substrate **50** outside of footprint **13**. As such, lateral connections with vias are not necessary for coupling signal conductive pads **52**b. Accordingly, real estate (surface area) located laterally and intermediate adjacent signal bumps **52**b of sides **57** can be utilized to form traces **56**.

More specifically, additional real estate (surface area) is provided intermediate adjacent signal conductive pads **52**b of sides **57** enabling additional conductive traces **56** coupled with conductive pads **52** located in the interior of array **61** to pass intermediate adjacent signal conductive pads **52**b of sides **57**. This provides electrical coupling of an increased number of conductive pads **52** with external circuitry outside of footprint **13** of integrated circuit package **10** using traces **56** formed upon surface **54**. Such is provided without having to utilize as many vias **51** and via conductors **53** as would otherwise be required. Such provides the added benefit of reducing the number of layers including conductive circuitry within external substrate **50** compared with other arrangements wherein sides **57** individually include some power conductive pads **52**a.

For example, if one of conductive pads **52** located within side **57** were coupled with power (i.e., a power conductive pad **52**a) then the real estate adjacent thereto on at least one side would be coupled with a via conductor **53** to provide coupling with the power or ground location coupled at another level of substrate **50**. Accordingly, a trace **56** could not be formed over this portion of surface **54** as is provided in the depicted configuration.

Referring to FIG. **4**, a plurality of traces **59** are depicted formed upon a surface **58** of an intermediate layer **63** of external substrate **50**. Layer **63** is located intermediate opposing surfaces **49**, **54** of substrate **50**. The depicted vias **51** and via conductors **53** correspond to the depicted vias **51** and via conductors **53** illustrated in FIG. **3**. Via conductors **53** are coupled with selected traces **59** upon surface **58** providing coupling with circuitry (not shown) outside of the footprint **13** of integrated circuit package **10**. Some via conductors **53** are not coupled with traces **59** formed upon surface **58**. Such via conductors **53** are typically coupled with traces formed upon other layers of substrate **50** (not shown).

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

What is claimed is:

1. A method of packaging an integrated circuit comprising:

providing a semiconductor die including a plurality of bond pads;

providing a package substrate including a plurality of conductive bumps including plural power bumps and plural signal bumps;

arranging individual signal bumps to be immediately adjacent at least one power bump; and

electrically coupling the bond pads of the semiconductor die with respective conductive bumps.

2. The method according to claim **1** further comprising:

providing an external substrate having a plurality of conductive pads; and

electrically coupling the conductive bumps with respective conductive pads of the external substrate.

3. The method according to claim **1** wherein the providing the package substrate comprises providing a package substrate including conductive bumps formed as balls of a ball-grid array integrated circuit package.

4. The method according to claim **1** further comprising:

forming plural vias within the package substrate; and

providing conductors within the vias.

[5. A method of packaging an integrated circuit comprising:

providing a semiconductor die including a plurality of pads;

providing a package substrate including a plurality of conductive bumps arranged in an array including plural power bumps and plural signal bumps;

arranging plural sides of the array to individually include at least a majority of signal bumps; and

electrically coupling the pads of the semiconductor die with respective conductive bumps.**]**

6. **[**The method according to claim **5** further comprising**]** *A method of packaging an integrated circuit comprising:*

providing a semiconductor die including a plurality of pads;

providing a package substrate including a plurality of conductive bumps arranged in an array including plural power bumps and plural signal bumps;

arranging plural sides of the array to individually include at least a majority of signal bumps;

electrically coupling the pads of the semiconductor die with respective conductive bumps; and

arranging individual signal bumps to be immediately adjacent at least one power bump.

7. The method according to **[**claim **5]** *claim 6* further comprising:

providing an external substrate having a plurality of conductive pads; and

electrically coupling the conductive bumps with respective conductive pads of the external substrate.

8. The method according to **[**claim **5]** *claim 6* wherein the providing the package substrate comprises providing a package substrate including conductive bumps formed as balls of a ball-grid array integrated circuit package.

9. The method according to **[**claim **5]** *claim 6* further comprising:

forming plural vias within the package substrate; and

providing via conductors within the vias.

10. A method of forming an integrated circuit package comprising:

providing a package substrate including a plurality of conductive bumps including plural power bumps and plural signal bumps; and

arranging individual signal bumps to be immediately adjacent at least one power bump.

11. The method according to claim **10** further comprising providing a plurality of conductive pads configured to couple with the **[**a**]** plurality of bond pads of an integrated circuit and the power bumps and the signal bumps.

12. The method according to claim **10** wherein the providing the package substrate comprises providing the package substrate including conductive bumps formed as balls of a ball-grid array integrated circuit package.

[13. A method of packaging an integrated circuit comprising:

providing a package substrate including a plurality of conductive bumps arranged in an array including plural power bumps and plural signal bumps; and

arranging plural sides of the array to individually include a majority of signal bumps.**]**

14. **[**The method according to claim **13** further comprising**]** *A method of packaging an integrated circuit comprising:*

providing a package substrate including a plurality of conductive bumps arranged in an array including plural power bumps and plural signal bumps;

arranging plural sides of the array to individually include a majority of signal bumps; and

arranging individual signal bumps to be immediately adjacent at least one power bump.

15. The method according to **[**claim **13]** *claim 14* further comprising providing a plurality of conductive pads configured to couple with **[**the**]** a plurality of bond pads of an integrated circuit and the power bumps and the signal bumps.

16. The method according to **[**claim **13]** *claim 14* wherein the providing the package substrate comprises providing a package substrate including conductive bumps formed as balls of a ball-grid array integrated circuit package.

17. A method of packaging an integrated circuit comprising:

providing a semiconductor die including a plurality of pads;

providing a package substrate including a plurality of conductive bumps arranged in an array including plural power bumps and plural signal bumps;

arranging plural sides of the array to individually include at least a majority of signal bumps;

arranging plural rows or columns of the array to individually include at least a majority of power bumps; and

electrically coupling the pads of the semiconductor die with respective conductive bumps.

18. The method according to claim 17 wherein the plural rows or columns of the array are individually adjacent to respective ones of the plural sides of the array.

19. The method according to claim 18 further comprising arranging each of the majority of signal bumps in the plural sides of the array to be immediately adjacent at least one of the plural power bumps.

20. The method according to claim 17 wherein the plurality of conductive bumps arranged in an array include a center array substantially spaced apart from a periphery array.

21. The method according to claim 20 wherein the center array includes a majority of power bumps.

22. The method according to claim 17 wherein the plural power bumps comprise Vss or Vdd bumps.

23. The method according to claim 17 further comprising arranging each of the majority of signal bumps in the plural sides of the array to be immediately adjacent at least one of the plural power bumps.

24. The method according to claim 17 further comprising arranging a plural of corner bumps diagonally arranged intermediate adjacent sides of the array.

25. The method according to claim 17 further comprising:

providing an external substrate having a plurality of conductive pads; and

electrically coupling the conductive bumps with respective conductive pads of the external substrate.

26. The method according to claim 17 wherein the providing the package substrate comprises providing a package substrate including conductive bumps formed as balls of a ball-grid array integrated circuit package.

27. The method according to claim 17 further comprising:

forming plural vias within the package substrate; and

providing conductors within the vias.

28. A method of packaging an integrated circuit comprising:

providing a package substrate including a plurality of conductive bumps arranged in an array including plural power bumps and plural signal bumps;

arranging plural sides of the array to individually include a majority of signal bumps; and

arranging plural rows or columns of the array to individually include at least a majority of power bumps.

29. The method according to claim 28 wherein the plural rows or columns of the array are individually adjacent to the plural sides of the array.

30. The method according to claim 28 wherein the plurality of conductive bumps arranged in an array include a center array substantially spaced apart from a periphery array.

31. The method according to claim 30 wherein the center array includes a majority of power bumps.

32. The method according to claim 29 further comprising arranging individual ones of the majority of signal bumps in the plural sides of the array to be immediately adjacent at least one of the majority of power bumps of the plural rows or columns of the array.

33. The method according to claim 28 wherein the plural power bumps comprise Vss or Vdd bumps.

34. The method according to claim 28 further comprising arranging individual ones of the majority of signal bumps in the plural sides of the array to be immediately adjacent at least one of the plural power bumps.

35. The method according to claim 28 further comprising:

providing an external substrate having a plurality of conductive pads; and

electrically coupling the conductive bumps with respective conductive pads of the external substrate.

36. The method according to claim 28 further comprising arranging a plurality of corner bumps diagonally arranged intermediate adjacent sides of the array.

37. The method according to claim 28 wherein the providing the package substrate comprises providing a package substrate including conductive bumps formed as balls of a ball-grid array integrated circuit package.

38. The method according to claim 28 further comprising:

forming plural vias within the package substrate; and

providing conductors within the vias.

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