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(54) **SYSTEM AND METHOD FOR POWER-EFFICIENT CHARGING AND DISCHARGING OF A CAPACITIVE LOAD FROM A SINGLE SOURCE**

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(51) **Int. Cl.**
***H02M 3/07*** (2006.01)

(52) **U.S. Cl.** .......................................... **363/60**; 307/109

(58) **Field of Classification Search** .................... 363/56, 363/59, 60, 61; 320/166; 307/106, 109, 110
See application file for complete search history.

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(57) **ABSTRACT**

A system and method for efficiently charging and discharging a capacitive load from a single voltage source. The system includes a first switch for selectively connecting the voltage source to the load and a second switch for selectively providing a short across the load as may be common in the art. A particularly novel aspect of the invention resides in the provision of plural capacitive elements and a switching mechanism for selectively connecting each of the capacitive elements to the load whereby the load is gradually charged or discharged. In the illustrative embodiment, the switching mechanism includes a set of switches for selectively connecting each of the capacitive elements to the capacitive load and a switch control mechanism for selectively activating the switches.

**16 Claims, 4 Drawing Sheets**

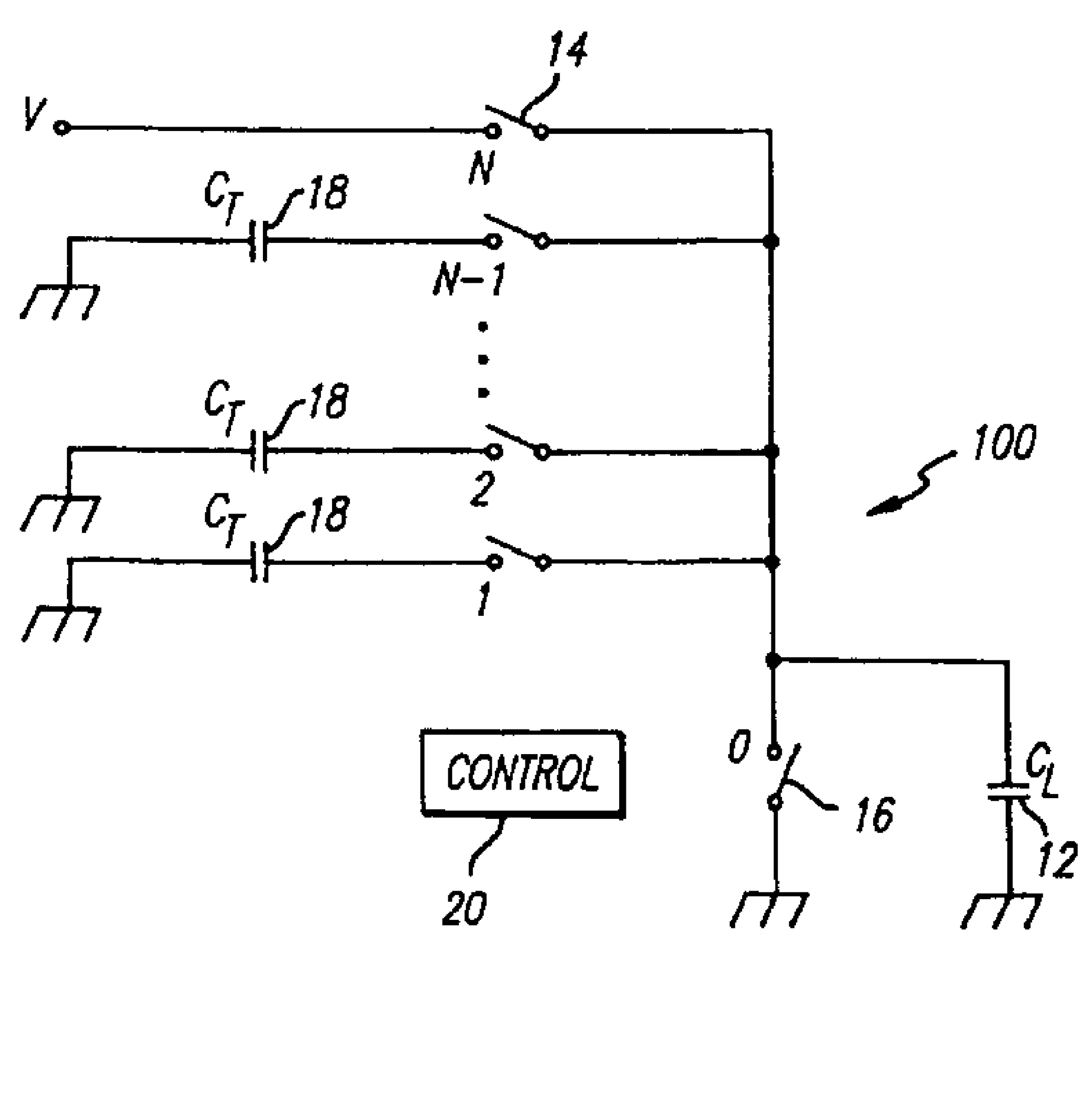

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FIG. 1 PRIOR ART

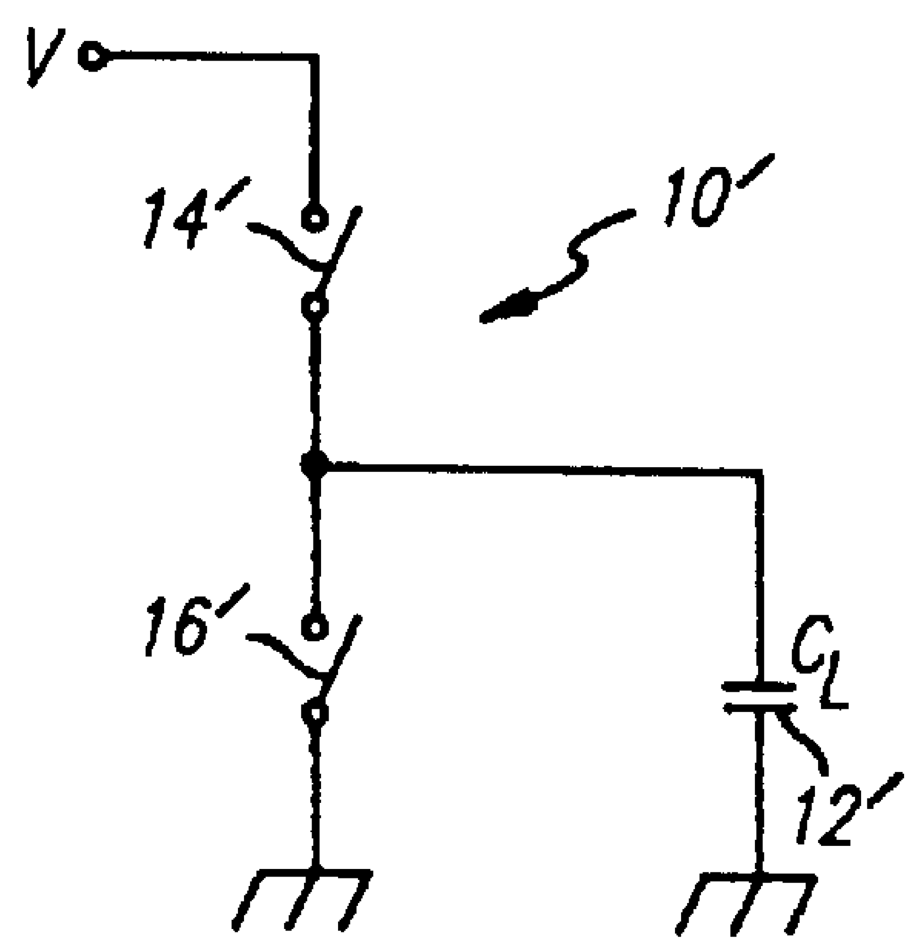



FIG. 2 PRIOR ART

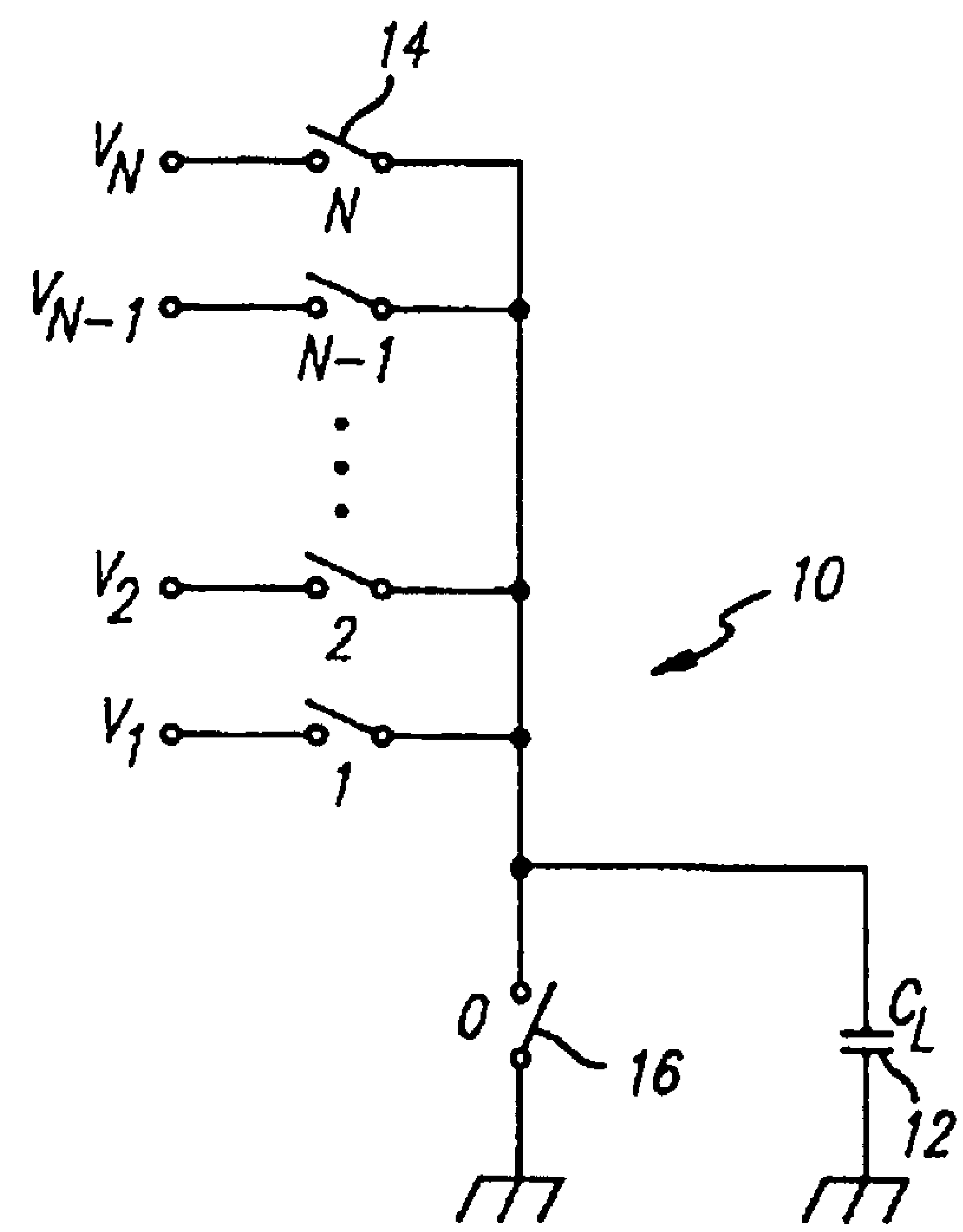
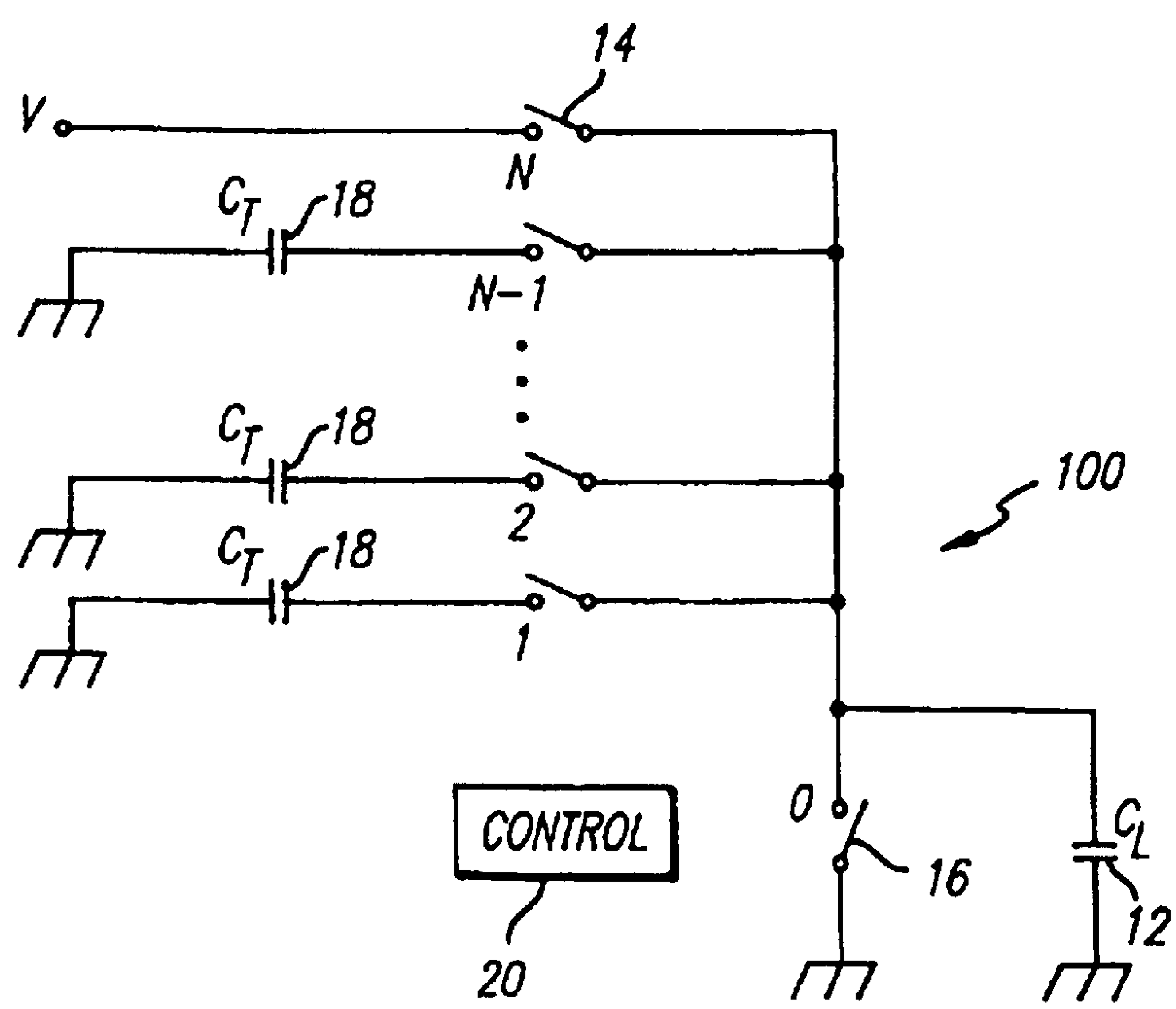



FIG. 3



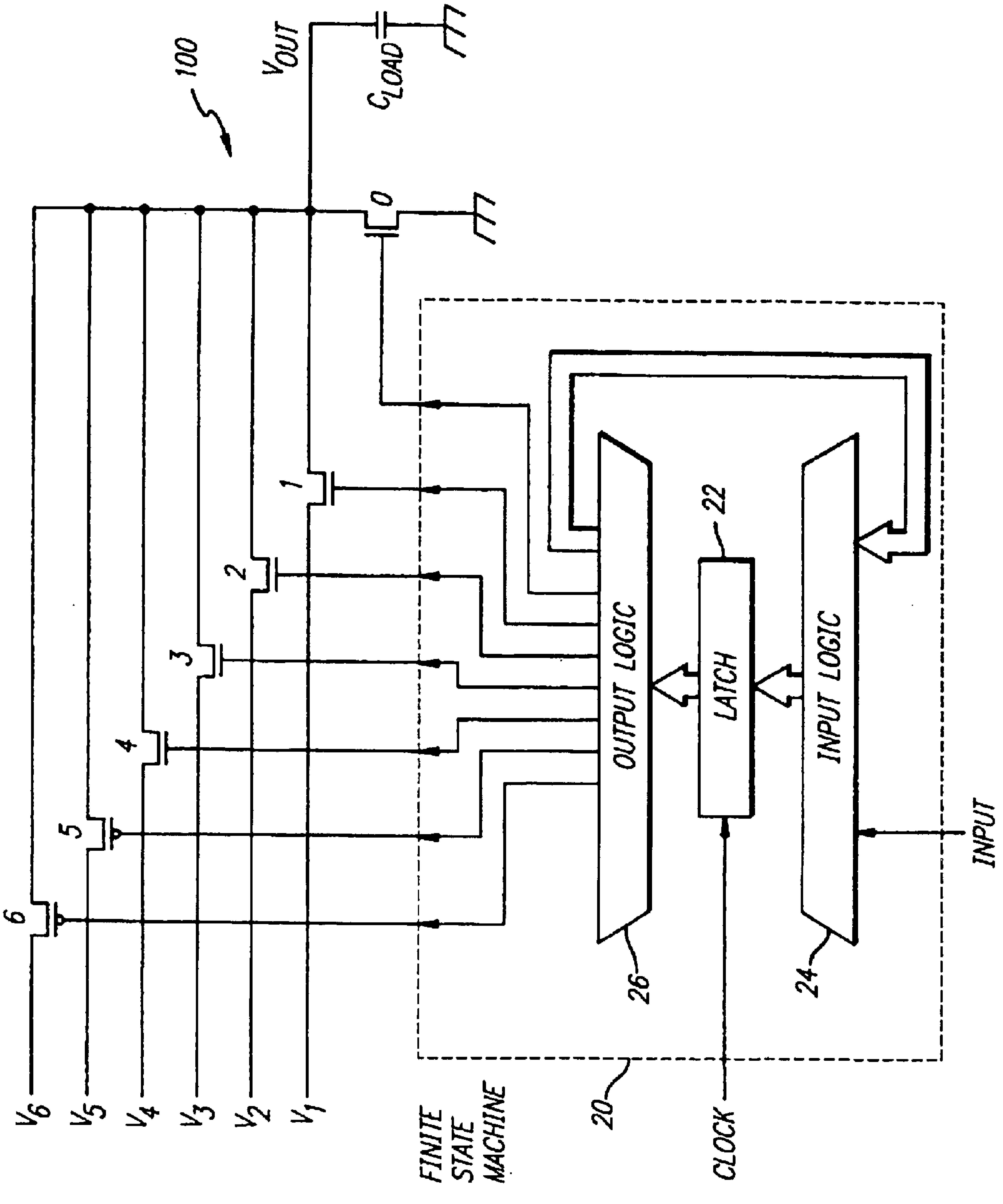

100
$V_{OUT}$
$C_{LOAD}$
0
1
2
3
4
5
6
$V_6$
$V_5$
$V_4$
$V_3$
$V_2$
$V_1$
FINITE STATE MACHINE
20
OUTPUT LOGIC
26
22
LATCH
INPUT LOGIC
24
INPUT
CLOCK

FIG. 4

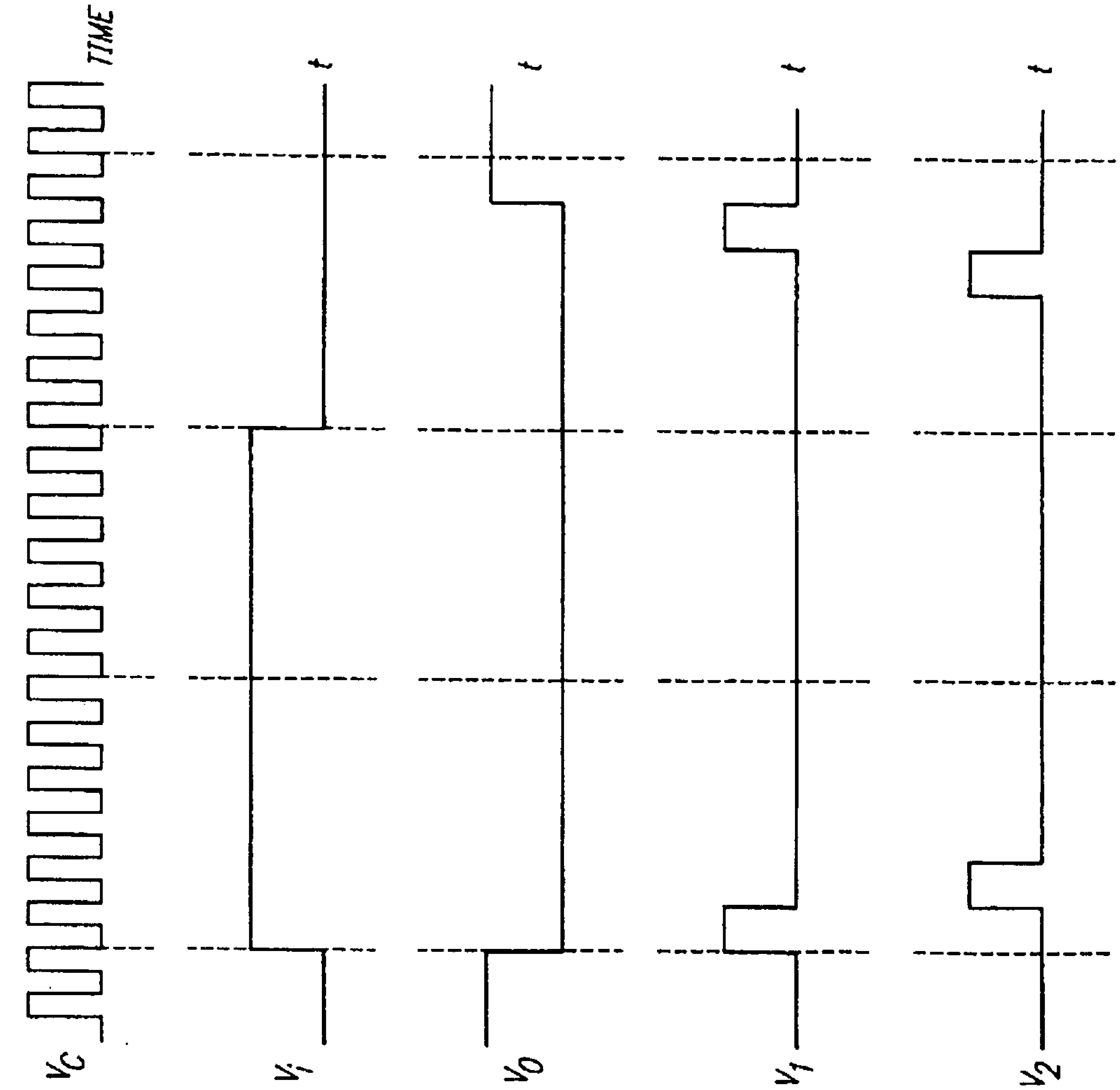



FIG. 5(a) CLOCK

FIG. 5(b) INPUT

FIG. 5(c) SWITCH #0 CONTROL

FIG. 5(d) SWITCH #1 CONTROL

FIG. 5(e) SWITCH #2 CONTROL

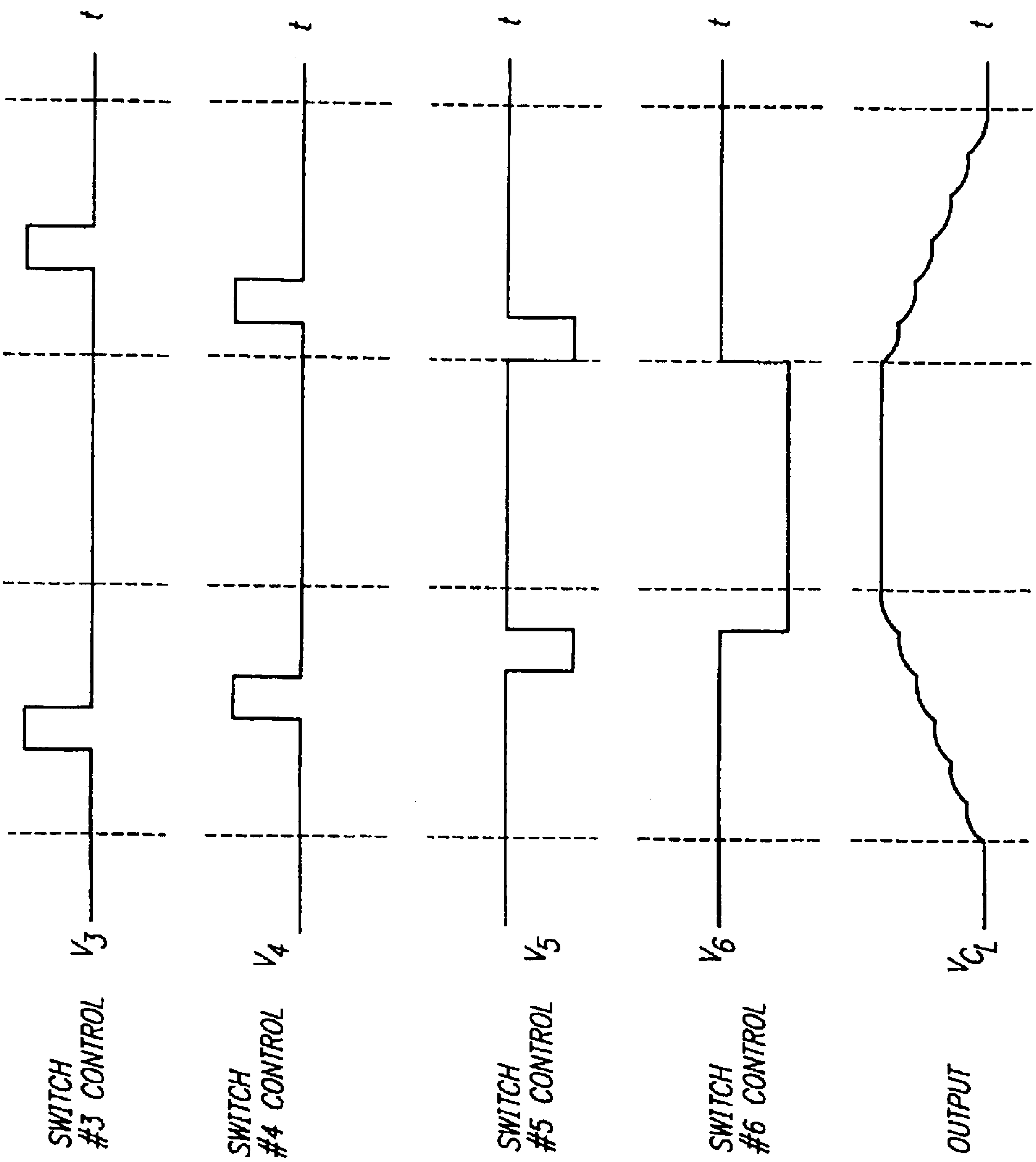



FIG. 5(f)

FIG. 5(g)

FIG. 5(h)

FIG. 5(i)

FIG. 5(j)

# SYSTEM AND METHOD FOR POWER-EFFICIENT CHARGING AND DISCHARGING OF A CAPACITIVE LOAD FROM A SINGLE SOURCE

**Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.**

## *CROSS-REFERENCE TO RELATED APPLICATIONS*

*This Reissue Application, Reissue application Ser. No. 08/986,327, and Reissue application Ser. No. 09/758,631 are all three reissue applications of U.S. Pat. No. 5,473,526, issued Dec. 5, 1995. This application is a continuation of Reissue application Ser. No. 09/758,631, filed Jan. 10, 2001 (now issued as U.S. Reissue Pat. No. RE 38,918, issued Dec. 13, 2005), entitled "System And Method For Power-Efficient Charging And Discharging Of A Capacitive Load From A Single Source", which is a continuation of application Ser. No. 08/986,327, entitled "System And Method For Power-Efficient Charging And Discharging Of A Capacitive Load From A Single Source," filed Dec. 5, 1997 (now issued as U.S. Reissue Pat. No. RE 37,552, issued Feb. 19, 2002).*

## *GOVERNMENT'S INTEREST IN APPLICATION*

*This invention was made with government support under DABT-63-92-C-0052 awarded by ARPA. The government has certain rights in the invention.*

## BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to electronic circuits and systems. More specifically, the present invention relates to power dissipation in electronic circuits and systems.

2. Description of the Related Art

Power dissipation of electronic circuitry is an important design consideration for many applications. Power dissipation provides a measure of the efficiency of the system. The efficiency of the system impacts the design of the power supply for the system. That is, low efficiency leads to higher costs due to the waste of energy and the need for larger power supplies.

For battery powered systems, power dissipation limits battery life. This necessitates larger batteries which increases the cost and weight of the system while limiting the applicability thereof. As an example, consider coronary pacemakers where power dissipation is a critical concern due to the difficultly of accessing the battery for replacement and the cost and inconvenience associated with the use of larger batteries.

In addition, the dissipated energy is released in the form of heat. Accordingly, systems which exhibit considerable power dissipation often require measures such as heat sinks to protect or cool system components from the heat created by the circuit. The use of heat sinks and the like adds to the cost, size and weight of the system and thereby limits the utility of same.

For the CMOS (complementary-metal-oxide semiconductor) based system, used widely in the design of computers, digital logic circuits and the like, capacitive effects are primarily responsible for the dissipation of power. Such capacitive effects arise due to junction capacitances within semiconductor devices, interlead capacitances



between lines connecting the circuit to external devices and the capacitance of a load.

In accordance with conventional teachings, power dissipation is directly related to the operating frequency (f), the capacitance (C) and the square of the voltage ($V^2$) applied to the capacitive element.

In addition to the elimination of unnecessary capacitances and the reduction of the switching frequency to the lowest value that supports the functional specification of the circuit, most prior approaches to the problem have focused on reducing the voltage applied to the capacitive elements. However, in addition to costly interfacing issues, attempts to lower the voltage of digital processors and the like have been limited by the fact that the trend is to higher processing speeds which cannot be attained at arbitrarily low operating voltages.

Thus, there is an ongoing need in the art for a system and technique for minimizing the power dissipated by a digital system.

## SUMMARY OF THE INVENTION

The need in the art is addressed by the present invention which, in a most general sense, provides a system and method for efficiently charging and discharging a capacitive load from a single voltage source. The inventive system includes a first switch for selectively connecting the voltage source to the load and a second switch for selectively providing a short across the load as may be common in the art. A particularly novel aspect of the invention resides in the provision of plural capacitive elements and a switching mechanism for selectively connecting each of the capacitive elements to the load whereby the load is gradually charged or discharged.

In the illustrative embodiment, the switching mechanism includes a set of switches for selectively connecting each of the capacitive elements to the capacitive load and a switch control mechanism for selectively activating the switches.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a simplified representation of a conventional driver for a capacitive load.

FIG. **2** shows a system for charging the load capacitance by several steps and thereby reducing power dissipation.

FIG. **3** is a simplified schematic of a preferred embodiment of the circuit of the present invention for reducing the power dissipation of a capacitive load.

FIG. **4** is a diagram showing the control circuit of the driver constructed in accordance with the teachings of the present invention.

FIG. **5** is a timing diagram which illustrates the operation of the driver of the present invention.

## DESCRIPTION OF THE INVENTION

Illustrative embodiments and exemplary applications will now be described with reference to the accompanying drawings to disclose the advantageous teachings of the present invention.

While the present invention is described herein with reference to illustrative embodiments for particular applications, it should be understood that the invention is not limited thereto. Those having ordinary skill in the art and access to the teachings provided herein will recognize additional modifications, applications, and embodiments within the scope thereof.

Most of the power dissipation in digital CMOS circuits is due to repeated charging and discharging of capacitive loads including those internal to the circuit and those associated with the output signals.

FIG. **1** is a simplified representation of a conventional driver for a capacitive load. The load $C_L$ represents the capacitance of a load and the interlead capacitance of the lines connecting the driver **10'** to the load **12'**. The load **12'** is charged to the supply voltage V by connecting the load **12'** to the power rail via a first switch **14'**. In practice, the switch **14'** may be a metal-oxide semiconductor field-effect transistor (MOSFET) which has a nominal "on" resistance. When the switch **14'** is closed, a charge CV passes through the resistance of the switch **14'**. The voltage drop across the resistance varies from an initial value of V to a final value of zero, so the average voltage drop V traversed by the charge is V/2, if the capacitance is linear. The energy dissipated is:

$$E_{conv}=QV'=CV\ (V/2)=CV^2/2 \quad [1]$$

A similar argument applies to the discharge process, so a complete conventional charge-discharge cycle dissipates all the energy provided by the power supply, $QV=CV^2$.

In accordance with the present teachings, power dissipation is reduced by charging the capacitance of the load $C_L$ in several steps. This is illustrated in FIG. **2**.

FIG. **2** shows a system **10** for charging the load capacitance by several steps and thereby reducing power dissipation. Here, a bank of supply voltages $V_1$ to $V_N$ are used to charge the load **12**. The voltages of the supplies are evenly distributed between ground and $V_N$ so that the voltage difference between any two adjacent supplies is the same. Each of the voltages is selectively applied to the load **12** by N switches including the first switch **14** and N−1 additional switches. Between charge cycles, switch **0** is closed. To charge the load, switch **0** is opened and the supplies $V_1$ through $V_N$ are connected to the load in succession by selectively closing the switches, that is, by momentarily closing switch **1**, opening switch **1**, momentarily closing switch **2** etc. To discharge the load, the supplies $V_{N-1}$ through $V_1$ are switched in in reverse order. Then switch **0** is closed connecting the output to ground.

If N steps are used, the dissipation per step is again given by the transferred charge and the average voltage drop across the switch resistance:

$$E_{step}=QV'=(CV/N)\ (V/2N)=CV2/2N^2 \quad [2]$$

To charge the capacitance all the way to the supply voltage V, N steps are used, so the total energy dissipation is:

$$\begin{aligned} E_{stepwise} &= N{*}E_{step} \quad [3] \\ &= N{*}CV^2/2N^2 \\ &= CV^2/2N \\ &= E_{conv}/N \end{aligned}$$

Again, a full charge-discharge cycle will cause twice the dissipation of the charging only. Thus, according to this simplified analysis, charging by several steps reduces the energy dissipation per charge-discharge cycle and thereby the total power dissipation, by a factor of N.

The multiple supply voltages of FIG. **2** may be generated with a battery stack. For equipment not powered by batteries or when the desired voltage increment is not a multiple of the battery cell voltage, a power supply unit would seemingly have to generate these multiple supply voltages with an associated cost in expense, complexity and power dissipation.

FIG. **3** is a simplified schematic of a preferred embodiment of the circuit of the present invention for reducing the power dissipation of a capacitive load. The circuit **100** is essentially identical to that of FIG. **2** with the exception that the supplies $V_1$−$V_{N-1}$ are replaced with a corresponding number of capacitors $C_T$ **18** which will be referred to as "tank" capacitors. Each tank capacitor $C_T$ has a capacitance which is much, much larger (e.g. an order of magnitude) than the load capacitance $C_L$. Switch operations are sequenced by a control circuit **20**.

FIG. **4** is a diagram showing the control circuit **20** interconnected to plural MOSFET switches for an N=6 implementation of the driver constructed in accordance with the teachings of the present invention. In FIG. **4**, the tank capacitors **18** are eliminated for simplicity. The control signals may be provided by the circuit **20** or may be supplied by a host microprocessor. The control circuit **20** may be implemented in several configurations. For example, the control circuit may be implemented with a microprocessor or with a shift register and a counter. In the alternative, a latch **22** and input and output logic circuits **24** and **26**, respectively, may be used as shown in FIG. **4**. The input and output logic circuits may be designed by a computer aided logic design program of which several are currently available. If a computer aided logic design program is used, the desired outputs would be specified in response to the expected input signals. The program would then design the logic circuits.

Timing signals are provided by a system clock (not shown) through the latch **22**. In practice, the clock rate should be at least (N+1) times the output signal rate. In the preferred embodiment, switches **0**–**4** are implemented with n-channel MOSFET devices. Switches **5** and **6** are implemented with p-channel devices.

FIG. **5** is a timing diagram which illustrates the operation of the driver **100** of the present invention. In FIG. **5**(a), the clock pulses are shown. The input signal is shown in FIG. **5**(b). FIGS. **5**(c)–(i) show the controls for switch **0**–**6** and FIG. **5**(j) shows the output at the load $C_L$.

The operation of the circuits of FIGS. **3** and **4** is essentially the same as that of FIG. **2**. That is, in the initial standby condition switch **0** is closed and there is no charge on any of the capacitors in the system. Next, when an input pulse is to be transferred to the load, switch **0** is opened and switch **1** is closed. Since there is no charge on the load, $C_L$ nor on any of the tank capacitors $C_T$, there will be no charge transfer through any of the switches as each is closed, in turn, momentarily. When the first switch **14** is closed, a charge is applied to the load **12**.

On the trailing edge of input pulse, a discharge cycle is initiated by when the switches are momentarily closed in reverse order. Thus, switch N is opened and switch N−1 is closed. Then switch N−1 is opened and switch N−2 is closed and etc. On the closure of switch N−1, the associated tank capacitor will receive most of the charge on the load capacitance. Each capacitor down the line will receive a lower charge than the immediately proceeding capacitor. After switch **1** opens, switch **0** closes to complete the cycle dumping the remaining charge on the load $C_L$ to ground. Thus, over several cycles the tank capacitors will approach their steady state voltages, for example, the (N−1) th through 1st tank capacitors may have charges of say 5, 4, 3, 2 and 1 volts respectively. Then, at the beginning of the next cycle, on the closure of the first switch, the voltage on the first tank capacitor is applied to the load, then the voltage on the second capacitor is applied to the load and so on. Thus, in the example, first 1 volt is applied to the load, then 2 volts, then three volts and etc. As a result, the voltage on the load will gradually increase as shown in FIG. **5**(j).

The circuits of FIG. **3** and **4** will provide the same power dissipation reduction as that of FIG. **2**, but without multiply supply lines and without complicating the power supply. This is illustrated by the following analysis. Assume that each tank capacitor $C_T$ is charged to the voltage of the corresponding supply of FIG. **2**, and that the load capacitance $C_L$ is discharged. The load capacitance is charged by closing and opening switches **1** through N in succession. Each tank capacitor (and the power supply) delivers a charge given by:

$$q=C_L V/N \qquad [4]$$

Since the tank capacitors are much larger than the load, the tank voltages do not change significantly, so the dissipation in the switches will be the same as for the case in FIG. **2**, where the supply voltages are constant. To discharge the load capacitance, switches N−1 through **0** are closed and opened in succession. During the discharge, each tank capacitor receives a charge of the same size as that delivered during charge phase, and an equally sized charge is dumped to ground via switch **0**. Over the full charge-discharge cycle, only the power supply injects any charge into the circuit. No net charge is drawn from any tank capacitor, so the tank voltages do not change.

The voltages of the tank capacitor bank are self-stabilizing. To appreciate this, assume that the voltage of one of the tank capacitors is slightly higher than it should be. Then, the charge delivered by this tank capacitor during the charging of the load will be somewhat larger than that given by equation [4], since the "step" from the voltage below is now slightly larger. During the discharge phase, the step from the voltage above is slightly smaller and the charge received is therefore smaller as well. Therefore, over the full cycle, a net decrease of the charge on the storage capacitor occurs, which causes a decrease in the capacitor voltage. The initial deviance is automatically counteracted.

Even if the tank capacitor voltages differ from the "correct" values, the circuit will work logically correctly, since each charging (discharging) cycle ends by connecting the load to he supply rail (ground). Voltage deviations simply bring higher dissipation. This happens during start-up, before the tank voltages have had time to converge to the even distribution between the supply voltage and ground.

The implementation cost of a driver such as that shown in FIG. **3** is determined by the tank capacitors, the switches, the mechanism controlling the switches, and the interconnections of same. Note that all extra interconnections are local. As for the conventional case, only one connection to the power supply is needed. Also, several drivers may share the same capacitor bank and part of the control mechanism.

The problem of maintaining the appropriate voltages on the tank capacitors is obviated by the fact that the capacitor voltages will converge automatically to the desired voltages. No additional circuitry is required. Only one supply line must be routed to the chip and the power supply need not be any more complicated than a conventional supply. In practice, the tank capacitors would be located off-chip.

For a CMOS implementation, the following design procedure may be followed to provide a driver configuration which exhibits minimal power dissipation.

Equation [3] indicates that dissipation decreases monotonically with increasing N. The number N cannot, however, be usefully made arbitrarily large because each step requires that a switch be turned on and off, which itself causes dissipation. Also, the energy used to drive each switch depends on the width of the device, which should be just enough to allow the charging to complete before the next step commences. Thus, for a given total allowable charging time 'T', there is an optimal number of steps and a set of optimal device sizes which lead to minimal total dissipation determined as follows.



Again, consider the circuit in FIG. **3** and assume the gates of the switch devices are driven conventionally. The load is charged and discharged once; the energy needed to drive the gates of the switch devices is:

$$E_{sw} = \left(\sum_{i=1}^{N} C_i + \sum_{i=0}^{N-1} C_i\right)V^2 \qquad [5]$$

Allot each step one Nth of the total charging time T. Then:

$$T/N=mR_i C_L \qquad [6]$$

Here, m is the number of RC time constants spent waiting for each charging step to complete. From equation [6], it is evident that all the switch devices should have equal on-resistance: $R_i=R_{sw}$. Decreasing the on-resistance of device i by increasing the width means increasing the gate capacitance:

$$R_i C_i=\rho_i \qquad [7]$$

$\rho_i$ is a quality measure of the switch. It varies with i, since the bulk-to-channel and gate-to-channel voltages are different for different switches. Combining equations [5], [6], and [7] yields:

$$E_{sw} = \frac{Nm}{T}\left(\sum_{i=1}^{N} \rho_i + \sum_{i=0}^{N-1} \rho_i\right)C_L V^2 \qquad [8]$$

Introducing $\overline{\rho}$, a weighted average of $\rho_i$ for the different switches:

$$\overline{\rho} = \frac{1}{2N}\left(\sum_{i=1}^{N} \rho_i + \sum_{i=0}^{N-1} \rho_i\right) \qquad [9]$$

If N is sufficiently large, $\overline{\rho}$ is close to the unweighed average of ρ over the entire voltage range. Combining equations [3], [8] and [9] yields the following expression for the total energy dissipation:

$$E_{tot} = \left(\frac{1}{N} + 2N^2 m\frac{\overline{\rho}}{T}\right)C_L V^2 \qquad [10]$$

The number N that minimizes $E_{tot}$ is given by:

$$N_{opt} = \sqrt[3]{\frac{T}{4m\overline{\rho}}} \qquad [11]$$

The corresponding energy dissipation is:

$$E_{opt} = \frac{3}{2}\sqrt[3]{\frac{4m\bar{\rho}}{T}}\,C_L V^2 \quad [12]$$

It remains to select the value for m. If it is chosen too small, there will still be a significant voltage across a switch when the next switch is to close. Hence, there is an increase in the average voltage across each switch and therefore a dissipation increase (the first term in equation [10] is changed slightly). If on the other hand, m is chosen unnecessarily large, time is wasted that could have been used to increase the number of steps. Thus, in general, optimization methods for the value of m vary according to the application, however, one skilled in the art will be able to select a suitable value for m using conventional teachings (e.g., a simulation program).

By using the number of stages given by equation [10], the designer can minimize the power dissipation of the driver. The minimum is rather shallow, however, so a lower N (as would most often be dictated by practical considerations) will still give a considerable improvement over the conventional case; N=2 already gives almost 50% reduction. Once N and m have been selected, the on-resistance of each switch is given by equation [6]. The corresponding gate capacitance, and thereby the width of the device, is given by equation [7]. The values of $\rho$ for a certain process can be found by circuit simulation or by measuring the on-resistances of test devices of known widths.

Thus, the present invention has been described herein with reference to a particular embodiment for a particular application. Those having ordinary skill in the art and access to the present teachings will recognize additional modifications applications and embodiments within the scope thereof. For example, the switches may be closed in some other sequence as may be appropriate for a given application without departing from the scope of the present invention. In addition, alternative circuit topologies for the network of tank capacitors and switches may be appropriate. The second terminal of the load may be connected to a potentially variable) voltage other than ground.

It is therefore intended by the appended claims to cover any and all such applications, modifications and embodiments within the scope of the present invention.

Accordingly,

What is claimed is:

[**1**. A system for efficiently charging and discharging a capacitive load from a single voltage source of a first potential consisting of:

a first switch for selectively charging the load;

a second switch for selectively discharging the load;

plural capacitive elements; and

switch means for selectively connecting each of the capacitive elements to the capacitive load to gradually charge or discharge the capacitive load.]

[**2**. The invention of claim **1** wherein said switch means includes plural third switches connected between said capacitive elements and said load.]

[**3**. The invention of claim **2** wherein said switch means includes means for selectively activating the first, second and third switches.]

[**4**. The invention of claim **3** wherein the capacitive load has a first terminal connected to the first switch and a second terminal connected to a source of a second potential.]

[**5**. The invention of claim **4** wherein the second switch has a first terminal connected to the first terminal of the load and a second terminal connected to said source of a second potential.]

[**6**. The invention of claim **5** wherein each of the third switches has a first terminal connected to the first terminal of the load and a second terminal connected to a first terminal of an associated one of the plural capacitive elements.]

[**7**. The invention of claim **6** wherein the means for selectively activating the first, second and third switches includes a finite state machine.]

[**8**. The invention of claim **7** wherein the finite state machine is designed to receive a clock signal and an input signal and provide selective activation signals for the first, second and third switches in response thereto.]

[**9**. The invention of claim **8** wherein a second terminal, of each of the plural capacitive elements is connected to said source of a second potential.]

[**10**. The invention of claim **9** wherein each of the capacitive elements has a capacitance which is at least an order of magnitude greater than the capacitance of the load.]

[**11**. A method for efficiently charging and discharging a capacitive load from a single voltage source including the steps of:

providing a first switch for selectively connecting the voltage source to the load;

providing a second switch for selectively providing a short across the load;

providing plural capacitive elements;

providing plural third switches for selectively connecting each of the capacitive elements to the capacitive load; and

selectively activating the first, second and third switches to gradually charge or discharge the capacitive load.]

*12. A method for driving a capacitive load, comprising:*

*minimizing power dissipation by discharging the capacitive load by incremental voltage steps using a switching system which includes a switch for selectively discharging the load; and*

*electrically coupling a capacitive storage system to the capacitive load at an electrically floating node for discharging the capacitive load by one of the incremental voltage steps.*

*13. The method of claim 12, further comprising: charging and discharging the capacitive load between an upper voltage and a lower voltage by the incremental voltage steps.*

*14. The method of claim 13, wherein one of the incremental voltage steps is the difference of the upper and lower voltages divided by an integer N.*

*15. A system for driving a capacitive load, comprising:*

*means for minimizing power dissipation by discharging the capacitive load by incremental voltage steps using a switching system which includes a switch for selectively discharging the load; and means for electrically coupling a capacitive storage system to the capacitive load at an electrically floating node for discharging the capacitive load by one of the incremental voltage steps.*

*16. The system of claim 15, wherein the load capacitor is charged and discharged between an upper voltage and a lower voltage by the incremental voltage steps.*

*17. The system of claim 16, wherein one of the incremental voltage steps is the difference of the upper and lower voltages divided by an integer N.*

*18. A method for driving a load, the method comprising:*

*charging the load to a first level;*

*discharging the load to a second level using a switching system which includes a switch for selectively discharging the load, wherein during discharging to the second level, a first capacitor is charged to the second level by using the discharging charge of the load;*

*discharging the load to a third level using a switch; and*

*re-charging the load by using the charge of the first capacitor,*

*wherein the first level is higher from the second level and the second level is higher that the third level.*

*19. A method of claim 18, wherein during discharging the load to the third level, a second capacitor is charged to the third level by using the discharging charge of the load.*

*20. A system for charging and discharging a capacitive load in N steps, N being greater than 1, comprising:*

*N−1 capacitive devices; and*

*a first switching device operable to selectively couple and de-couple the N−1 capacitive devices to and from the capacitive load during a charging and a discharging of the capacitive load;*

*a switching system including a switch for selectively discharging the load,*

*whereby energy is recovered from the capacitive load and whereby the recovered energy is always stored substantially only in capacitance.*

*21. A system of claim 20, wherein the first switching device is operable to selectively couple and de-couple the N−1 capacitive devices to and from the capacitive load during both the charging and the discharging of the capacitive load.*

*22. The system of claim 21, wherein each of the N−1 capacitive devices includes a capacitor.*

*23. The system of claim 22, wherein a capacitance of the capacitor is greater than a capacitance of the capacitive load.*

*24. The system of claim 20, wherein the first switching device includes a MOSFET.*

*25. The system of claim 20, wherein the selective coupling and de-coupling of the N−1 capacitive devices to the capacitive load causes at least one of the charging and the discharging of the capacitive load to occur in the N steps.*

*26. The system of claim 20, further comprising:*

*a second switching device operable to selectively couple the capacitive load to a voltage source, and*

*a third switching device operable to selectively provide a short across the capacitive load.*

*27. A method for charging and discharging a capacitive load comprising:*

*selectively coupling and de-coupling a capacitive device to and from the capacitive load to cause the charging and the discharging of the capacitive load to occur in a plurality of steps using a switching system which includes a switch for selectively discharging the load,*

*whereby energy is recovered from the capacitive load and whereby the recovered energy is always stored substantially only in capacitance.*

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