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(54) **CMOS IMAGE SENSOR HAVING A CHOPPER-TYPE COMPARATOR TO PERFORM ANALOG CORRELATED DOUBLE SAMPLING**

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(Under 37 CFR 1.47)

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H01L 27/00 (2006.01)

(52) **U.S. Cl.** **250/208.1**; 250/214.1

(58) **Field of Classification Search** 250/208.1, 250/214.1; 348/241, 294, 300

See application file for complete search history.

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(57) **ABSTRACT**

A CMOS image sensor performing an analog correlated double sampling is disclosed. The CMOS image sensor may include an image capture device for capturing an image for analog image signal from an object an analog-to-digital converter for converting the analog image signal to a digital value using a ramp signal. In such an arrangement the analog-to-digital converter may includes a chopper-type comparator receiving the analog image signal and the ramp signal and a capacitor for receiving a start voltage of the ramp signal and charging a voltage level corresponding the start voltage of the ramp signal in a reset mode and for receiving a down-ramping signal of the ramp signal in a count mode in order to remove an device offset voltage. The analog-to-digital converter may also include a ramp signal generator providing the ramp signal to the analog-to-digital converter.

19 Claims, 9 Drawing Sheets

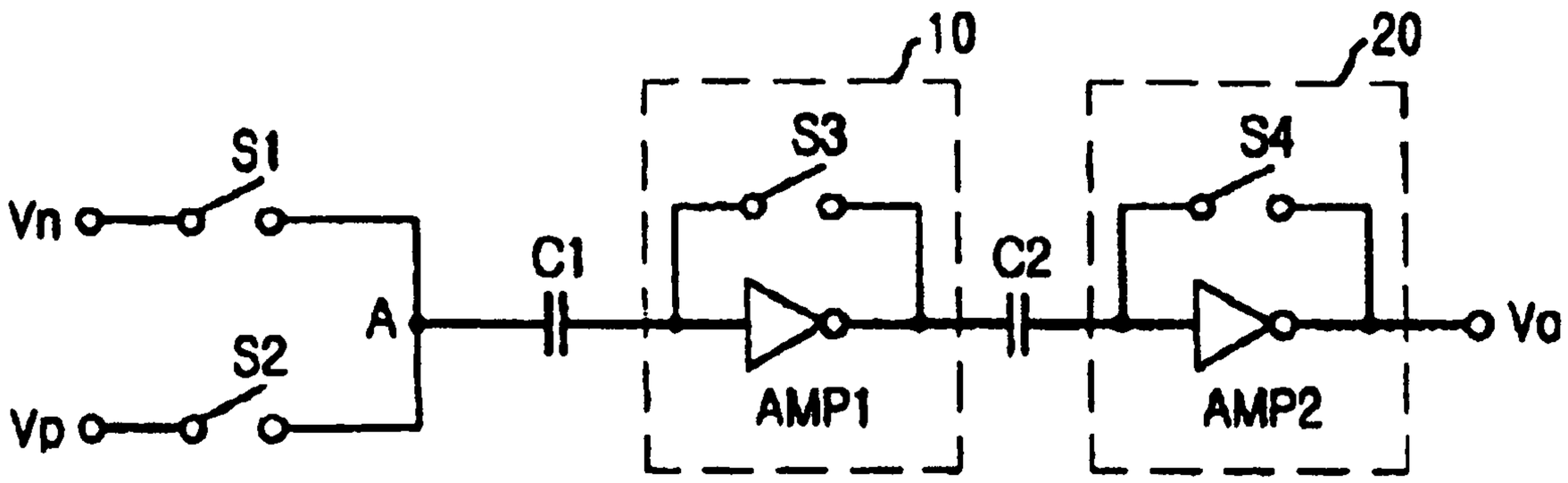


FIG. 1
(PRIOR ART)

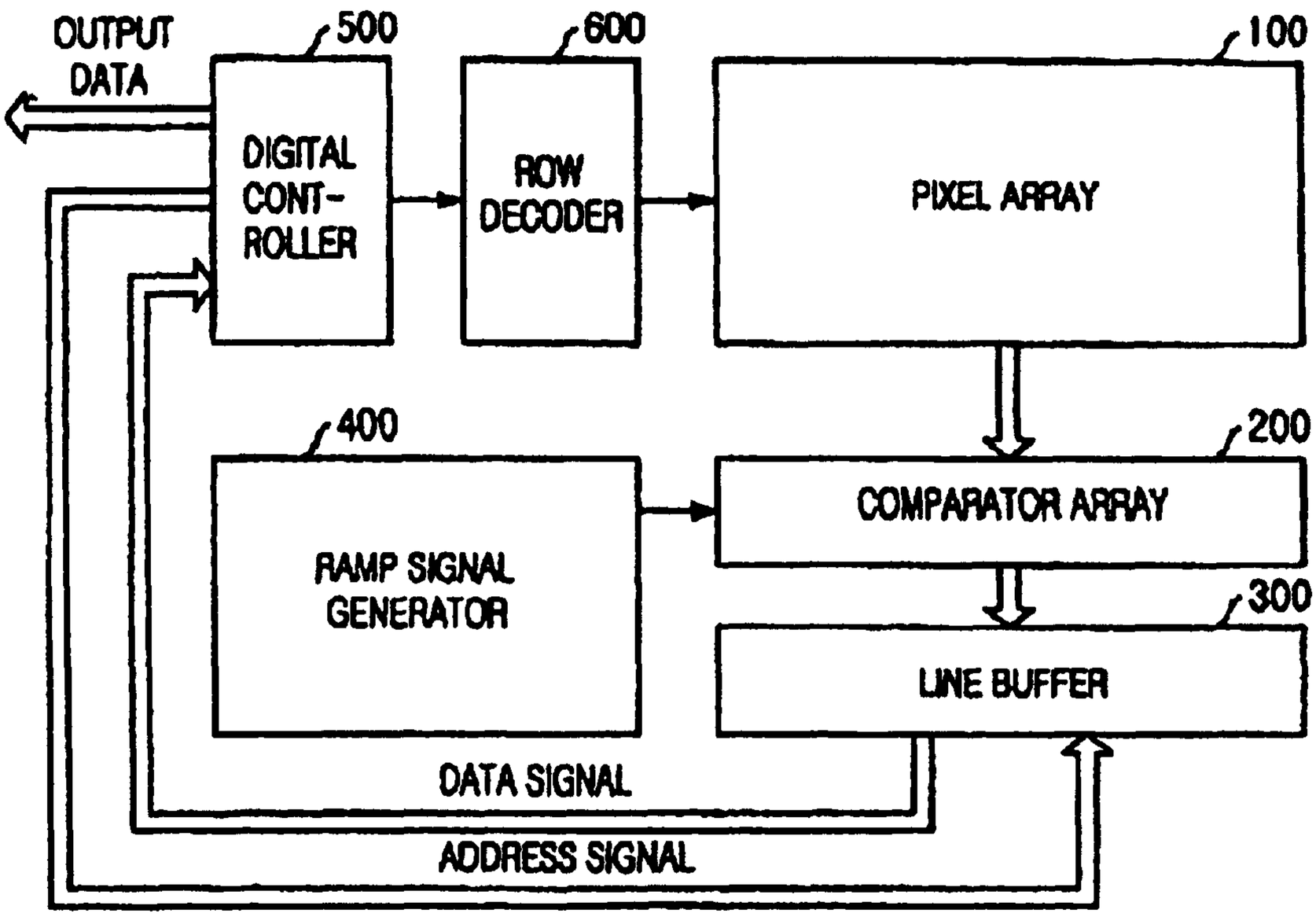


FIG. 2
(PRIOR ART)

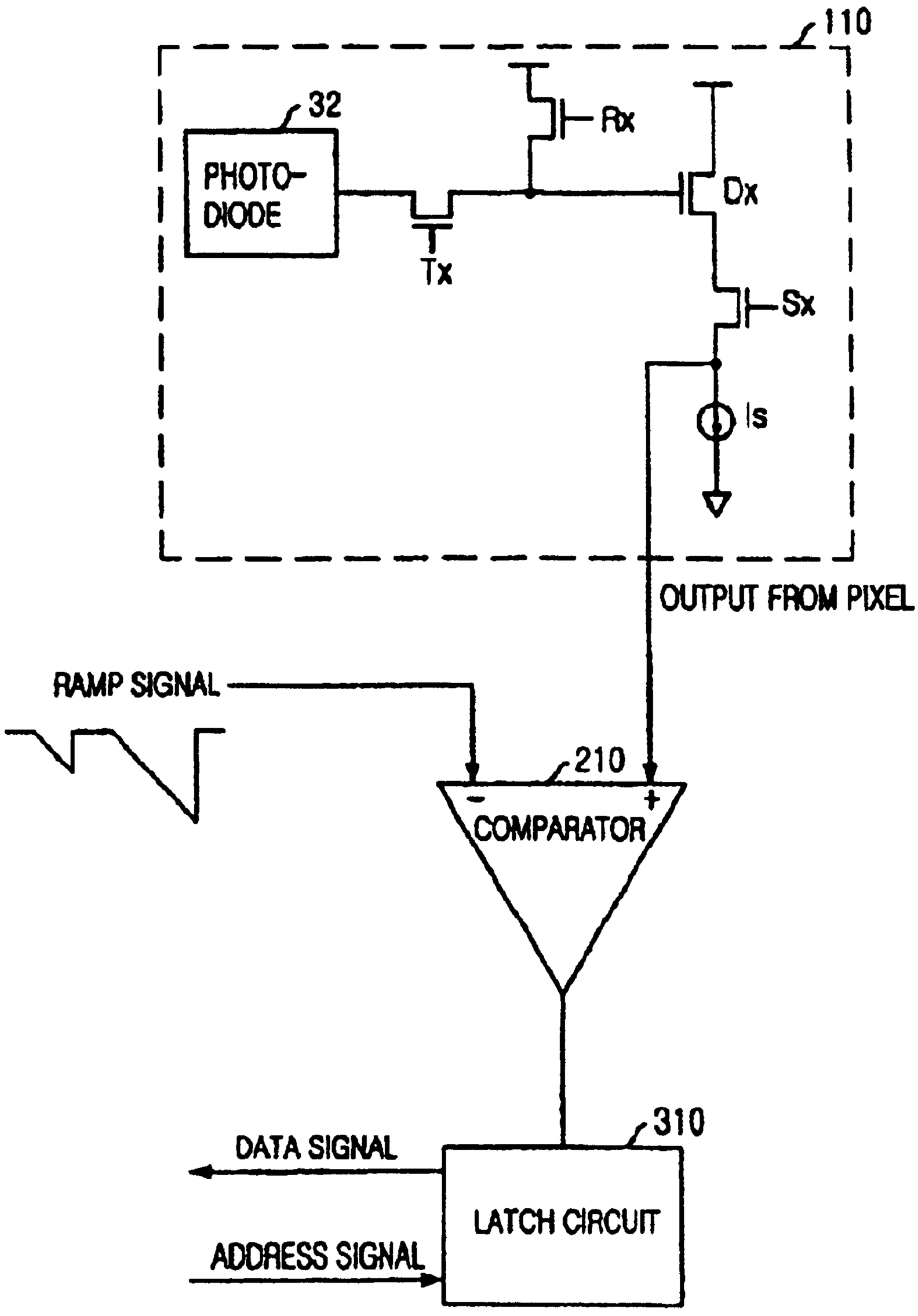


FIG. 3
(PRIOR ART)

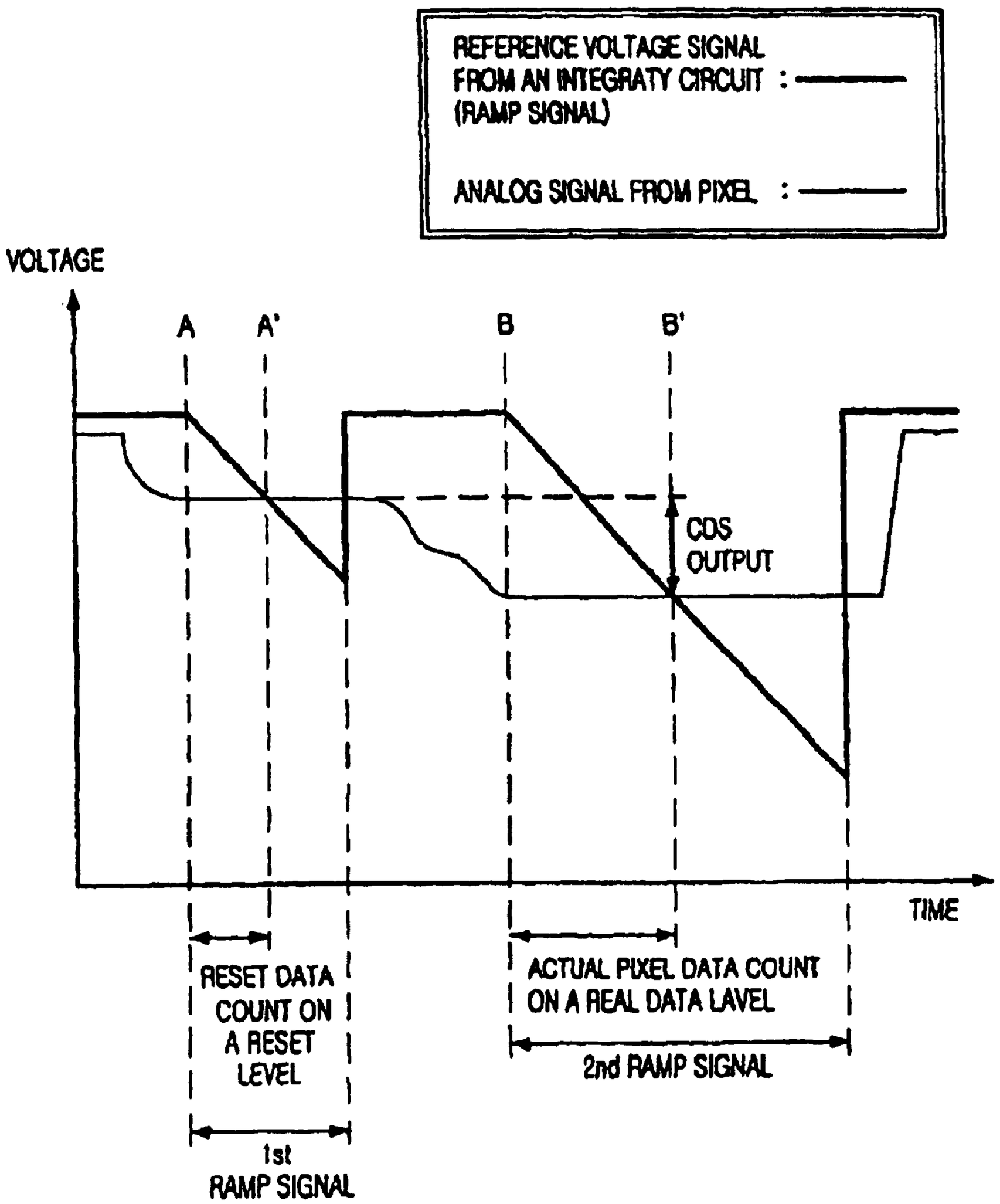


FIG. 4
(PRIOR ART)

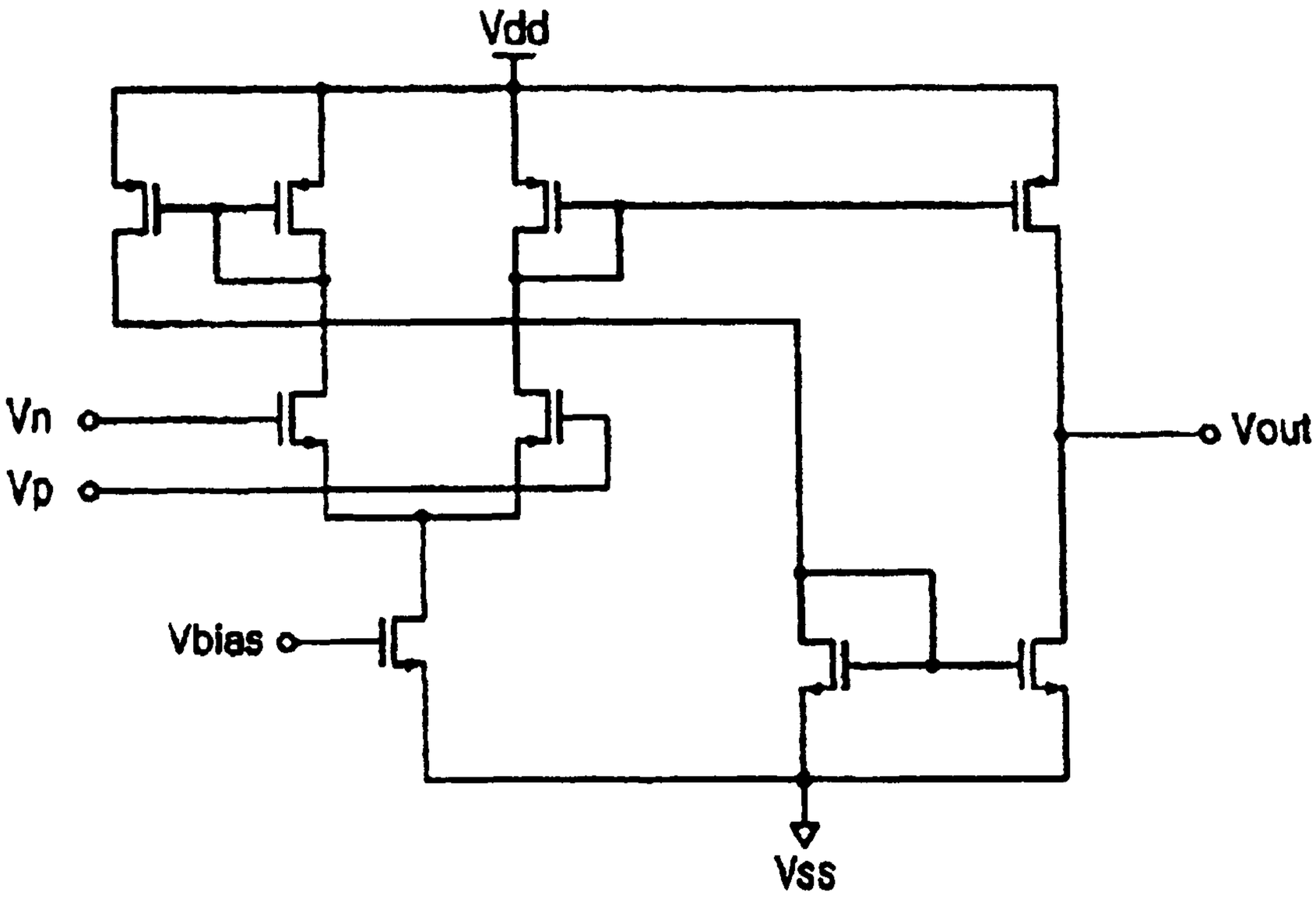


FIG. 5
(PRIOR ART)

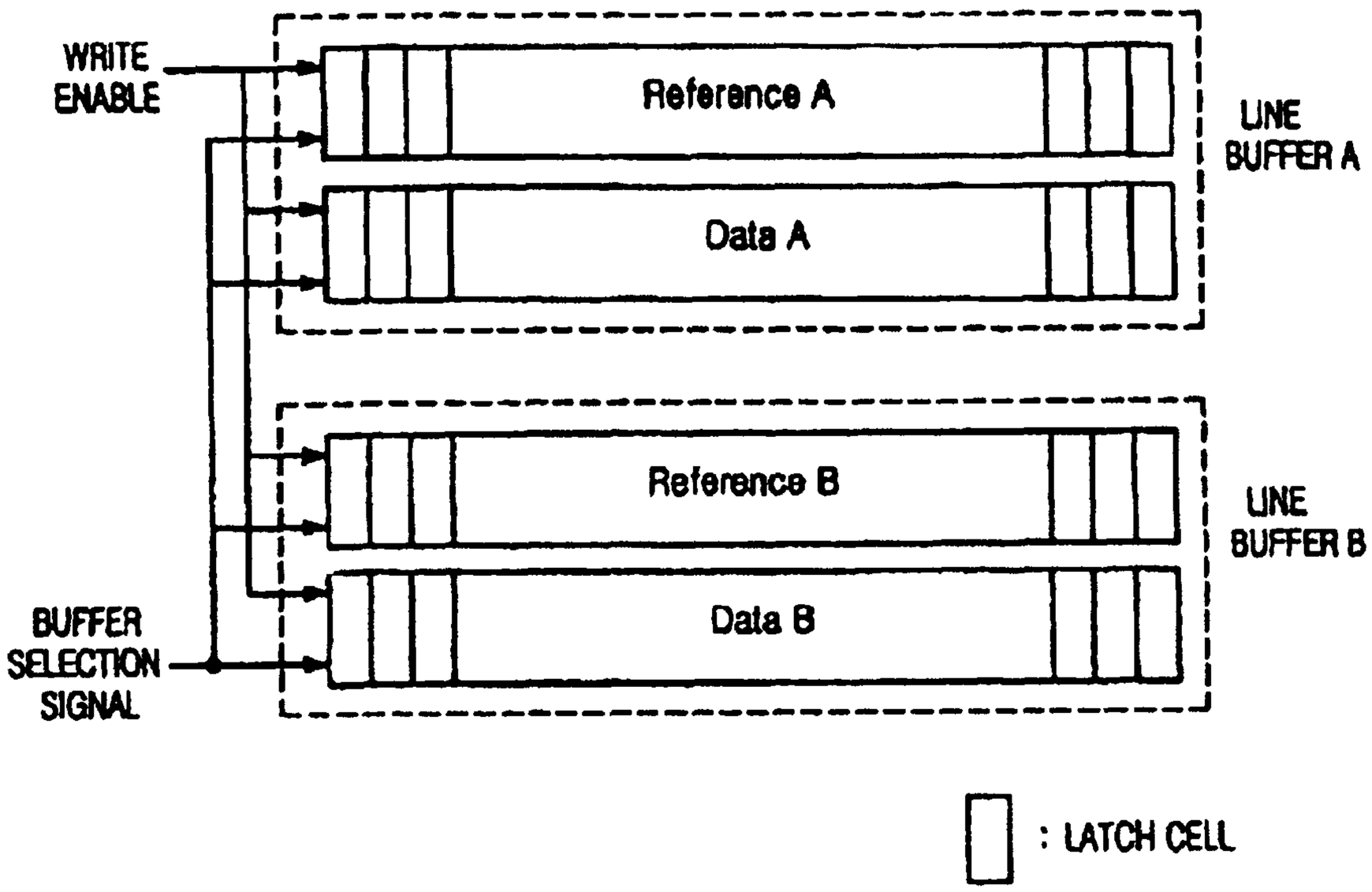


FIG. 6

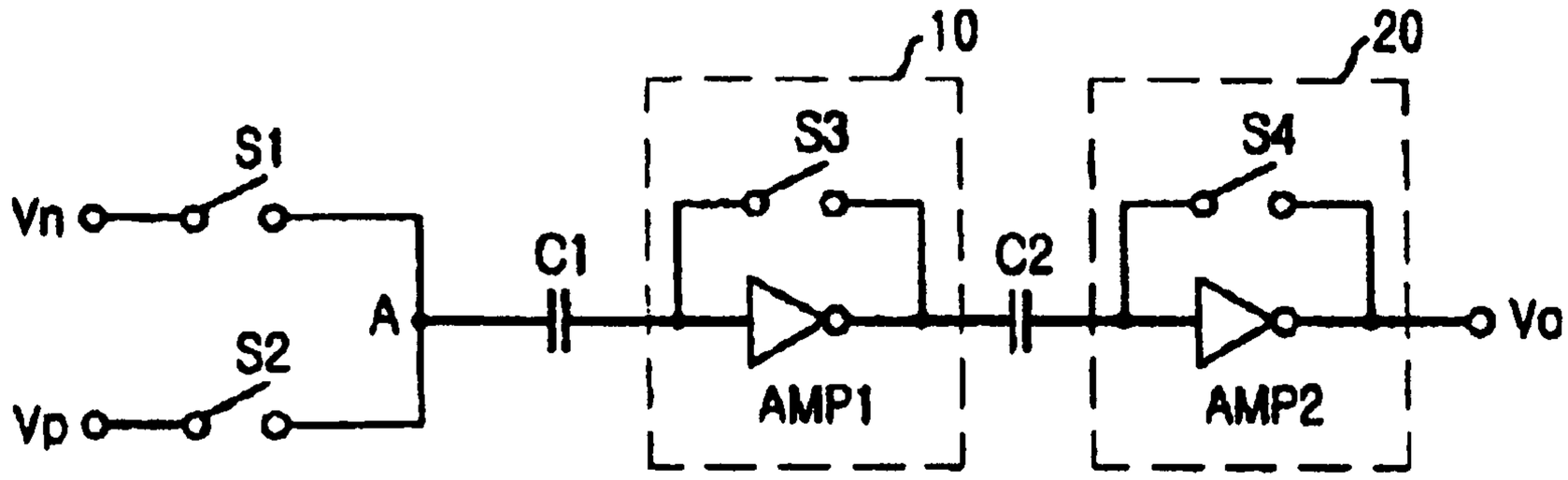


FIG. 7

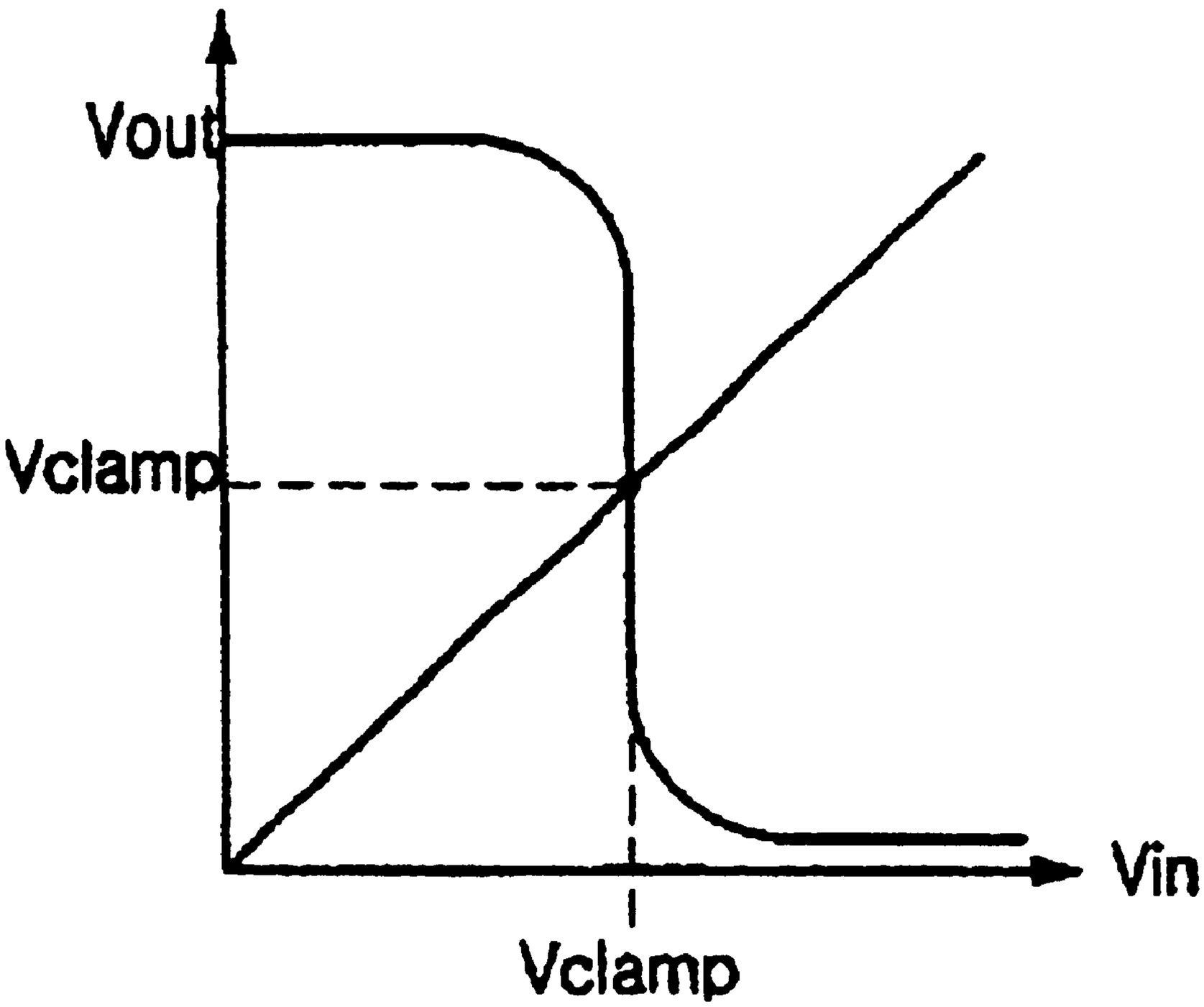
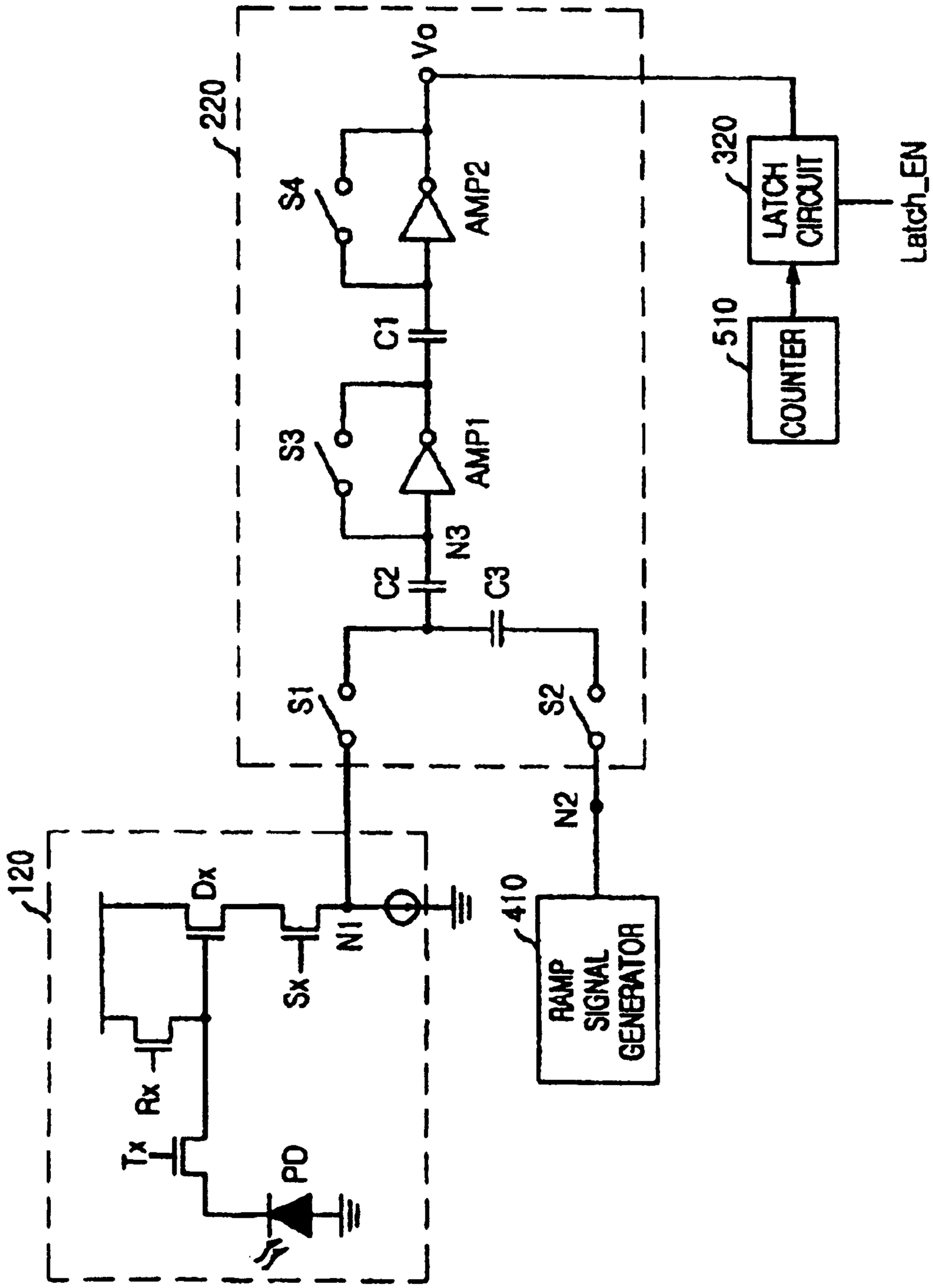


FIG. 8


220
Vo
S4
AMP2
C1
S3
AMP1
N3
C2
C3
S1
S2
N2
120
Dx
N1
Sx
Rx
Tx
PD
320
LATCH CIRCUIT
Latch_EN
510
COUNTER
410
RAMP SIGNAL GENERATOR

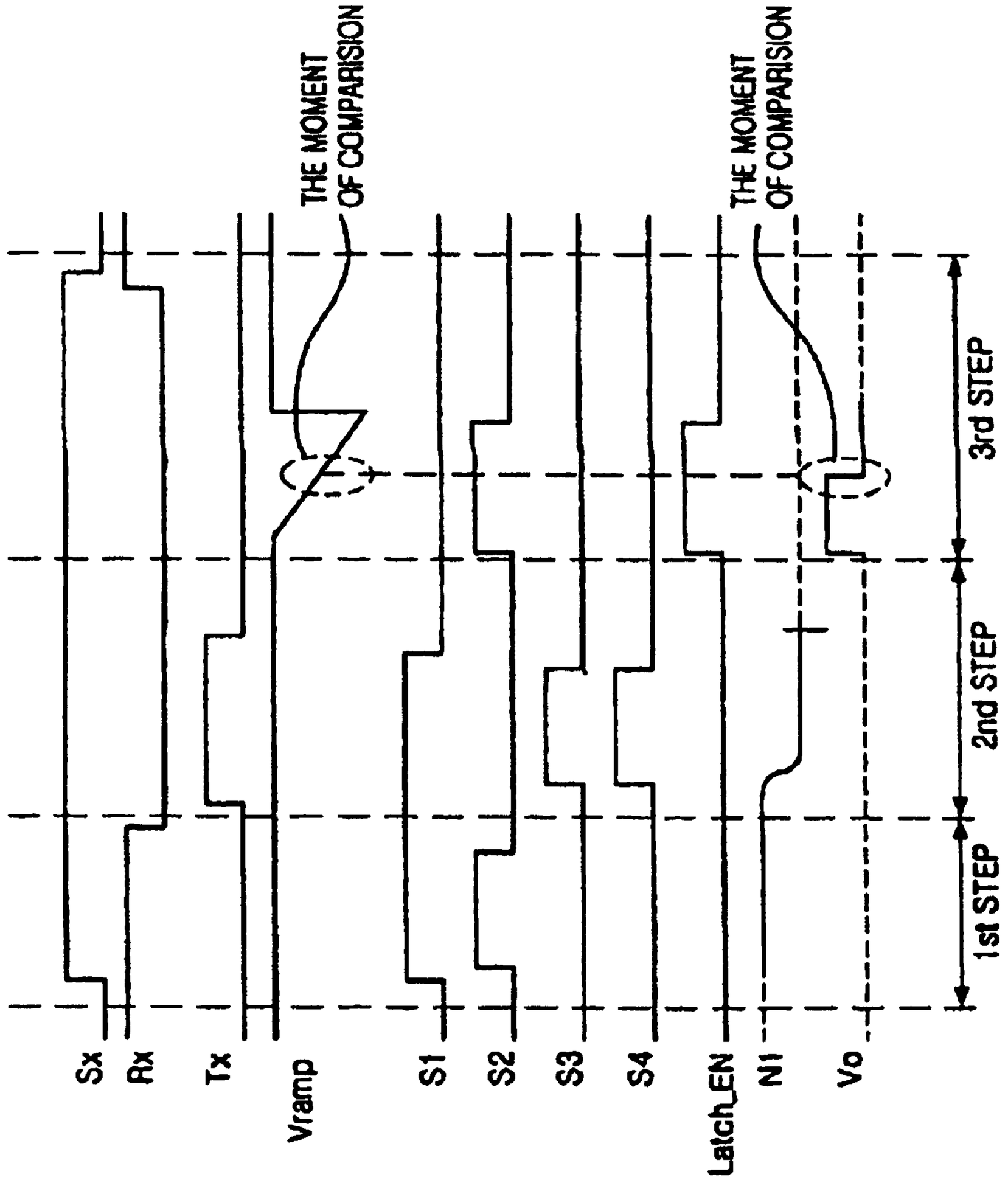

THE MOMENT OF COMPARISION
THE MOMENT OF COMPARISION
3rd STEP
2nd STEP
1st STEP
Sx
Rx
Tx
Vramp
S1
S2
S3
S4
LatchEN
N1
Vo

FIG. 9

CMOS IMAGE SENSOR HAVING A CHOPPER-TYPE COMPARATOR TO PERFORM ANALOG CORRELATED DOUBLE SAMPLING

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

TECHNICAL FIELD

The invention relates to image sensors and, more particularly, to a complimentary metal oxide semiconductor (CMOS) image sensor able to perform analog correlated double sampling (CDS).

DESCRIPTION OF THE RELATED ART

Generally, an image sensor is an apparatus that captures images from objects by using the property that silicon semiconductors react with visible light. Most previous image sensors have used charge coupled devices (CCD) as image capturing devices.

However, current CMOS technology has matured to the point that the imagers implemented using CMOS transistors are becoming more popular. CMOS imagers have an advantage over CCD imagers in that supplementary analog and digital circuits can be integrated together with a CMOS image sensing portion on a single chip with very low cost, which makes it possible for the CMOS image sensor to have analog-to-digital conversion circuits and other image processing logic circuits integrated on a single imager.

The on-chip analog-to-digital conversion circuits are comprised of as many comparators as columns in a pixel array of the CMOS image sensor and the picture quality of the CMOS image sensor depends largely on the quality of these comparators that convert analog pixel signals into digital signals.

FIG. **1** is a block diagram illustrating a conventional CMOS image sensor with the function of correlated double sampling. As shown in FIG. **1**, the conventional CMOS image sensor includes a pixel array **100**, a comparator array **200**, a line buffer **300**, a ramp signal generator **400**, a digital controller **500** and a row decoder **600**. The pixel array **100** has unit pixels arranged in the Bayer Pattern and the ramp signal generator **400** generates a ramp signal (as a reference signal for comparison) that is required to find a digital value according to an input analog signal from the pixel. The line buffer **300** consists of 4 arrays of dynamic latch circuits to store the digital value from the comparator array **200** and the digital controller **500** controls the row decoder **600**, the line buffer **300** and the ramp generator **400**, and performs additional image signal processing. The row decoder **600** selects a specific row of the pixel array **100** to read out the analog pixel signals under the control of the digital controller **500**.

When the row decoder **600** selects a row line of the pixel array **100**, the analog pixel signals are input to the comparator array **200**, along with the ramp signal produced by the ramp signal generator **400**. The comparators of the comparator array **200** compare the analog pixel signals with the ramp signal to find the digital pixel signals for analog-to-digital conversion.

The comparator array **200** has as many comparators as columns in the pixel array **100** and these comparators perform the analog-to-digital conversion on a row-by-row basis. The converted digital data (signals) are stored in the line buffer **300** on a column by column basis. The digital pixel signals stored in the line buffer **300** are then transferred to the digital controller **500**, which performs the image processing on them and then outputs the digital image signals through the output pins of the CMOS image sensor.

FIG. **2** is a block diagram illustrating the analog-to-digital conversion circuits of a column of the conventional CMOS image sensor in FIG. **1**. Additionally, FIG. **3** is a waveform of ramp signal to be compared with the analog pixel signal. There are two ramps in the overall ramp signal, which actually perform two analog-to-digital conversions for correlated double sampling (CDS).

Referring to FIG. **2**, analog-to-digital conversion is carried out by a comparator **210**, which is a so-called column ADC(analog-to-digital converter), to compare the analog signal obtained from a unit pixel **110** with the ramp signal from the ramp signal generator **400**. The resulting output signal of the comparator **210** controls the latch **310** to catch and keep the digital gray code that becomes a digital pixel signal in gray code. The gray counter (not shown) is used for minimal error owing to the asynchronous output signal of the comparator **210**.

The unit pixel **110** includes a photodiode **32** to generate a voltage from an image of an object; a transfer transistor Tx to cut the current pass, which will give the photodiode the chance to collect the photo-generated electrons to produce the pixel voltage; and a source-follower (or drive) transistor Dx driven by the photodiode voltage transferred through the transfer transistor Tx, which has a function to safely transfer the pixel voltage to the comparator. The unit pixel **110** also includes a reset transistor Rx that has two functions, to flush out all the electrons in the photodiode and to apply a reset signal to a gate of the source-follower transistor Dx; a selection transistor Sx to let the source-follower voltage out to a comparator **210**; and a bias current source Is to supply the bias current to the source-follower transistor Dx.

To reduce fixed pattern noise (FPN), correlated double sampling (CDS) is used when reading the pixel data. CDS includes two phases, reading reset voltage and reading data voltage. To read the reset voltage, the transfer transistor Tx should be turned off, the reset transistor Rx is to be on for a time long enough to charge the floating node connected to the gate of source-follower transistor Dx up to VDD and then off, and the select transistor Sx must be on to apply the output voltage of the source-follower to the comparator. After the completion of AD(analog-to-digital) conversion cycle, the digital value of the pixel reset voltage is stored in the reset bank of line buffer.

To read the data voltage, the transfer transistor Tx is turned on for some time long enough to complete the process of charge sharing of the photodiode and the floating node of the Dx transistor and then off, and the select transistor Sx is turned on to apply the data voltage of the transistor Dx to the comparator for AD conversion. During the second phase, the Rx transistor is always off. After the second phase, the digital value of pixel data is stored in the data bank of line buffer. The actual CDS process is carried out by the digital control block **500**, which digitally subtracts the reset value from the data value, to filter out all the signal sources of fixed pattern noise.

The process of AD conversion of this imager is simple. When the ramp generator **400**, a simple switched-capacitor integrator, starts to generate a ramp signal, the digital control block **500** starts to count the gray code and the gates of digital latches in the line buffer **300** controlled by the comparator **200** that compares the ramp signal (+) and the pixel

voltage (−), opens the gates of latches when the ramp signal is higher than the pixel voltage, and closes the gates when it is lower are open and ready for the digital latches to follow the codes of the gray counter. The comparator **200** then closes the gates of latches in the line buffer **300** when the ramp signal is the same as, or lower than, the pixel voltage, which means that the latches of the column controlled by the comparator of that column keep the digital value in gray code converted from the analog pixel voltage. In other words, the ramp generator scans from the voltage higher than the maximum possible pixel voltage to the voltage lower than the minimum possible pixel voltage so that the comparator can convert all the analog pixel voltages to digital codes. The gray codes in the line buffer are then transferred to the digital control block **500**, converted to the binary codes, and processed with the CDS operation after the completion of AD conversion of a full row of pixel voltages.

FIG. **4** is a circuit diagram of the conventional comparator of FIG. **2**. However, the detailed description will be omitted because this CMOS differential amplifier is well known to those skilled in the art to which the subject matter pertains.

Typically, a CMOS differential amplifier has an offset voltage and, for the case that a few hundreds of comparators are implemented with such differential amplifiers, the offset voltages of the comparators are not uniform. Therefore, these mismatches of offset voltages of comparators result in the fixed pattern noise in the image captured by this imager. That is why CDS is important in this type of AD conversion. But the traditional CDS performed in the images of FIG. **1** is done digitally, which causes quantization noise.

FIG. **5** is a block diagram of the line buffer **300** of FIG. **1**. Referring to FIG. **5**, two registers of 8-bit or 9-bit latch cells are required for one pixel value owing to CDS operation.

One weak point that the comparator implemented with the CMOS differential amplifier has is that when it is not actually comparing, the static bias currents are still flowing, which results in poor power efficiency. Poor efficiency is a serious defect when applying sensors to mobile applications.

Another weak point is that it is impossible to use a specific gamma correction for the pixel analog signals because the start voltage of the ramp signal is different from one another due to the various offset voltages of the comparators.

SUMMARY OF THE INVENTION

The disclosed CMOS image sensor may include an image capturer for capturing an image for analog image signal from an object and an analog-to-digital converter that converts the analog image signal to a digital value using a ramp signal. In such an arrangement, the analog-to-digital converter may include a chopper-type comparator receiving the analog image signal and the ramp signal and a first capacitor that receives a start voltage of the ramp signal and charging a voltage level corresponding the start voltage of the ramp signal in a reset mode and for receiving a down-ramping signal of the ramp signal in a count mode in order to remove an device offset voltage. The CMOS image sensor may also include a ramp signal generator providing the ramp signal to the analog-to-digital converter.

In a rest mode, the start voltage of the ramp signal is charged in the first capacitor and a reset voltage of the image capturer is simultaneously charged in the chopper-type comparator. In a charge transfer mode, the analog image signal from the image capturer is provided to the chopper-type comparator. In a count mode, the down-ramping signal of the ramp signal is provided to the chopper-type comparator in a count mode.

The disclosed apparatus may use analog correlated double sampling, which the CDS is carried out based on analog signals, rather than on conventional digital correlated double sampling carried out after converting analog signals from a pixel to digital signals.

In the disclosed apparatus, an analog signal and an offset voltage from a pixel of the CMOS image sensor are stored in a second capacitor, the ramp signal and the offset voltage are stored in a third capacitor, and then the offset voltage is removed by a switching operation between the second and third capacitors.

Also disclosed is a a method for removing a device offset voltage in a CMOS image sensor. The method may include charging a start voltage of a ramp signal in a capacitor and simultaneously charging a rest voltage of an image capturer in a chopper-type comparator in a reset mode and providing to the chopper-type comparator an analog image signal from the image capturer in a charge transfer mode. The method may also include providing a down-ramping signal of the ramp signal to the chopper-type comparator in a count mode.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram illustrating a conventional CMOS image sensor with a correlated double sampling;

FIG. **2** is a block diagram illustrating the analog-to-digital conversion circuit of the conventional CMOS image sensor of FIG. **1**;

FIG. **3** is a waveform of ramp signal with an analog signal from a pixel in the correlated double sampling (CDS);

FIG. **4** is a circuit diagram of a conventional comparator of FIG. **2**;

FIG. **5** is a block diagram of the line buffer of FIG. **1**;

FIG. **6** is a circuit diagram illustrating a chopper-type comparator to be employed in a CMOS image sensor;

FIG. **7** is a transfer curve of the inverter amplifier illustrating a clamp voltage induced in capacitors of FIG. **6**;

FIG. **8** is a circuit diagram illustrating a CMOS image sensor having the chopper-type comparator; and

FIG. **9** is a timing chart useful in operating the chopper-type comparator of FIG. **8**.

DETAILED DESCRIPTION

Hereinafter, the disclosed apparatus will be described in detail referring to the accompanying drawings.

Referring to FIG. **6**, a chopper-type comparator, which the disclosed apparatus employs, includes switches S**1** and S**2** to selectively connect input signal Vn or Vo to node A, a first stage **10** having an inverting amplifier IN**1** and a switch S**3** connected in parallel to the inverting amplifier IN**1** and a capacitor C**1** connected between node A and the first stage **10**. The chopper-type comparator may also include a second stage **20** having an inverting amplifier IN**12** and a switch S**4** connected in parallel to the inverting amplifier IN**12** and a capacitor C**2** connected between the first and second stages **10** and **20**. The capacitor C**1** stores a clamp voltage of the first stage **10** and the capacitor C**2** stores a clamp voltage of the second stage **20**.

FIG. **7** is a waveform illustrating the clamp voltage induced in the capacitor of FIG. **6**. If short circuits are respectively formed between the input and output terminals of the inverting amplifiers IN**1** and IN**2** through the switches S**3** and S**4**, clamp voltages of the inverting amplifiers IN**1** and IN**2** are induced.

As mentioned above, the chopper-type comparator disclosed herein includes many switches S**1** to S**4**. The switch-

ing operation of the switches S1 to S4 makes an offset voltage caused by charge injection as the following equation:

$$Voffset=Vth/(A1*A2)$$

where Vth is a logic threshold voltage to subsequently connected next digital circuit and A1 and A2 are gains of the first and second stages, respectively. However, this offset voltage is weaker than that in the conventional differential amplifier. Further, the larger the size of the first and second stages **10** and **20**, the smaller the offset voltage.

It is possible to reduce the offset voltage by increasing the gains of the first and second stages **10** and **20** and the fixed pattern noise can be considerably reduced by the smaller offset voltage.

Referring to FIG. **8**, the CMOS image sensor includes a chopper-type comparator **220**, a unit pixel **120**, a ramp signal generator **410**, a latch circuit **320** and a counter **510** to calculate a digital value corresponding to an analog signal (typically, the counter is provided in a digital controller of the CMOS image sensor). In order to implement the correlated double sampling (CDS), the chopper-type comparator **220** has an additional capacitor C**3** in the input terminal of the ramp signal so that the fixed pattern noise caused between the pixels may be improved.

Referring to FIGS. **8** and **9**, the chopper-type comparator **220** carries out the comparison through three steps. First, if a transfer transistor Tx is set to be turned off and a reset transistor Rx and a selection transistor Sx are set to be turned on, a reset level (Vrest) is induced at a source-follower transistor Dx and a voltage Vp (Vp=Vreset−Vth) is created at node N**1**. However, because the voltage Vth includes an offset voltage (Voffset), the more correct voltage Vp is given by:

$$VP=Vreset-(Vth+Voffset).$$

On the other hand, a starting voltage (Vstart) of a ramp voltage (Vramp) is applied to node N**2** and, on this time, the voltage level at node N**2** is Vramp (=Vstart).

Also, the switches S**1** and S**2** are turned on and a capacitor C**3** stores a voltage level of VC**3**. Subsequently, the switch S**2** is turned off immediately after a predetermined time to maintain such a stored voltage as shown in FIG. **9**. The voltage Vc**3** stored in the capacitor C**3** is given by:

$$Vc3=Vrest=(Vth-Voffset)-Vstart$$

To apply an actual data from the unit pixel **120** to the comparator **220**, the reset transistor Rx is tuned off and the transfer and selection transistors Tx and Sx are turned on so that the photocharges generated in the photodiode are applied to a gate of the source-follow transistor Dx. At this time, because the gate voltage of the source-follow transistor Dx is Vpixel, a voltage level on node N**1** is Vn**1** (=Vpixel−(Vth+Voffset)).

Subsequently, the switches S**3** and S**4** are turned on and then voltage levels of Vclamp**1** and Vclamp**2** are respectively induced in the capacitors C**2** and C**3** based on the operation voltage of the inverting amplifiers IN**1** and IN**2**.

On the other hand, because the switch Si is continuously turned on, the capacitors C**2** and C**1** respectively stores voltage levels of Vc**2** and Vc**1** as follows:

$$Vc2=Vpixel-(Vth+Voffset)-Vclamp1$$

$$Vc1=Vclamp1-Vclamp2$$

In summary, the first and second stages mentioned above, 'Vreset−(Vth+Voffset)−Vstart' is sampled at the first stage and 'Vpixel−(Vth+Voffset)−Vclamp**1**' is sampled at the second stage. Accordingly, a double sampling for removing the offset voltages in the capacitors C**3** and C**2** can be achieved, which is called an analog correlated double sampling in the present disclosure.

At the third stage, the switches S**1**, S**3** and S**4** are turned off and the switch S**2** is turned on to compare the ramp signal from the ramp signal generator **410** to the pixel voltage. Because the switches S**1**, S**3** and S**4** are turned off, the voltage levels of the capacitor C**1**, C**2** and C**3** are kept continuous, even if the switch S**2** is turned on.

At this time, the input voltage (N**3**) of the inverting amplifier IN**1** is given by:

$$VN3=Vramp+VC3-VC2=Vramp-Vstart+Vreset-Vpixel+Vclamp1$$

On the other hand, because the start voltage of the ramp signal is Vstart, VN**3** is expressed as follow:

$$VN3=Vreset-Vpixel+Vclamp1$$

As shown in the above polynomial of VN**3**, the voltage levels of Vth and Voffset, which exist within the polynomials of VC**3** and VC**2**, are removed; thereby achieving the analog correlated double sampling. The voltage level of "Vreset−Vpixel" is a net image data caused by the analog pixel data. Also, since the voltage of Vclamp**1** is an operation voltage of the inverting amplifier IN**1**, the comparison can be obtained while the input voltage of the inverting amplifier IN**1** becomes Vclamp**1**.

A latch enable signal Latch_EN is set to a high voltage level to drive the latch circuit **310** and a clock counting value of the counter **510** increases one by one as the ramp signal from the ramp signal generator **410** gradually decreases.

On the other hand, the ramp signal from the ramp signal generator **410** can be expressed as follow:

$$Vramp=Vstart-\Delta V$$

Accordingly, the voltage level of VN**3** can be expressed as follow:

$$VN3=(Vreset-Vpixel)-\Delta V+Vclamp1$$

According to the feature of the ramp signal, the voltage level of ΔV gradually increases with the lapse of time and eventually it is the same as "Vreset−Vpixel." An input voltage of the inverting amplifier IN**1** becomes "Vclamp**1**" and an input voltage of the inverting amplifier IN**12** becomes "Vclamp**2** simultaneously, so that the two inverting amplifiers IN**1** and IN**2** are at the operation voltage at the same time.

This point in time is the comparison moment and, if the ramp signal is dropped a little, the signal is amplified by the gains of the inverting amplifiers IN**1** and IN**2** and Vo is dropped to a ground voltage level.

If Vo is dropped to the ground voltage level, the final value, which is continuously counted by the counter **510**, is stored in the latch circuit **320**. Accordingly, the latched value is a digital value from the unit pixel **120**.

Finally, the latch enable signal Latch_EN is set to a logic low level in order to store the digital values in the latch circuit **320** until the data stored to latch **310** is transmitted to the digital controller (reference numeral **500** of FIG. **1**).

The current of the comparator is consumed in the inverting amplifiers IN**1** and IN**2** only when the comparison is carried out so that there is little static current and it is possible to reduce the power consumption sharply. Also, because the comparator stores the reset level in the capacitor C**3** in the analog signal level, only one ramp signal is required to obtain the digital signal corresponding to the input analog signal with the simple digital control algorithm and operations used in the CMOS image sensor. Further, because it is not necessary to store the digital value corresponding to the reset level of the CMOS image sensor, the entire size of the memories can be reduced by half.

As apparent from the above, the disclosed comparator can reduce the fixed pattern noise, such as the offset voltage, in the CMOS image sensor by considerably removing the offset voltage that exist between pixels using the analog correlated double sampling. The comparator can be made by a simple circuit design without a subtractor because only one ramp signal is used to obtain the digital value. Also, the ramp signal generator for the comparison can has a simple structure so that the chip size of the CMOS image sensor using the disclosed analog correlated double sampling is smaller than others using the digital correlated double sampling. Further, the disclosed apparatus may be employed in other integration circuits in which a low-voltage operation is required to reduce a power consumption or it is necessary to remove the offset value to obtain an exact digital value.

The comparator may have a simple structure that connects, in series, signal processing stages to process input data and the ramp signal. Further, the disclosed device may include a CMOS inverter with a low-operation voltage and a chopper type voltage comparator. Because the chopper type voltage comparator uses an inverter as a voltage amplifier, which consumes the current only when the comparison of inputs is carried out, the disclosed device can reduce the power consumption thereof.

The disclosure introduces a new architecture of CMOS image sensor that has many advantages over the previous one. Such advantages include smaller size of chip area, reduced power consumption, reduced FPN and possibility of implementing analog gamma correction. The disclosed CMOS image sensor is capable of reducing power consumption and a size of chip through the reduction of an offset voltage efficiently therein.

Although certain apparatus constructed in accordance with the teachings of the invention have been described herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers all embodiments of the teachings of the invention fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.

What is claimed is:

1. A CMOS image sensor comprising:

an image capturer for capturing an image and producing an analog image signal from an object;

an analog-to-digital converter for converting the analog image signal to a digital value using a ramp signal, wherein the analog-to-digital converter includes:

a) a chopper-type comparator receiving the analog image signal and the ramp signal; and

b) a capacitor for receiving a start voltage of the ramp signal and charging a voltage level corresponding the start voltage of the ramp signal in a reset mode and for receiving a down-ramping signal of the ramp signal in a count mode in order to remove a device offset voltage; and

a ramp signal generator providing the ramp signal to the analog-to-digital converter.

2. The CMOS image sensor as recited in claim **1**, further comprising a latch circuit for storing the digital value converted by the analog-to-digital converter, wherein the latch circuit has a plurality of buffer lines to store the digital value only, *wherein the capacitor is a first capacitor and wherein the chopper-type comparator comprises: a plurality of capacitors and switches; and at least two inverting amplifiers, wherein the switches are controlled by a digital controller in the CMOS image sensor.*

3. The CMOS image sensor as recited in claim **1**, wherein the capacitor is a first capacitor and wherein the chopper-type comparator comprises:

a plurality of capacitors and switches; and

at least two inverting amplifiers, wherein the switches are controlled by a digital controller in the CMOS image sensor.

4. The CMOS image sensor as recited in claim **3**, wherein the chopper-type comparator comprises:

a first switch connected to the image capturer;

a second switch connected to the ramp signal generator;

a second capacitor connected to the first switch, wherein the first capacitor is connected between the first switch and the second switch;

a first inverting amplifier connected to the second capacitor;

a third switch connected between input and output terminals of the first inverting amplifier;

a third capacitor connected to the first inverting amplifier;

a fourth switch connected between input and output terminals of **[**the**]** *a* second inverting amplifier; and

[a**]** *wherein the* second inverting amplifier *is* connected to the third capacitor and the latch circuit to store the digital value.

5. The CMOS image sensor as recited in claim **4**, wherein the first switch is turned on in response to a control signal from the digital controller in the **[**rest**]** *reset* mode and in a charge transfer mode in which photocharges are transferred to the analog-to-digital converter.

6. The CMOS image sensor as recited in claim **5**, wherein the first, third, and fourth switches are turned on in response to a control signal from the digital controller in the charge transfer mode in which photocharges are transferred to the analog-to-digital converter.

7. A method for removing a device offset voltage in a CMOS image sensor, the method comprising:

charging a start voltage of a ramp signal in a capacitor and simultaneously charging a **[**rest**]** *reset* voltage of an image capturer in a chopper-type comparator in a reset mode;

providing to the chopper-type comparator an analog image signal from the image capturer in a charge transfer mode; and

providing a down-ramping signal of the ramp signal to the chopper-type comparator in a count mode.

8. A CMOS image sensor comprising:

an image capturer including a plurality of pixel sensor circuits configured to provide analog signals in a reset mode and a read mode, wherein each pixel sensor circuit is further configured to provide a reset signal in the reset mode and a pixel output signal in the read mode, and wherein an offset signal is superimposed on the reset signal and the pixel output signal of each pixel sensor circuit;

a ramp signal generator configured to provide a ramp signal, wherein the ramp signal includes a ramp signal waveform beginning as a start signal;

a chopper circuit configured to receive the analog signals and the ramp signal, wherein the chopper circuit is further configured to generate a control signal to control operation of a logic component, and wherein the chopper circuit is further configured such that:

during the reset mode, the chopper circuit generates a reset mode signal corresponding to a difference between first and second signals, wherein the first signal includes the reset signal, wherein the second signal includes a sum of the offset signal and the start signal, and wherein the reset signal, offset signal, and start signal are sampled concurrently;

during the read mode, the chopper circuit generates a clamped logic level signal, wherein the chopper circuit further generates a read mode signal that corresponds to a difference between the pixel output signal and a third signal, and wherein the third signal includes a sum of the offset signal and the clamped logic level signal; and

during the read mode, the chopper circuit generates the control signal using a signal corresponding to a difference between the reset mode signal and the read mode signal.

9. The CMOS image sensor of claim 8, wherein the ramp signal waveform includes a down-ramping waveform.

10. The CMOS image sensor of claim 8, wherein the chopper circuit comprises:

a plurality of capacitors and switches; and

at least two inverting amplifiers, wherein the switches are configured to respond to control signals provided by a digital controller in the CMOS image sensor.

11. The CMOS image sensor of claim 10, wherein the chopper circuit further comprises:

a first switch configured to receive the analog signals from the image capturer;

a second switch configured to receive the ramp signal from the ramp signal generator;

a first capacitor connected between the first switch and the second switch;

a first inverting amplifier connected to the first capacitor;

a third switch connected between input and output terminals of the first inverting amplifier;

a second capacitor connected between the first switch and the input terminal of the first inverting amplifier;

a second inverting amplifier;

a third capacitor connected between the output terminal of the first inverting amplifier and an input terminal of the second inverting amplifier;

a fourth switch connected between input and output terminals of the second inverting amplifier;

wherein the output terminal of the second inverting amplifier is provided as the control signal from the chopper circuit.

12. The CMOS image sensor of claim 11, wherein the first, second, third, and fourth switches are configured to respond to control signals from the digital controller.

13. The CMOS image sensor of claim 8, further comprising a latch circuit configured to store a digital value of a digital counter if a difference between the reset mode signal and the read mode signal corresponds to a magnitude of the ramp signal waveform.

14. A method of compensating for an offset voltage of a pixel sensor in a CMOS image sensor, the method comprising:

providing a reset voltage from the pixel sensor during a reset mode, wherein the offset voltage is superimposed on the reset voltage;

providing a ramp voltage waveform beginning at a start voltage;

concurrently sampling the reset voltage, the offset voltage superimposed on the reset voltage, and the start voltage;

generating a reset mode voltage, wherein the reset mode voltage corresponds to a difference between first and second voltages, wherein the first voltage includes the reset voltage, and wherein the second voltage includes a sum of the offset voltage and the start voltage;

generating a clamped logic level voltage;

providing a pixel output voltage during a pixel sensor read mode, wherein the offset voltage is superimposed on the pixel output voltage;

generating a read mode voltage corresponding to a difference between the pixel output voltage and a third voltage, wherein the third voltage includes a sum of the offset voltage and the clamped logic level voltage; and

generating a control signal to a logic circuit, wherein the control signal corresponds to a difference between the reset mode voltage and the read mode voltage.

15. The method of claim 14, wherein said generating a reset mode voltage comprises:

configuring a capacitor to receive the reset voltage and the offset voltage at a first terminal; and

configuring the capacitor to receive the start signal at a second terminal.

16. A CMOS image sensor comprising: an image capturer including a plurality of pixel sensor circuits, wherein each pixel sensor circuit is configured to provide a reset signal in a reset mode and a pixel output signal in a read mode, and wherein an offset signal is superimposed on the reset signal and the pixel output signal of each pixel sensor circuit during the reset mode and read mode, respectively;

a ramp signal generator configured to provide a ramp signal, wherein the ramp signal includes a ramp signal waveform beginning as a start signal;

a chopper circuit configured to receive the reset signal with the superimposed offset signal from a given pixel sensor circuit during the reset mode and the pixel output signal with the superimposed offset signal from the given pixel sensor circuit during the read mode, wherein the chopper circuit is configured to receive the ramp signal from the ramp signal generator, and wherein the chopper circuit is configured to generate a control signal to control operation of a logic component;

wherein, during the reset mode, the chopper circuit is configured to generate a reset mode signal across a charging element by concurrently sampling the reset signal and the offset signal from the given pixel sensor circuit and the start signal from the ramp signal generator, wherein the reset mode signal corresponds to a difference between first and second signals, and wherein the first signal includes the reset signal, and wherein the second signal includes a sum of the offset signal and the start signal;

wherein, during the read mode, the chopper circuit is further configured to generate a clamped logic level signal and is further configured to generate a read mode signal that corresponds to a difference between the pixel output signal and a third signal, wherein the third sig-

nal includes a sum of the offset signal and the clamped logic level signal; and

wherein, during the read mode, the chopper circuit is further configured to generate the control signal using a signal corresponding to a difference between the reset mode signal and the read mode signal.

17. The CMOS image sensor of claim 16, wherein the charging element comprises a capacitor connected between first and second inputs of the chopper circuit.

18. A CMOS image sensor comprising:

an image capturer having a plurality of pixel sensor circuits, wherein each pixel sensor circuit is configured to provide an analog signal at its output;

a ramp signal generator configured to provide a ramp signal;

a chopper circuit configured to receive the analog signal from a given pixel sensor circuit and to receive the ramp signal from the ramp signal generator, wherein the chopper circuit is configured to:

provide a logic level control signal to control operation of a logic component, wherein the logic level control signal is used to generate a digital signal corresponding to a magnitude of the analog signal provided from the output of the given pixel sensor circuit; and

store a signal across a charging element, wherein the signal stored across the charging element corresponds to a difference between the analog signal from the given pixel sensor circuit and the ramp signal from the ramp signal generator, wherein the analog signal from the given pixel sensor circuit and the ramp signal from the ramp signal generator are concurrently sampled to store the signal across the charging element during a mode of at least two modes of operation of the given pixel sensor circuit to generate the logic level control signal to the logic component, wherein the charging element comprises a capacitor connected between first and second inputs of the chopper circuit.

19. The CMOS image sensor of claim 18, wherein the at least two modes of operation comprise a reset mode in which a reset signal is provided from the output of the given pixel sensor circuit and a read mode in which a pixel output signal is provided from the output of the given pixel sensor circuit.

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