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(54) **CMOS IMAGE SENSOR HAVING A CHOPPER-TYPE COMPARATOR TO PERFORM ANALOG CORRELATED DOUBLE SAMPLING**

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(Under 37 CFR 1.47)

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H01L 27/00 (2006.01)

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(58) **Field of Classification Search** 250/208.1, 250/214.1; 348/241, 294, 300
See application file for complete search history.

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(57) **ABSTRACT**

A CMOS image sensor performing an analog correlated double sampling is disclosed. The CMOS image sensor may include an image capture device for capturing an image for analog image signal from an object an analog-to-digital converter for converting the analog image signal to a digital value using a ramp signal. In such an arrangement the analog-to-digital converter may includes a chopper-type comparator receiving the analog image signal and the ramp signal and a capacitor for receiving a start voltage of the ramp signal and charging a voltage level corresponding the start voltage of the ramp signal in a reset mode and for receiving a down-ramping signal of the ramp signal in a count mode in order to remove an device offset voltage. The analog-to-digital converter may also include a ramp signal generator providing the ramp signal to the analog-to-digital converter.

19 Claims, 9 Drawing Sheets

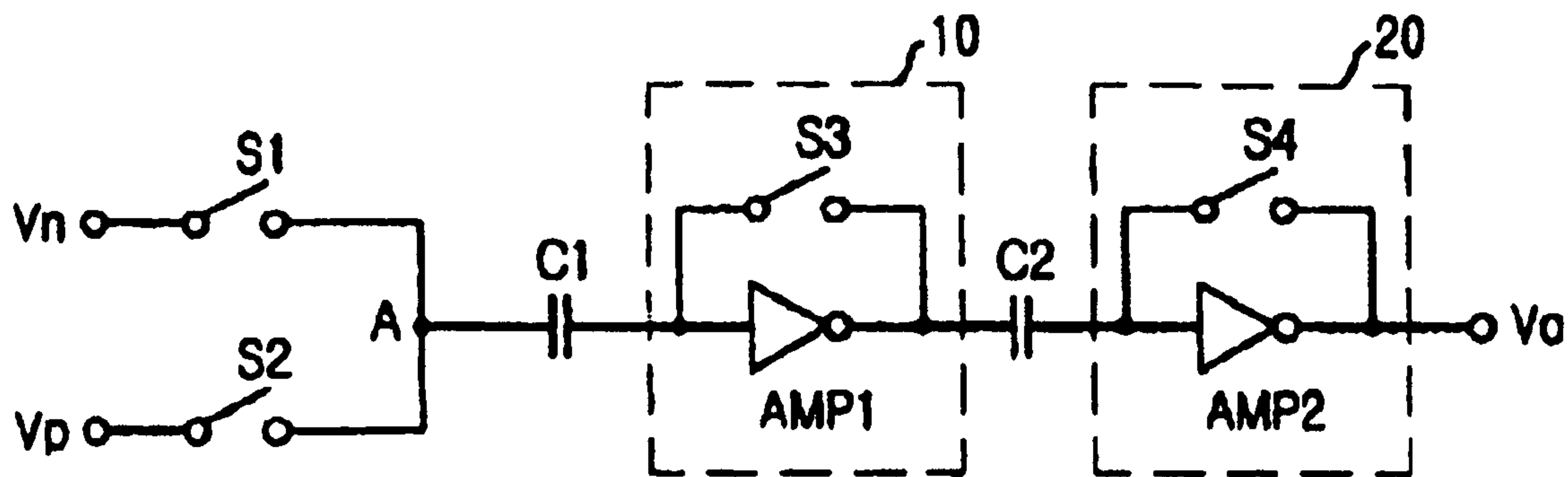


FIG. 1
(PRIOR ART)

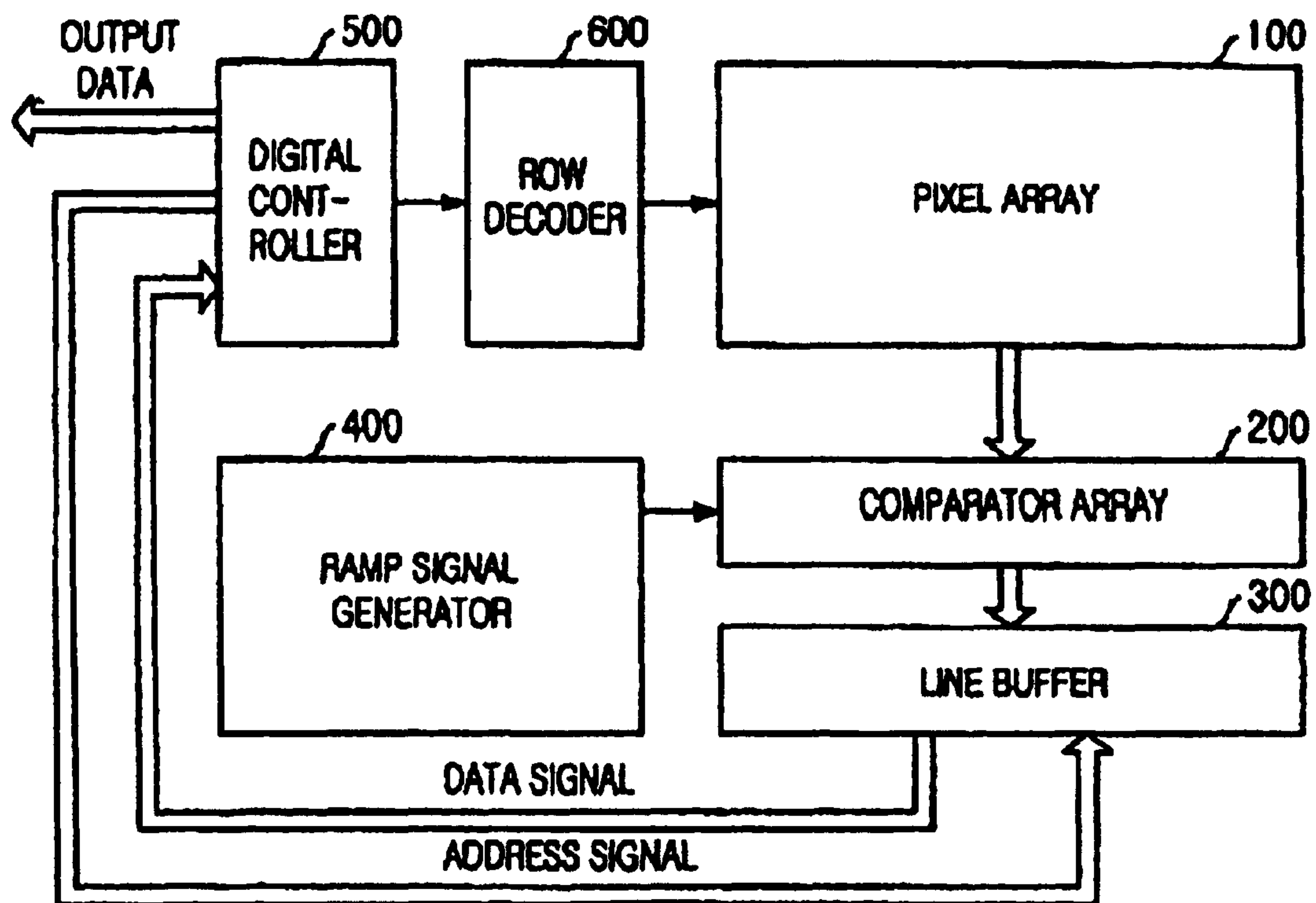


FIG. 2
(PRIOR ART)

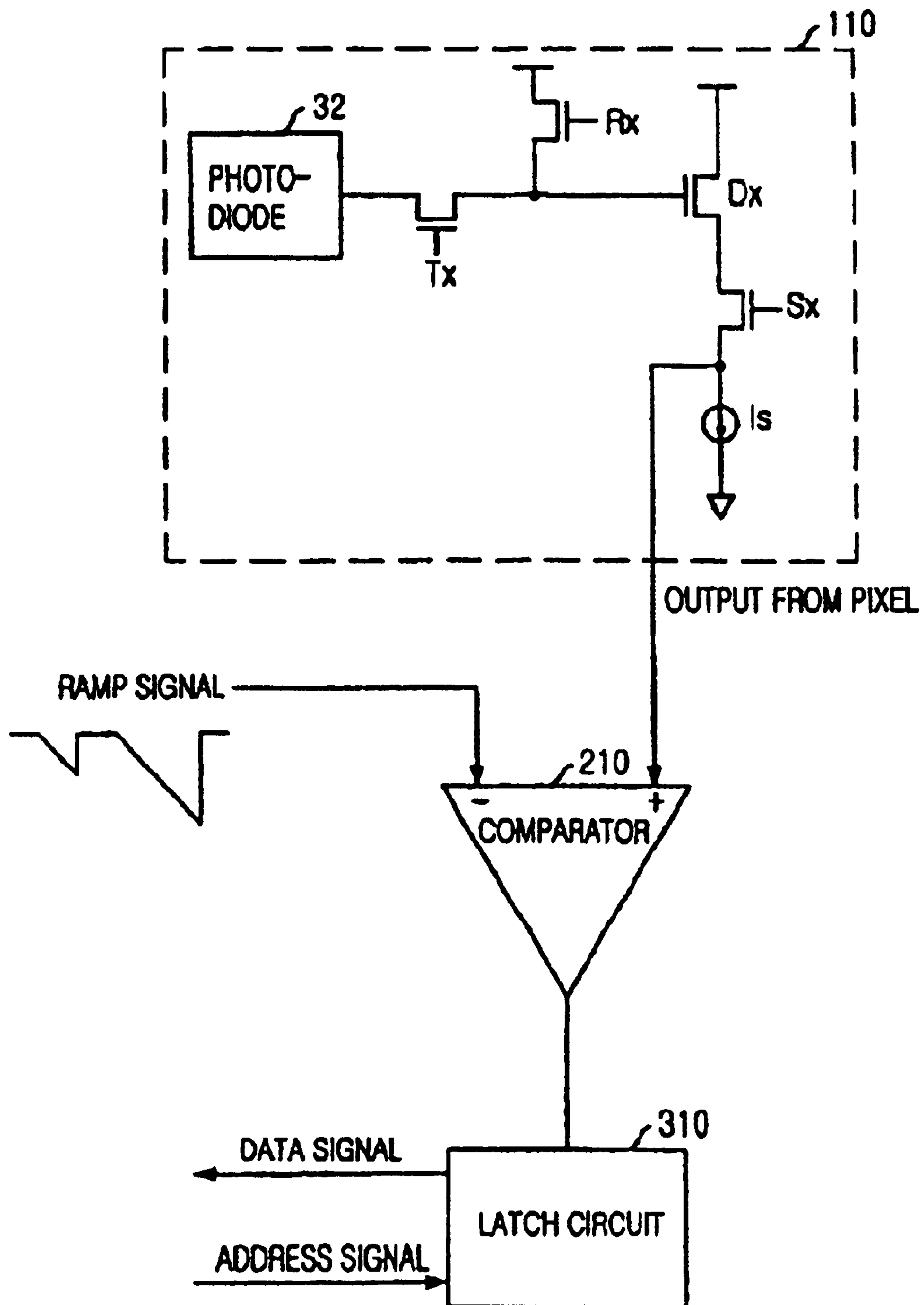


FIG. 3
(PRIOR ART)

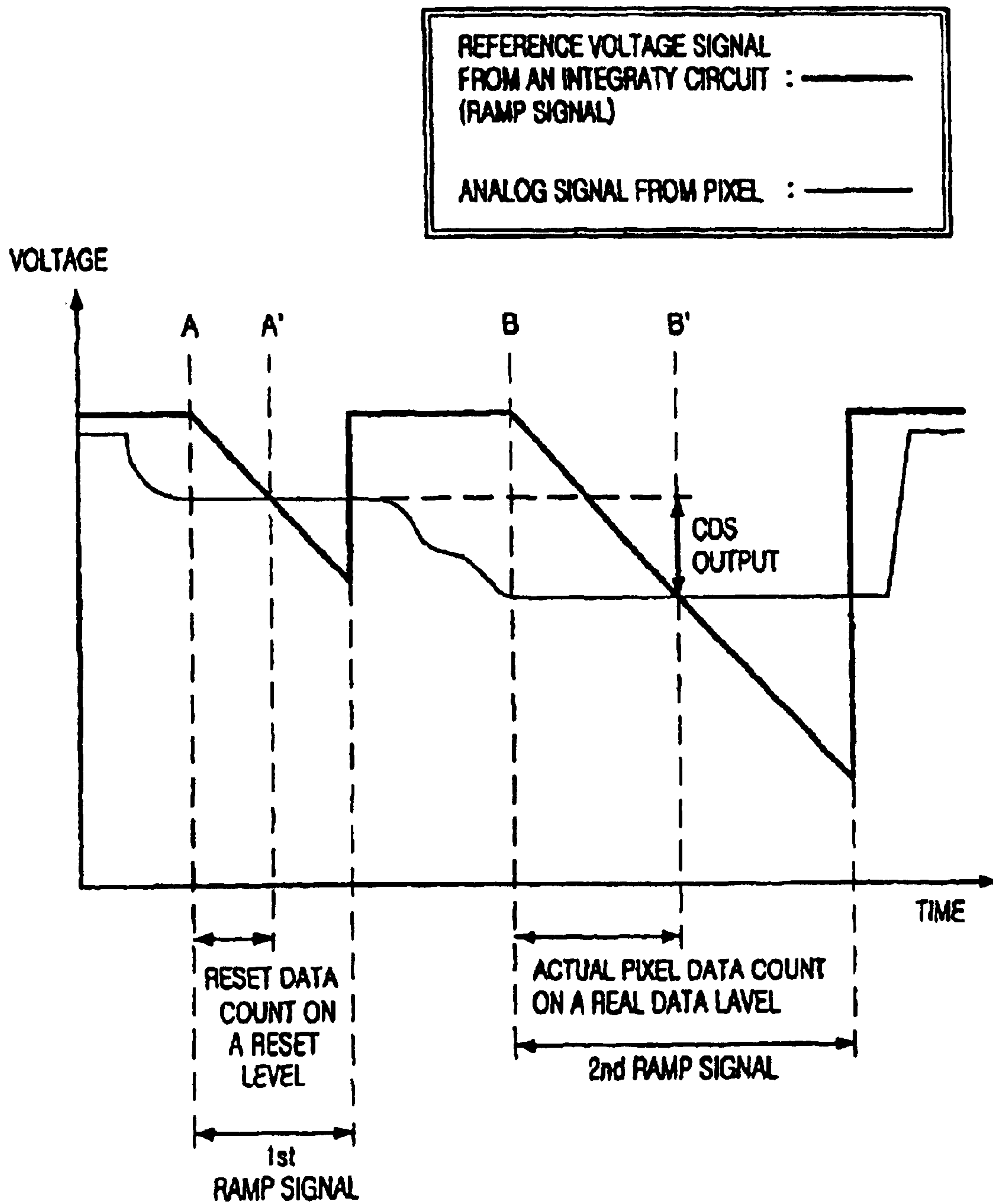


FIG. 5
(PRIOR ART)

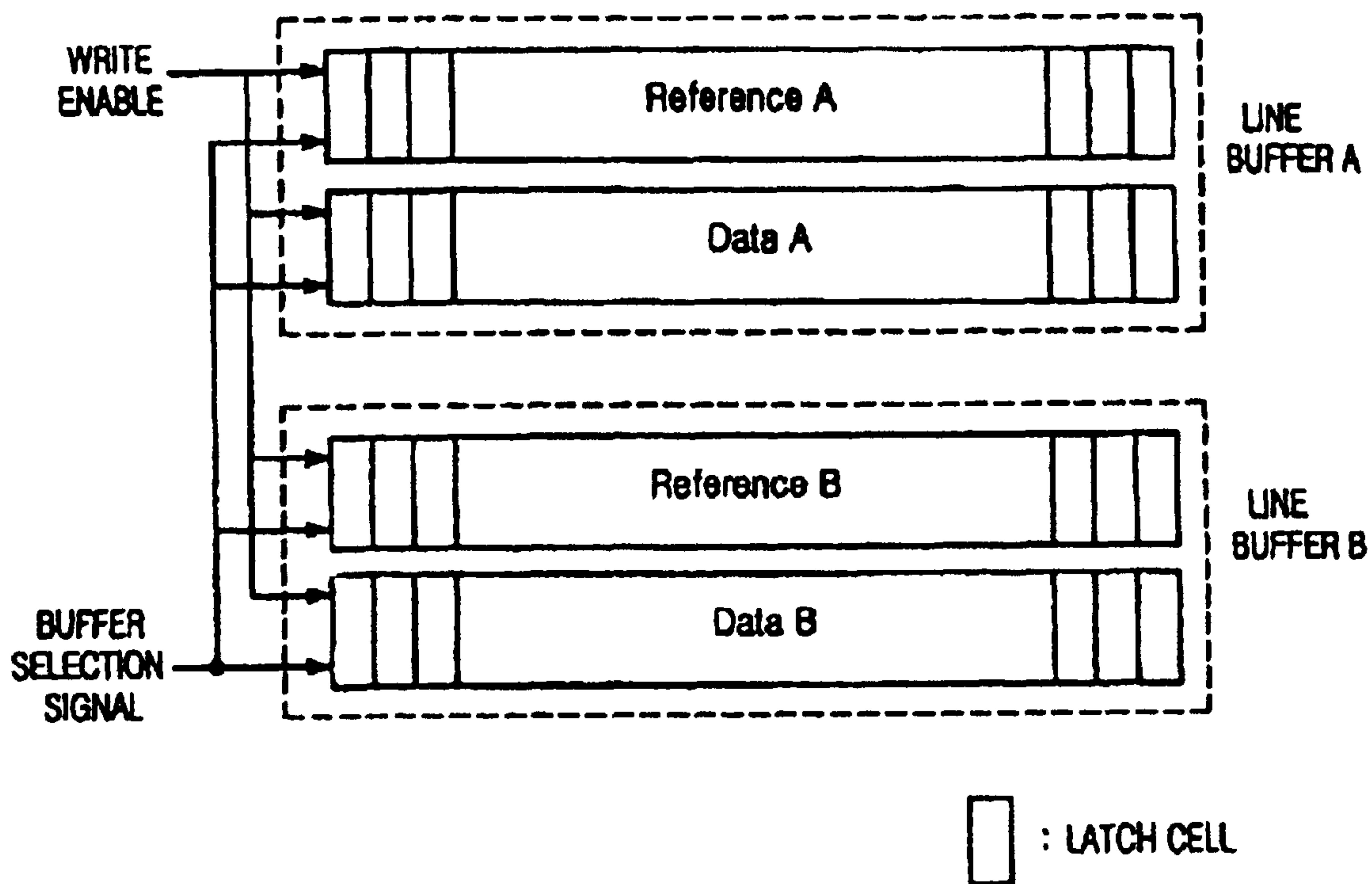


FIG. 6

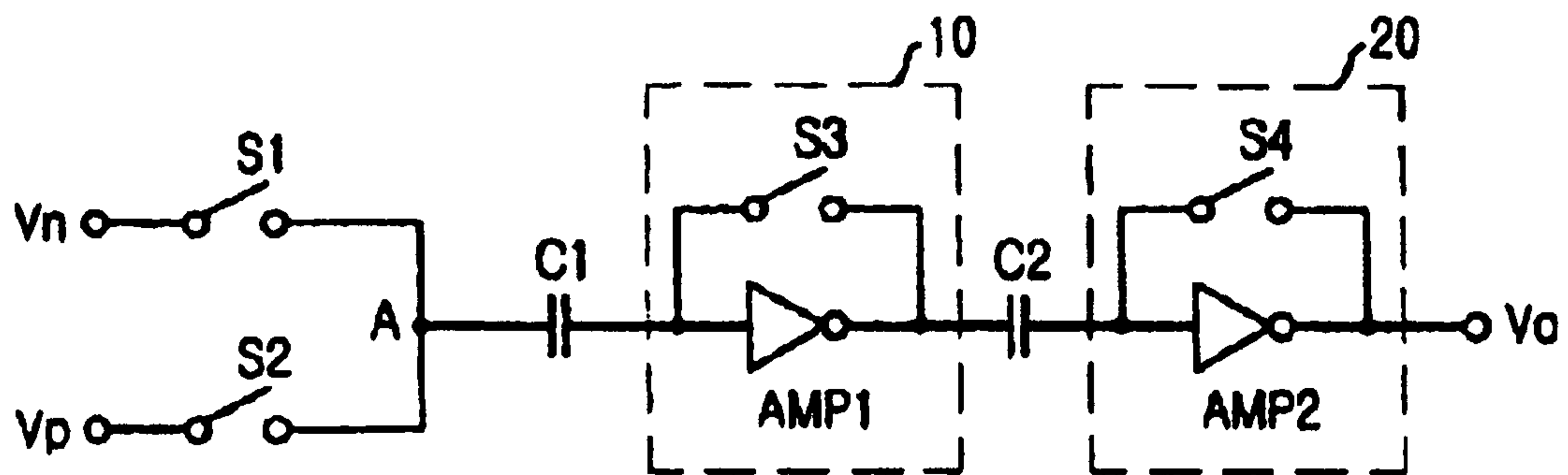


FIG. 7

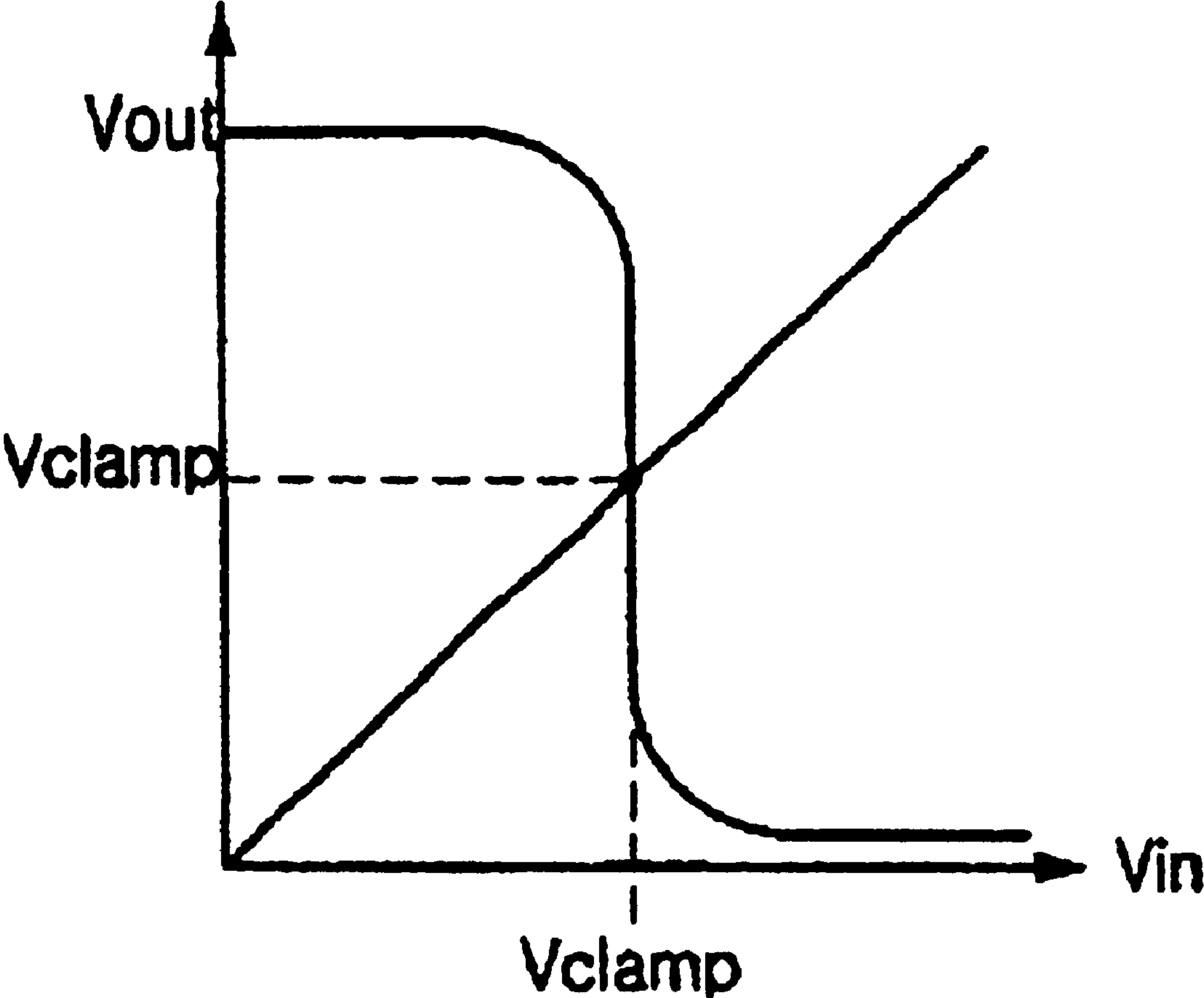
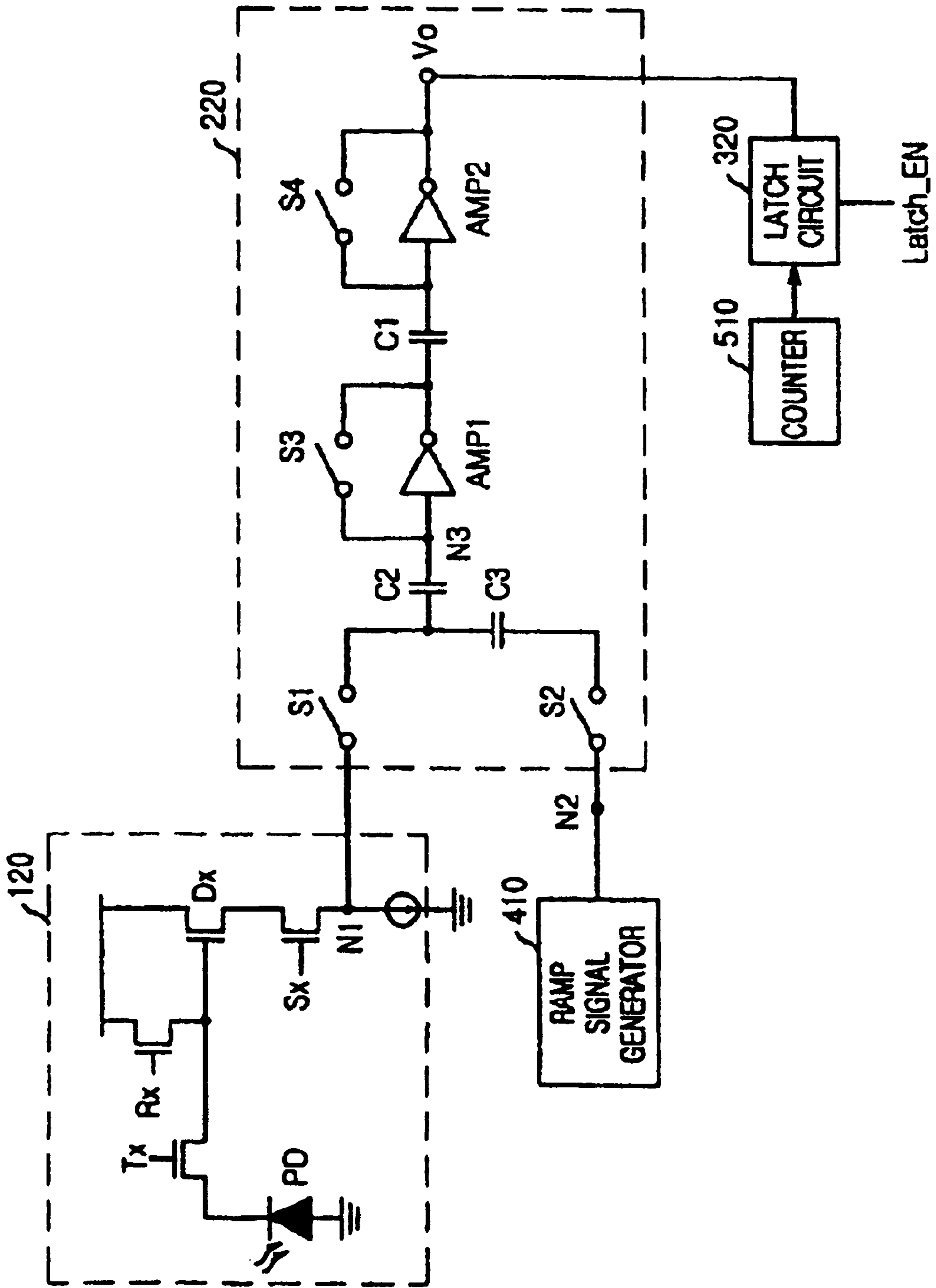


FIG. 8



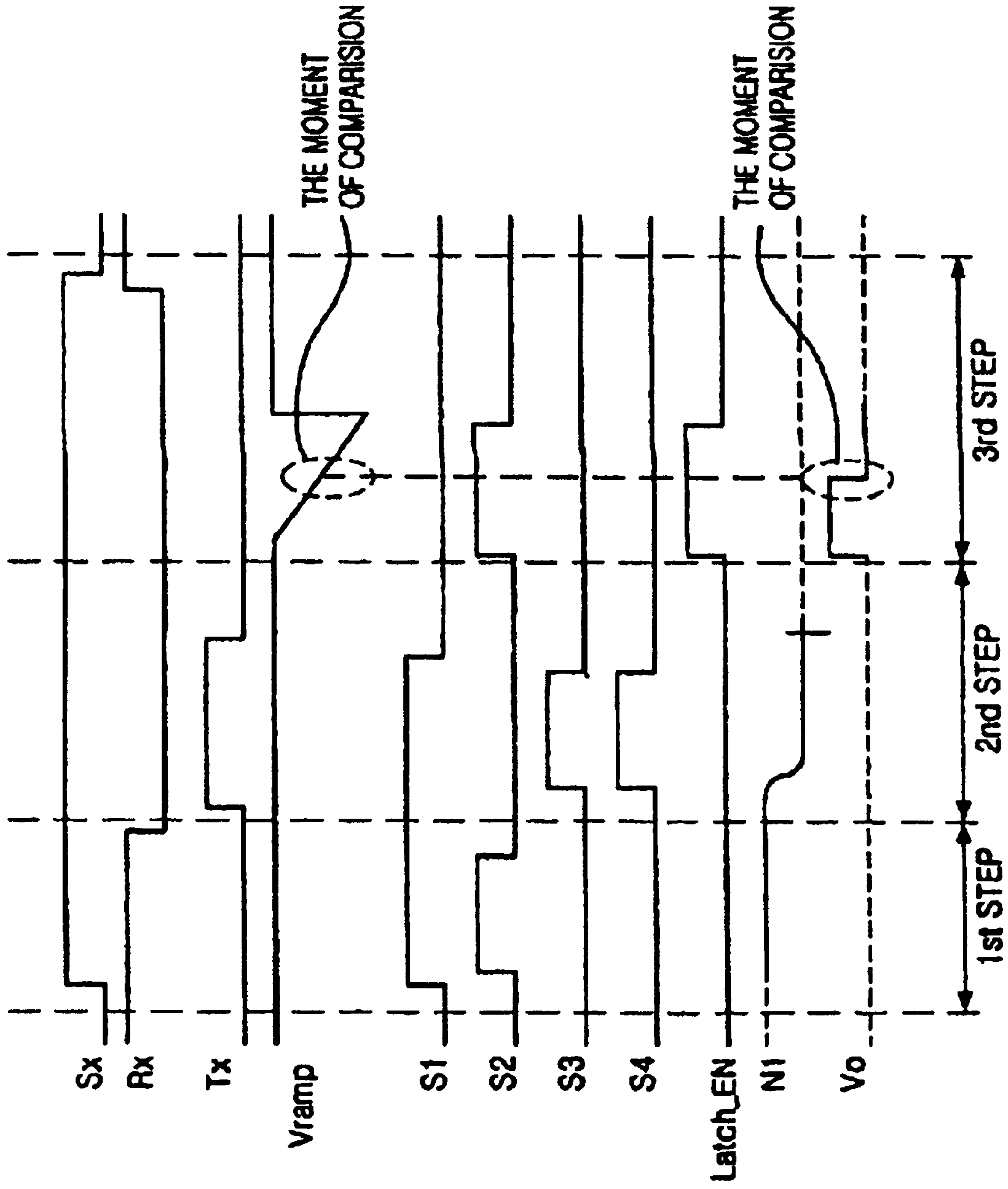


FIG. 9

1

**CMOS IMAGE SENSOR HAVING A
CHOPPER-TYPE COMPARATOR TO
PERFORM ANALOG CORRELATED DOUBLE
SAMPLING**

Matter enclosed in heavy brackets [] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

TECHNICAL FIELD

The invention relates to image sensors and, more particularly, to a complimentary metal oxide semiconductor (CMOS) image sensor able to perform analog correlated double sampling (CDS).

DESCRIPTION OF THE RELATED ART

Generally, an image sensor is an apparatus that captures images from objects by using the property that silicon semiconductors react with visible light. Most previous image sensors have used charge coupled devices (CCD) as image capturing devices.

However, current CMOS technology has matured to the point that the imagers implemented using CMOS transistors are becoming more popular. CMOS imagers have an advantage over CCD imagers in that supplementary analog and digital circuits can be integrated together with a CMOS image sensing portion on a single chip with very low cost, which makes it possible for the CMOS image sensor to have analog-to-digital conversion circuits and other image processing logic circuits integrated on a single imager.

The on-chip analog-to-digital conversion circuits are comprised of as many comparators as columns in a pixel array of the CMOS image sensor and the picture quality of the CMOS image sensor depends largely on the quality of these comparators that convert analog pixel signals into digital signals.

FIG. 1 is a block diagram illustrating a conventional CMOS image sensor with the function of correlated double sampling. As shown in FIG. 1, the conventional CMOS image sensor includes a pixel array 100, a comparator array 200, a line buffer 300, a ramp signal generator 400, a digital controller 500 and a row decoder 600. The pixel array 100 has unit pixels arranged in the Bayer Pattern and the ramp signal generator 400 generates a ramp signal (as a reference signal for comparison) that is required to find a digital value according to an input analog signal from the pixel. The line buffer 300 consists of 4 arrays of dynamic latch circuits to store the digital value from the comparator array 200 and the digital controller 500 controls the row decoder 600, the line buffer 300 and the ramp generator 400, and performs additional image signal processing. The row decoder 600 selects a specific row of the pixel array 100 to read out the analog pixel signals under the control of the digital controller 500.

When the row decoder 600 selects a row line of the pixel array 100, the analog pixel signals are input to the comparator array 200, along with the ramp signal produced by the ramp signal generator 400. The comparators of the comparator array 200 compare the analog pixel signals with the ramp signal to find the digital pixel signals for analog-to-digital conversion.

The comparator array 200 has as many comparators as columns in the pixel array 100 and these comparators perform the analog-to-digital conversion on a row-by-row basis. The converted digital data (signals) are stored in the line

2

buffer 300 on a column by column basis. The digital pixel signals stored in the line buffer 300 are then transferred to the digital controller 500, which performs the image processing on them and then outputs the digital image signals through the output pins of the CMOS image sensor.

FIG. 2 is a block diagram illustrating the analog-to-digital conversion circuits of a column of the conventional CMOS image sensor in FIG. 1. Additionally, FIG. 3 is a waveform of ramp signal to be compared with the analog pixel signal. There are two ramps in the overall ramp signal, which actually perform two analog-to-digital conversions for correlated double sampling (CDS).

Referring to FIG. 2, analog-to-digital conversion is carried out by a comparator 210, which is a so-called column ADC(analog-to-digital converter), to compare the analog signal obtained from a unit pixel 110 with the ramp signal from the ramp signal generator 400. The resulting output signal of the comparator 210 controls the latch 310 to catch and keep the digital gray code that becomes a digital pixel signal in gray code. The gray counter (not shown) is used for minimal error owing to the asynchronous output signal of the comparator 210.

The unit pixel 110 includes a photodiode 32 to generate a voltage from an image of an object; a transfer transistor Tx to cut the current pass, which will give the photodiode the chance to collect the photo-generated electrons to produce the pixel voltage; and a source-follower (or drive) transistor Dx driven by the photodiode voltage transferred through the transfer transistor Tx, which has a function to safely transfer the pixel voltage to the comparator. The unit pixel 110 also includes a reset transistor Rx that has two functions, to flush out all the electrons in the photodiode and to apply a reset signal to a gate of the source-follower transistor Dx; a selection transistor Sx to let the source-follower voltage out to a comparator 210; and a bias current source Is to supply the bias current to the source-follower transistor Dx.

To reduce fixed pattern noise (FPN), correlated double sampling (CDS) is used when reading the pixel data. CDS includes two phases, reading reset voltage and reading data voltage. To read the reset voltage, the transfer transistor Tx should be turned off, the reset transistor Rx is to be on for a time long enough to charge the floating node connected to the gate of source-follower transistor Dx up to VDD and then off, and the select transistor Sx must be on to apply the output voltage of the source-follower to the comparator. After the completion of AD(analog-to-digital) conversion cycle, the digital value of the pixel reset voltage is stored in the reset bank of line buffer.

To read the data voltage, the transfer transistor Tx is turned on for some time long enough to complete the process of charge sharing of the photodiode and the floating node of the Dx transistor and then off, and the select transistor Sx is turned on to apply the data voltage of the transistor Dx to the comparator for AD conversion. During the second phase, the Rx transistor is always off. After the second phase, the digital value of pixel data is stored in the data bank of line buffer. The actual CDS process is carried out by the digital control block 500, which digitally subtracts the reset value from the data value, to filter out all the signal sources of fixed pattern noise.

The process of AD conversion of this imager is simple. When the ramp generator 400, a simple switched-capacitor integrator, starts to generate a ramp signal, the digital control block 500 starts to count the gray code and the gates of digital latches in the line buffer 300 controlled by the comparator 200 that compares the ramp signal (+) and the pixel

5

ing operation of the switches S1 to S4 makes an offset voltage caused by charge injection as the following equation:

$$V_{\text{offset}}=V_{\text{th}}/(A1*A2)$$

where V_{th} is a logic threshold voltage to subsequently connected next digital circuit and A1 and A2 are gains of the first and second stages, respectively. However, this offset voltage is weaker than that in the conventional differential amplifier. Further, the larger the size of the first and second stages 10 and 20, the smaller the offset voltage.

It is possible to reduce the offset voltage by increasing the gains of the first and second stages 10 and 20 and the fixed pattern noise can be considerably reduced by the smaller offset voltage.

Referring to FIG. 8, the CMOS image sensor includes a chopper-type comparator 220, a unit pixel 120, a ramp signal generator 410, a latch circuit 320 and a counter 510 to calculate a digital value corresponding to an analog signal (typically, the counter is provided in a digital controller of the CMOS image sensor). In order to implement the correlated double sampling (CDS), the chopper-type comparator 220 has an additional capacitor C3 in the input terminal of the ramp signal so that the fixed pattern noise caused between the pixels may be improved.

Referring to FIGS. 8 and 9, the chopper-type comparator 220 carries out the comparison through three steps. First, if a transfer transistor Tx is set to be turned off and a reset transistor Rx and a selection transistor Sx are set to be turned on, a reset level (V_{rest}) is induced at a source-follower transistor Dx and a voltage V_{p} ($V_{\text{p}}=V_{\text{reset}}-V_{\text{th}}$) is created at node N1. However, because the voltage V_{th} includes an offset voltage (V_{offset}), the more correct voltage V_{p} is given by:

$$V_{\text{p}}=V_{\text{reset}}-(V_{\text{th}}+V_{\text{offset}}).$$

On the other hand, a starting voltage (V_{start}) of a ramp voltage (V_{ramp}) is applied to node N2 and, on this time, the voltage level at node N2 is V_{ramp} ($=V_{\text{start}}$).

Also, the switches S1 and S2 are turned on and a capacitor C3 stores a voltage level of V_{C3} . Subsequently, the switch S2 is turned off immediately after a predetermined time to maintain such a stored voltage as shown in FIG. 9. The voltage V_{c3} stored in the capacitor C3 is given by:

$$V_{\text{c3}}=V_{\text{rest}}=(V_{\text{th}}-V_{\text{offset}})-V_{\text{start}}$$

To apply an actual data from the unit pixel 120 to the comparator 220, the reset transistor Rx is turned off and the transfer and selection transistors Tx and Sx are turned on so that the photocharges generated in the photodiode are applied to a gate of the source-follower transistor Dx. At this time, because the gate voltage of the source-follower transistor Dx is V_{pixel} , a voltage level on node N1 is V_{n1} ($=V_{\text{pixel}}-(V_{\text{th}}+V_{\text{offset}})$).

Subsequently, the switches S3 and S4 are turned on and then voltage levels of V_{clamp1} and V_{clamp2} are respectively induced in the capacitors C2 and C3 based on the operation voltage of the inverting amplifiers IN1 and IN2.

On the other hand, because the switch Si is continuously turned on, the capacitors C2 and C1 respectively stores voltage levels of V_{c2} and V_{c1} as follows:

$$V_{\text{c2}}=V_{\text{pixel}}-(V_{\text{th}}+V_{\text{offset}})-V_{\text{clamp1}}$$

$$V_{\text{c1}}=V_{\text{clamp1}}-V_{\text{clamp2}}$$

6

In summary, the first and second stages mentioned above, ' $V_{\text{reset}}-(V_{\text{th}}+V_{\text{offset}})-V_{\text{start}}$ ' is sampled at the first stage and ' $V_{\text{pixel}}-(V_{\text{th}}+V_{\text{offset}})-V_{\text{clamp1}}$ ' is sampled at the second stage. Accordingly, a double sampling for removing the offset voltages in the capacitors C3 and C2 can be achieved, which is called an analog correlated double sampling in the present disclosure.

At the third stage, the switches S1, S3 and S4 are turned off and the switch S2 is turned on to compare the ramp signal from the ramp signal generator 410 to the pixel voltage. Because the switches S1, S3 and S4 are turned off, the voltage levels of the capacitor C1, C2 and C3 are kept continuous, even if the switch S2 is turned on.

At this time, the input voltage (V_{N3}) of the inverting amplifier IN1 is given by:

$$V_{\text{N3}}=V_{\text{ramp}}+V_{\text{C3}}-V_{\text{C2}}=V_{\text{ramp}}-V_{\text{start}}+V_{\text{reset}}-V_{\text{pixel}}+V_{\text{clamp1}}$$

On the other hand, because the start voltage of the ramp signal is V_{start} , V_{N3} is expressed as follow:

$$V_{\text{N3}}=V_{\text{reset}}-V_{\text{pixel}}+V_{\text{clamp1}}$$

As shown in the above polynomial of V_{N3} , the voltage levels of V_{th} and V_{offset} , which exist within the polynomials of V_{C3} and V_{C2} , are removed; thereby achieving the analog correlated double sampling. The voltage level of " $V_{\text{reset}}-V_{\text{pixel}}$ " is a net image data caused by the analog pixel data. Also, since the voltage of V_{clamp1} is an operation voltage of the inverting amplifier IN1, the comparison can be obtained while the input voltage of the inverting amplifier IN1 becomes V_{clamp1} .

A latch enable signal Latch_EN is set to a high voltage level to drive the latch circuit 310 and a clock counting value of the counter 510 increases one by one as the ramp signal from the ramp signal generator 410 gradually decreases.

On the other hand, the ramp signal from the ramp signal generator 410 can be expressed as follow:

$$V_{\text{ramp}}=V_{\text{start}}-\Delta V$$

Accordingly, the voltage level of V_{N3} can be expressed as follow:

$$V_{\text{N3}}=(V_{\text{reset}}-V_{\text{pixel}})-\Delta V+V_{\text{clamp1}}$$

According to the feature of the ramp signal, the voltage level of ΔV gradually increases with the lapse of time and eventually it is the same as " $V_{\text{reset}}-V_{\text{pixel}}$." An input voltage of the inverting amplifier IN1 becomes " V_{clamp1} " and an input voltage of the inverting amplifier IN12 becomes " V_{clamp2} " simultaneously, so that the two inverting amplifiers IN1 and IN2 are at the operation voltage at the same time.

This point in time is the comparison moment and, if the ramp signal is dropped a little, the signal is amplified by the gains of the inverting amplifiers IN1 and IN2 and V_{o} is dropped to a ground voltage level.

If V_{o} is dropped to the ground voltage level, the final value, which is continuously counted by the counter 510, is stored in the latch circuit 320. Accordingly, the latched value is a digital value from the unit pixel 120.

Finally, the latch enable signal Latch_EN is set to a logic low level in order to store the digital values in the latch circuit 320 until the data stored to latch 310 is transmitted to the digital controller (reference numeral 500 of FIG. 1).

The current of the comparator is consumed in the inverting amplifiers IN1 and IN2 only when the comparison is carried out so that there is little static current and it is possible to reduce the power consumption sharply. Also, because the comparator stores the reset level in the capacitor C3 in the analog signal level, only one ramp signal is required to obtain the digital signal corresponding to the input analog signal with the simple digital control algorithm and operations used in the CMOS image sensor. Further, because it is not necessary to store the digital value corresponding to the reset level of the CMOS image sensor, the entire size of the memories can be reduced by half.

As apparent from the above, the disclosed comparator can reduce the fixed pattern noise, such as the offset voltage, in the CMOS image sensor by considerably removing the offset voltage that exist between pixels using the analog correlated double sampling. The comparator can be made by a simple circuit design without a subtractor because only one ramp signal is used to obtain the digital value. Also, the ramp signal generator for the comparison can have a simple structure so that the chip size of the CMOS image sensor using the disclosed analog correlated double sampling is smaller than others using the digital correlated double sampling. Further, the disclosed apparatus may be employed in other integration circuits in which a low-voltage operation is required to reduce a power consumption or it is necessary to remove the offset value to obtain an exact digital value.

The comparator may have a simple structure that connects, in series, signal processing stages to process input data and the ramp signal. Further, the disclosed device may include a CMOS inverter with a low-operation voltage and a chopper type voltage comparator. Because the chopper type voltage comparator uses an inverter as a voltage amplifier, which consumes the current only when the comparison of inputs is carried out, the disclosed device can reduce the power consumption thereof.

The disclosure introduces a new architecture of CMOS image sensor that has many advantages over the previous one. Such advantages include smaller size of chip area, reduced power consumption, reduced FPN and possibility of implementing analog gamma correction. The disclosed CMOS image sensor is capable of reducing power consumption and a size of chip through the reduction of an offset voltage efficiently therein.

Although certain apparatus constructed in accordance with the teachings of the invention have been described herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers all embodiments of the teachings of the invention fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.

What is claimed is:

1. A CMOS image sensor comprising:

an image capturer for capturing an image and producing an analog image signal from an object;

an analog-to-digital converter for converting the analog image signal to a digital value using a ramp signal, wherein the analog-to-digital converter includes:

a) a chopper-type comparator receiving the analog image signal and the ramp signal; and

b) a capacitor for receiving a start voltage of the ramp signal and charging a voltage level corresponding the start voltage of the ramp signal in a reset mode and for receiving a down-ramping signal of the ramp signal in a count mode in order to remove a device offset voltage; and

a ramp signal generator providing the ramp signal to the analog-to-digital converter.

2. The CMOS image sensor as recited in claim 1, further comprising a latch circuit for storing the digital value converted by the analog-to-digital converter, wherein the latch circuit has a plurality of buffer lines to store the digital value only, wherein the capacitor is a first capacitor and wherein the chopper-type comparator comprises: a plurality of capacitors and switches; and at least two inverting amplifiers, wherein the switches are controlled by a digital controller in the CMOS image sensor.

3. The CMOS image sensor as recited in claim 1, wherein the capacitor is a first capacitor and wherein the chopper-type comparator comprises:

a plurality of capacitors and switches; and

at least two inverting amplifiers, wherein the switches are controlled by a digital controller in the CMOS image sensor.

4. The CMOS image sensor as recited in claim 3, wherein the chopper-type comparator comprises:

a first switch connected to the image capturer;

a second switch connected to the ramp signal generator;

a second capacitor connected to the first switch, wherein the first capacitor is connected between the first switch and the second switch;

a first inverting amplifier connected to the second capacitor;

a third switch connected between input and output terminals of the first inverting amplifier;

a third capacitor connected to the first inverting amplifier;

a fourth switch connected between input and output terminals of [the] a second inverting amplifier; and

[a] wherein the second inverting amplifier is connected to the third capacitor and the latch circuit to store the digital value.

5. The CMOS image sensor as recited in claim 4, wherein the first switch is turned on in response to a control signal from the digital controller in the [rest] reset mode and in a charge transfer mode in which photocharges are transferred to the analog-to-digital converter.

6. The CMOS image sensor as recited in claim 5, wherein the first, third, and fourth switches are turned on in response to a control signal from the digital controller in the charge transfer mode in which photocharges are transferred to the analog-to-digital converter.

7. A method for removing a device offset voltage in a CMOS image sensor, the method comprising:

charging a start voltage of a ramp signal in a capacitor and simultaneously charging a [rest] reset voltage of an image capturer in a chopper-type comparator in a reset mode;

providing to the chopper-type comparator an analog image signal from the image capturer in a charge transfer mode; and

providing a down-ramping signal of the ramp signal to the chopper-type comparator in a count mode.

8. A CMOS image sensor comprising:

an image capturer including a plurality of pixel sensor circuits configured to provide analog signals in a reset mode and a read mode, wherein each pixel sensor circuit is further configured to provide a reset signal in the reset mode and a pixel output signal in the read mode, and wherein an offset signal is superimposed on the reset signal and the pixel output signal of each pixel sensor circuit;

a ramp signal generator configured to provide a ramp signal, wherein the ramp signal includes a ramp signal waveform beginning as a start signal;

a chopper circuit configured to receive the analog signals and the ramp signal, wherein the chopper circuit is further configured to generate a control signal to control operation of a logic component, and wherein the chopper circuit is further configured such that:

during the reset mode, the chopper circuit generates a reset mode signal corresponding to a difference between first and second signals, wherein the first signal includes the reset signal, wherein the second signal includes a sum of the offset signal and the start signal, and wherein the reset signal, offset signal, and start signal are sampled concurrently;

during the read mode, the chopper circuit generates a clamped logic level signal, wherein the chopper circuit further generates a read mode signal that corresponds to a difference between the pixel output signal and a third signal, and wherein the third signal includes a sum of the offset signal and the clamped logic level signal; and

during the read mode, the chopper circuit generates the control signal using a signal corresponding to a difference between the reset mode signal and the read mode signal.

9. The CMOS image sensor of claim 8, wherein the ramp signal waveform includes a down-ramping waveform.

10. The CMOS image sensor of claim 8, wherein the chopper circuit comprises:

a plurality of capacitors and switches; and

at least two inverting amplifiers, wherein the switches are configured to respond to control signals provided by a digital controller in the CMOS image sensor.

11. The CMOS image sensor of claim 10, wherein the chopper circuit further comprises:

a first switch configured to receive the analog signals from the image capturer;

a second switch configured to receive the ramp signal from the ramp signal generator;

a first capacitor connected between the first switch and the second switch;

a first inverting amplifier connected to the first capacitor;

a third switch connected between input and output terminals of the first inverting amplifier;

a second capacitor connected between the first switch and the input terminal of the first inverting amplifier;

a second inverting amplifier;

a third capacitor connected between the output terminal of the first inverting amplifier and an input terminal of the second inverting amplifier;

a fourth switch connected between input and output terminals of the second inverting amplifier;

wherein the output terminal of the second inverting amplifier is provided as the control signal from the chopper circuit.

12. The CMOS image sensor of claim 11, wherein the first, second, third, and fourth switches are configured to respond to control signals from the digital controller.

13. The CMOS image sensor of claim 8, further comprising a latch circuit configured to store a digital value of a digital counter if a difference between the reset mode signal and the read mode signal corresponds to a magnitude of the ramp signal waveform.

14. A method of compensating for an offset voltage of a pixel sensor in a CMOS image sensor, the method comprising:

providing a reset voltage from the pixel sensor during a reset mode, wherein the offset voltage is superimposed on the reset voltage;

providing a ramp voltage waveform beginning at a start voltage;

concurrently sampling the reset voltage, the offset voltage superimposed on the reset voltage, and the start voltage;

generating a reset mode voltage, wherein the reset mode voltage corresponds to a difference between first and second voltages, wherein the first voltage includes the reset voltage, and wherein the second voltage includes a sum of the offset voltage and the start voltage;

generating a clamped logic level voltage;

providing a pixel output voltage during a pixel sensor read mode, wherein the offset voltage is superimposed on the pixel output voltage;

generating a read mode voltage corresponding to a difference between the pixel output voltage and a third voltage, wherein the third voltage includes a sum of the offset voltage and the clamped logic level voltage; and

generating a control signal to a logic circuit, wherein the control signal corresponds to a difference between the reset mode voltage and the read mode voltage.

15. The method of claim 14, wherein said generating a reset mode voltage comprises:

configuring a capacitor to receive the reset voltage and the offset voltage at a first terminal; and

configuring the capacitor to receive the start signal at a second terminal.

16. A CMOS image sensor comprising: an image capturer including a plurality of pixel sensor circuits, wherein each pixel sensor circuit is configured to provide a reset signal in a reset mode and a pixel output signal in a read mode, and wherein an offset signal is superimposed on the reset signal and the pixel output signal of each pixel sensor circuit during the reset mode and read mode, respectively;

a ramp signal generator configured to provide a ramp signal, wherein the ramp signal includes a ramp signal waveform beginning as a start signal;

a chopper circuit configured to receive the reset signal with the superimposed offset signal from a given pixel sensor circuit during the reset mode and the pixel output signal with the superimposed offset signal from the given pixel sensor circuit during the read mode, wherein the chopper circuit is configured to receive the ramp signal from the ramp signal generator, and wherein the chopper circuit is configured to generate a control signal to control operation of a logic component;

wherein, during the reset mode, the chopper circuit is configured to generate a reset mode signal across a charging element by concurrently sampling the reset signal and the offset signal from the given pixel sensor circuit and the start signal from the ramp signal generator, wherein the reset mode signal corresponds to a difference between first and second signals, and wherein the first signal includes the reset signal, and wherein the second signal includes a sum of the offset signal and the start signal;

wherein, during the read mode, the chopper circuit is further configured to generate a clamped logic level signal and is further configured to generate a read mode signal that corresponds to a difference between the pixel output signal and a third signal, wherein the third sig-

11

nal includes a sum of the offset signal and the clamped logic level signal; and

wherein, during the read mode, the chopper circuit is further configured to generate the control signal using a signal corresponding to a difference between the reset mode signal and the read mode signal.

17. *The CMOS image sensor of claim 16, wherein the charging element comprises a capacitor connected between first and second inputs of the chopper circuit.*

18. *A CMOS image sensor comprising:*

an image capturer having a plurality of pixel sensor circuits, wherein each pixel sensor circuit is configured to provide an analog signal at its output;

a ramp signal generator configured to provide a ramp signal;

a chopper circuit configured to receive the analog signal from a given pixel sensor circuit and to receive the ramp signal from the ramp signal generator, wherein the chopper circuit is configured to:

provide a logic level control signal to control operation of a logic component, wherein the logic level control signal is used to generate a digital signal corre-

12

sponding to a magnitude of the analog signal provided from the output of the given pixel sensor circuit; and

store a signal across a charging element, wherein the signal stored across the charging element corresponds to a difference between the analog signal from the given pixel sensor circuit and the ramp signal from the ramp signal generator, wherein the analog signal from the given pixel sensor circuit and the ramp signal from the ramp signal generator are concurrently sampled to store the signal across the charging element during a mode of at least two modes of operation of the given pixel sensor circuit to generate the logic level control signal to the logic component, wherein the charging element comprises a capacitor connected between first and second inputs of the chopper circuit.

19. *The CMOS image sensor of claim 18, wherein the at least two modes of operation comprise a reset mode in which a reset signal is provided from the output of the given pixel sensor circuit and a read mode in which a pixel output signal is provided from the output of the given pixel sensor circuit.*

* * * * *