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(54) **SEAL RING STRUCTURE FOR RADIO FREQUENCY INTEGRATED CIRCUITS**

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Related U.S. Patent Documents

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Issued: **Nov. 22, 2005**
Appl. No.: **10/370,345**
Filed: **Feb. 19, 2003**

U.S. Applications:

(62) Division of application No. 09/933,965, filed on Aug. 22, 2001, now Pat. No. 6,537,849.

(51) **Int. Cl.**
H01L 23/552 (2006.01)
H01L 21/00 (2006.01)

(52) **U.S. Cl.** **257/660**; 257/659; 438/64

(58) **Field of Classification Search** 257/659–660; 438/64, 106, 637
See application file for complete search history.

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6,028,497 A * 2/2000 Allen et al. 333/246
6,105,226 A * 8/2000 Gore et al. 29/25.35
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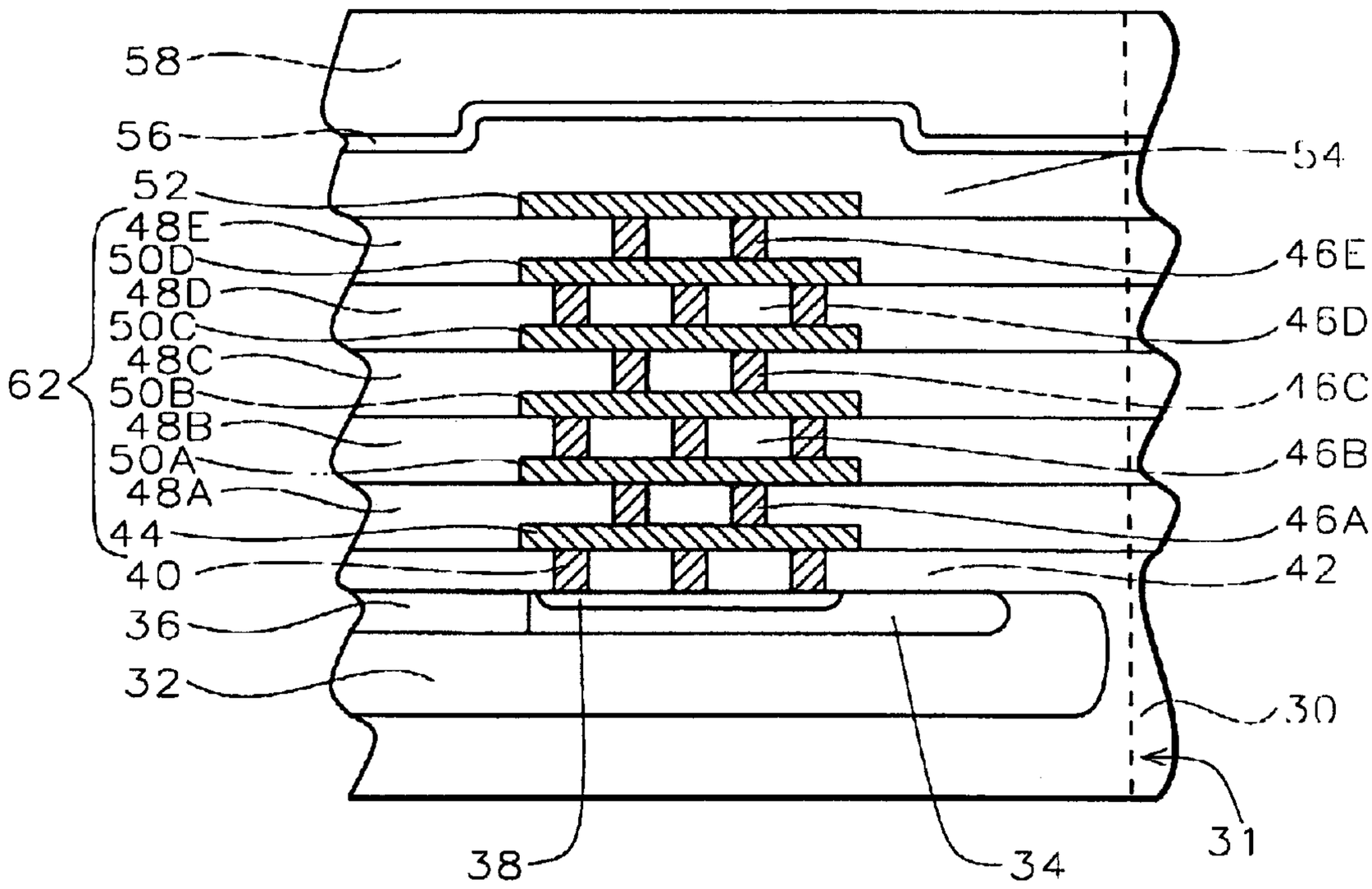
(57) **ABSTRACT**

Described is a method wherein a seal ring is formed by patterning multiple layers each comprised of a dielectric layer with conductive vias covered by a conductive layer. Discontinuities are made in the seal ring encapsulating an integrated circuit. There are no overlaps between different sections of the seal ring thereby reducing coupling of high frequency circuits in the seal ring structures. In addition, the distance between signal pads, circuits and the seal ring are enlarged. Electrical connection is made between deep N-wells and the seal ring. This encapsulates the integrated circuit substrate and reduces signal coupling with the substrate.

19 Claims, 2 Drawing Sheets



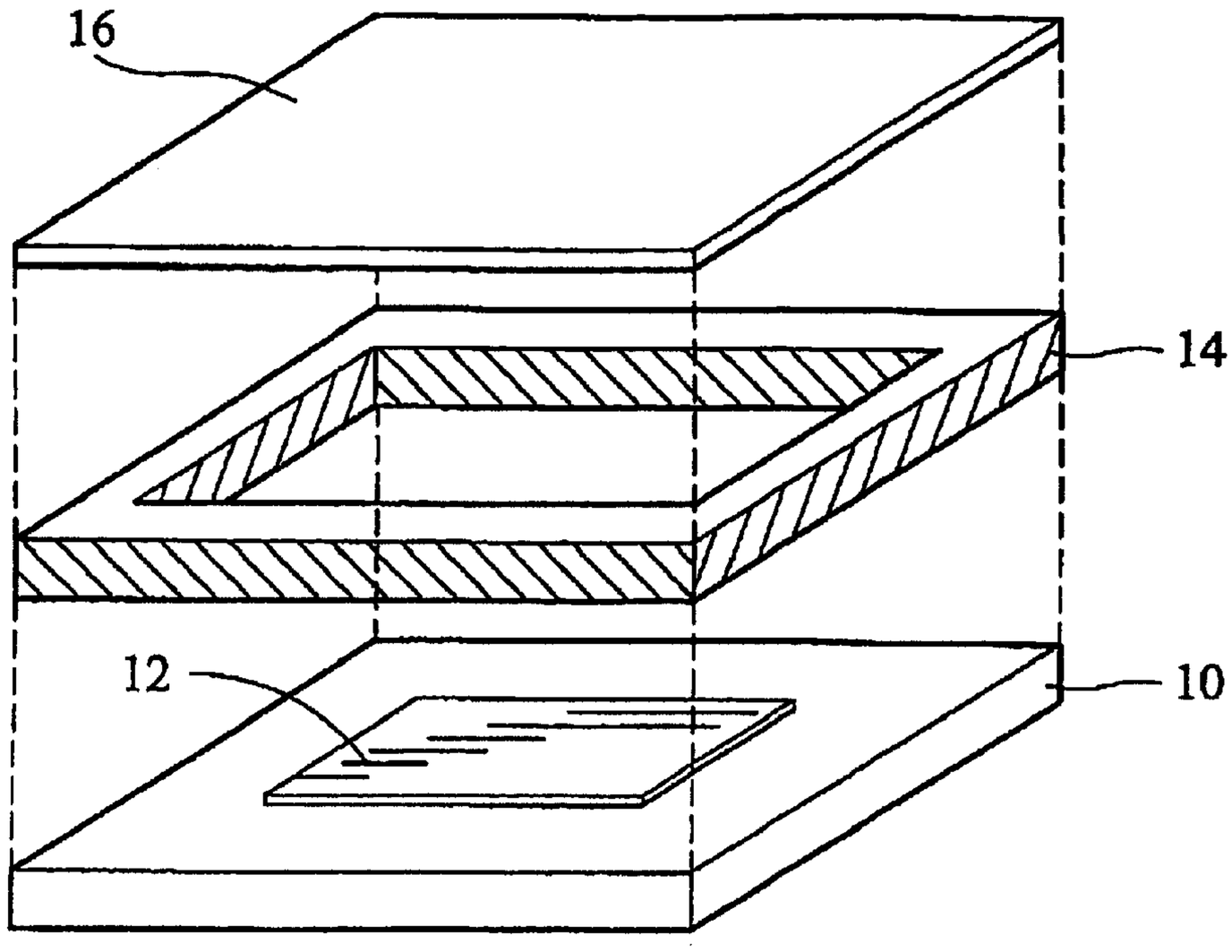


FIG. 1 (PRIOR ART)

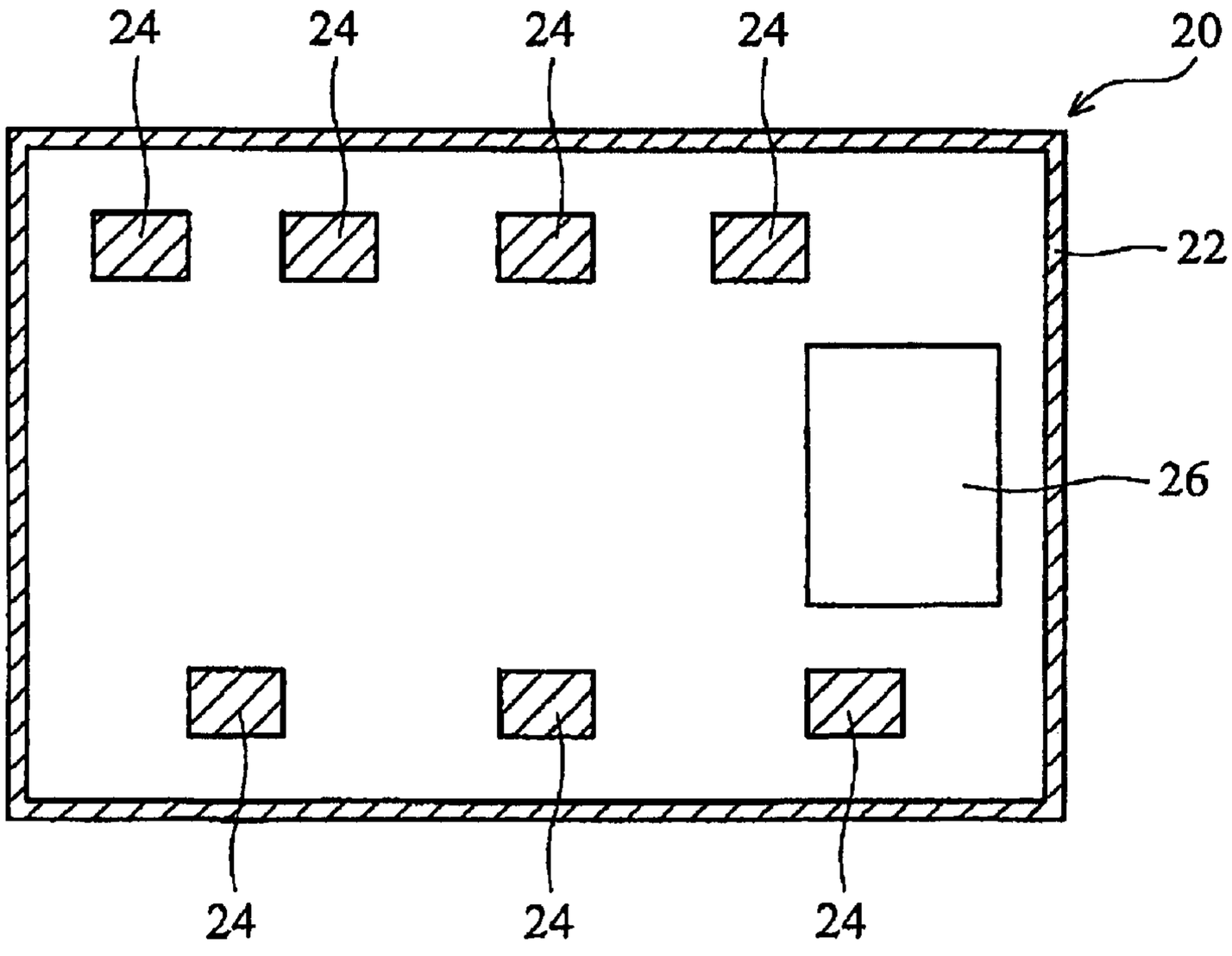
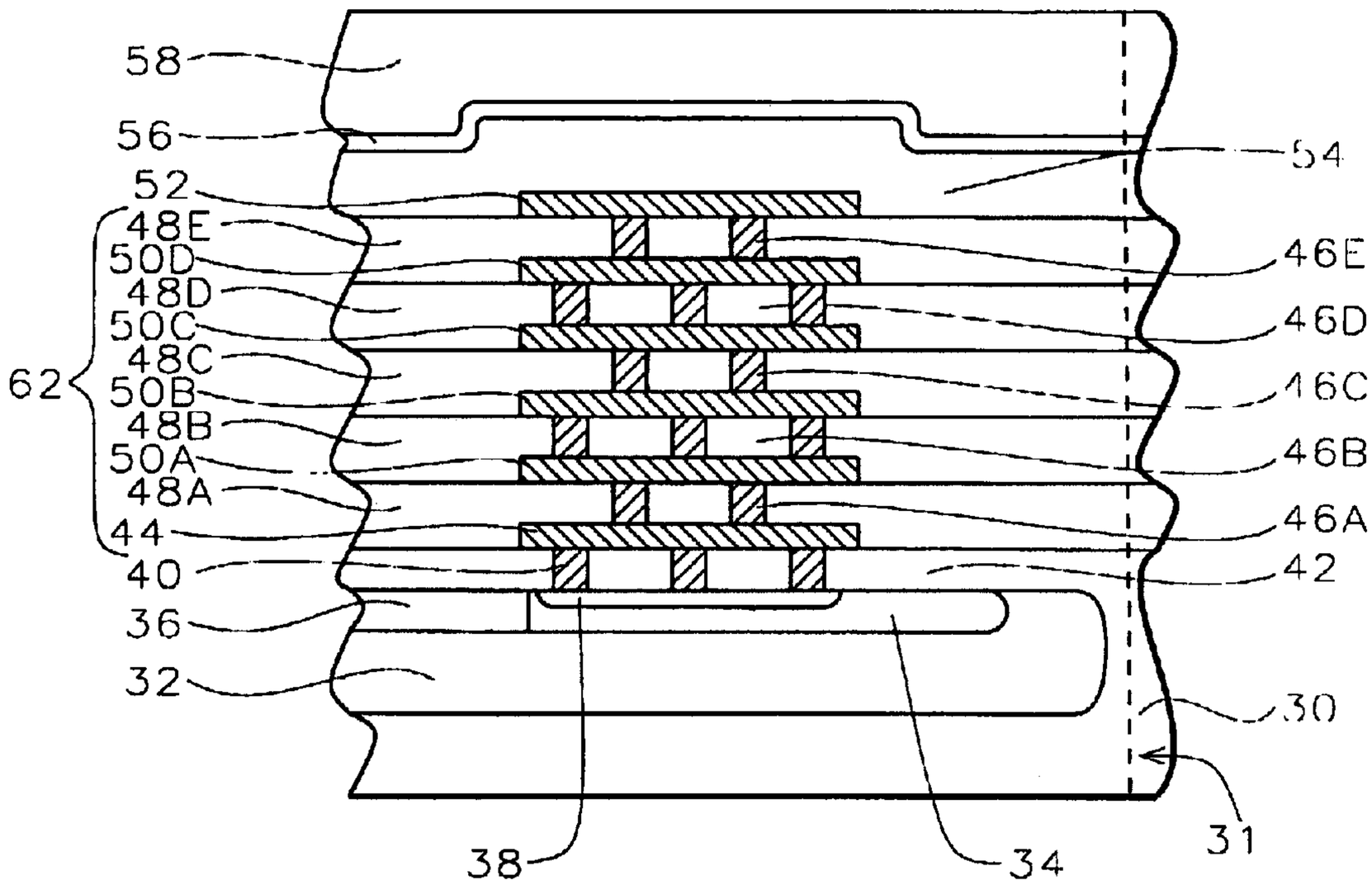


FIG. 2 (PRIOR ART)


58
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48E
50D
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46E
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FIG. 3

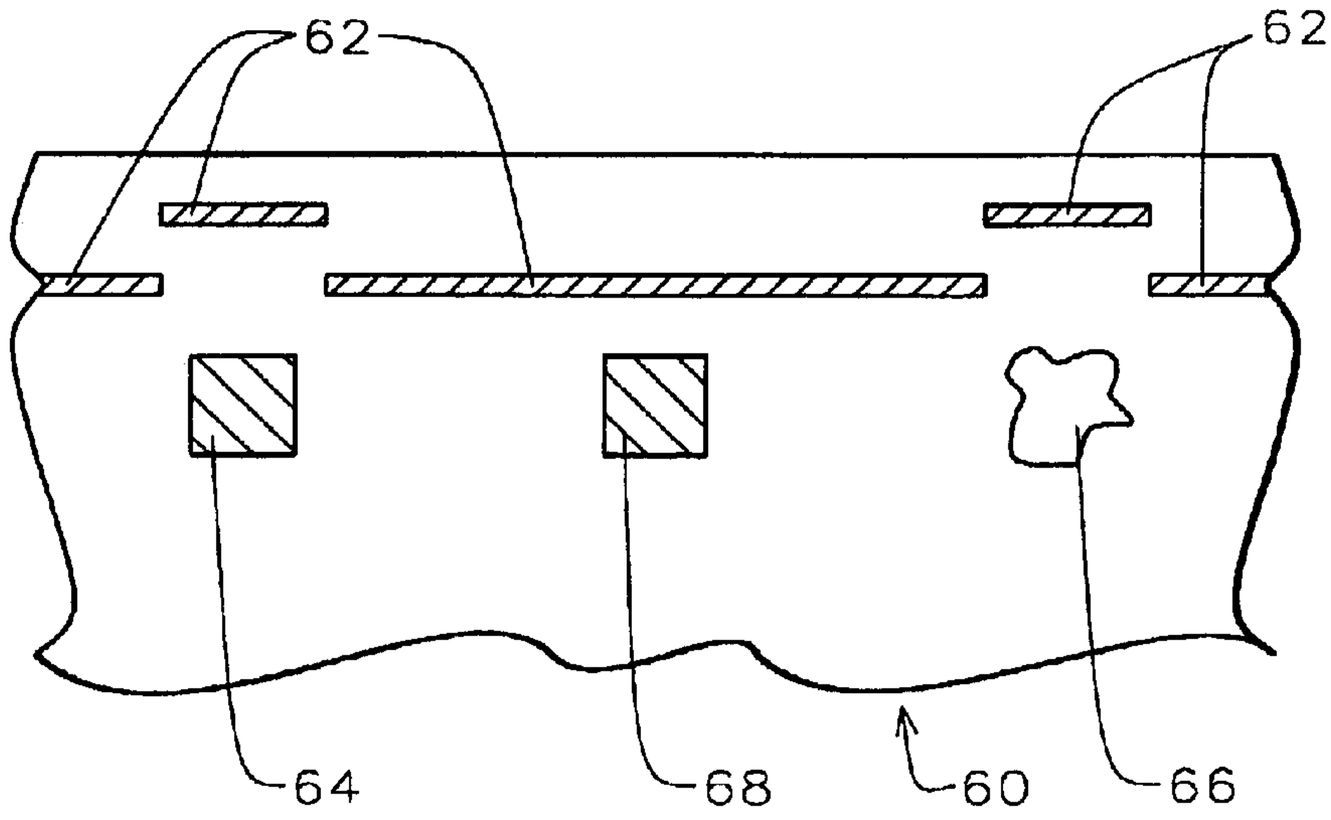
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FIG. 4

SEAL RING STRUCTURE FOR RADIO FREQUENCY INTEGRATED CIRCUITS

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

This is a division of U.S. patent application Ser. No. 09/933,965, filing date Aug. 22, 2001 now U.S. Pat. No. 6,537,849, Seal Ring Structure For Radio Frequency Integrated Circuits, assigned to the same assignee as the present invention.

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention generally relates to an encapsulation process used in semiconductor manufacturing and, more particularly, to a method of encapsulation that improves isolation of radio frequency (RF) signals in the fabrication of integrated circuits.

(2) Description of Prior Art

As integrated circuit (IC) speeds increase, seal rings have been incorporated into the device encapsulation in order to reduce radio frequency (RF) interference and signal cross coupling. The seal ring is grounded or connected to a signal ground such as a DC supply line to eliminate the effect of interference. The seal ring may be part of the device packaging scheme; in this case a conductive lid is typically connected to the seal ring. Specific to this invention, the seal ring may be incorporated into the IC substrate fabrication and may include a conductive covering over the substrate.

FIG. **1** shows in exploded view a method where the seal ring is incorporated into the device package. A substrate **10** made of ceramic material, for example, has an integrated circuit die **12** attached by a conductive epoxy or eutectic bond. The die **12** is electrically connected to the substrate **10** using bond wires (not shown). A conductive seal ring **14** is attached and grounded by internal connections (not shown). The package is scaled using a lid **16** to prevent penetration by contaminants and moisture.

FIG. **2** shows a top view of an IC die **20** where a seal ring **22** is incorporated. A plurality of bonding pads **24** are shown which may be either signal inputs or outputs, or DC supply and ground. A portion of the circuit containing RF circuits **26** is shown. One problem with this method is that signals from the bonding pads **24** may be capacitively coupled to the seal ring **22**. This may result in unwanted signal interference appearing at one of the signal input or output bonding pads **24**. In addition, interference may be coupled to the RF circuit **26** resulting in signal distortion.

Other approaches employing seal rings exist. U.S. Pat. No. 5,717,245 to Pedder teaches a system using a dielectric multi-layer substrate where RF interference is reduced by grounding certain areas and encapsulating the substrate within a conductive seal ring. U.S. Pat. No. 6,028,497 to Allen et al. teaches a system where RF signals are passed through a network of holes in the base plate of the module. The holes each consist of a conductive pin surrounded by, but electrically isolated from, a conductive cylindrical shroud, thereby forming a coaxial connection. A compartmentalized seal ring attached to the top of the module segregates different circuit areas of the module. U.S. Pat. Nos. 5,864,092 and 6,105,226 to Gore et al. teach methods employing a leadless chip carrier package where a grounded conductor protrudes between input and output signal pads thereby preventing interference. U.S. Pat. No. 5,998,245 to

Yu teaches a method where ESD protection is incorporated into a seal ring structure on an IC die. U.S. Pat. No. 6,028,347 to Sauber et al. teaches a method where a portion of the seal ring is formed in trenches in the semiconductor surface. An encapsulating plastic covering over the surface fills the trenches thereby preventing movement of the cover and reducing stresses due to thermal expansion.

SUMMARY OF THE INVENTION

A principal object of the present invention is to provide a method that reduces cross coupling between circuits and pads in an integrated circuit.

Another object of the present invention is to provide a method that prevents cross coupling between circuits caused by the seal ring in an integrated circuit.

These objects are achieved by using a method where a seal ring is formed by stacking interconnected metal layers along the perimeter of the integrated circuit (IC). Discontinuities are formed in the seal ring encapsulating different sections of the IC. There are no overlaps between discontinuities in the seal ring thus isolating signals utilized on different sub-circuits within the IC. To further reduce unwanted signal coupling, the distances between the seal ring and both signal pads and circuits are enlarged. Electrical connection is made between the deep N-well and the seal ring to encapsulate the substrate and minimized signal coupling to the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

FIG. **1** schematically illustrating an exploded view cross-sectional representation of a prior art example employing seal rings;

FIG. **2** schematically illustrating a top view cross-sectional representation of a prior art example employing seal rings;

FIG. **3** schematically illustrating in cross-sectional representation a preferred embodiment of the present invention;

FIG. **4** schematically illustrating a top view of a preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention uses a method where a seal ring is formed by stacking interconnected conducting layers along the perimeter of the integrated circuit (IC). The embodiment provided herein describes a method of creating the seal ring and connecting the seal ring to the deep N-well.

Refer to FIG. **3**, depicting in cross-section a portion of an integrated circuit die where the seal ring is formed. A substrate **30** is provided. The substrate layer **30** may contain underlying layers, devices, junctions, and other features (not shown) formed during prior process steps. The cut line **31** represents the outer edge of the IC die of interest. During subsequent processing, the die would be separated from an adjacent IC die (not shown) on the substrate **30** along that cut line **31**. A deep N-well region **32** is formed as is conventional in the art. A p+source/drain (S/D) region **34** formed by conventional techniques is isolated from the remainder of the underlying circuitry (not shown) by shallow trench isolation **36**. A silicide **38** is formed over the S/D region **34** providing a low resistance connection to the S/D region **34**. Contacts **40** through first interlevel dielectric layer **42** make electrical connection to the first conductive layer **44**. A plurality of via

layers **46**a–**46**e through dielectric layers **48**a–**48**e, respectively, make electrical contact to a plurality of conductive layers **44** and **50**a–**50**d, respectively. A top conductive layer **52** is then provided. This is followed by a passivation layer **54** composed of USG oxide, for example, deposited by chemical vapor deposition (CVD), for example, to a thickness of between about 8000 Å and 20,000 Å. This completes the seal ring **62** composed of the conductive layers **44**, **50**a–**50**d and **52** and via layers **46**a–**46**e. The seal ring **62** makes electrical contact to the deep N-well **32** via contact **40**, silicide **38** and S/D region **34**. Typical widths of the seal ring **62** are between about 5 μm to 15 μm.

A nitride layer **56** composed of Si_3N_4 is then conformally deposited by CVD to a thickness of between about 2000 Å and 10,000 Å. The CVD process provides excellent step coverage along the sidewalk of the structure. A polyimide layer **58** is then deposited by spin-on techniques to a thickness of between about 2 μm and 6 μm.

When the completed IC is electrically connected in a circuit, the deep N-well **32** is electrically connected to a positive supply voltage (Vdd) thereby holding the deep N-well **32** and seal ring **62** at signal ground. This minimizes signal coupling within the substrate and the S/D region.

Referring now to FIG. **4** showing a top view of a portion of an integrated circuit **60**, a portion of seal ring **62** and an important point of the present invention is depicted. Notice that there are discontinuities in the seal ring **62**. For example, the spacing between adjacent sections of the seal ring **62** is between about 10 and 30 microns. More specifically, the seal ring **62** is spaced further from signal pad **64** and radio frequency circuit **66** than from signal ground pad **68**. Typical distances between the seal ring and signal ground pads would be between about 10 μm and 30 μm, while distances between the seal ring and signal pins would be between about 20 μm and 50 μm. It should be noted that both DC ground pins and fixed DC voltage supply pins are effectively signal grounds. The additional spacing between the seal ring **62** and signal pads **64** and radio frequency circuits **66** reduces the coupling between distinct circuits. The breaks in the seal ring **62** prevent interference from being propagated to other sub-circuits within the integrated circuit. It should also be noted that preferably, the seal ring **62** breaks do not overlap along the perimeter of the integrated circuit **60**; this further reduces the potential for signal interference. If the seal ring **60** breaks must overlap (not preferred), then the distance between the different portions of the seal ring must be increased.

The present invention is achieved by using a method where a seal ring is formed by stacking interconnected conductive layers along the perimeter of the IC. Discontinuities formed in the seal ring encapsulating different sections of the IC isolate signals utilized on different sub-circuits within the IC. To further reduce unwanted signal coupling, the distances between the seal ring and both signal pads and circuits are enlarged. Electrical connection made between the deep N-well and the seal ring encapsulates the substrate and minimizes signal coupling to the substrate.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A seal ring for an integrated circuit wherein said seal ring surrounds an active region of the integrated circuit and comprises alternate first and second sections, the first sections are discontinuous and spaced from the active region to form an inner perimeter for surrounding said active region, and the second sections are discontinuous and spaced from the active region to form an outer perimeter for surrounding said active region, said outer perimeter surrounding said inner perimeter.

2. The seal ring according to claim **1** wherein said integrated circuit further comprises signal pads, ground pads and radio frequency circuits.

3. The seal ring according to claim **2** wherein a spacing between said seal ring and said signal pads or said radio frequency circuits is greater than a spacing between said seal ring and ground pads.

4. The seal ring according to claim **3** wherein the spacing between said seal ring and said signal pads or said radio frequency circuits is between about 20 and 50 microns.

5. The seal ring according to claim **3** wherein the spacing between said seal ring and said ground pads is between about 10 and 30 microns.

6. The seal ring according to claim **1** wherein a spacing between said first and second sections is between about 10 and 30 microns.

7. The seal ring according to claim **1** wherein a width of said seal ring is between about 5 and 15 microns.

8. The seal ring according to claim **1** wherein said active area is a semiconductor device comprising at least one N-well.

9. The seal ring according to claim **8** wherein said seal ring is electrically connected to said N-well via a contact, a silicide and a source/drain region of said integrated circuit.

10. The seal ring according to claim **8** wherein said N-well is electrically connected to a positive supply voltage (Vdd).

11. The seal ring according to claim **1** wherein the first sections do not overlap the second sections.

12. A semiconductor device with a seal ring for an integrated circuit, comprising:

alternate first and second sections of the seal ring, discontinuous and spaced apart from an active region of the integrated circuit; wherein the first and second sections forms a separate inner perimeter and an outer perimeter for surrounding the active region.

13. The semiconductor device according to claim 12 wherein said integrated circuit further comprises first pads, second pads and circuits.

14. The semiconductor device according to claim 13 wherein a spacing between said seal ring and said first pads or said circuits is greater than a spacing between said seal ring and said second pads.

15. The semiconductor device according to claim 12 wherein said first pads, second pads and circuits respectively comprises signal pads, ground pads and radio frequency circuits.

16. The semiconductor device according to claim 15 wherein the spacing between said seal ring and said signal pads or said radio frequency circuits is between about 20 and 50 microns.

17. The semiconductor device according to claim 16 wherein the spacing between said seal ring and said ground pads is between about 10 and 30 microns.

18. The semiconductor device according to claim 12 wherein said active area is a semiconductor device comprising at least one N-well, and said seal ring is electrically connected to said N-well via a contact, a silicide and a source/drain region of said integrated circuit.

19. The semiconductor device according to claim 12 wherein the first sections do not overlap the second sections.

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