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(54) **EXTENDED CARDBUS/PC CARD CONTROLLER WITH SPLIT-BRIDGE TECHNOLOGY**

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See application file for complete search history.

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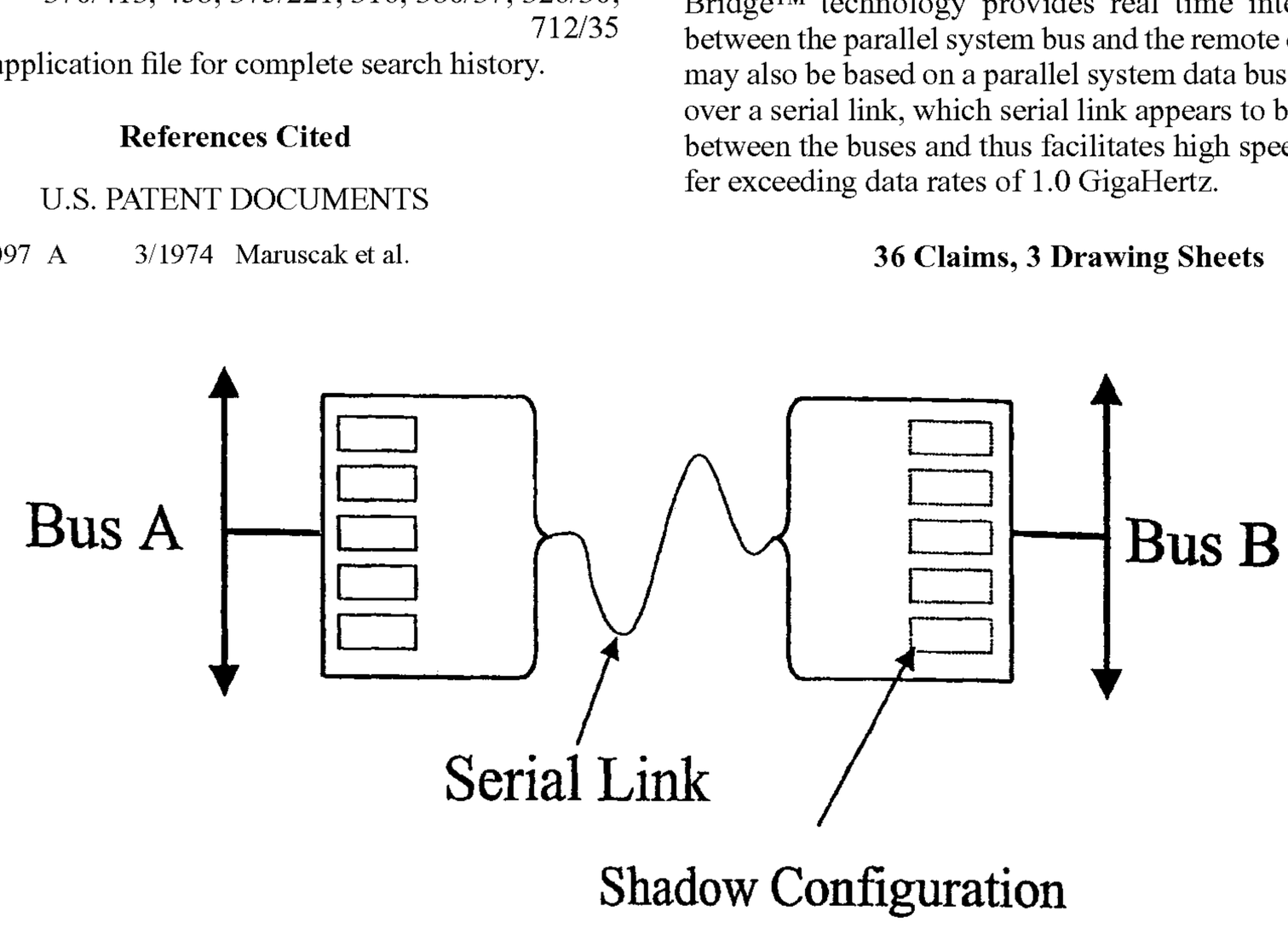
Primary Examiner—Glenn A Auve

(57) **ABSTRACT**

An improved extended cardbus/PC card controller (**20**) incorporating proprietary Split-Bridge™ high speed serial communication technology for interconnecting a conventional parallel system bus via a high speed serial link with a remote peripheral device. The extend cardbus/PC card controller is adapted to interface the parallel system bus, which may be PCI, PCMCIA, integrated, or some other parallel I/O bus architecture, with peripheral devices via PC cards, and now optionally via a high speed serial link using the proprietary serial Split-Bridge™ technology. The serial Split-Bridge™ technology provides real time interconnection between the parallel system bus and the remote device which may also be based on a parallel system data bus architecture, over a serial link, which serial link appears to be transparent between the buses and thus facilitates high speed data transfer exceeding data rates of 1.0 GigaHertz.

36 Claims, 3 Drawing Sheets



Split-Bridge

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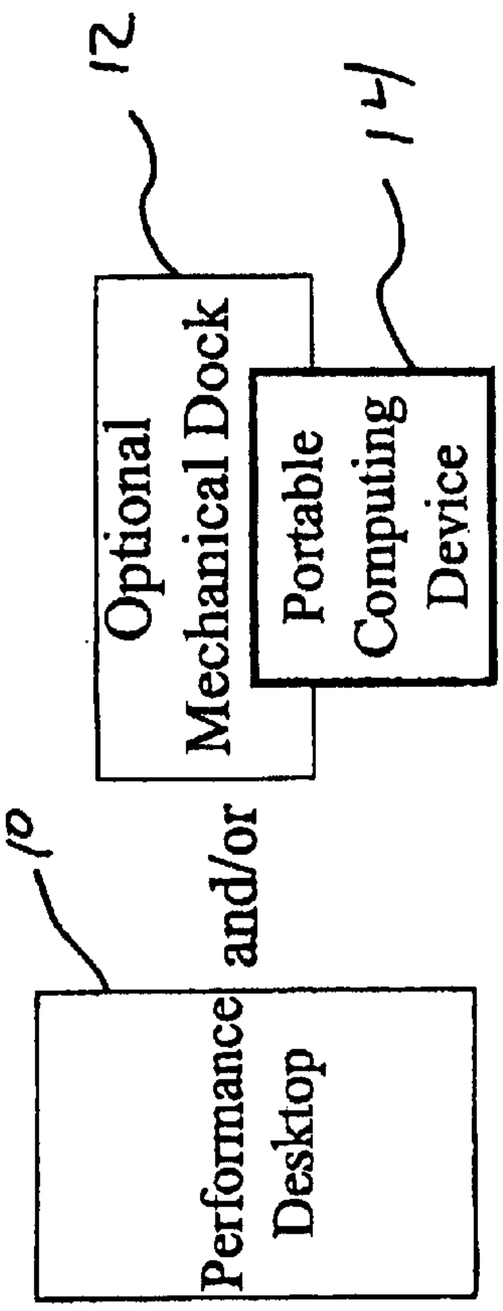


FIGURE 1
(PRIOR ART)

Figure 2
(PRIOR ART)

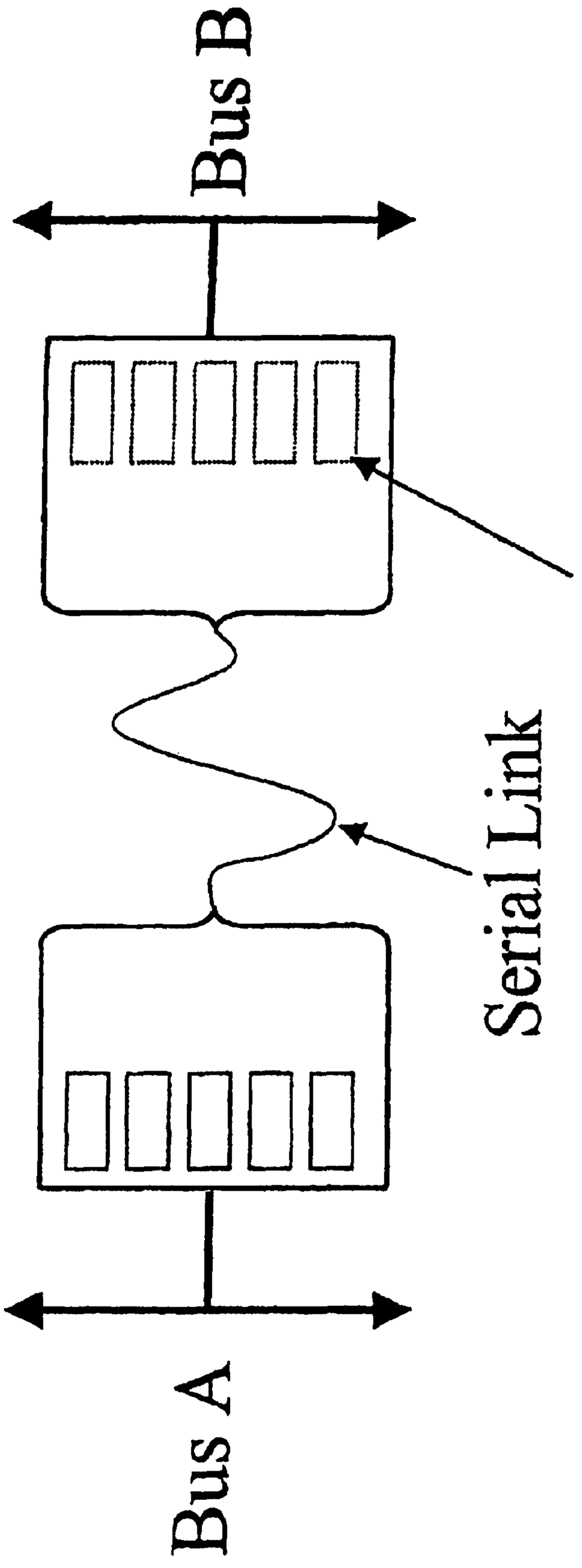


FIGURE 3

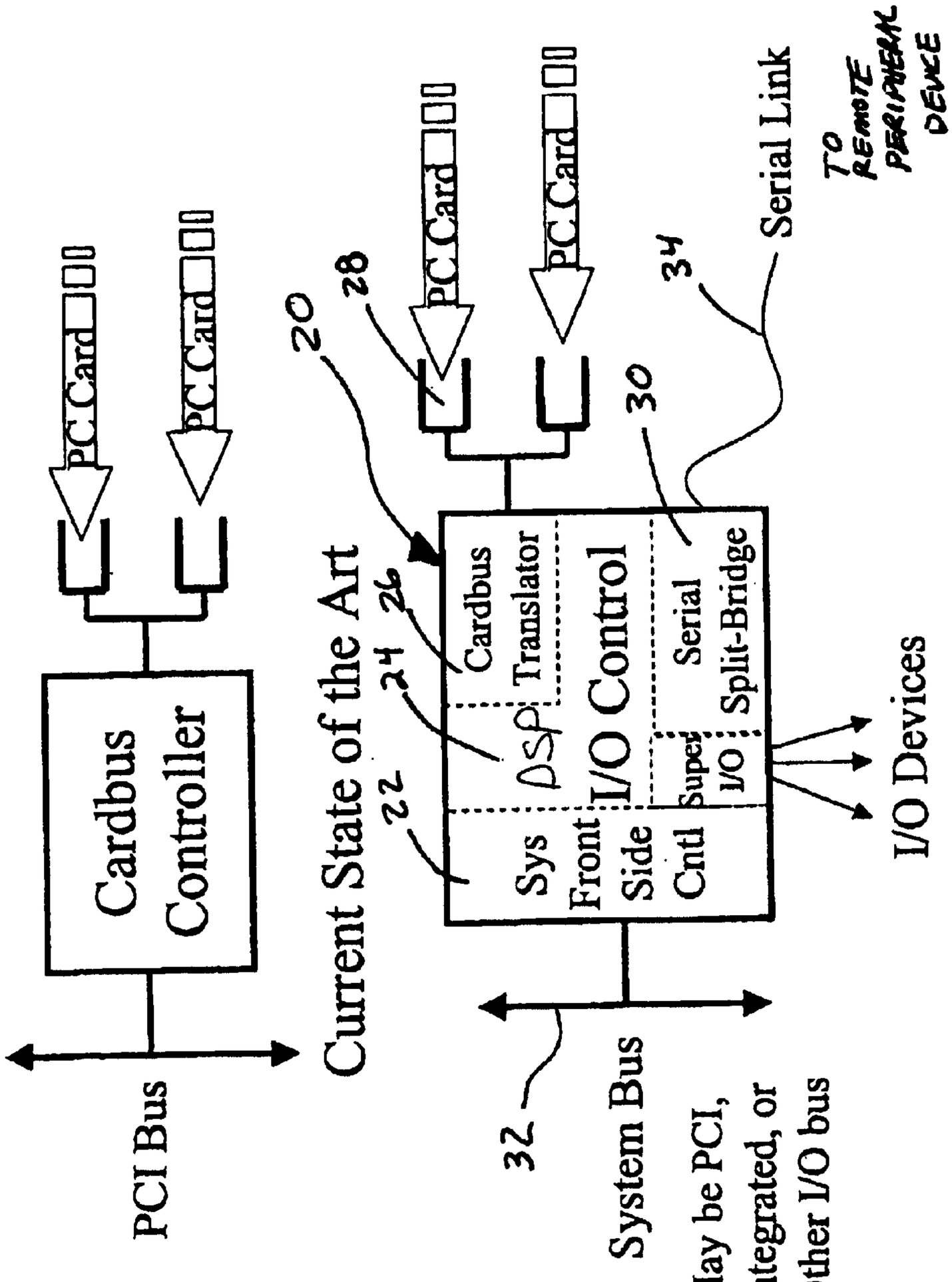


Figure 4

Figure 5

Extended Cardbus/PC Card Co

EXTENDED CARDBUS/PC CARD CONTROLLER WITH SPLIT-BRIDGE TECHNOLOGY

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims priority of provisional patent application serial No. 60/198,317 entitled Split-Bridge Systems, Applications and Methods of Use filed on Apr. 19, 2000, as well as co-pending and commonly assigned patent applications Ser. No. 09/130,057 filed Jun. 6, 1998, Ser. No. 09/130,058 filed Jun. 6, 1998, Ser. No. 08/679,131 now issued as U.S. Pat. No. 5,941,965; and co-pending patent application Ser. No. 09/559,678, entitled Modular Computer Based on Universal Connectivity Station, the teachings of each incorporated herein by reference.

FIELD OF THE INVENTION

The present invention is generally related to data processing systems, and more particularly to computer systems having at least one host processor and connectable to a plurality of peripherals devices including notebook computers, storage devices, displays, keyboards, mouse's and so forth.

BACKGROUND OF THE INVENTION

Computer systems today are powerful, but are rendered limited in adapting to changing computing environments. The PCI bus is pervasive in the industry, but as a parallel data bus is not easily bridged to other PCI based devices. Full bridges are known, such as used in traditional laptop computer/docking stations. However, separating the laptop computer from the docking station a significant distance has not been possible. Moreover, the processing power of computer systems has been resident within the traditional computer used by the user because the microprocessor had to be directly connected to and resident on the PCI motherboard. Thus, upgrading processing power usually meant significant costs and/or replacing the computer system.

PCI

The PCI bus is primarily a wide multiplexed address and data bus that provides support for everything from a single data word for every address to very long bursts of data words for a single address, with the implication being that burst data is intended for sequential addresses. Clearly the highest performance of the PCI bus comes from the bursts of data, however most PCI devices require reasonable performance for even the smallest single data word operations. Many PCI devices utilize only the single data mode for their transfers. In addition, starting with the implementation of the PCI 2.1 version of the specification, there has been at least pseudo isochronous behavior demanded from the bus placing limits on an individual device's utilization of the bus, thus virtually guaranteeing every device gets a dedicated segment of time on a very regular interval and within a relatively short time period. The fundamental reason behind such operation of the PCI bus is to enable such things as real time audio and video data streams to be mixed with other operations on the bus without introducing major conflicts or interruption of data output. Imagine spoken words being broken into small unconnected pieces and you get the picture. Prior to PCI 2.1 these artifacts could and did occur because devices could get

on the bus and hold it for indefinite periods of time. Before modification of the spec for version 2.1, there really was no way to guarantee performance of devices on the bus, or to guarantee time slot intervals when devices would get on the bus. Purists may argue that PCI is still theoretically not an isochronous bus, but as in most things in PC engineering, it is close enough.

Traditional High Speed Serial

Typical high speed serial bus operation on the other hand allows the possibility of all sizes of data transfers across the bus like PCI, but it certainly favors the very long bursts of data unlike PCI. The typical operation of a serial bus includes an extensive header of information for every data transaction on the bus much like Ethernet, which requires on the order of 68 bytes of header of information for every data transaction regardless of length. In other words, every data transaction on Ethernet would have to include 68 bytes of data along with the header information just to approach 50% utilization of the bus. As it turns out Ethernet also requires some guaranteed dead time between operations to "mostly" prevent collisions from other Ethernet devices on the widely disperse bus, and that dead time further reduces the average performance.

The typical protocol for a serial bus is much the same as Ethernet with often much longer header information. Virtually all existing serial bus protocol implementations are very general and every block of data comes with everything needed to completely identify it. FiberChannel (FC) has such a robust protocol that virtually all other serial protocols can be transmitted across FC completely embedded within the FC protocol, sort of like including the complete family history along with object size, physical location within the room, room measurements, room number, street address, city, zip code, country, planet, galaxy, universe, . . . etc. and of course all the same information about the destination location as well, even if all you want to do is move the object to the other side of the same room. Small transfers across all of these protocols, while possible, are extremely expensive from a bandwidth point of view. Of course the possibility of isochronous operation on the more general serial bus is not very reasonable.

Recreating High Speed Serial for PCI

In creating the proprietary Split-Bridge™ technology, Mobility electronics of Phoenix, Ariz., the present applicant, actually had to go back to the drawing board and design a far simpler serial protocol to allow a marriage to the PCI bus, because none of the existing implementations could coexist without substantial loss of performance. For a detailed discussion of Applicant's proprietary Split-Bridge™ technology, cross reference is made to Applicant's co-pending commonly assigned patent applications identified as Ser. No. 09/130,057 and 09/130,058 both filed Jun. 6, 1998, the teachings of each incorporated herein by reference. The Split-Bridge™ technology approach is essentially custom fit for PCI and very extensible to all the other peripheral bus protocols under discussion like PCIx, and LDT™ of AMD corporation. Split-Bridge™ technology fundamentals are a natural for extending anything that exists within a computer. It basically uses a single-byte of overhead for 32 bits of data and address—actually less when you consider that byte enables, which are not really "overhead", are included as well.

Armed with the far simpler protocol, all of the attributes of the PCI bus are preserved and made transparent across a high speed serial link at much higher effective bandwidth than any existing serial protocol. The net result is the liberation of a widely used general purpose bus, and the new found

ability to separate what were previously considered fundamental inseparable parts of a computer into separate locations. When the most technical reviewers grasp the magnitude of the invention, then the wheels start to turn and the discussions that follow open up a new wealth of opportunities. It now becomes reasonable to explore some of the old fundamentals, like peer-to-peer communication between computers that has been part of the basic PCI specification from the beginning, but never really feasible because of the physical limits of the bus prior to Split-Bridge™ technology. The simplified single-byte overhead also enables very efficient high speed communication between two computers and could easily be extended beyond PCI.

The proprietary Split-Bridge™ technology is clearly not "just another high speed link" and distinguishing features that make it different represent novel approaches to solving some long troublesome system architecture issues.

First of all is the splitting of a PCI bridge into two separate and distinct pieces. Conceptually, a PCI bridge was never intended to be resident in two separate modules or chips and no mechanism existed to allow the sharing of setup information across two separate and distinct devices. A PCI bridge requires a number of programmable registers that supply information to both ports of a typical device. For the purpose of the following discussion, the two ports are defined into a north and south segment of the complete bridge.

The north segment is typically the configuration port of choice and the south side merely takes the information from the registers on the north side and operates accordingly. The problem exists when the north and south portions are physically and spatially separated and none of the register information is available to the south side because all the registers are in the north chip. A typical system solution conceived by the applicant prior to the invention of Split-Bridge™ technology would have been to merely create a separate set of registers in the south chip for configuration of that port. However, merely creating a separate set of registers in the south port would still leave the set up of those registers to the initialization code of the operating system and hence would have required a change to the system software.

Split-Bridge™ technology, on the other hand, chose to make the physical splitting of the bridge into two separate and spaced devices "transparent" to the system software (in other words, no knowledge to the system software that two devices were in fact behaving as one bridge chip). In order to make the operations transparent, all accesses to the configuration space were encoded, serialized, and "echoed" across the serial link to a second set of relevant registers in the south side. Such transparent echo between halves of a PCI bridge or any other bus bridge is an innovation that significantly enhances the operation of the technology.

Secondly, the actual protocol in the Split-Bridge™ technology is quite unique and different from the typical state of the art for serial bus operations. Typically transfers are "packetized" into block transfers of variable length. The problem as it relates to PCI is that the complete length of a given transfer must be known before a transfer can start so the proper packet header may be sent.

Earlier attempts to accomplish anything similar to Split-Bridge™ technology failed because the PCI bus does not inherently know from one transaction to the next when, or if, a transfer will end or how long a block or burst of information will take. In essence the protocol for the parallel PCI bus (and all other parallel, and or real time busses for that matter) is incompatible with existing protocols for serial buses.

An innovative solution to the problem was to invent a protocol for the serial bus that more or less mimics the protocol on the PCI. With such an invention it is now possible to substantially improve the performance and real time operation here to for not possible with any existing serial bus protocol.

The 8 bit to 10 bit encoding of the data on the bus is not new, but follows existing published works. However, the direct sending of 32 bits of information along with the 4 bits of control or byte enables, along with an additional 4 bits of extension represents a 40 bit for every 36 bits of existing PCI data, address, and control or a flat 10% overhead regardless of the transfer size or duration, and this approach is new and revolutionary. Extending the 4 bit extension to 12 or more bits and include other functionality such as error correction or retransmit functionality is also within the scope of the Split-Bridge™ technology.

New Applications of the Split-Bridge™ Technology

Basic Split-Bridge™ technology was created for the purpose of allowing a low cost, high speed universal dock solution for all laptop computers and it has accomplished that task very well. By taking advantage of the standard and pervasive nature of the PCI bus in many other applications in computing, dramatic improvements in the price performance for other machines can be realized as well. The present invention is rendered possible due to the attributes of applicant's proprietary Split-Bridge™ technology.

SUMMARY OF THE INVENTION

The present invention achieves technical advantages as an improved extended cardbus/PC card controller incorporating the proprietary serial high speed Split-Bridge™ technology providing serial communications between a parallel system bus and a remote peripheral device. The improved controller includes the conventional system frontside controls, I/O controls, a cardbus translator having PC card slots adapted to receive a PCMCIA card or cards, and one end of the split bridge serial communication link comprising the proprietary serial Split-Bridge™ technology. The controller may further include super I/O circuitry for communicating remote I/O devices with the system bus as the super I/O devices become more readily available in the market.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates prior art computer systems depicted as a traditional performance desk top computer shown at **10**, and a portable computing device **12**, such as a notebook or laptop computer, mechanically coupled to mechanical docking station **14**;

FIG. **2** is a block diagram of a prior art bridge **16** used to couple two system computing buses, such as used between the portable computing device **12** and the mechanical docking station **14** shown in FIG. **1**;

FIG. **3** illustrates the proprietary Split-Bridge™ technology serial communication technology of the applicant enabling high speed serial communications within the modular computer system of the present invention;

FIG. **4** is a diagram of a conventional cardbus/PC controller; and

FIG. **5** is a block diagram of an improved extended cardbus/PC card controller having an integrated serial Split-Bridge™ interface according to the preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. **3**, there is depicted the proprietary Split-Bridge™ technology serial communications technology of

the present applicant, discussed in great detail in commonly assigned U.S. patent applications Ser. No. 09/130,057 filed Jun. 6, 1998, and Ser. No. 09/130,058 also filed Jun. 6, 1998 the teachings of which are incorporated herein by reference.

Applicant's Split-Bridge™ technology revolutionizes the status quo for computer systems. The Split-Bridge™ technology does not require the need for custom hardware or custom software to achieve full performance serial communication between devices, including devices having parallel data buses including the PCI bus. In fact, for each device in a modular computer system, the Split-Bridge™ technology appears just like a standard PCI bridge, and all software operating systems and device drivers already take such standard devices into consideration. By utilizing standard buses within each device operating within the modular computer system, each device does not require any additional support from the Operating System (OS) software. The modular computing system has simple elegance, allowing the PCI bus which is so pervasive in the computer industry, that possible applications of the initial PCI form of Split-Bridge™ technology are all most limitless.

Originally implemented in PCI, there is nothing fundamental that ties the Split-Bridge™ technology to PCI, and thus, the Split-Bridge™ technology can migrate as bus architectures grow and migrate. The 64 bit PCI is compatible with the Split-Bridge™ technology, as is future PCIx and/or LDT™ that are currently under consideration in the industry and which are straight forward transitions of the Split-Bridge™ technology. Implementations with other protocols or other possible and natural evolutions of the Split-Bridge™ technology.

Referring to FIG. **5**, there is depicted generally at **20** an improved card/bus controller according to the preferred embodiment of the present invention. Cardbus controller **20** is seen to have conventional system front side control circuitry **22**, input/output (I/O) control circuitry **24** a cardbus translator circuitry **26** adapted to couple to and communicably interface with one or more PC cards inserted into respective slots **28**, and being improved to include a serial Split-Bridge™ interface generally show at **30**. The serial Split-Bridge™ interface portion **30** is adapted to serially communicate data and control signals between the parallel system bus **32** via a duplex serial link **34** to a remote peripheral device (not shown) converting the parallel data to outgoing serial data and converting incoming serial data to parallel data.

The proprietary Split-Bridge™ technology, when employed in the extended cardbus/PC card controller **20**, significantly expands the interconnectivity of a standard communications network by allowing devices accessing the parallel systems bus **32** to communicate with a variety of external devices via PC cards, an extended cardbus, or advantageously via a serial link when employing the high speed serial Split-Bridge™ technology according to the present invention.

All of the electronics comprising the controller **20** can be embodied in discrete circuitry, in an application specific integrated circuit (ASIC), or combination thereof, to provide the multi-function interface capability between the parallel system bus **32** and remote peripheral devices. By employing a serial Split-Bridge™ technology interface **30** in a controller **30** with commercially available custom electronic control circuitry since much of such as Cardbus, the controller **20** can communicate with either Cardbus or PCMCIA, or via the serial link Split-Bridge™ remote PCI devices. Since much of the PCI interface electronics are commonly used by the respective interfaces, the integrating of the circuitry **30** is very economical.

The present invention **20** facilitates the evolution of information transfer to offer high speed serial link connectivity exceeding data rates of 1.0 GHZ for use with PCI, Cardbus, integrated, or other parallel I/O bus architectures. Moreover, conventional digital signal processors, such as those manufactured by Texas Instruments Incorporated of Dallas, Tex., (DSPs) being employed on extended Cardbus/PC card controllers are well adapted to interface with and incorporate the serial Split-Bridge™ technology interface. Integrating commercially available Cardbus/PC card controller electronics with the proprietary serial Split-Bridge™ technology significantly improves performance and available features of the device **30** with nominal additional cost associated therewith. In fact, the price versus performance improvement of the present invention shown in FIG. **4** is a quantum leap over existing price-performance points.

The Split-Bridge™ serial interface electronics **30** can be designed into a custom Application Specific Integrated Circuit (ASIC) along with other electronics, moreover, multiple interfaces **30** can be employed on to a single controller **20** and multiplexed to interface with multiple internal or external devices and users. Accordingly, limitation to integration of a single Split-Bridge™ interface is not to be inferred, but rather parallel buses and possibly future general serial buses, can be interfaced to other devices using the proprietary Split-Bridge™ serial technology.

In summary, the improved Cardbus/PC card controller **20** facilitates improved connectivity between a system parallel bus and remote peripheral devices, allowing data connectivity via either the proprietary serial Split-Bridge™ technology, or via the standard PC card slots such as those based on the PCMCIA standards. Existing electronics, including DSPs, are well adapted to interface with ASICs or other discrete/custom componentry comprising the interface and employing the serials Split-Bridge™ technology.

Though the invention has been described with respect to a specific preferred embodiment, many variations and modifications will become apparent to those skilled in the art upon reading the present application. It is therefore the intention that the appended claims be interpreted as broadly as possible in view of the prior art to include all such variations and modifications.

We claim:

1. An interface comprising:

first electronics adapted to interface parallel data from a parallel data bus to a first bus; and

second electronics **[**adapted**]** *configured* to interface *said* parallel data from said parallel data bus into serial data **[**adapted**]** *and configured* to interface with a second remote bus, said second electronics *configured to* convert**[**ing**]** said parallel data *in*to said serial data *and, without inserting bus wait states, send said serial data to said second remote bus* without requiring any external signal from said second remote bus.

2. The interface as specified in claim **1** wherein said second electronics comprises **[**Split-Bridge™**]** *split-bridge* serial interface electronics.

3. The interface as specified in claim **1** wherein said parallel data bus is based on PCI-*type* or PCMCIA-*type* interface standards.

4. The interface as specified in claim **1** wherein said serial data has a serial data rate exceeding 1.0 Giga bits/second.

5. The interface as specified in claim **1** wherein said first electronics comprises a digital signal processor (DSP).

6. The interface card as specified in claim 1 wherein said first electronics comprises Cardbus electronics.

7. The interface card as specified in claim 1 wherein said first electronics and said second electronics are adapted to [concurrently] support transfer of data to said [respective] first *bus* and *said* second [buses] *remote bus*, *respectively*.

8. A method of interfacing parallel data on a parallel system bus to a first bus and a second remote bus, comprising the steps of:

a) converting a first portion of the parallel data on the parallel system bus to parallel data adapted to communicate with said first bus; and

b) converting a second portion of the parallel data on the parallel system bus to high-speed serial data, which said serial data is sent, *without inserting bus wait states, to the second remote bus* without requiring or receiving a signal from said second remote bus before sending said serial data.

9. The method as specified in claim 8 further comprising the step of using a [Split-Bridge™] *split-bridge* serial interface.

10. The method as specified in claim 8 wherein said parallel system bus is based on PCI-*type* or Cardbus-*type* bus standard.

11. The method as specified in claim 8 wherein said serial data is sent at a data rate exceeding 1.0 GHZ.

12. The method as specified in claim 8 wherein said step a) and said step b) are performed in a single electronic device.

13. The method as specified in claim 12 wherein said electronic device comprises a Digital Signal Processor (DSP).

14. The method as specified in claim 8 wherein a retry message is sent in advance of sending said serial data.

15. The method as specified in claim 8 wherein said step a) uses Cardbus electronics.

16. An interface comprising:

first electronics adapted to interface parallel data from a parallel data bus to a first bus; and

second electronics configured to interface said parallel data from said parallel data bus into serial data and configured to interface with a second remote bus, said second electronics configured to convert said parallel data into said serial data and, without additional bus wait states, send said serial data to said second remote bus, said second electronics configured to add tag data indicative of a transaction type to the serial data.

17. The interface as specified in claim 16 wherein said second electronics comprises split-bridge serial interface electronics.

18. The interface as specified in claim 16 wherein said parallel data bus is based on PCI-type or PCMCIA-type interface standards.

19. The interface as specified in claim 16 wherein said serial data has a serial data rate exceeding 1.0 Giga bits/second.

20. The interface as specified in claim 16 wherein said first electronics comprises a digital signal processor (DSP).

21. The interface card as specified in claim 16 wherein said first electronics comprises Cardbus electronics.

22. The interface card as specified in claim 16 wherein said first electronics and said second electronics are adapted to support transfer of data to said first bus and said second remote bus, respectively.

23. A method of interfacing parallel data on a parallel system bus to a first bus and a second remote bus, comprising:

a) converting a first portion of the parallel data on the parallel system bus to parallel data adapted to communicate with said first bus; and

b) converting a second portion of the parallel data on the parallel system bus to high-speed serial data, which said serial data is sent, without requiring bus wait states, to the second remote bus, said serial data including a tag indicative of a transaction type.

24. The method as specified in claim 23 further comprising the step of using a split-bridge serial interface.

25. The method as specified in claim 23 wherein said parallel system bus is based on PCI or Cardbus bus standard.

26. The method as specified in claim 23 wherein said serial data is sent at a data rate exceeding 1.0 GHZ.

27. The method as specified in claim 23 wherein said step a) and said step b) are performed in a single electronic device.

28. The method as specified in claim 27 wherein said electronic device comprises a Digital Signal Processor (DSP).

29. The method as specified in claim 23 wherein a retry message is sent in advance of sending said serial data.

30. The method as specified in claim 23 wherein said step a) uses Cardbus electronics.

31. An interface, comprising:

first electronics configured to interface parallel data from a parallel data bus to a first bus; and

second electronics configured to interface said parallel data from said parallel data bus into serial data and configured to interface with a second remote bus, said second electronics configured to add tag data indicative of a transaction type to the serial data.

32. The interface as specified in claim 31 wherein said parallel data bus is based on PCI standard.

33. The interface as specified in claim 31 wherein said second electronics further comprises a data register configured to store said parallel data.

34. The interface as specified in claim 33 wherein said second electronics is configured to mirror said data register parallel data to a register of another remote said interface.

35. The interface as specified in claim 31 wherein said second electronics is configured to add said tag data during a transaction.

36. The interface as specified in claim 35 wherein the second electronics is configured to proceed to a data cycle without delay.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : RE41,494 E
APPLICATION NO. : 11/183298
DATED : August 10, 2010
INVENTOR(S) : Frank W. Ahern et al.

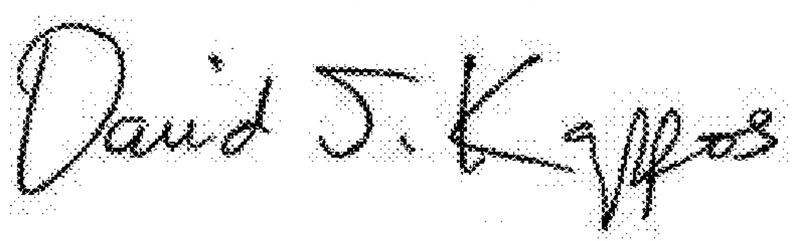
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 1, lines 12-21, delete "This application claims priority of provisional patent application serial No. 60/198,317 entitled Split-Bridge Systems, Applications and Methods of Use Filed on Apr. 19, 2000, as well as co-pending and commonly assigned patent applications Ser. No. 09/130,057 filed Jun. 6, 1998, Ser. No. 09/130,058 filed Jun. 6, 1998, Ser. No. 08/679,131 no issued as U.S. Pat. No. 5,941,965; and co-pending patent application Ser. No. 09/559,678, entitled Modular Computer Based on Universal Connectivity Station, the teaching of each incorporated herein by reference" and insert
-- This application claims [priority of provisional patent application serial No. 60/198,317 entitled Split-Bridge Systems, Applications and Methods of Use filed on Apr. 19, 2000, as well as co-pending and commonly assigned patent applications Ser. No. 09/130,057 filed Jun. 6, 1998, Ser. No. 09/130,058 filed Jun. 6, 1998, Ser. No. 08/679,131 now issued as U.S. Pat. No. 5,941,965; and co-pending patent application Ser. No. 09/559,678, entitled Modular Computer Based on Universal Connectivity Station, the teachings of each incorporated herein by reference] *the benefit of U.S. Provisional Application No. 60/198,317, filed April 19, 2000, the teachings of which are hereby incorporated by reference herein. This application is also a continuation-in-part application of U.S. Application No. 09/130,057, filed August 6, 1998, now U.S. Patent No. 6,088,752, the teachings of which are hereby incorporated by reference herein. This application is also a continuation-in-part application of U.S. Application No. 09/130,058, filed August 6, 1998, now U.S. Patent No. 6,070,214, the teachings of which are hereby incorporated by reference herein. This application is also a continuation-in-part application of U.S. Application No. 09/559,678, filed April 27, 2000, the teachings of which are hereby incorporated by reference herein. This application is also related to U.S. Application No. 08/679,131, now US Patent No. 5,941,965, the teachings of which are hereby incorporated by reference herein.* --, therefor.

In column 6, line 62, in Claim 3, delete "PCI-*type* or PCMCIA-*type*" and insert
-- [PCI or] PCMCIA --, therefor.

In column 7, line 22, in Claim 10, delete "PCI-*type* or Cardbus-*type*" and insert
-- [PCI or] *a* Cardbus --, therefor.

Signed and Sealed this
Twelfth Day of July, 2011



David J. Kappos
Director of the United States Patent and Trademark Office

In column 7, line 51, in Claim 18, delete "*PCI-type or PCMCIA-type*" and insert -- *PCMCIA* --, therefor.

In column 8, line 22, in Claim 25, delete "*PCI or Cardbus*" and insert -- *Cardbus* --, therefor.

In column 8, line 43, in Claim 32, delete "*PCI*" and insert -- *a Cardbus* --, therefor.