

US00RE41337E

(19) **United States**
(12) **Reissued Patent**
McClure

(10) **Patent Number:** **US RE41,337 E**
(45) **Date of Reissued Patent:** **May 18, 2010**

(54) **SYNCHRONOUS TEST MODE
INITIALIZATION**

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(21) Appl. No.: **09/596,027**

(22) Filed: **Jun. 15, 2000**

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Reissue of:

(64) Patent No.: **5,767,709**
Issued: **Jun. 16, 1998**
Appl. No.: **08/588,729**
Filed: **Jan. 19, 1996**

(51) **Int. Cl.**
H03K 5/13 (2006.01)

(52) **U.S. Cl.** **327/141; 142/198; 142/202**

(58) **Field of Classification Search** **327/141-143,**
327/198, 202

See application file for complete search history.

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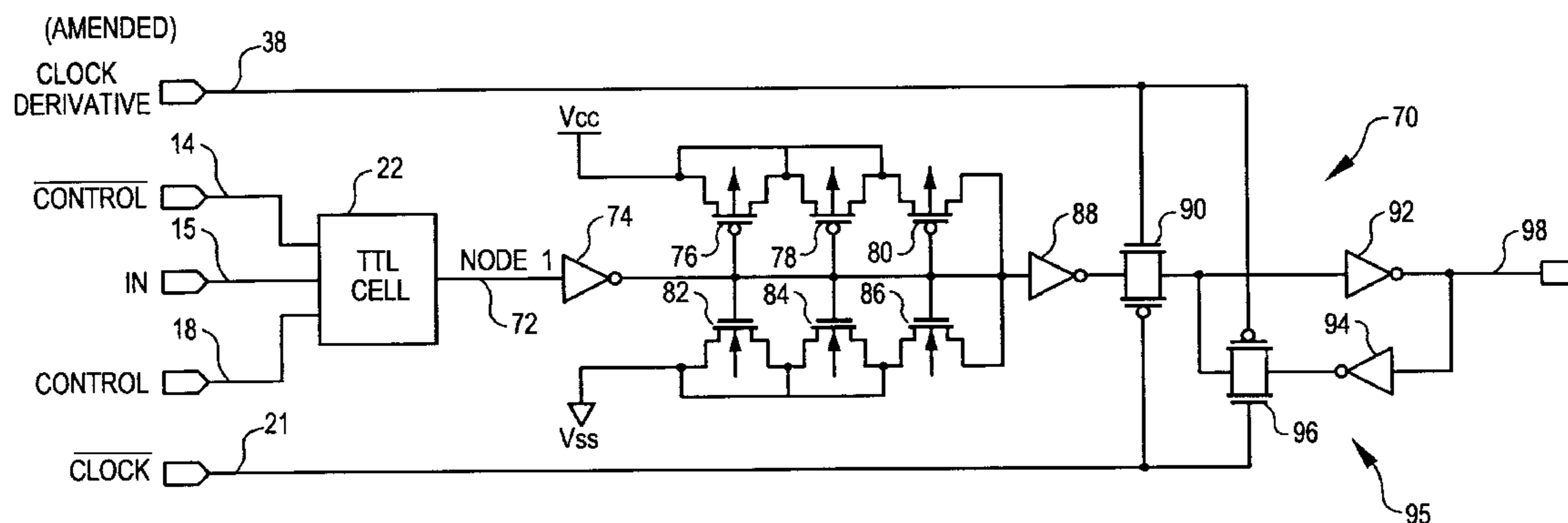
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(57) **ABSTRACT**

The entire data path of a synchronous integrated circuit device is initialized in a test mode upon power-up of the synchronous integrated circuit device. Upon power-up of the integrated circuit device in the test mode, a clock signal (either an external clock signal or an associated internal clock signal) is internally clocked. As the clock signal goes to a low logic state upon power-up of the device, a master latch [(flip-flop)] *flip-flop* element of the integrated circuit device is loaded with data and is allowed to conduct; a slave latch [(flip-flop)] *flip-flop* element of the integrated circuit device does not conduct. As the clock signal goes to a high logic state, the data in the master latch is latched. Also upon the high logic state of the clock, the slave latch element is loaded with data and is allowed to conduct.

37 Claims, 4 Drawing Sheets



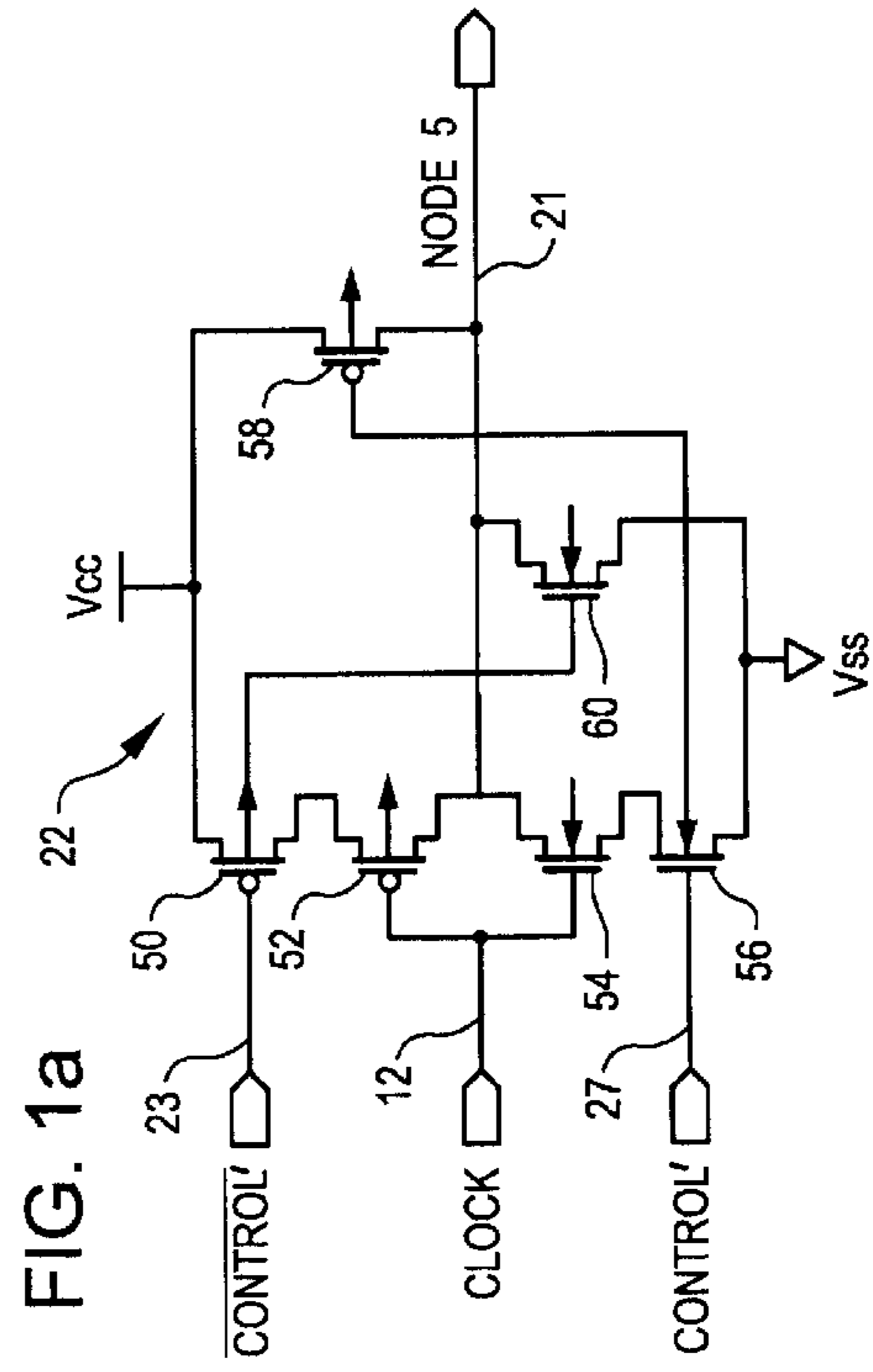
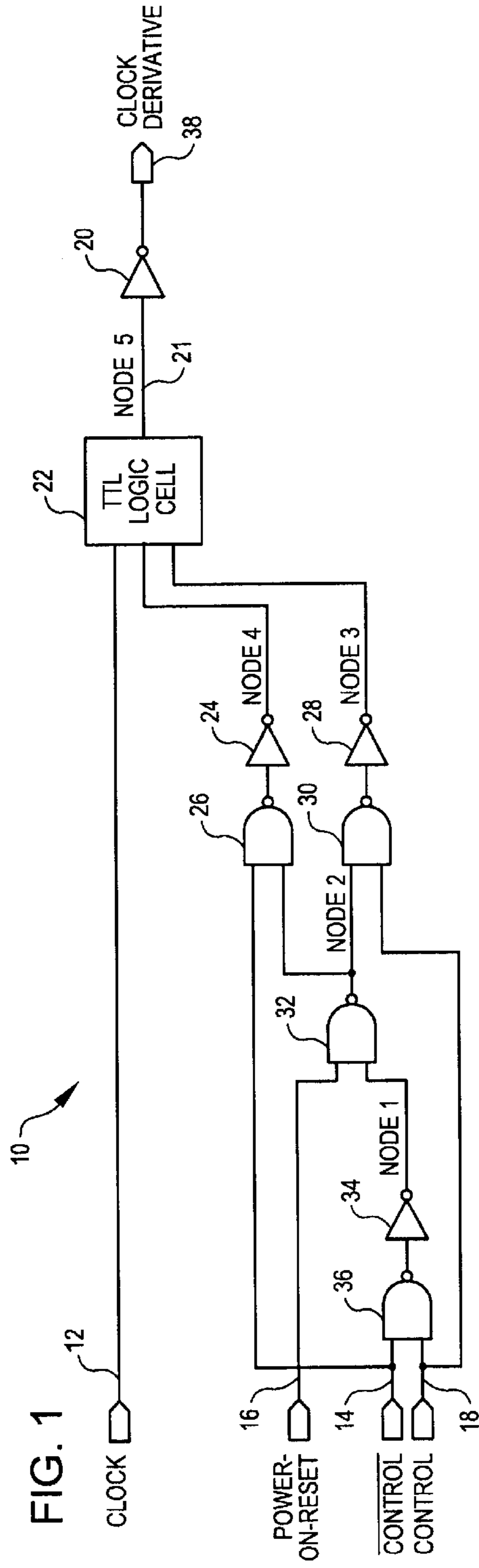


FIG. 1a

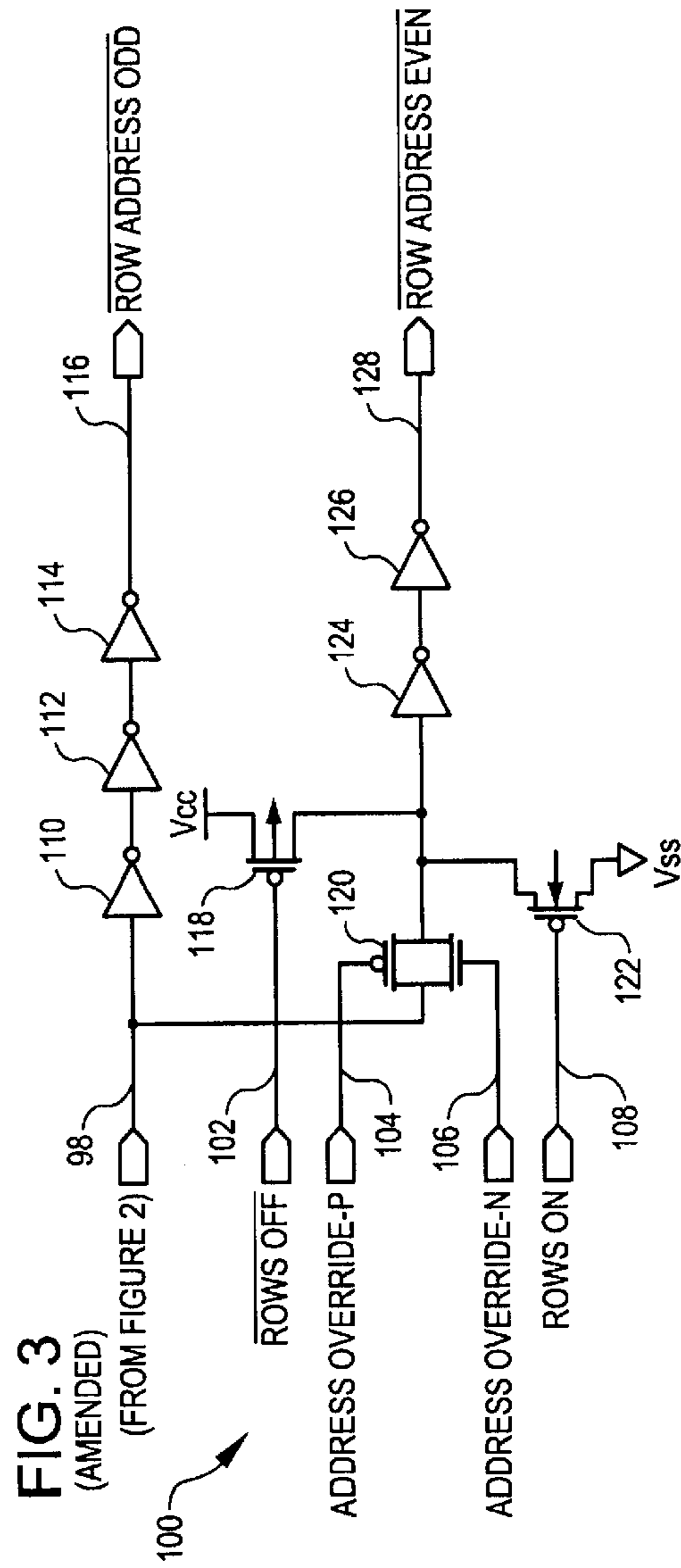
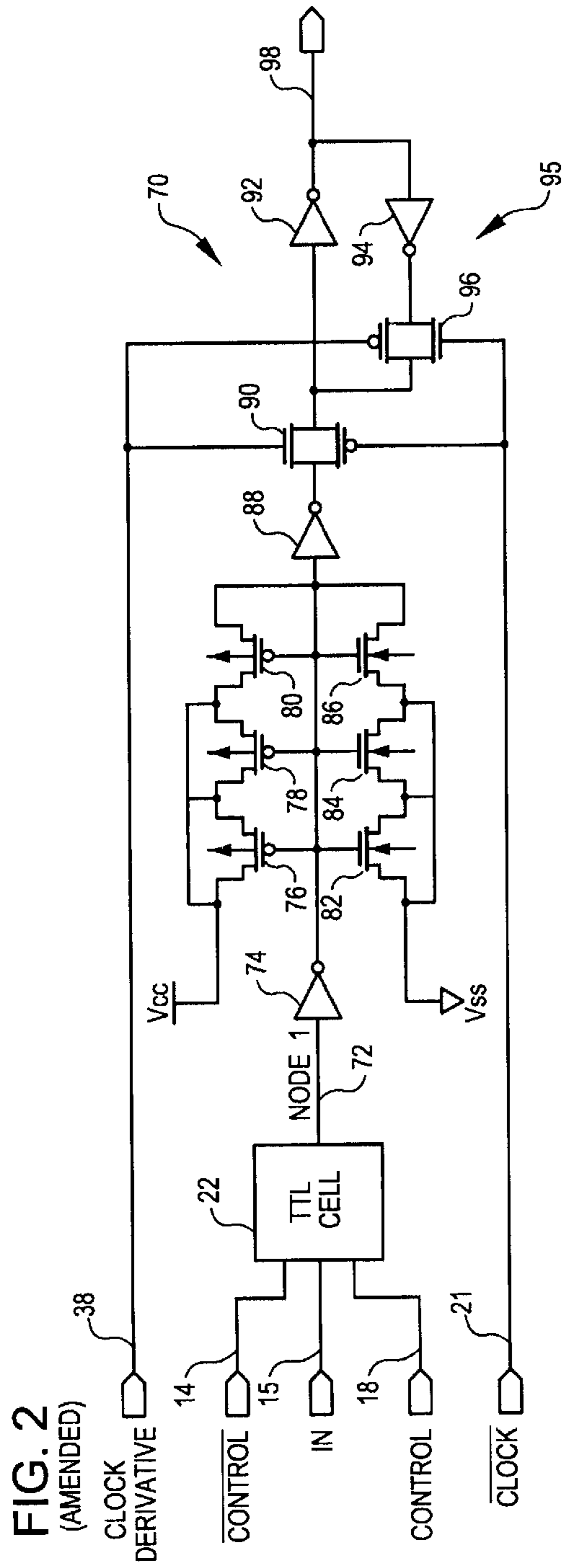


FIG. 4
(AMENDED)

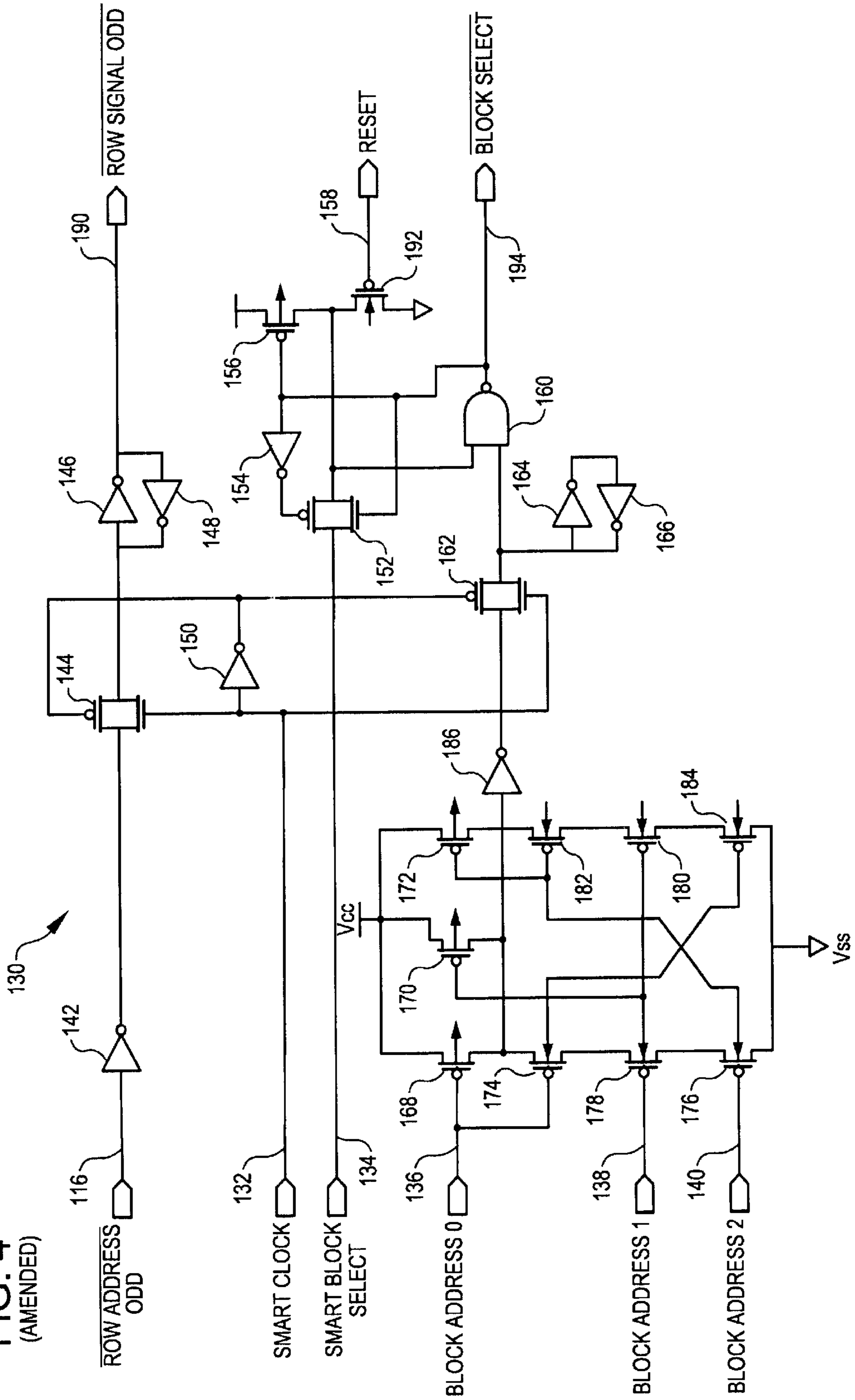


FIG. 5
(AMENDED)

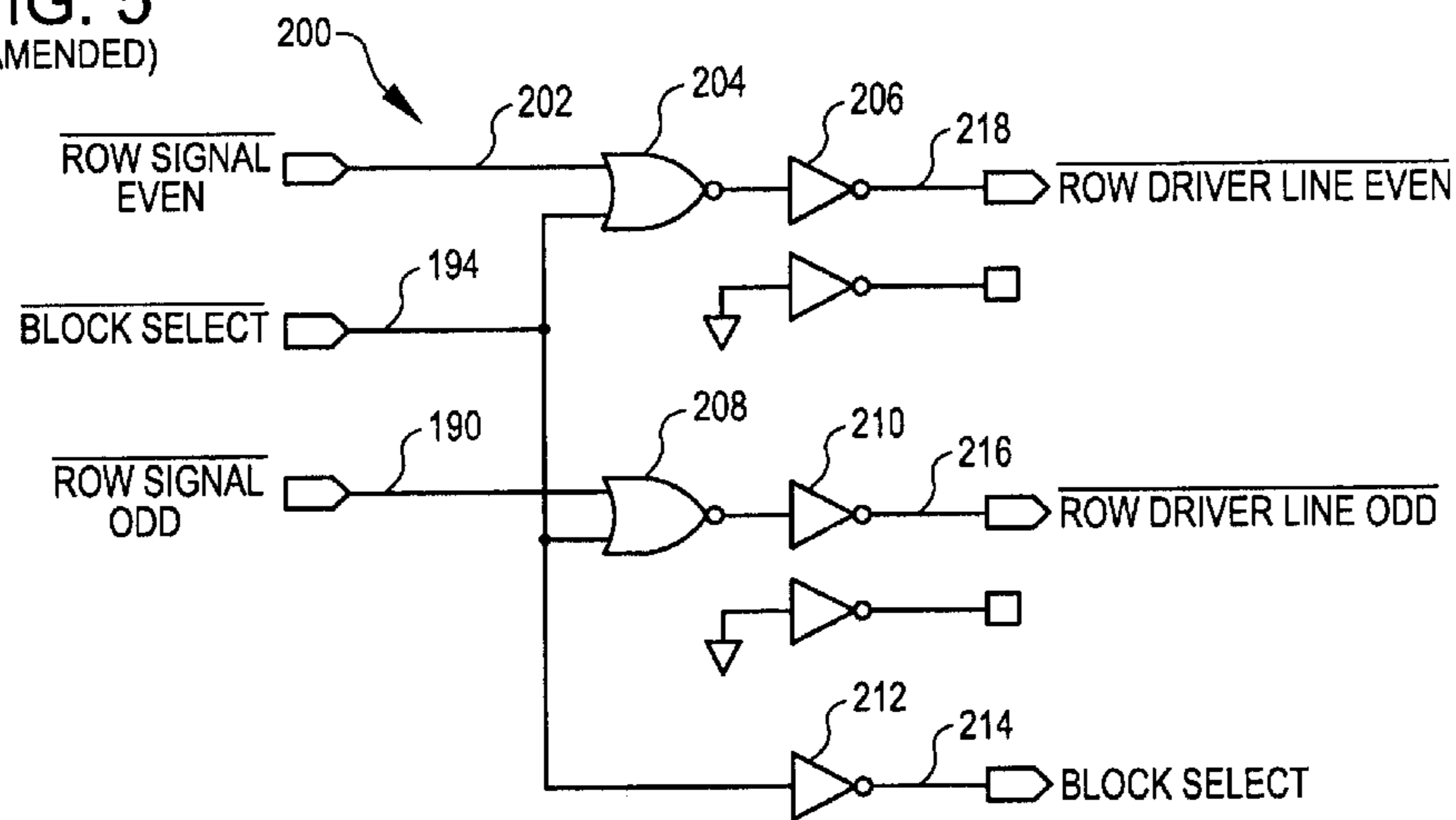
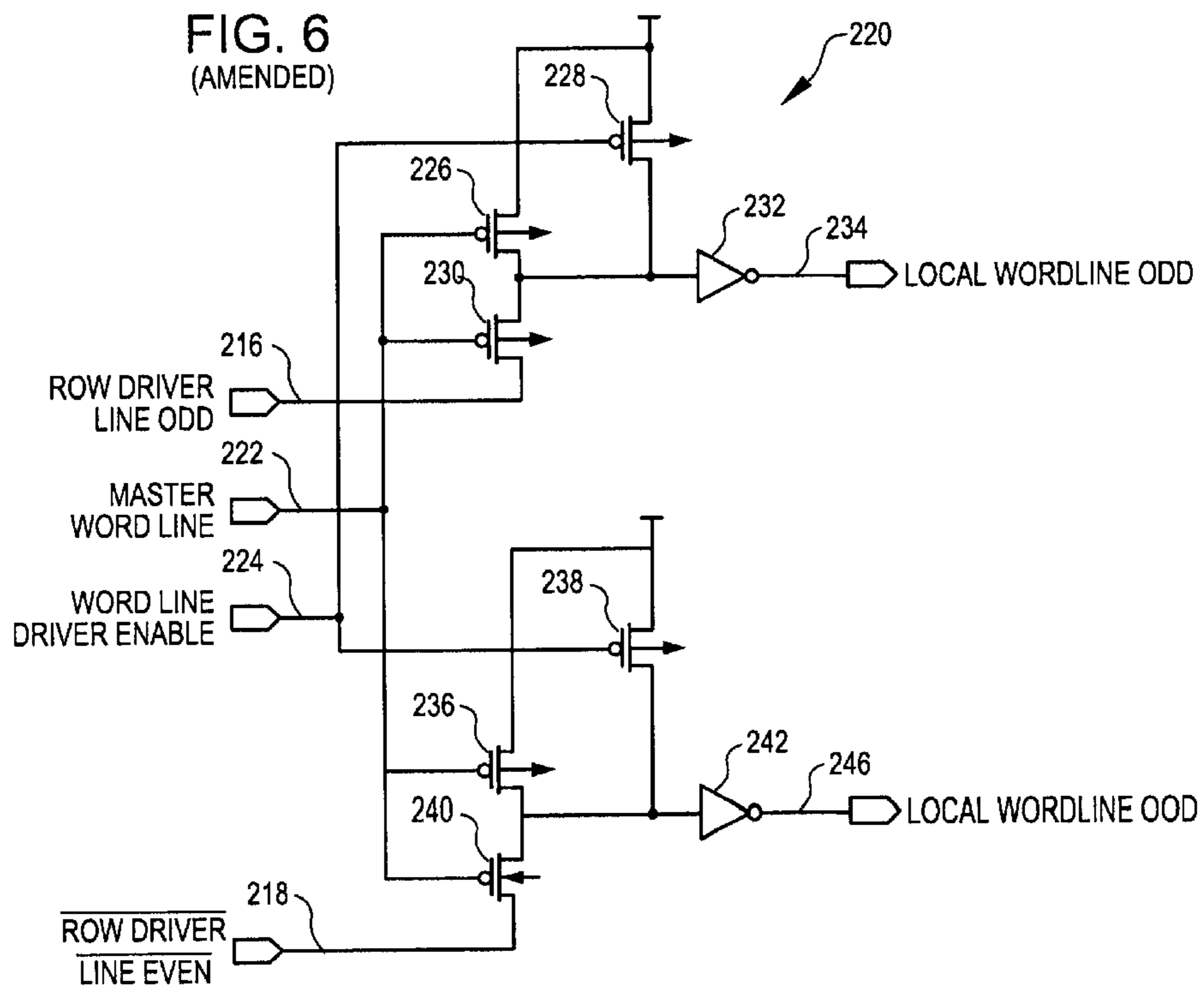


FIG. 6
(AMENDED)



**SYNCHRONOUS TEST MODE
INITIALIZATION**

Matter enclosed in heavy brackets [] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

CROSS REFERENCE TO RELATED
APPLICATIONS

The subject matter of the present application is related to [copending U.S. application Ser. No. 08/173,197, filed Dec. 22, 1993] *U.S. Pat. No. 5,577,051*, titled "Improved Static Memory Long Write Test", [attorney docket no. 93-C-82, copending U.S. application Ser. No. 08/172,854, filed Dec. 22, 1993] *U.S. Pat. No. 5,835,427*, titled "Stress Test Mode", [attorney docket no. 93-C-56] all of which are assigned to SGS-Thomson Microelectronics, Inc. and expressly incorporated herein by reference.

Additionally, the following [pending U.S. patent applications] *U.S. patents* by David Charles McClure entitled:

"Architecture Redundancy", [Ser. No. 08/582,484 (Attorney's Docket No. 95-C-136)] *U.S. Pat. No. 5,612,918*, and

"[Redundancy Control", [Ser. No. 08/580,827 (Attorney's Docket No. 95-C-143), which were both filed on Dec. 29, 1995] *U.S. Pat. No. 5,790,462*, which were both filed on Dec. 29, 1995, and have the same ownership as the present application, and to that extent are [arguable] *arguably* related to the present application, which are herein incorporated by reference;

and entitled:

"Test Mode Activation and Data Override", Ser. No. 08/587,709 [(Attorney's Docket No. 95-C-137)]

Ser. No. 09/457,558 which is a continuation of Ser. No. 08/587,709,

Ser. No. 09/454,800 which is a divisional of Ser. No. 08/587,709,

"Pipelined Chip Enable Control Circuitry and Methodology", [Ser. No. 08/588,730 (Docket No. 95-C-138)] *U.S. Pat. No. 5,701,275,*

U.S. Pat. No. 5,798,980 which is a divisional of U.S. Pat. No. 5,701,275,

"Output Driver Circuitry Having a Single Slew Rate Resistor", [Ser. No. 08/588,988 (Docket No. 95-C-139)] *U.S. Pat. No. 5,801,563,*

"Synchronized Stress Test Control", [Ser. No. 08/589,015 (Docket No. 95-C-142)] *U.S. Pat. No. 5,712,584,*

"Write Pass Through Circuit", [Ser. No. 08/588,662 (Attorney's Docket No. 95-C-144)] *U.S. Pat. No. 5,657,292,*

"Data-Input Device for Generating Test Signals on Bit and Bit-Complement Lines", [Ser. No. 08/588,762 (Attorney's Docket No. 95-C-145)] *U.S. Pat. No. 5,845,059,*

"Synchronous Output Circuit", [Ser. No. 08/588,901 (Attorney's Docket No. 95-C-146)] *U.S. Pat. No. 5,619,456,*

"Write Driver Having a Test Function", [Ser. No. 08/589,141 (Attorney's Docket No. 95-C-147)] *U.S. Pat. No. 5,745,432,*

"Circuit and Method for Tracking the Start of a Write to a Memory Cell", Ser. No. 08/589,139 [(Attorney's Docket No. 95-C-148)] (*since abandoned*),

U.S. Pat. No. 5,808,960 which is a continuation of Ser. No. 08/589,139,

"Circuit and Method for Terminating a Write to a Memory Cell", Ser. No. 08/588,737 [(Attorney's Docket No. 95-C-149)] (*since abandoned*),

U.S. Pat. No. 5,825,691 which is a continuation of Ser. No. 08/588,737,

"Clocked Sense Amplifier with Wordline Tracking", [Ser. No. 08/587,728 (Attorney's Docket No. 95-C-150)] *U.S. Pat. No. 5,802,004,*

U.S. Pat. No. 5,828,622 which is a divisional of U.S. Pat. No. 5,802,004,

"Memory-Row Selector Having a Test Function", Ser. No. 08/589,140 [(Attorney's Docket No. 95-C-151)] (*since abandoned*),

U.S. Pat. No. 5,848,018 which is a continuation of Ser. No. 08/589,140,

"Device and Method for Isolating Bit Lines from a Data Line", [Ser. No. 08/588,740 (Attorney's Docket No. 95-C-154)] *U.S. Pat. No. 5,691,950,*

"Circuit and Method for Setting the Time Duration of a Write to a Memory Cell", [Ser. No. 08/587,711 (Attorney's Docket No. 95-C-156)] *U.S. Pat. No. 5,864,696,*

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"Low-Power Read Circuit and Method for Controlling A Sense Amplifier", [Ser. No. 08/589,024,] *U.S. Pat. No. 5,619,466 [(Attorney's Docket No. 95-C-168)],*

"Device and Method for Driving a Conductive Path with a Signal", Ser. No. 08/587,708 [(Attorney's Docket No. 169)] (*since abandoned*),

U.S. Pat. No. 5,896,336 which is a continuation of Ser. No. 08/587,708,

U.S. Pat. No. 5,883,838 which is a divisional of Ser. No. 08/587,708,

and the following [pending U.S. patent applications] *U.S. patents* by Mark A. Lysinger entitled:

"Burst Counter Circuit and Method of Operation Thereof", Ser. No. 08/589,023 [(Attorney's Docket No. 95-C-141)] (*since abandoned*),

U.S. Pat. No. 5,805,523 which is a continuation of Ser. No. 08/589,023,

"Switching Master/Slave Circuit", [Ser. No. 08/588,648 (Attorney's Docket No. 96-C-03)] *U.S. Pat. No. 5,783,958,*

which have the same effective filing data and ownership as the present application, and to that extent are arguably related to the present application, are incorporated herein by reference.

BACKGROUND OF THE INVENTION

The present invention relates generally to the testing of integrated circuit devices, and more specifically to the testing of synchronous integrated circuit devices having a stress test mode or other test mode.

Stress test modes are commonly used in modern synchronous integrated circuit devices to subject the integrated circuit device to various types of tests which "stress" the device. It is important to stress various element and signals of the device for maximum fault coverage. For instance, the external clock signal supplied to the integrated circuit device is an important signal to test because it controls many of the gates contained within the device. Thus, for maximum fault coverage of the device, it is important to stress the external clock signal both at a low logic state and a high logic state. Difficulties are encountered in trying to establish the logic states of the device during a stress test mode. These difficulties are encountered in a memory cell stress test mode of the device, in which all rows and columns are enabled and bitlines true or bitlines complement of the memory cell are pulled to power supply voltage V_{SS} , or in a periphery stress test mode in which all rows and columns of the device are disabled. The difficulty lies in the fact that master/slave

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latches on the inputs of the integrated circuit device do not allow data to flow all the way through the device since only one master latch or one slave latch will conduct at a time.

Another prior art problem encountered with synchronized integrated circuit test modes is that entering a test mode after the integrated circuit device has been powered-up can result in device latch-up. Once the device powers-up, it has initialized to a certain voltage, such as 3 volts or 5 volts. Transition to a test mode from this voltage condition causes huge current spikes which can result in device latch-up as all the rows, columns, bitlines, etc. of the device simultaneously switch from a normal operation mode to a test mode. It would thus be desirable to enter a test mode upon power-up of the device in order to avoid possible device latch-up.

There is thus an unmet need in the art to be able to initialize the entire data path of an integrated circuit device in a test mode during device power-up and to be able to adequately test the external clock signal of the device or a derivative clock signal thereof in both a high logic state and a low logic state.

SUMMARY OF THE INVENTION

It is an object of the present invention to initialize the entire data path of an integrated circuit device during a test mode upon power-up of the synchronous integrated circuit device.

It is further an object of the present invention to adequately test the external clock signal or internal clock signals associated with the external clock signal of the synchronous integrated circuit device.

Therefore, according to the present invention, the entire data path of the synchronous integrated circuit device is initialized in a test mode upon power-up of the integrated circuit device. Upon power-up of the integrated circuit device in the test mode, a clock signal (either an external clock signal or an associated internal clock signal) is internally clocked. As the clock signal goes to a low logic state upon power-up of the device, a master latch [(flip-flop)] *flip-flop* element of the integrated circuit device is loaded with data and is allowed to conduct; a slave latch [(flip-flop)] *flip-flop* element of the integrated circuit device does not conduct. As the clock signal goes to a high logic state, the data in the master latch is latched. Also upon the high logic state of the clock, the slave latch element is loaded with data and is allowed to conduct.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as a preferred mode of use, and further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

FIG. 1 is a schematic diagram of a clock input buffer, according to a preferred embodiment of the present invention;

FIG. 1a is a schematic diagram of a TTL (transistor transistor logic) cell, according to the preferred embodiment of the present invention;

FIG. 2 is a schematic diagram of an address input buffer, according to the preferred embodiment of the present invention;

FIG. 3 is a schematic diagram of row address driver circuitry, according to the preferred embodiment of the invention;

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FIG. 4 is a schematic diagram of word line and block select latch circuitry, according to the preferred embodiment of the invention;

FIG. 5 is a schematic diagram of word line select circuitry, according to the preferred embodiment of the present invention; and

FIG. 6 is a schematic diagram of local wordline driver circuitry, according to the preferred embodiment of the present invention.

DESCRIPTION OF THE INVENTION

The entire data path of a synchronous integrated circuit device is initialized in a test mode upon power-up of the integrated circuit device. Upon power-up of the integrated circuit device in the test mode, a clock signal (either an external clock signal or an associated internal clock signal) is internally clocked. As the clock signal goes to a low logic state upon power-up of the device, a master latch [(flip-flop)] *flip-flop* element of the integrated circuit device is loaded with data and is allowed to conduct; a slave latch [(flip-flop)] *flip-flop* element of the integrated circuit device does not conduct. As the clock signal goes to a high logic state, the data in the master latch is latched. Also upon the high logic state of the clock, the slave latch element is loaded with data and is allowed to conduct. Using the present invention, both the master and slave latch elements are sequentially loaded with the correct data state and then allowed to sequentially conduct.

Conduction of the master latch elements and conduction of the slave latch elements initializes an address path of the integrated circuit device such that either no columns or rows of the integrated circuit device are selected or such that all columns or rows of the integrated circuit device are selected. If all columns and rows of the integrated circuit device are selected, all bitlines true of the integrated circuit device are held at a first voltage level and all bitlines complement of the integrated circuit device are held at a second voltage level.

FIGS. 1 and 1a illustrate the clock control circuitry which controls the external clock or derivative signal thereof of the synchronous integrated circuit device. FIGS. 2 to 6 illustrate the address control circuitry which are driven by the clock circuitry of FIG. 1. Referring to FIG. 1, a schematic diagram of a clock input buffer 10, according to a preferred embodiment of the present invention, is shown. Clock input buffer 10 is provided with Clock signal 12. Power-On-Reset signal 16, Control bar signal 14 and Control signal 18. Clock signal 12 is equal to the external clock signal provided to a clock pin of the integrated circuit device or is a derivative signal thereof and is provided as an input signal to TTL clock cell 22, shown in FIG. 1a. The power-on-reset signal is an internally generated signal which changes logic state once a threshold value of positive power supply Vcc is passed as Vcc rises. Control signal 18 and Clock bar signal 14 are provided to NAND logic gate 36 as input signals. The output signal of NAND logic gate 36 is inverted by inverter 34 before being presented to a second NAND logic gate 32 as an input signal. The second input signal of NAND logic gate 32 is Power-On-Reset signal 16. The output signal of NAND logic gate 32 feeds both NAND logic gates 26 and 30. A second input signal to NAND logic gate 26 is Control bar signal 14 and a second input signal to NAND logic gate 30 is Control signal 18. The output signal of NAND logic gate 26 is inverted by inverter 24 and the output signal of inverter 24 is an input signal to TTL Clock Cell 22. The output signal of NAND logic gate 30 is inverted by inverter 28 and the output signal of inverter 28 is another input signal to TTL Clock

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Cell 22. The output signal of TTL Clock Cell 22 is inverted by inverter 20 to produce Clock Derivative signal 38.

Control bar derivative signal [14] 23 from Node 4 and Control derivative signal [18] 27 from Node 3 control TTL cell 22 shown in FIG. 1a. TTL cell 22 contains the following elements: p-channel MOS transistors 50, 52 and 58 and n-channel MOS transistors 54, 56 and 60. The gates of transistors 50 and 60 are supplied with Control bar signal [14]23. The gates of transistors 52 and 54 are supplied with Clock signal 12, and the gates of transistors 56 and 58 are supplied with the Control signal [18]27. A first source/drain of transistor 50 and a first source/drain of transistor 58 are connected to power supply voltage Vcc as shown. A second source/drain of transistor 50 is connected to a first source/drain of transistor 52. A second source/drain of transistor 52 is connected to a first source/drain of transistor 54, a first source/drain of transistor 60 and a second source/drain of transistor 58 to form output signal [23] 21 on Node 5. A second source/drain of transistor 54 is connected to a first source/drain of transistor 56. A second source/drain of transistor 56 is connected to a second source/drain of transistor 60 and power supply voltage V_{SS}.

When in the periphery stress test mode Control bar signal 14 and Control signal 18 are a high logic state. Referring again to FIG. 1, during power-up of the integrated circuit device Power-On-Reset signal 16 pulses high. When Power-On-Reset signal 16, Control bar signal 14 and Control signal 18 are all a high logic state, Node 1 of FIG. 1 is a high logic state and Node 2 is a low logic state, which means that Node 3 and Node 4 are both a low logic state. Once Power-On-Reset signal 16 goes to a low logic state, Node 2 goes to a high logic state, Node 3 and Node 4 are equal to the logic state of Control bar signal 14 and Control signal 18 both of which are now a high logic state.

Referring once more to FIG. 1a, during power-up in a periphery stress test mode, Control' bar derivative signal 23 (shown at Node [3] 4 of FIG. 1) and Control' derivative signal 27 (shown at Node [4] 3 of FIG. 1) are both a low logic state and signal 21 at Node 5 is forced to a high logic state. This gives the appearance that Clock input signal 12 was a low logic state. Conversely, when the Power-On-Reset signal 16 goes to a low logic state, and when Control' bar derivative signal 23 and Control' derivative signal 27 [go to] remain at high logic states, signal 21 is forced to a low logic state which gives the appearance that Clock signal 12 was a high logic state. Thus, a high logic state on controls signals Control' bar derivative signal 23 and Control' derivative signal 27 during a periphery stress test mode forces the equivalent of a high going clock input. During a memory cell stress test mode, the equivalent of a low going clock input is forced. Upon power-up of the device, Power-On-Reset signal 16 goes high and Clock derivative signal [12] 38 is forced to a low logic state during which the master latch of the device is loaded with data and allowed to conduct. Following completion of the power-on reset cycle, Power-On-Reset signal 16 goes low and data is latched into the master latch; also data is loaded into the slave latch [which is allowed to device conduct]. Using the circuitry of FIG. 1a, the state of Clock derivative signal [12] 38 is forced to the desired logic state during a test mode, either a periphery stress test mode or a memory cell stress test mode.

The operation of FIG. 1a to force the condition of the Clock derivative signal [12] 38 as desired may be further illustrated with reference to a second input buffer circuit. Referring to FIG. 2, a schematic diagram of an address input buffer 70, according to the preferred embodiment of the present invention, is shown. Input buffer 70 includes the

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following elements: TTL (transistor transistor logic) cell 22, inverters 74, 88, 92 and 94, and passgates 90 and 96. The details of TTL cell 22 are similar to those shown in FIG. 1a. Input buffer 70 contains a master latch 95 comprised of elements inverter 92, inverter 94 and [passgate] passgates 90 and 96. Input buffer 70 is supplied with the following input derivative signals: Clock signal 38, Control bar signal 14, IN data signal 15, Control signal 18 and Clock bar signal [13] 21 and generates output signal 98.

When control bar signal 14 and Control signal 18 are both a high logic state, signal 72 at Node 1 is a low logic state. Because of the way the TTL cell of FIG. 1a forces Clock derivative signal 38 to the desired logic state. Clock derivative signal 38 is initially a low logic state but will ultimately go to a high logic state so that the master latch 95 initially conducts, thereby forcing signal 98 to a [high] low logic state. Clock signal [12] 38 will then go to a high logic state, [turning off] thus latching master latch 95.

Signal 98 propagates to Row Address Driver circuitry 100 of FIG. 3, according to the preferred embodiment of the invention. Row address driver circuitry 100 is composed of inverters 110, 112, 114, 124 and 126, p-channel MOS transistor 118, n-channel MOS transistor 122, and passgate 120. Signal 98 from FIG. 1 is provided to a series of inverters 110, 112 and 114 which delay and [inverter] invert signal 98 to produce Row Address signal 116. Signal 98 is also presented to passgate 120 which is controlled by Address Override-P signal 104 and Address Override-N signal 106. The output signal of passgate 120 is pulled up towards Vcc by p-channel transistor 118 whose gate is controlled by Rows On bar signal 102 and is pulled down towards V_{SS} by n-channel transistor 122 whose gate is controlled by Rows Off signal 108. The output signal of passgate 120 passes through two inverters 124 and 126 to become Row Address bar signal 128. Row Address bar signal 128 is the inverse of Row Address signal 116. Rows On bar signal 102 forces Row Address bar signal [116] 128 on (in an asserting condition) when it is a low logic state in the test mode and Rows Off signal 108 forces Row Address bar signal [116] 128 off (not in an asserting condition) when it is a high logic state in the test mode. P-channel MOS transistor 118 and n-channel MOS transistor 122 act as row address override devices in the test mode.

Rows On bar signal 102 and Rows Off signal 108 are controlled based upon which type of test mode being entered: a memory cell stress mode in which all rows are enabled or a periphery stress mode in which all the row are disabled. Based on the logic states of signal 98. Rows On bar signal 102 and Rows Off signal 108 and further based upon the fact that Address Override-P signal 104 is a high logic state and Address Override-N signal 106 is a low logic state in any test mode. Row Address signal 116 and Row Address bar signal 128 are both forced to a high logic state in a memory cell stress mode in an asserting condition for the Word Line and Block Select Latch circuitry 130 of FIG. 4 or are both forced to a low logic state in a periphery stress mode.

The Row Address signal 116 generated by FIG. 3 feeds the Word Line and Block Select Latch circuitry 140 shown in FIG. 4, according to the preferred embodiment of the invention. In addition to Row Address signal 116, circuitry 130 is supplied with Smart Clock signal 132, Smart Block Select signal 134, Block Address0 signal 136, Block Address1 signal 138 and Block Address2 signal 140, and Reset signal 192. Circuitry 130 generates Row signal 190 and Block Select bar signal 194. Smart Clock signal 132 is a high-going narrow pulse generated from the rising edge of

Clock *derivative* signal [12] 38 and Smart Block Select signal 134 is a derivative signal of Smart Clock signal 132. The elements of circuitry 130 include: inverters 142, 146, 148, 150, 154, 164, 166 and 186; passgates 144, 152 and 162; NAND logic gate 160; p-channel MOS transistor 156, 168, 170, 172; and n-channel MOS transistors 174, 176, 178, 180, 182 and 184.

Row Address signal 116 is supplied by FIG. 3 to the input terminal of inverter 142. Smart Clock signal 132 is provided to a control terminal of both passgates 144 and [152] 162 as shown and accordingly controls passgates 144 and [152] 162; it additionally is provided to the input terminal of inverter 150. Smart Block Select signal 134 is an input signal to passgate 152 which is indirectly controlled by Block Address signals 136, 138 and 140. Block Address0 signal 136 is provided to the gates of transistors 168, 174 and 184. Block Address1 signal 138 is provided to the gates of transistors 178, 170 and 180. Block Address2 signal 140 is provided to the gates of transistors 182, 172 and 176.

The output terminal of 142 provides an inverted row address signal to passgate 144. The output of slave passgate 144 is provided to the input terminal of inverter 146 which produces Row output signal 190. The output terminal of inverter 150 controls a control terminal of both passgates 144 and 162 while Smart Clock signal 132 controls the other control terminal of passgates 144 and 162 as shown.

Following the powering-up of the integrated circuit device which is controlled by Power-On-Reset signal 16. Power-On-Reset signal 16 goes low and Clock *derivative* signal [12] 38 goes from a low logic state to a high logic state. This also causes Smart Clock signal 132 to go to the high logic state since Smart Clock signal 132 is a derivative signal of Clock *derivative* signal [12] 38, as previously discussed. A high logic state of Smart Clock signal 132 causes slave latch member 144 to load in data supplied by Row Address signal 116 and to conduct. Thus, the conduction of slave latch 144 follows the conduction of the master latch of FIGS. 1 and 1a.

The Row signal 190 and Block Select bar signal 194 generated by circuitry 130 are supplied to Word Line Select circuitry 200 of FIG. 5, according to the preferred embodiment of the present invention. In addition to signals 190 and 194 circuitry 200 is provided with Row bar signal 202, which is the inverse of Row signal 190. The elements of circuitry 200 include NOR logic gates 204 and 208; and inverters 206, 210 and 212. Circuitry 200 produces signal Row Driver Line even bar signal 218, Row Driver Line odd bar signal 216 and Block Select signal [216] 214 (the inverse signal of Block Select bar signal 194).

Row Driver Line odd bar signal 216 and Row Driver Line even bar signal 218 from circuitry 200 feeds the Local Wordline Driver circuitry 220 of FIG. 6, according to the preferred embodiment of the present invention. Circuitry 220 in addition to signals 216 and 218 is provided with a Master Word Line signal 222 and Word Line Driver Enable signal 224. The elements of circuitry 220 include p-channel MOS transistors 226, 228, 236 and 238; n-channel MOS transistors 230 and 240; and inverters 232 and 242. Circuitry 220 produces Local Wordline odd signal 234 and Local Wordline even bar signal 246. When Row Driver Line odd bar signal 216 and Row Driver Line even bar signal 218 are both a high logic state, Local Wordline Odd signal 234 and Local Wordline even bar signal 246 will be off (a low logic state). Since Local Wordline Odd signal 234 and Local Wordline even bar signal 246 are the local wordlines of the device, all wordlines of the device are off.

The internal clocking of the synchronous integrated circuit device described above provides several advantages

over the prior art. The entire data path of a synchronous integrated circuit device may be set up based upon exercising only the internally generated power-on-reset signal of the integrated circuit device. It is not necessary, as it was in the prior art, to exercise the clock device pin in order to enter or affect the test mode. Since the clock signal is internally forced, testing of the clock signal in two logic states, both a high logic state and a low logic state, is possible. Thus, the clock is testing in both a memory cell stress test mode and in a periphery stress test mode. The exercise of the clock signal in both logic states is an important advantage since the clock signal is typically connected to many gates of the synchronous integrated circuit device.

Since the test mode is entered internally and the clock signal is internally forced, the test is more reliable than it is to exercise the clock device pin to enter the test mode; one need not worry about pin continuity problems during testing since the device is internally clocked. Also, because the clock pin need not be probed to enter the test mode, the number of pins which must be exercised by test equipment is reduced and thus more devices may be simultaneously tested due to the reduced pin count.

A further advantage of the present invention is provided by powering-up the integrated circuit device in the test mode, rather than switching to the test mode subsequent to powering-up the device as is done in the prior art. Powering-up the device in the test mode prevents the huge current spikes which may result in a latch-up condition of the device.

The present invention is desirable in any system or device employing synchronous integrated circuits. Thus it is envisioned that the present invention is suitable for use in a number of device types, including: memory devices such as SRAM (static random access memory), DRAM (dynamic random access memory) and BRAM (burst RAM) devices; programmable devices; logic devices; gate arrays; ASICs (application specific integrated circuits); and microprocessors. The present invention is further suitable for use in any system or systems which employ such devices types.

While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention. For instance, the address path circuitry shown in the figures is but one example of how the circuitry and methodology of the present invention may be implemented.

What is claimed is:

1. A method of internally controlling a clock signal of an integrated circuit device such that a data path of the integrated circuit device is initialized in a test mode, comprising the steps of:

upon a power-up condition in the test mode of the integrated circuit device forcing the clock signal of the integrated circuit device to a first logic state, thereby causing a master element of the integrated circuit device to load in first data and to conduct; and

upon completion of the power-up condition forcing the clock signal of the integrated circuit device to a second logic state, thereby latching in the first data to the master element and causing a slave element of the integrated circuit device to load in second data generated by the master element and to conduct.

2. The method of claim 1, wherein the first logic state is a low logic state and the second logic state is a high logic state.

3. The method of claim 1, wherein the power-up condition of the integrated circuit device is controlled by a power-on-reset signal of the integrated circuit device.

4. The method of claim 3, wherein the power-on-reset signal is an internally generated signal which changes logic state once a threshold value of a positive power supply is passed as the positive power supply rises.

5. The method of claim 1, wherein the clock signal of the integrated circuit device is an external clock signal of the integrated circuit device or a derivative signal of the external clock signal.

6. The method of claim 1, wherein the master element of the integrated circuit device is a master latch element and the slave element is a slave latch element.

7. The method of claim 1, wherein the master element of the integrated circuit device is a master flip-flop element and the slave element is a slave flip-flop element.

8. The method of claim 1, wherein upon the power-up condition of the integrated circuit device, the clock signal is internally clocked.

9. The method of claim 1, wherein when the master element is conducting the slave element does not conduct and when the slave element is conducting the master element does not conduct.

10. The method of claim 1, wherein the test mode is entered upon the power-up condition of the integrated circuit device.

11. The method of claim 1, wherein the data path is an address path.

12. The method of claim 1, wherein in the test mode the integrated circuit device is tested as a voltage above a normal operating voltage of the integrated circuit device.

13. The method of claim 12, wherein the clock signal is tested in both the first logic state and the second logic state at the voltage.

14. The method of claim 1, wherein the integrate circuit device is a synchronous clocked device.

15. The method of claim 1, wherein conduction of the master element and conduction of the slave element initializes an address path of the integrated circuit device such that a plurality of columns and a plurality of rows of the integrated circuit device are not selected.

16. The method of claim 1, wherein conduction of the master element and conduction of the slave element initializes an address path of the integrated circuit device such that a plurality of columns and a plurality of rows of the integrated circuit device are selected.

17. The method of claim 16, wherein a plurality of bitlines true of the integrated circuit device are held at a first voltage level and a plurality of bitlines complement of the integrated circuit device are held at a second voltage level.

18. A method, comprising:

providing power to an integrated circuit;

loading a first data bit into a master latch and causing the integrated circuit to enter a test mode before the power attains a predetermined level, the master latch being disposed on the integrated circuit;

generating a second data bit from the first data bit;

latching the data bit in the master latch; and

loading the second data bit into a slave latch that is disposed on the integrated circuit.

19. The method of claim 18 wherein generating the second data bit comprises generating the second data bit equal to the first data bit.

20. The method of claim 18 wherein generating the second data bit comprises generating the second data bit equal to a complement of the first data bit.

21. The method of claim 18 wherein generating the second data bit comprises generating the second data bit before and after the power attains the predetermined level.

22. The method of claim 18 wherein:

loading the first data bit into the master latch comprises simulating an external clock signal having a first clock state; and

latching the first data bit in the master latch and loading the second data bit into the slave latch comprise simulating the external clock signal having a second clock state.

23. The method of claim 18 wherein:

loading the first data bit into the master latch comprises simulating an external clock signal inside the integrated circuit, the clock signal having a first clock state; and

latching the first data bit in the master latch and loading the second data bit into the slave latch comprise simulating the clock signal having a second clock state.

24. A method, comprising:

generating a power-on reset signal having a first reset state when power supplied to an integrated circuit has a predetermined first level causing the integrated circuit to enter a test mode;

generating the power-on reset signal having a second reset state when the power has a second predetermined level;

loading a first data bit into a master latch of the integrated circuit in response to the power-on reset signal having the first state;

generating a second data bit from the first data bit;

storing the first data bit in the master latch in response to the power-on reset signal having the second state; and

loading the second data bit into a slave latch of the integrated circuit in response to the power-on reset signal having the second state.

25. The method of claim 24 wherein:

generating the power-on reset signal having the first state comprises generating the power-on reset signal having the first state when an integrated-circuit supply voltage has a first predetermined voltage level; and

generating the power-on reset signal having the second state comprises generating the power-on reset signal having the second state when the supply voltage has a second predetermined voltage level.

26. The method of claim 24 wherein generating the second data bit comprises generating the second data bit in response to the power-on reset signal having either the first state or the second state.

27. The method of claim 24 wherein storing the first data bit in the master latch and loading the second data bit into the slave latch comprise generating a test signal having a first test state.

28. The method of claim 24 wherein storing the first data bit in the master latch and loading the second data bit into the slave latch comprise generating multiple test signals each having a first test state.

29. The method of claim 24 wherein storing the first data bit in the master latch and loading the second data bit into the slave latch comprise:

generating a test signal having a test state; and

simulating an external clock signal having a clock state in response to the test signal having the test state.

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30. The method of claim 24 wherein:

loading the first data bit into the master latch comprises
simulating an external clock signal having a first clock
state in response to the power-on reset signal having
the first reset state; and

storing the first data bit in the master latch and loading
the second data bit into the slave latch comprise,
generating a test signal having a test state, and
simulating the clock signal having a second clock state
in response to the test signal having the test state.

31. The method of claim 24 wherein:

loading the first data bit into the master latch comprises,
simulating an external clock signal having a first clock
state in response to the power-on reset signal having
the first reset state,

generating a test signal having a test state, and
generating the first data bit in response to the test sig-
nal; and

storing the first data bit in the master latch and loading
the second data bit into the slave latch comprise simu-
lating the clock signal having a second clock state in
response to the power-on reset signal having the sec-
ond reset state and the test signal having the test state.

32. The method of claim 24 wherein:

loading a first data bit into the master latch comprises,
simulating an external clock signal having a first clock
state in response to the power-on reset signal having
the first reset state,

generating a test signal having a first test state, and
generating the first data bit in response to the test sig-
nal; and

storing the first data bit in the master latch and loading
the second data bit into the slave latch comprise,
generating the test signal having a second test state,
and

simulating the clock signal having a second clock state
in response to the power-on reset signal having the
second reset signal and the test signal having the
second test state.

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33. A method, comprising:

providing power to an integrated circuit;

loading a first data bit into a master latch and causing the
integrated circuit to enter a test mode before the power
attains a predetermined level, the master latch being
disposed on the integrated circuit;

latching the first data bit in the master latch; and

loading the first data bit into a slave latch of the inte-
grated circuit.

34. The method of claim 33 wherein:

loading the first data bit into the master latch comprises
generating a clock signal having a first clock state; and

latching the first data bit in the master latch and loading
the first data bit into the slave latch comprise generat-
ing the clock signal having a second clock state.

35. The method of claim 33 wherein:

loading the first data bit into the master latch comprises
generating a clock signal inside the integrated circuit,
the clock signal having a first clock state; and

latching the first data bit in the master latch and loading
the first data bit into the slave latch comprise generat-
ing the clock signal having a second clock state.

36. The method of claim 18 wherein:

latching the first data bit comprises latching the first data
bit in the master latch after powering up the integrated
circuit; and

loading the second data bit comprises loading the second
data bit into the slave latch when the power attains the
predetermined level.

37. The method of claim 33 wherein:

latching the first data bit comprises latching the first data
bit in the master latch when the power attains the pre-
determined level; and

loading the first data bit into the slave latch comprises
loading the first data bit into the slave latch when the
power attains the predetermined level.

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