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**Chiu et al.**

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(54) **CIRCUIT LAYOUT ARRANGEMENT FOR KEY SWITCH SIGNAL RECOGNITION**

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(57) **ABSTRACT**

A key switch signal recognition circuit including a plurality of key switch buttons, a plurality of key switch signal output lines, and a plurality of key switch button contact areas is disclosed. Each of the key switch contact areas includes a first wire set and a second wire set. The first wire set has at least one wire, and each wire of the first wire set has one end connected to a common line and an opposite end forming an open end. The second wire set has at least one wire respectively disposed in parallel to and electrically insulated from the wire of the first wire set. The wire of the second wire set is respectively connected to a key switch signal output line. When depressing one key switch button to touch the corresponding key switch button contact area, the electrically conductive element of the depressed key switch button electrically connects the first wire set and second wire set of the touched key switch contact area, causing the respective key switch signal output line to send a key switch signal corresponding to the depressed key switch button.

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**Related U.S. Patent Documents**

Reissue of:

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(51) **Int. Cl.**  
**H03K 17/94** (2006.01)

(52) **U.S. Cl.** ..... **341/22; 341/26; 200/5 A; 400/477**

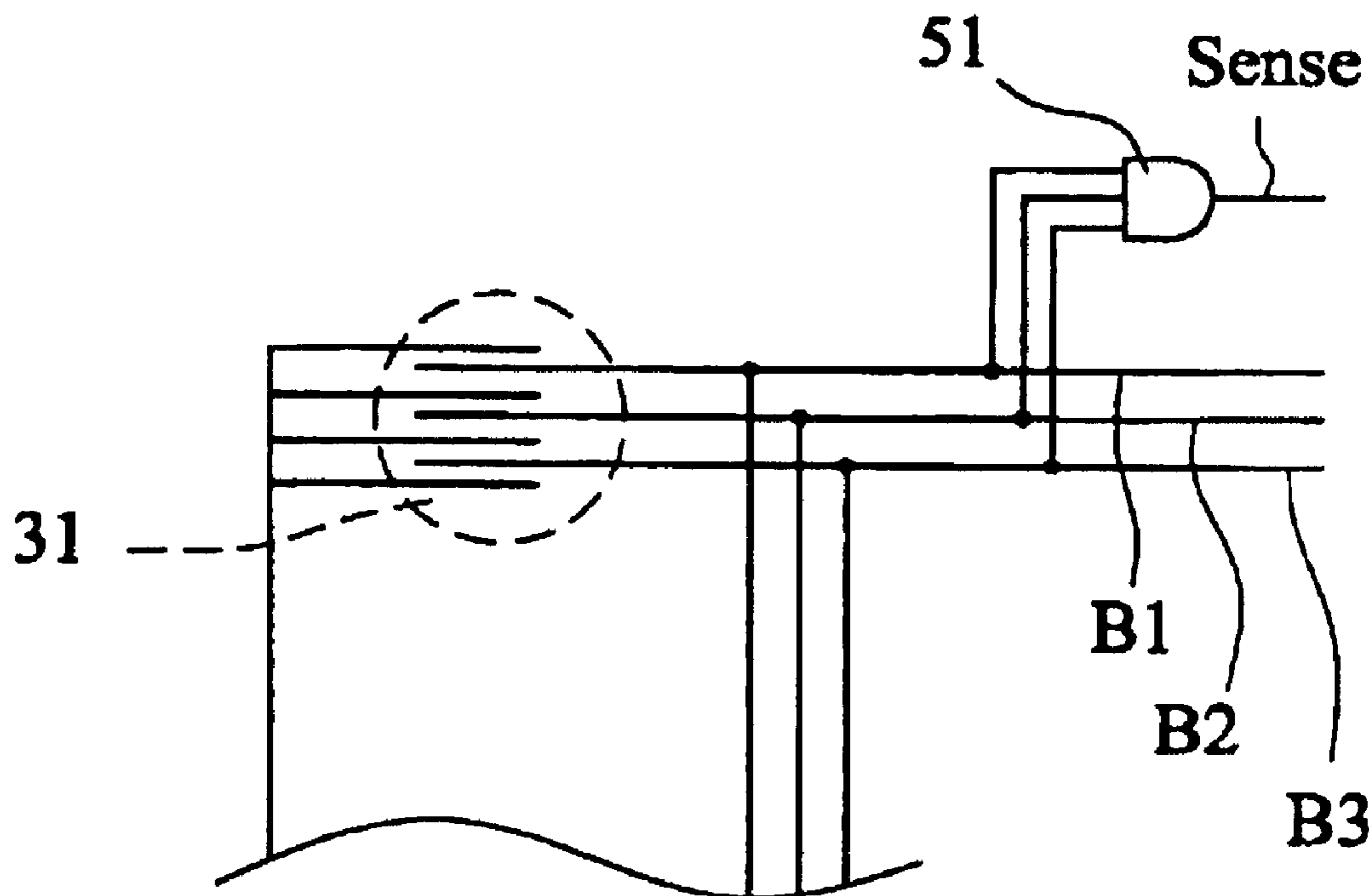
(58) **Field of Classification Search** ..... **341/22, 341/26; 200/5 A; 400/472, 477**  
See application file for complete search history.

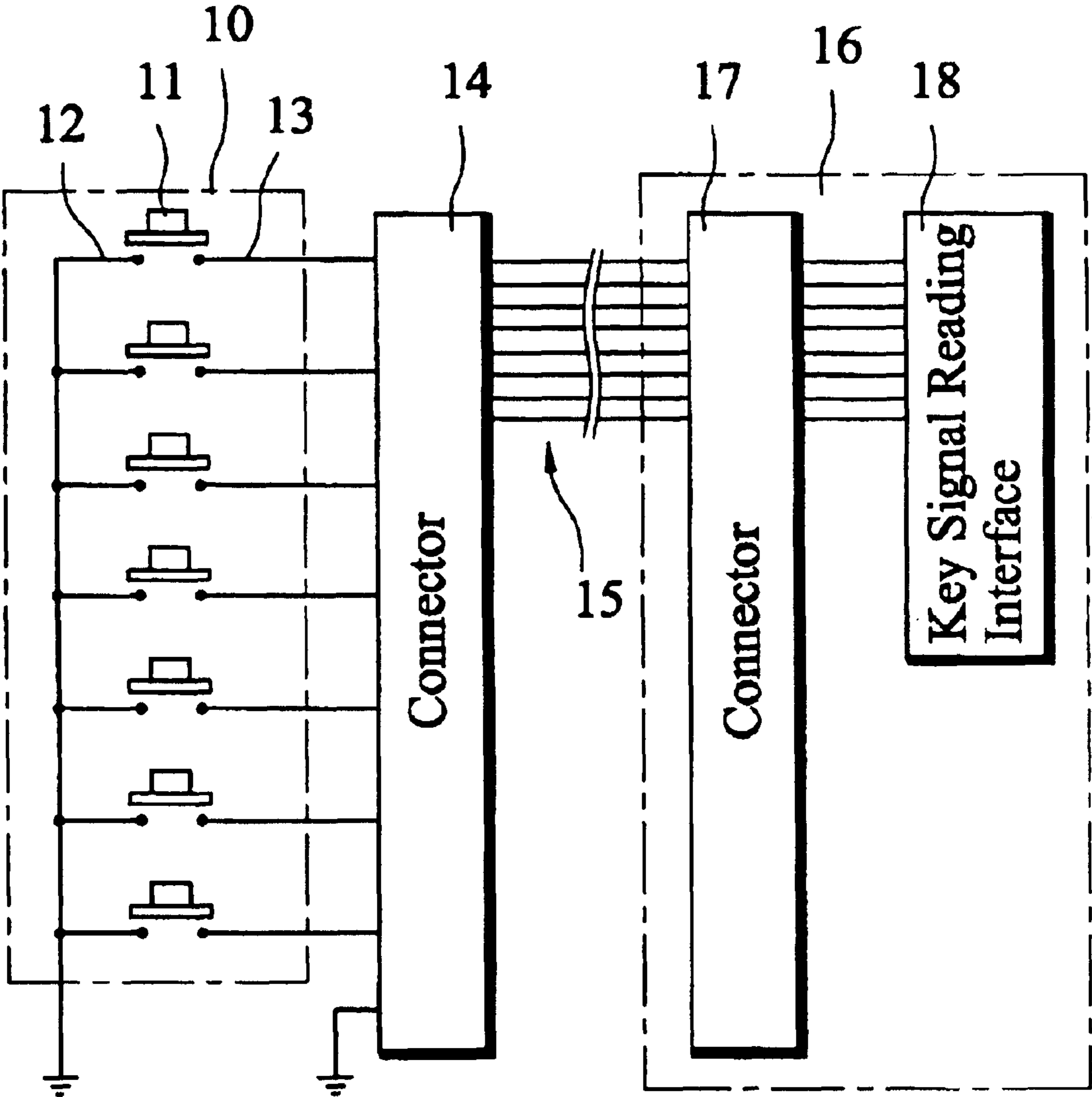
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**25 Claims, 5 Drawing Sheets**





*FIG. 1 (Prior Art)*



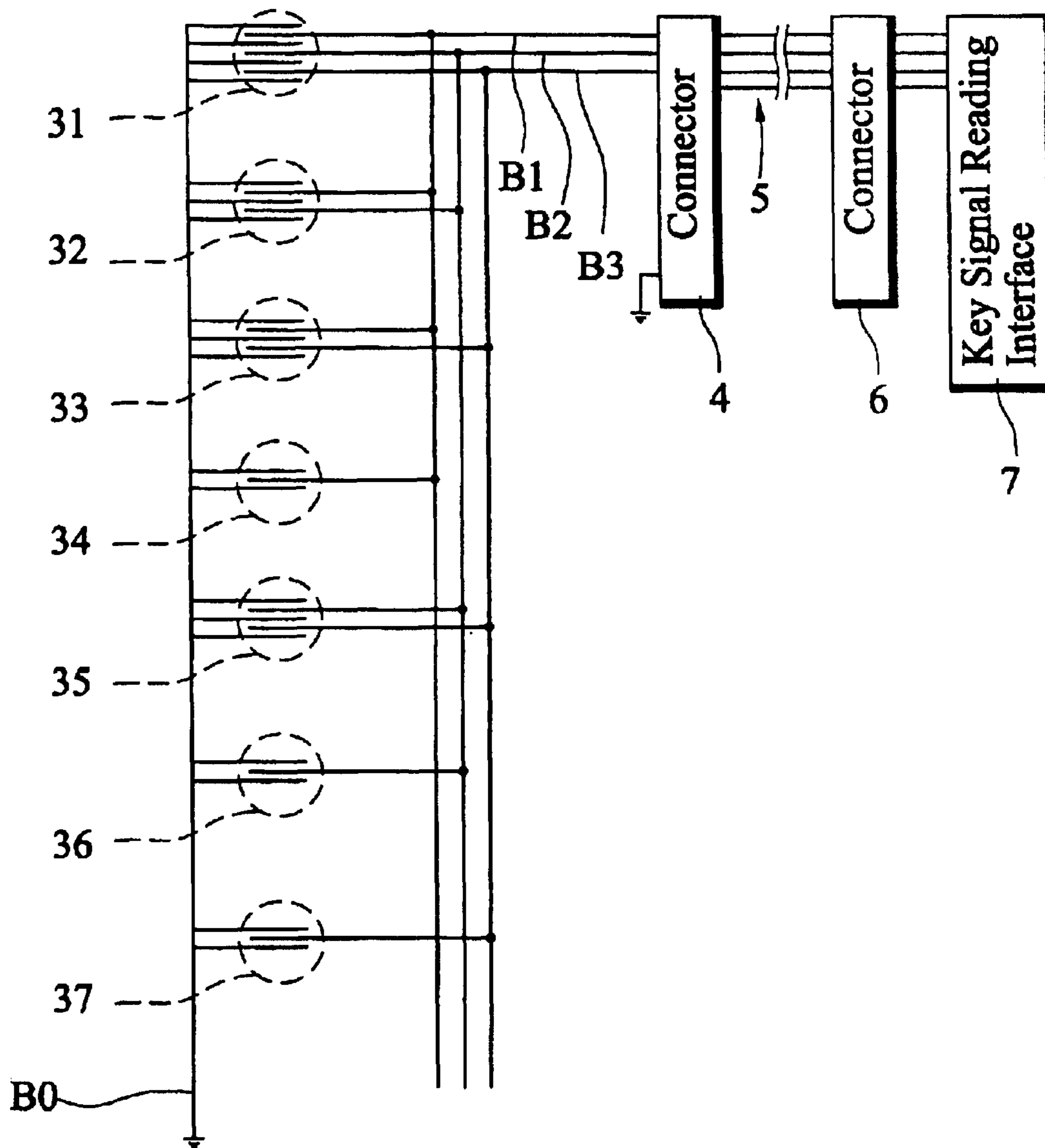
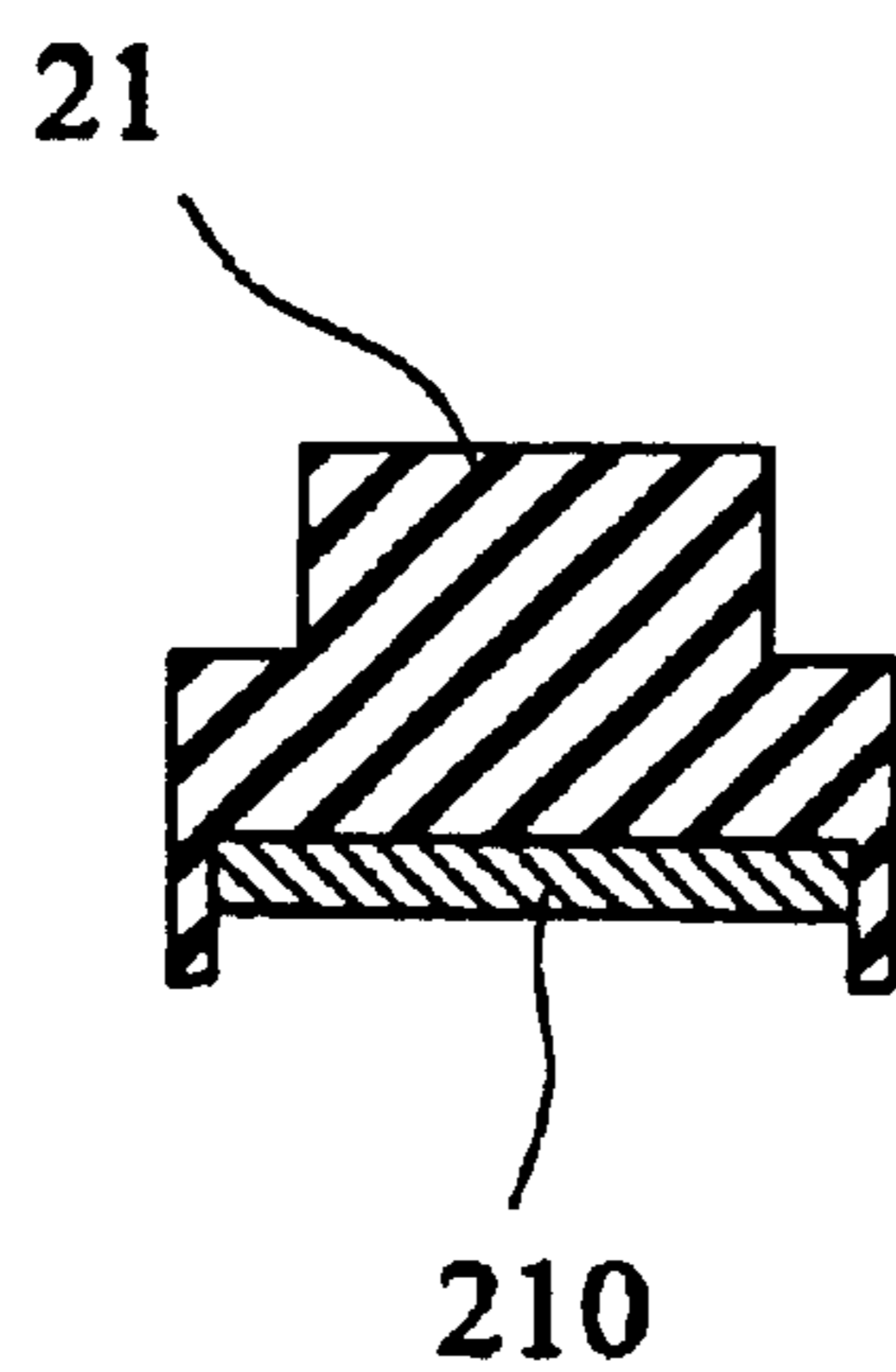
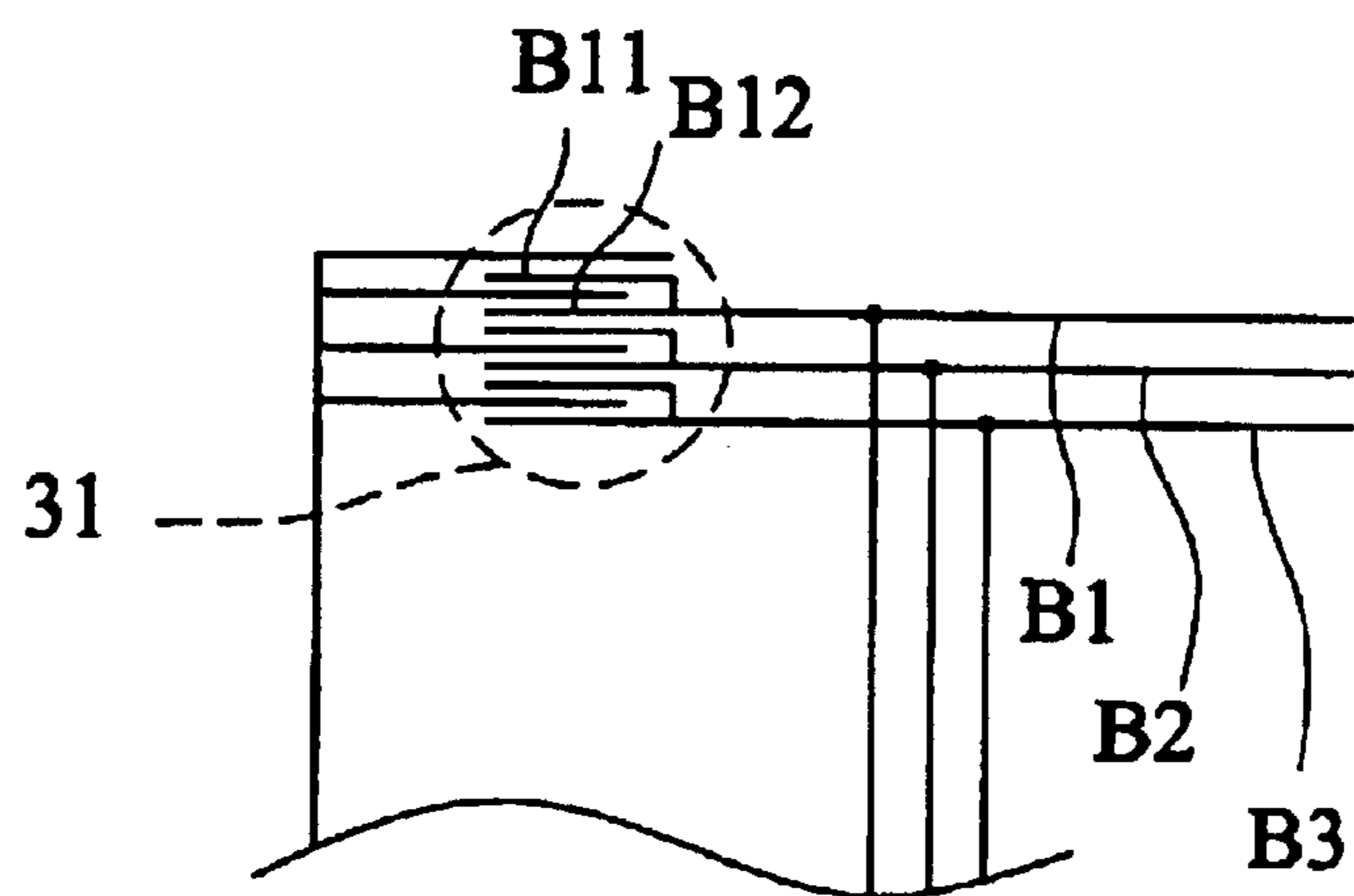


FIG.3



**FIG. 4**



**FIG. 5**

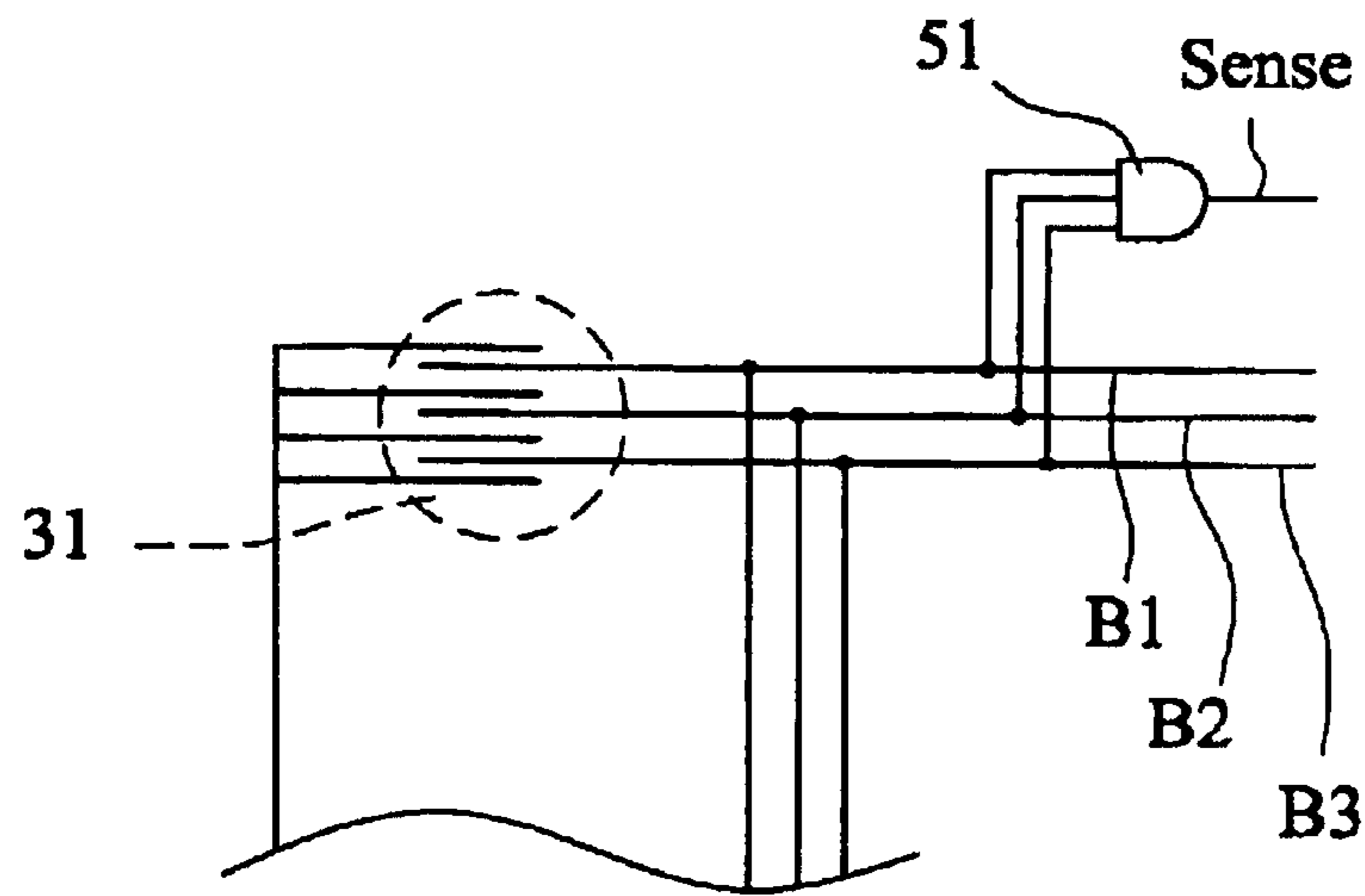


FIG. 6

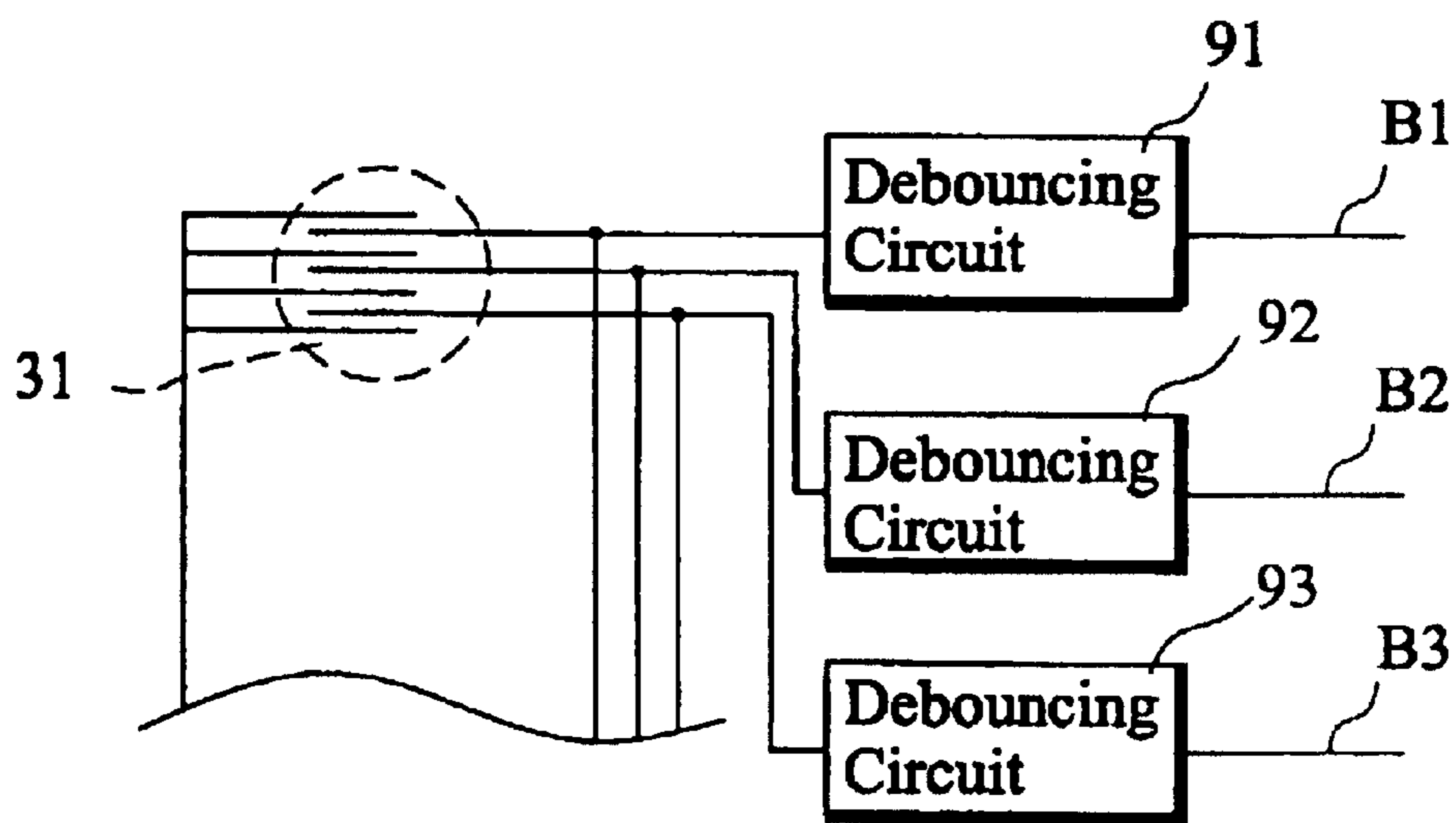


FIG. 7

## CIRCUIT LAYOUT ARRANGEMENT FOR KEY SWITCH SIGNAL RECOGNITION

**Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.**

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

The present invention relates to a key switch signal recognition circuit, and more particularly to a simple circuit layout of key switch signal recognition circuit.

#### 2. Description of the Prior Art

Key switch circuits are intensively used in office automation equipment, industrial instrument, electric and electronic consumers products, and electric home appliances to serve as input interface means between the user and the machine. According to the conventional key switch circuit designs, one key switch button is matched with one circuit loop. The key switch buttons can be switches, micro switches, and membrane switches.

FIG. 1 shows a prior art switch button type key switch signal recognition circuit including a number of key switches. According to this design, a number of key switch contact areas may be arranged on a substrate **10** such as a printed circuit board, and a number of key switch buttons **11** are suspended above the key switch contact area. Each key switch contact area is generally formed of two corresponding copper foil wires **12** and **13**. One copper foil wire **12** is connected to a common point, such as a grounding terminal or a power source terminal. The other copper foil wire **13** is connected to a first connector **14**. The pins of the first connector **14** are respectively connected through a cable **15** to a second connector **17** mounted on a circuit board **16**. The second connector **17** of the circuit board **16** is further connected to a key switch signal reading interface **18** or a key switch signal processing circuit. According to this conventional key switch circuit design, a number of independent circuit loops are needed to transmit click signal from the key switch buttons, the cable **15** must have a number of wires, and the connectors **14** and **17** each must have a number of pins and one grounding wire. Further, when the numbers of the key switch button are changed, the model of the connector, the number of wires of the cable, and the number of pins of the key switch signal reading interface must be relatively changed.

In some key switch circuit designs, an encoder is used to achieve the object of using a limited number of wires to recognize a number of key switch buttons. However, the use of the encoder greatly increases the cost of the key switch circuit. Therefore, these conventional key switch circuit designs do not satisfy current market requirements. For example, in the design of a key switch circuit for a scanner, the factors of ease of use, highly expandability, less number of component parts, and lost cost must be taken into account.

Therefore, it is desirable to provide an improved key switch signal recognition circuit to mitigate and/or obviate the aforementioned problems.

### SUMMARY OF THE INVENTION

Accordingly, the primary object of the present invention is to provide a key switch signal recognition circuit, which uses the architecture of a circuit layout to achieve accurate signal recognition of a number of key switch buttons, so that the

number of key switch contact wires, the number of wires of the cable, and the number of pins of the related connector can be minimized.

It is another object of the present invention to provide a key switch signal recognition circuit, which uses a limited number of wires to achieve signal recognition of a number of key switch buttons. No signal encoder is required.

The present invention will be apparent to those skilled in the art by reading the following description of preferred embodiments thereof, with reference to the accompanying drawings, in which:

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a circuit diagram of a key switch signal recognition circuit according to the prior art;

FIG. 2 is an exploded view of a key switch signal recognition circuit according to the present invention;

FIG. 3 shows a circuit layout in accordance with a first embodiment of the present invention;

FIG. 4 is a cross sectional view of the key switch button taken along line 1—1 of FIG. 2;

FIG. 5 is a circuit layout of a second embodiment of the present invention;

FIG. 6 is a circuit layout of a third embodiment of the present invention, showing the key switch signal output lines respectively connected to an input of an AND gate; and

FIG. 7 is a circuit layout of a fourth embodiment of the present invention showing each of the key switch signal output lines is further connected with a debouncing circuit.

### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 2 is an exploded view of the key switch signal recognition circuit of the present invention. FIG. 3 shows the circuit layout in accordance with the first embodiment of the present invention. As illustrated, the key switch signal recognition circuit comprises for example seven key switch buttons **21~27**, and three [keys witch] *key switch* signal output lines **B1~B3**.

Each key switch button is provided with an electrically conductive *element*. FIG. 4 is a cross sectional view of the key switch button, taken along line 1—1 of FIG. 2, showing that an electrically conductive element **210** is mounted at the bottom side of the key switch button **21**. The electrically conductive element **210** is preferably made of electrically conductive rubber.

During installation, the key switch buttons **21~27** are mounted in respective through holes **21a~27a** arranged on a frame **2** corresponding to respective contact areas **31~37** arranged on a substrate **3** below the frame **2**. A connector **4** is mounted on the substrate **3**, having a set of pins respectively connected to the key switch signal output lines **B1~B3**.

When clicking either of the key switch buttons **21~27**, the corresponding contact area of the substrate **3** is triggered to output a signal to the corresponding pin of the connector **4** through the key switch signal output line **B1~B3**.

According to the present design, each contact area of the substrate comprises a first wire set and a second wire set. The first wire set comprises at least one wire. Each wire of the first wire set has one end connected to a common line. The other end of each wire of the first wire set is an open end. The second wire set comprises at least one wire respectively disposed in parallel to and electrically insulated from the at least one wire of the first wire set. The other end of

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each wire of the second wire set is respectively connected to an assigned bit line, which is selected subject to a bit encoding mode. The bit-encoding mode can be known BCD code or any suitable encoding format.

Therefore, when depressing one key switch button to touch the corresponding contact area, the respective electrically conductive element electrically connects the first wire set and second wire set of the touched contact area, causing the respective key switch signal output line to send a key switch signal corresponding to the depressed key switch button.

As illustrated in FIG. 3, the wires of the first wire set (left-sided wires) of the first contact area 31 are connected to a common line B0. The second wire set (the right-sided wires) of the first contact area 31 includes three wires respectively connected to key switch signal output lines B1, B2 and B3. The right side of the first wire set of the first contact area 31 is an open side. The left side of the second wire set of the first contact area 31 is also an open side. The wires of the first wire set of the first contact area 31 are disposed in parallel to and electrically insulated from the wires of the second wire set of the first contact area 31.

The wires of the first wire set (left-sided wires) of the second contact area 32 are connected to the aforesaid common line B0. The second wire set (the right-sided wires) of the second contact area 32 includes two wires respectively connected to the first and second key switch signal output lines B1 and B2. The wires of the first wire set of the second contact area 32 are disposed in parallel to and electrically insulated from the wires of the second wire set of the second contact area 32.

The wires of the first wire set (left-sided wires) of the third contact area 33 are connected to the aforesaid common line B0. The second wire set (the right-sided wires) of the third contact area 33 includes two wires respectively connected to the first and third key switch signal output lines B1 and B3. The wires of the first wire set of the third contact area 33 are disposed in parallel to and electrically insulated from the wires of the second wire set of the third contact area 33.

The wires of the first wire set (left-sided wires) of the fourth contact area 34 are connected to the aforesaid common line B0. The second wire set (the right-sided wires) of the fourth contact area 34 includes one wire connected to the first key switch signal output line B1. The wires of the first wire set of the fourth contact area 34 are disposed in parallel to and electrically insulated from the wires of the second wire set of the fourth contact area 34.

The wires of the first wire set (left-sided wires) of the fifth contact area 35 are connected to the aforesaid common line B0. The second wire set (the right-sided wires) of the fifth contact area 35 includes two wires respectively connected to the second and third key switch signal output lines B2 and B3. The wires of the first wire set of the fifth contact area 35 are disposed in parallel to and electrically insulated from the wires of the second wire set of the fifth contact area 35.

The wires of the first wire set (left-sided wires) of the sixth contact area 36 are connected to the aforesaid common line B0. The second wire set (the right-sided wires) of the sixth contact area 36 includes one wire connected to the second key switch signal output line B2. The wires of the first wire set of the sixth contact area 36 are disposed in parallel to and electrically insulated from the wires of the second wire set of the sixth contact area 36.

The wires of the first wire set (left-sided wires) of the seventh contact area 37 are connected to the aforesaid common line B0. The second wire set (the right-sided wires) of

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the seventh contact area 37 includes one wire connected to the third key switch signal output lines B3. The wires of the first wire set of the seventh contact area 37 are disposed in parallel to and electrically insulated from the wires of the second wire set of the seventh contact area 37.

Subject to the aforesaid circuit layout, a bit definition table illustrating the relation between the key switch buttons and the bit codes for the key switch signal recognition is obtained as shown in TABLE 1:

TABLE 1

Key switch	Bit definition		
	B1-bit	B2-bit	B3-bit
7	0	0	0
6	0	0	1
5	0	1	0
4	0	1	1
3	1	0	0
2	1	0	1
1	1	1	0

It is noted that the present invention requires only three bit lines (key switch signal output lines B1, B2, B3) for recognizing signals from the seven key switch buttons 21~27 without the use of any encoding circuit or encoder.

In actual practice, the key switch signal output lines B1, B2 and B3 are connected to the respective pins of the connector 4, and the connector 4 is connected to a cable 5. According to the preferred embodiment of the present invention, the cable 5 comprises three signal lines and one grounding line. A second connector 6 is used to connect the cable 5 to a circuit board or signal-reading interface 7.

FIG. 5 shows a second embodiment of the present invention. According to this embodiment, the wires of the first wire set (left-sided wires) of the first contact area 31 are connected to the common line B0, the three wires of the second wire set (right-sided wires) of the first contact area 31 each has one end respectively connected to the first, second and third key switch signal output lines B1, B2 and B3 and an opposite end terminating in two parallel end portions B11 and B12 disposed in parallel to and electrically insulated from the wires of the first set of the first contact area 31.

FIG. 6 shows a third embodiment of the present invention. According to this embodiment, the first, second and third key switch signal output lines B1, B2 and B3 are respectively connected to the signal input end of a respective AND gate 51. The AND gate 51 is induced to output a triggering signal Sense to the key switch signal reading circuit (not shown) when the corresponding key switch signal output line B1, B2 or B3 is logically high.

FIG. 7 shows a fourth embodiment of the present invention. According to this embodiment, the first, second and third key switch signal output lines B1, B2 and B3 are respectively connected to respective debouncing circuits 91, 92 and 93 capable of preventing the respective key switch signal output line to output an unusable signal at the initial stage when the respective key switch button is depressed.

Although the present invention has been described with reference to the preferred embodiments, it is apparent to those skilled in the art that a variety of modifications and changes may be made without departing from the scope of the present invention which is intended to be defined by the appended claims.



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What is claimed is:

1. A key switch signal recognition circuit comprising:  
a plurality of key switch buttons, said key switch buttons  
each provided with an electrically conductive element;  
a plurality of key switch key signal output lines;  
an AND gate having an output and a plurality of inputs  
respectively connected to said plurality of key switch  
key signal output lines; and

a plurality of contact areas arranged on a substrate corre-  
sponding to said key switch buttons, said contact areas  
each comprising a first wire set and a second wire set,  
said first wire set comprising at least one wire having  
one end connected to a common line and an opposite  
end forming an open end, said second wire set compris-  
ing at least one wire respectively disposed in parallel to  
and electrically insulated from the wire of said first  
wire set, the wire of said second wire set being respec-  
tively connected to the key switch signal output line  
which is selected subject to a predetermined bit encod-  
ing mode;

when one of said key switch buttons is depressed to touch  
the corresponding contact area, the electrically conduc-  
tive element of the depressed key switch button electri-  
cally connects the first wire set and second wire set of  
the touched contact area, causing the respective key  
switch signal output line to send a key switch signal  
corresponding to the depressed key switch button, said  
output of said [And] AND gate outputting a triggering  
signal responsive to the key switch signal output line of  
a corresponding contact area is at a logically high level.

2. The key switch signal recognition circuit of claim 1,  
wherein said bit encoding mode is a BCD encoding format.

3. The key switch signal recognition circuit of claim 1,  
wherein said key switch signal output lines comprises a  
grounding wire.

4. The key switch signal recognition circuit of claim 1,  
wherein the open end of the wire of the first wire set and the  
second wire set is terminated into two parallel end portions.

5. The key switch signal recognition circuit of claim 1,  
wherein the key switch signal output lines are further respec-  
tively connected to a debouncing circuit.

6. *An apparatus comprising:*

*two or more key switch buttons;*

*two or more key switch signal output lines;*

*an AND gate having an output and a plurality of inputs  
respectively connected to said two or more key switch  
signal output lines; and*

*two or more contact areas corresponding to said two or  
more key switch buttons, said contact areas connected  
to at least one of said two or more key switch signal  
output lines, and configured to cause at least one of  
said two or more key switch signal output lines to send  
a key switch signal in response to a depressed corre-  
sponding key switch button, wherein at least one of said  
two or more contact areas is connected to only one of  
said two or more output lines, wherein at least one of  
said two or more contact areas is connected to two or  
more of said two or more output lines, and*

*wherein said AND gate is configured to output a trigger-  
ing signal if the key switch signal output line of a corre-  
sponding contact area is at a logically high level.*

7. *The apparatus of claim 6, wherein said two or more key  
switch buttons are greater in number than said two or more  
key switch signal output lines.*

8. *The apparatus of claim 6, wherein said two or more key  
switch buttons comprise an electrically conductive element,*

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*said electrically conductive element configured to electri-  
cally connect a first wire set and a second wire set of at least  
one of said two or more contact areas if one of said two or  
more key switch buttons is depressed, said first wire set com-  
prising at least one wire having one end connected to a  
common line and an opposite end forming an open end, and  
said second wire set connected to at least one of said two or  
more key switch signal output lines.*

9. *The apparatus of claim 8, wherein said first wire set and  
said second wire set of said at least one of said two or more  
contact areas are connected to said two or more key switch  
signal output lines according to a predetermined bit encod-  
ing mode.*

10. *The apparatus of claim 9, wherein said bit encoding  
mode comprises a BCD encoding format.*

11. *The apparatus of claim 6, wherein said two or more  
key switch signal output lines comprise a grounding wire.*

12. *The apparatus of claim 6, wherein said two or more  
contact areas are arranged on a substrate, said two or more  
contact areas comprising a first wire set and a second wire  
set, said first wire set comprising at least one wire having  
one end connected to a common line and an opposite end  
forming an open end, said second wire set comprising at  
least one wire respectively disposed in parallel to and elec-  
trically insulated from the wire of said first wire set, the wire  
of said second wire set being respectively connected to at  
least one of said two or more key switch signal output lines.*

13. *The apparatus of claim 12, wherein the open end of  
the wire of the first wire set and the second wire set is termi-  
nated into two parallel end portions.*

14. *The apparatus of claim 6, wherein said two or more  
key switch signal output lines are connected to a debouncing  
circuit.*

15. *A method comprising:*

*causing at least one of two or more key switch signal  
output lines to send a key switch signal in response to a  
depressed corresponding key switch button, wherein at  
least one of two or more contact areas corresponding to  
said two or more key switch buttons is connected to only  
one of said two or more key switch signal output lines,  
and wherein at least one of said two or more contact  
areas is connected to two or more key switch signal  
output lines;*

*receiving said key switch signal via at least one of two or  
more inputs of an AND gate connected to said two or  
more key switch signal output lines; and*

*outputting a triggering signal at least via an output of said  
AND gate if the key switch signal output line is at a  
logically high level.*

16. *The method of claim 15, wherein said key switch sig-  
nal is sent at least via said two or more key switch signal  
output lines, and wherein said two or more key switch but-  
tons are greater in number than said two or more key switch  
signal output lines.*

17. *A method of claim 15, further comprising processing  
said key switch signal of said two or more key switch signal  
output lines at least via a bit encoding mode.*

18. *The method of claim 17, wherein said bit encoding  
mode comprises a BCD encoding format.*

19. *The method of claim 15, further comprising touching a  
contact area corresponding to at least one of said two or  
more key switch buttons if at least one of said two or more  
key switch buttons is depressed to cause at least one of two  
or more key switch signal output lines to send said key switch  
signal.*

20. *The method of claim 15, further comprising process-  
ing said key switch signal of said two or more key switch  
signal output lines at least via a debouncing circuit.*

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21. The key switch signal recognition circuit of claim 1, wherein at least one of said plurality of contact areas is connected to the key switch signal output line by only one wire of said second wire set, and wherein at least one of said plurality of contact areas is connected to the key switch signal output line by two or more wires of said second wire set. 5

22. An apparatus comprising:

key switch signal output line means for sending a key switch signal;

key switch button means for switching said key switch signal output line means; 10

an AND gate means having an output and a plurality of inputs respectively for connecting to said key switch signal output line means; and

contact area means corresponding to said key switch button means, said contact area means connected to at least one of said key switch signal output line means, and said contact area means configured to cause at least one of said key switch signal output line means to send a key switch signal in response to a depressed corresponding key switch button means, wherein at 20

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least one of said contact area means is connected to only one of said key switch signal output line means, wherein at least one of said contact area means is connected to two or more of said key switch signal output line means, and

wherein said AND gate means is further configured to output a triggering signal if the key switch signal output line means of a corresponding contact area means is at a logically high level.

23. The apparatus of claim 22, further comprising means for processing said key switch signal of said two or more key switch signal output lines at least via a bit encoding mode.

24. The apparatus of claim 23, wherein said bit encoding mode comprises a BCD encoding format.

25. The apparatus of claim 22, further comprising means for processing said key switch signal of said key switch signal output line means to prevent the respective key switch signal output line means to output an unstable signal.

\* \* \* \* \*

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : RE 41,017 E  
APPLICATION NO. : 11/337222  
DATED : December 1, 2009  
INVENTOR(S) : Chiu et al.

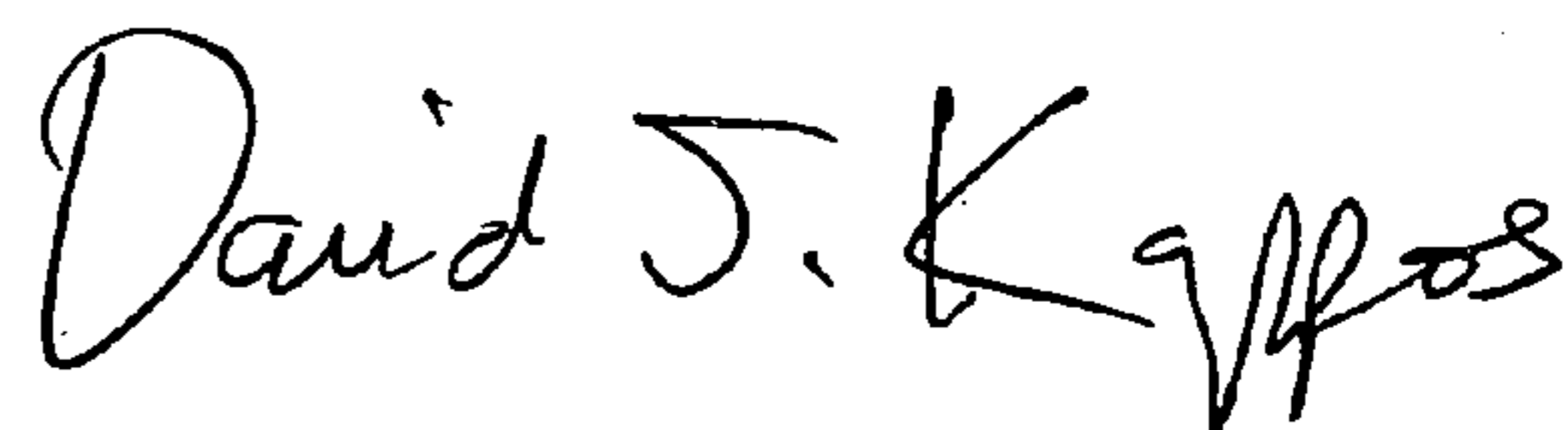
Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

At column 6, line 54, please replace "A method of" with --The method of--.

Signed and Sealed this

Nineteenth Day of October, 2010

A handwritten signature in black ink that reads "David J. Kappos". The signature is written in a cursive style with a large, stylized 'D' and 'K'.

David J. Kappos  
*Director of the United States Patent and Trademark Office*