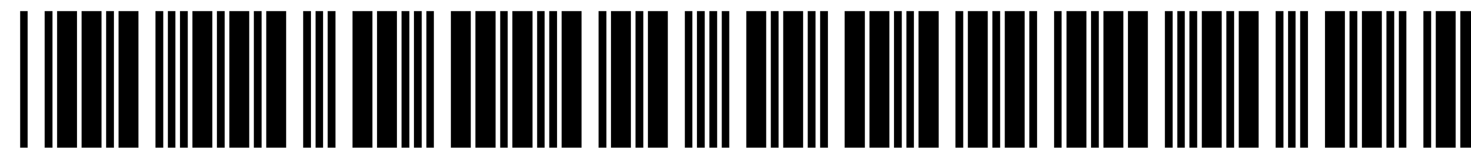

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(54) **METHOD TO PLATE C4 TO COPPER STUD**

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(*) Notice: This patent is subject to a terminal disclaimer.

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Related U.S. Patent Documents

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Issued: **Oct. 2, 2001**
Appl. No.: **09/389,232**
Filed: **Sep. 3, 1999**

U.S. Applications:
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(51) **Int. Cl.**
H01L 21/44 (2006.01)

(52) **U.S. Cl.** **438/612**; 438/613; 438/614; 438/627; 438/629; 438/637; 438/643; 438/653; 438/674; 438/675; 438/676; 438/677; 438/678; 438/687

(58) **Field of Classification Search** 438/612
See application file for complete search history.

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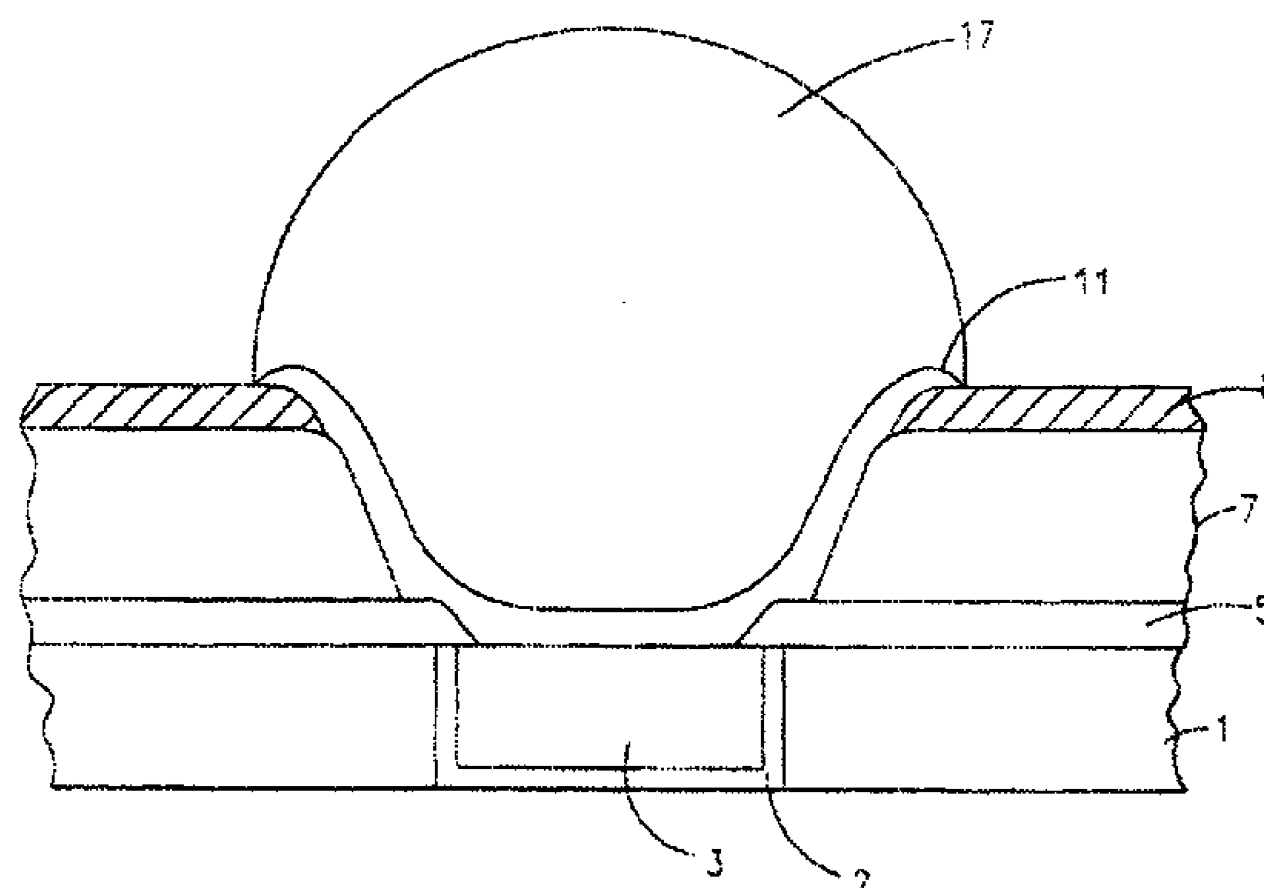
(57) **ABSTRACT**

A method for plating a second metal directly to a first metal without utilizing a mask. A semiconductor substrate is provided including at least one metal feature and at least one insulating layer covering the metal feature and the substrate. At least one recess is formed in the at least one insulating layer thereby exposing at least a portion of the metal feature. At least one conductive barrier layer is formed over the insulating layer and the exposed portion of the metal feature. A plating seed layer of a first metal is formed over the at least one barrier layer. A photoresist layer is deposited over the plating seed layer. Portions of the photoresist layer and portions of the plating seed layer outside of the at least one recess are removed. Photoresist remaining in the at least one recess is removed. A second metal is electroplated to the plating seed layer in the recess, using the barrier layer to conduct electrical current.

62 Claims, 2 Drawing Sheets



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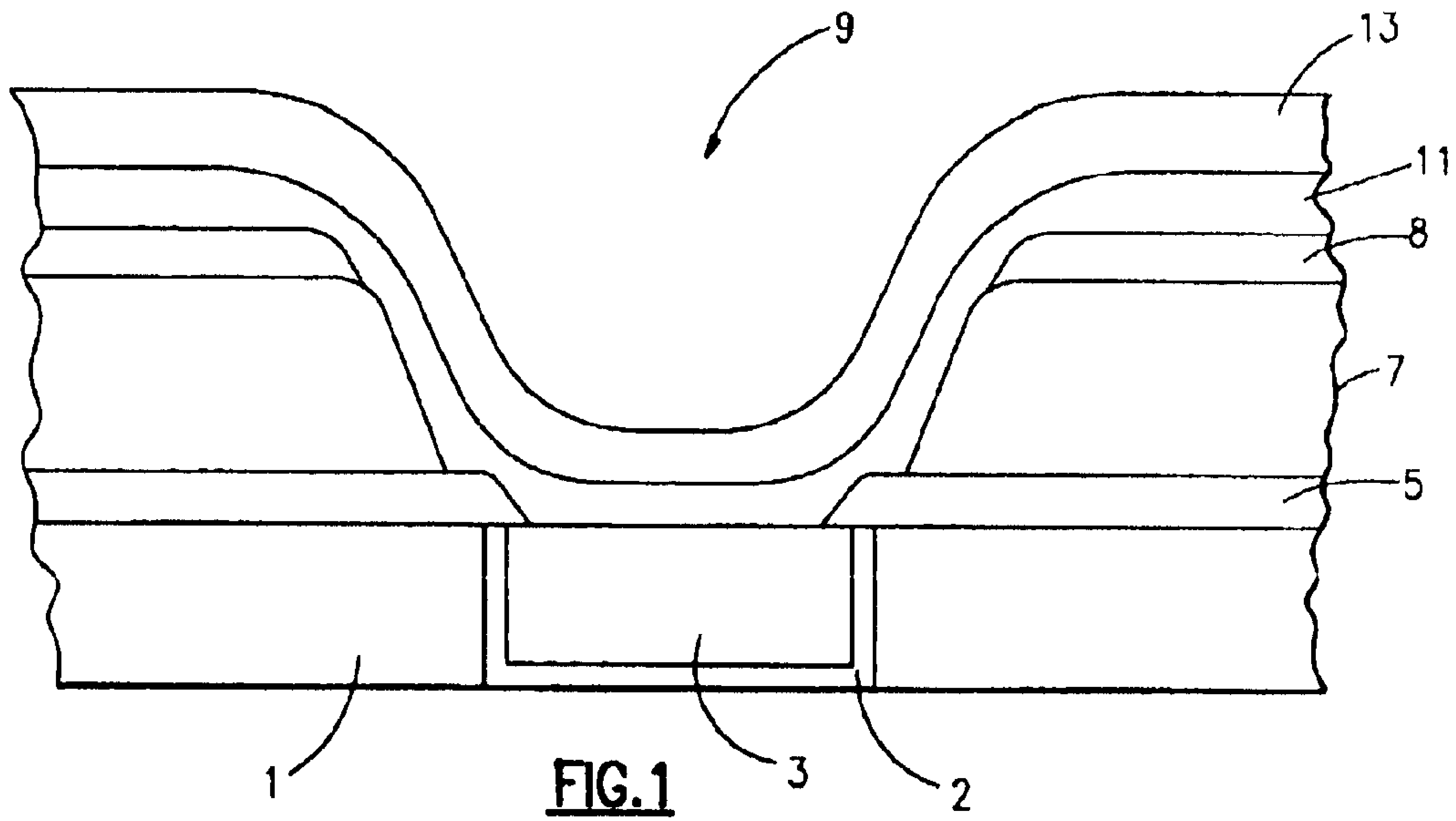

FIG. 1

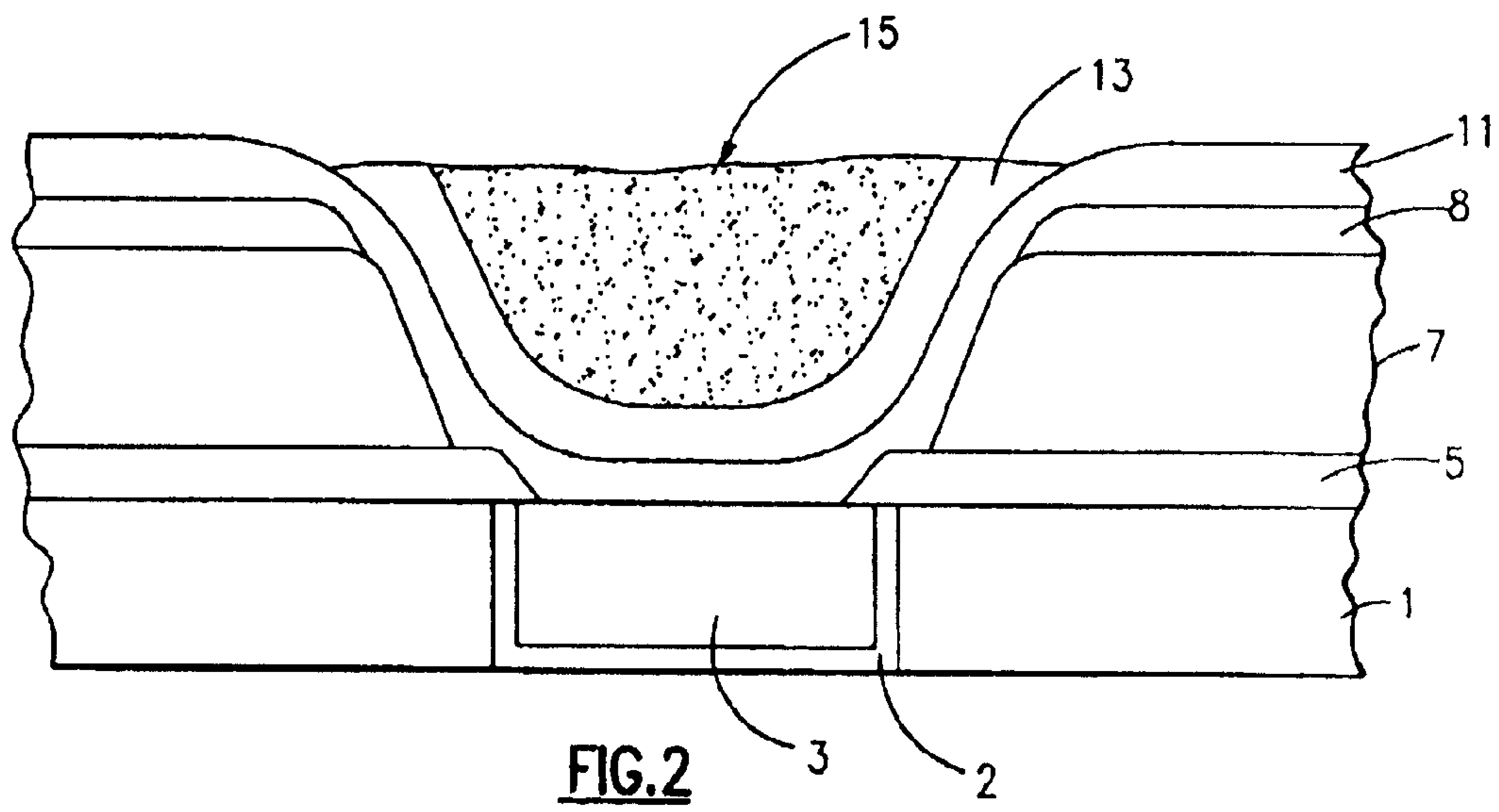

FIG. 2

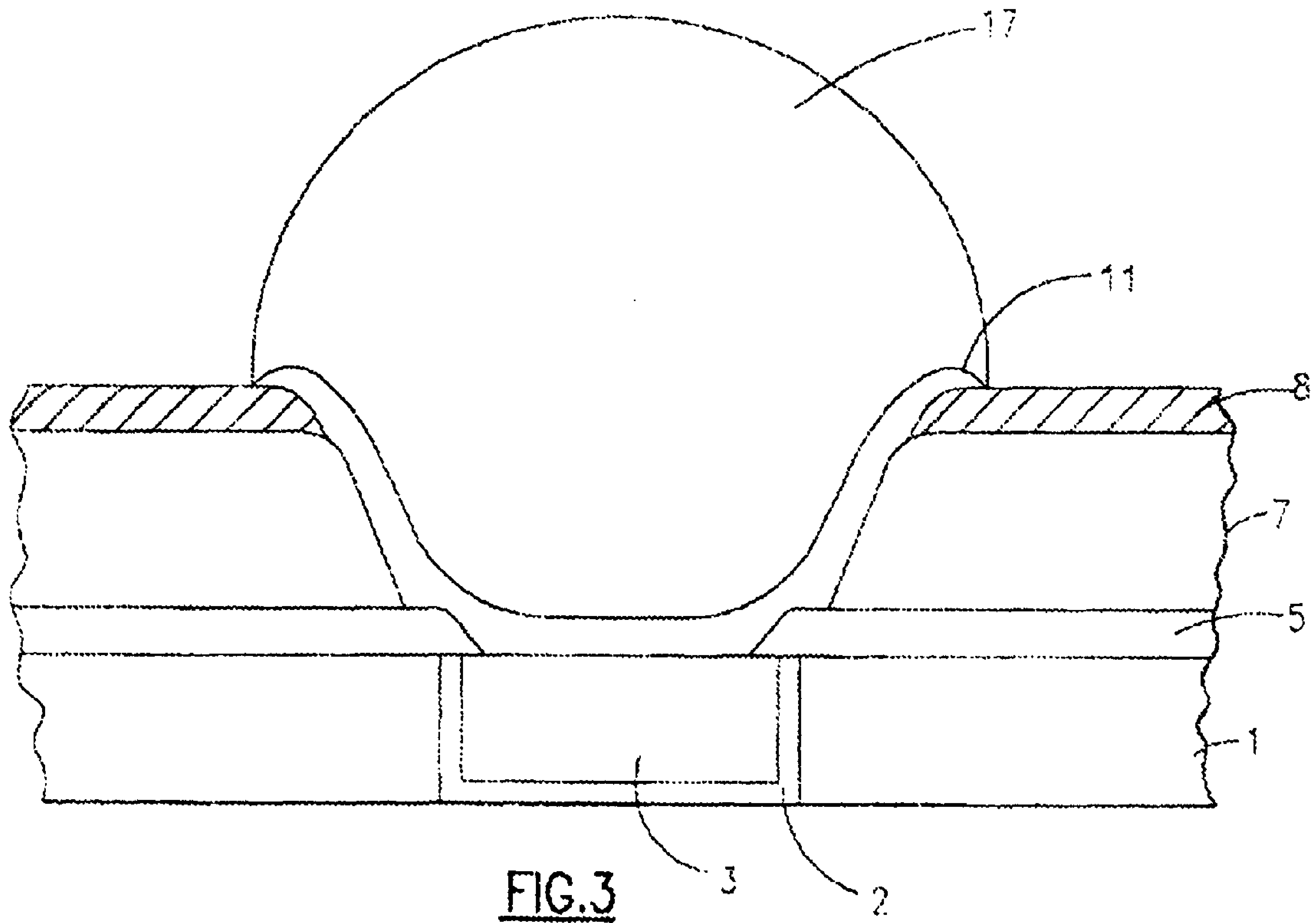

FIG.3

AMENDED

METHOD TO PLATE C4 TO COPPER STUD

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

RELATED APPLICATIONS

This application is a divisional application of application Ser. No. 09/004,808 filed Jan. 9, 1998 now U.S. Pat. No. 6,251,528.

TECHNICAL FIELD

The present invention relates to a process for plating a conductive material to a conductive feature in and/or on a substrate. More particularly, the present invention concerns electroplating a conductive material to a metal feature in and/or on a substrate using a highly conducting barrier film to conduct electrical current. In particular, the present invention provides methods for electroplating a solder ball utilized in a controlled collapse chip connection (C4) process to a metal feature provided in and/or on a substrate. Additionally, the present invention provides semiconductor structures prepared according to processes of the present invention.

BACKGROUND OF THE INVENTION

Various techniques have been investigated and utilized for attaching conductive material to semiconductor chips. These methods include the lift-off process, thru-mask methods, metal reactive ion etch (RIE) and metal and insulator damascene and various combinations of the above-listed methods. The lift-off and thru-mask methods are more valuable for large features, such as those typically encountered in chip packaging. Unlike the lift-off process and the thru-mask methods, the metal RIE and insulator damascene methods have been the process of choice for chip metallizations where the ground rules are typically below one micron.

In accordance with the damascene process, metal film may be deposited over the entire patterned substrate surfaces to fill trenches and vias. This metal deposition may then be followed by metal planarization to remove metal overburden and to isolate and define the wiring pattern. When metal deposition is by electroplating or by electroless plating processes, the plating may be preceded by the deposition of a plating base or seed layer over the entire surface of the patterned wafer or substrate. Also, layers that may improve adhesion, and/or prevent conductor/insulator interactions and/or interdiffusion may be deposited between the plating base or seed layer and the insulator.

In the metal RIE methods, blanket metal film is etched to define the conductor pattern. The gaps between the metal lines and vias are then filled with insulators. In high performance applications, the dielectric is planarized to define a flat metal level. One of the main advantages of the damascene process as compared to metal RIE is that it is often easier to etch an insulator as opposed to metal. Also, insulator gap fill and planarization may be more problematic.

In the metal damascene process, all the recesses in the insulator are first filled with metal before metal polishing. However, during the metal deposition into trenches and vias, all the narrower features become filled before their wider counterparts. Thus, all features with width less than 2 microns will be filled before those with width greater than 5 microns. Hence, to fill trenches or test pads with width of 50 microns, the smaller recesses typically with widths less than 5 microns are overplated. During metal chemical-mechanical polishing (CMP), the additional time needed to remove the excess metal overburden on the overplated smaller features causes dishing on the larger features. Also, because of the prolonged polishing times, insulator adjacent may severely erode. Severe dishing and insulator erosion in large metal features is a source of yield loss, especially when the occur at lower levels. Here they cause trapped metal defects at the next higher level. The longer time needed to remove the thicker metal overburden of the smallest metal lines and vias is one of the main culprits responsible for the low thruput and yield losses in the metal CMP process.

Moreover, this last metal wiring level, which may include Cu, Al, Au, Ni, W, α-Ta, and/or other metals and/or alloys with low resistivity, typically contains very wide metal lines for power bussing and large pads for wirebonds or C4 solder balls. In the CMP process, these relatively large metal structures are sensitive to dishing because of the prolonged polishing time.

After formation of wiring according to the above-described processes, further processing may be carried out on the substrate. For example, conductive elements, such as solder balls may be attached to portions of the wiring. One example of conductive elements that may be attached include solder balls for a C4 process.

Typically, patterns for a C4 process are created utilizing standard lithography techniques. According to such processes, a seed layer may be patterned, followed by lead-tin plating.

SUMMARY OF INVENTION

Broadly, an object of the present invention is to provide a process for selectively plating metal utilizing more than one metal as an electrode. One of the metals serves as a seed layer for plating and may be patterned. Another metal may act as a current carrying conductor during plating.

According to a particular application, an object of the present invention is to provide a process that permits attaching C4 solder balls directly to a final metal level in and/or on a substrate without requiring the utilization of a mask typical of traditional processes.

An advantage of the present invention is that it provides a less expensive process that known process for producing similar results.

Another advantage of the present invention is that it may utilize a barrier metal to carry plating current.

A further advantage of the present invention is that it may eliminate plating of metal on pins.

An additional advantage of the present invention is that *it* may provide higher productivity as compared to known processes.

In accordance with these and other objects and advantages, the present invention provides a method for plating a second metal directly to a first without utilizing a mask. A semiconductor substrate is provided including at least one metal feature of a first metal and at least one insulating layer covering said metal feature and the substrate. At least one recess is formed in the at least one insulating layer, thereby exposing at least a portion of the metal feature. At least one conductive barrier layer is formed over the insulating layer and the exposed portion of the metal feature. A plating seed layer is formed over the at least one barrier layer. A photoresist layer is deposited over the plating seed layer. Portions of the photoresist layer and portions of the plating seed layer

outside of the at least one recess are removed. Photoresist remaining in the at least one recess is removed. A second metal is plated to the plating seed layer in the recess.

Aspects of the present invention also provide a method for plating a second metal directly to a first metal without utilizing a mask. A semiconductor substrate is provided including at least one metal feature of a first metal and at least one insulating layer covering the metal feature and the substrate. At least one recess is formed in the at least one insulating layer, thereby exposing at least a portion of the metal feature. At least one conductive barrier layer is formed over the insulating layer and the exposed portion of the metal feature. A plating seed layer is formed over the at least one barrier layer. A pad is provided in the at least one recess for preventing removal of portions of the seed layer in the at least one recess. Portions of the photoresist layer and portions of the plating seed layer outside of the at least one recess are removed. The pad is removed. A second metal is electroplated to the plating seed layer in the recess.

Furthermore, aspects of the present invention provide a semiconductor structure including a semiconductor substrate. At least one metal feature of a first metal is provided in the substrate. At least one insulating layer at least partially covers the at least one metal feature. At least one recess is located in the at least one insulating layer over the at least one metal feature. At least one conductive barrier layer is located over the at least one electrical insulating layer and over a portion of the at least one metal feature under the at least one recess. At least one plating seed layer is located over a portion of the conductive barrier layer within the recess. A second metal is electroplated to the seed layer in the recesses.

Still other objects and advantages of the present invention will become readily apparent by those skilled in the art from the following detailed description, wherein it is shown and described only the preferred embodiments of the invention, simply by way of illustration of the best mode contemplated of carrying out the invention. As will be realized the invention is capable of other and different embodiments, and its several details are capable of modifications in various obvious respects, without departing from the invention. Accordingly, the description is to be regarded as illustrative in nature and not as restrictive.

SUMMARY OF THE DRAWINGS

The above objects and advantages of the present invention will be more clearly understood when considered in conjunction with the accompanying drawings, in which:

FIG. **1** represents a cross-sectional view of an embodiment of the present invention with a C4 opening etched over last metal;

FIG. **2** represents a cross-sectional view of an embodiment of the present invention illustrating a copper seedlayer after touch-up polishing to remove resist and copper seedlayer outside a depression, while leaving resist in the depression; and

FIG. **3** represents a cross-sectional view of an embodiment of the present invention illustrating a state in a process according to the present invention in which resist has been stripped, solder plated and reflowed, a barrier removed, copper seed layer consumed by solder reflow and a C4 ball arranged in a recess and joined to the structure.

BEST AND VARIOUS MODES FOR CARRYING OUT THE INVENTION

As described above, the present invention relates to electroplating a second metal on a metal feature of a first metal wherein the metal feature is arranged in and/or on a substrate. The present invention permits the second metal to be electroplated without utilizing a mask.

To carry out this process, methods of the present invention utilize a highly conducting barrier film alpha-Ta to carry current and selectively plate recesses in semiconducting and non-semiconducting substrates. The methods according to the present invention include providing a substrate. Various features may be provide in the substrate for accomplishing various tasks.

For example, the various features made of conductive material may be provided in and/or on the substrate. One example of such a feature is a metal last formed in the substrate. According to one example, the last is made of copper. However, as stated above, other features may be provided in the substrate having other forms and functions and made of other conductive materials.

Often, it is desired to attach devices, such as semiconductor chips, to a substrate, such as a chip carrier. A number of processes are available for attaching devices to a substrate. Many such processes may include providing electrical connections between a device and a substrate as well as attaching the device to the substrate.

An example of a device attachment method is the C4 process. This process is described in detail in U.S. Pat. No. 5,089,440 issued Feb. 18, 1992, to Christie et al., the entire disclosure of which is hereby incorporated by reference. Such methods are also described in U.S. Pat. Nos. 3,401,126 and 3,429,040 to Miller, the entire disclosure of which is hereby incorporated by reference. The present invention is particularly useful in such processes. However, usefulness of the present invention is by no means limited to such processes. In fact, the present invention may be useful in any application for selectively plating one metal to another metal utilizing more than one metal as an electrode.

According to the present invention, a conductive barrier film of α-Ta, TaN/α-Ta, α-Ta/TaN, or TaN/α-Ta/TaN with resistivity in the range of 14 to 50 micro-ohm cm is sputtered at least in at least one recess over a metal feature in a substrate. This is followed by the deposition of a plating base or seed layer over the barrier layer. A photoresist is deposited and patterned over the plating seed layer. The photoresist and seed layer are removed on all the field regions above the at least one recess, exposing the barrier layer. The photoresist remaining in the at least one recess is removed exposing the seed layer in the at least one recess. The substrate may then be electroplated, using the workpiece as the cathode. Accordingly, plating occurs on the seed layer in the at least one recess and not on other parts of the semiconductor substrate.

According to an alternate embodiment of the present invention, a barrier film of α-Ta, TaN/α-Ta, α-Ta/TaN, or TaN/α-Ta/TaN may be sputtered at least over the at least one recess in the substrate. A plating base or seed layer is deposited. The seed layer may then be polished off outside the at least one recess. The at least one recess may then be plated using the barrier film without seed layers at the periphery of the substrate wafers for electrical contact.

Further aspects of the present invention are concerned with semiconductor substrates that includes at least one semiconductor or circuit structure located on at least one of major surface.

In accordance with the present invention, as shown in FIG. **1**, a substrate **1** may be provided. Typical semiconductor substrates include silicon and group III-V semiconductors.

At least one feature made of a conducting material may be provided in and/or on the substrate. The substrate shown in FIG. **1** includes a last **3** formed in the substrate. The last in the substrate shown in FIG. **1** is copper. The last is surrounded by a layer **2** of an insulating material.

The substrate and the conductive feature may be covered by at least one layer of an electrically insulating material. The insulating layer be thermally grown or deposited such as by chemical vapor deposition or physical vapor deposition. Typically, the insulating layer is about 2000 to about 30,000 Å thick, and more typically about 4000 to about 20,000 Å thick.

In the embodiment shown in FIG. **1**, the substrate and the conductive feature are covered by an insulating layer made up of an oxide/nitride layer **5**. In the embodiment shown in FIG. **1**, a layer of polyimide **7** is deposited on the oxide/nitride layer **5**. A polyimide passivation **8** layer made of, for example, a nitride and/or another hard insulator, may be deposited over the polyimide. The passivation layer may help to prevent the polyimide layer from picking up moisture and/or scratches, for example.

In the particular application of the present invention shown in FIG. **1**, at least one recess **9** may be formed through the at least one insulating layer. The at least one recess is formed to as to expose at least a portion of the at least one conductive feature. Each conductive feature may have at least one recess formed exposing the conductive feature. More than one recess may be formed over some conductive features.

In the embodiment shown in FIG. **1**, the recess **9** exposes a portion of the last metal **3**. The recess may be formed according to known photolithography techniques. The recess may be formed during the deposition of the at least one insulating layer. Alternatively, the at least one recess may be formed in the at least one insulating layer after formation of the at least one insulating layer.

Next, a conductive barrier **11** may be provided over the insulating layer. Preferably, the conductive barrier may include a layer of tantalum nitride first sputter deposited over the insulating layer, the walls of the recess, and the exposed conductive feature to a thickness of about 15 Å to about 500 Å and more typically to a thickness of about 50 to about 300 to act as adhesion promoting layer between the insulating layer and subsequently to be applied tantalum layer. Then, a tantalum layer may be sputtered over the layer of tantalum nitride, where it may form α-Ta spontaneously. Typically, the thickness of the tantalum layer is about 500 Å to about 3000 Å **[**A**]** and more typically about 1000 Å to about 2000 Å. Also, α-Ta may be deposited directly over the insulator by sputtering methods. Typically, the thickness of the α-Ta is about 500 Å to about 5000 Å, and more typically about 1000 Å to about 3000.

After the deposition of the barrier layer, a seed layer **13** may be deposited over the barrier layer **11** including on the walls and bottom of the recess(es). The preferred seed layer is copper, which can be deposited by sputtering or evaporation and preferably by sputtering. The copper may be sputtered employing temperatures of less than about 150° C., preferably less than about 100° C., such as about 100° C. to about −10° C. The sputtering may be carried out in the absence of an anneal. The sputtering is typically carried out to provide a seed layer of about 100 Å to about 2000 Å and preferably about 400 Å to about 1000 Å. Also, the copper seed layer may be deposited by CVD methods or by electroless plating method *or by an electrolytic plating method.*

After formation of the seed layer, a photoresist may *be* deposited over the seed layer. Any of the well known photosensitive resist materials known in the art can be employed. The resist is typically applied by spinning on or by spraying.

The photoresist employed can be a positive photoresist or a negative photoresist. A positive photoresist material is one which on exposure to imaging radiation, is capable of being rendered soluble in a solvent in which the unexposed resist is not soluble. A negative resist material is one which is capable of polymerizing and/or insolubilizing upon exposure to imaging radiation.

An example of a type of photoresist material is based upon phenolic-formaldehyde Novolak polymers. A particular example of such is Shipley AZ-1350 which is a m-cresol formaldehyde novolak polymer composition. Such is a positive resist composition and includes therein a diazo ketone such as 2-diazo-1-naphthol-5-sulfonic acid ester.

The photoresist may be selectively removed everywhere except for in the recess(es). The resist remaining in the recess(es) may **[**protects**]** *protect* the seed layer in the recesses (both the side walls and bottom of the recesses). The seed layer lying outside of the recesses may be removed simultaneously with the photoresist. Actually, since the seed layer lies under the photoresist, the seed layer may be removed subsequent to the removal of the photoresist. They may be removed by the same process.

Both the photoresist and the seed layer may be removed by a process such as chemical-mechanical polishing. The chemical-mechanical polishing may employ, for example, an aqueous polishing slurry containing abrasive particles such as colloidal silica.

Next, the portions **15** of the resist layer remaining in the recess(es) that protected the seed layer within the recesses from removal is removed. The resist may be removed by dissolving in a suitable solvent for the photoresist material.

According to an alternative embodiment, photoresist may not be utilized. Such an embodiment may utilize a very hard pad to prevent dishing of the seed layer in the depression. A hard polishing pad, such as IC 1000 or IC 100/Suba IV from Rodel Inc., may be used to polish off the seed layer. One possible disadvantage of not using photoresist is that slurry utilized in chemical-mechanical polishing techniques may enter the recess. The slurry typically would then need to be removed. One way to remove the slurry is in a megasonic cleaning solution.

After removal of the resist, if necessary, conductive metal **17**, such as lead-tin or other terminal metallurgies, is electroplated on the portions of the seed layer remaining in the recesses, to result in the structure shown in FIG. **3**. During the electroplating, the barrier layer **11** may act as a cathode terminal for carrying the electroplating current. For lead-tin solders, plating, commercial solder plating baths such as NF 800 HS or NF 72 BC from Technic Inc., Rhode Island, may be used. Other proprietary commercially available lead-tin solders, eutectic solders, lead-free solders and/or other platable terminal metallurgies may be utilized.

The electroplating is continued *until* a desired amount of the conductive metal is plated in the recess(es). This usually takes about 10 min. to about 90 min, more typically about 20 min. to about 75 min. The thickness of the electroplated metal or alloy is typically about 25μ to about 200μ, and more typically about 40μ to about 75μ.

In the case of exposed α-Ta, the metal being plated will not plate on the barrier layer due to the formation of a very thin oxide layer when contacting the electroplating bath. The oxide layer may be described as a "superficial" layer. This oxide layer will form naturally if the barrier layer is a tantalum layer such as that described above. In another

embodiment, the oxide layer may be formed by momentarily reversing the polarity of the field, rendering the workpiece anodic, prior to the electroplating. The polarity change may be brief, such as about 10 seconds. Formation of the oxide layer may also be described as "anodization". The current density should be such that at the end of the current reversal, sufficient copper is left in the recesses for plating to initiate.

Next, the barrier layer **11** may be removed down to the polyimide or polyimide passivation layer, after the solder reflow. The barrier layer may be removed by utilizing the electroplated metal as a mask.

According to the process of the present invention, no lithograph step is required to define the seed layer since the chemical-mechanical polishing step makes the seed layer self-aligning to the recess(es). Not requiring a lithographic step simplifies the process. Additionally, the process may be less costly as compared to typical lithographically defined C4 processes. This simplification and cost advantage may be realized in any process requiring similar selective plating of metal(s).

The foregoing description of the invention illustrates and describes the present invention. Additionally, the disclosure shows and describes only the preferred embodiments of the invention but, as mentioned above, it is to be understood that the invention is capable of use in various other combinations, modifications, and environments and is capable of changes or modifications within the scope of the inventive concept as expressed herein, commensurate with the above teachings and/or the skill or knowledge of the relevant art. The embodiments described hereinabove are further intended to explain best modes known of practicing the invention and to enable others skilled in the art to utilize the invention in such, or other, embodiments and with the various modifications required by the particular applications or uses of the invention. Accordingly, the description is not intended to limit the invention to the form disclosed herein. Also, it is intended that the appended claims be construed to include alternative embodiments.

What is claimed is:

1. A method for plating a second metal directly to a first metal, said method comprising**[**the steps of**]**:

providing a semiconductor substrate including at least one metal feature and at least one insulating layer covering said metal feature and said substrate;

forming at least one recess in said at least one insulating layer thereby exposing at least a portion of said metal feature;

forming at least one conductive barrier layer over said insulating layer and said exposed portion of said metal feature;

forming a plating seed layer of a first metal over said at least one barrier layer;

depositing a photoresist layer over said plating seed layer *and in said at least one recess*;

removing portions of said photoresist layer and portions of said plating seed layer outside of said at least one recess;

removing photoresist remaining in said at least one recess; and

electroplating a second metal to said plating seed layer in said recess without utilizing a *lithographic* mask.

2. The method according to claim **1**, wherein said metal feature is a metal last provided in said semiconductor substrate.

3. The method according to claim **1**, wherein said conductive barrier is provided by sputter deposition of a layer of at least one nitride of tantalum on said insulating layer and said exposed portion of said metal feature and subsequent sputter deposition of a layer of tantalum on said tantalum nitride layer, such that the **[**layer including the nitride of tantalum**]** *layer of tantalum on said tantalum nitride layer* is in the α-phase.

4. The method according to claim **3**, wherein said tantalum nitride layer is about 10 Å to about 1000 Å thick and said tantalum layer is about 500 Å to about 5000 Å thick.

5. The method according to claim **1**, wherein said seed layer is formed by electrolytic or electroless plating of said first metal.

6. The method according to claim **5**, wherein said seed layer is copper.

7. The method according to claim **6**, wherein said copper is sputter coated on said *conductive barrier* layer**[**of tantalum**]**.

8. The method according to claim **7**, wherein said layer of tantalum is α-Ta/TaN layer.

9. The method according to claim **6**, wherein said copper layer is about 1000 Å to about 20,000 Å thick.

10. The method according to claim **3**, wherein said tantalum is alpha tantalum.

11. The method of claim **3**, wherein said tantalum layer is TaN/α-Ta/TaN-laminate.

12. The method according to claim **1**, wherein said portions of said photoresist layer and said *plating* seed layer outside of said *at least one* recess are removed by chemical-mechanical polishing.

13. The method according to claim **1**, wherein said photoresist is spun on said plating seed layer.

14. The method according to claim **1**, wherein said barrier layer forms a conductor for said electroplating of said second metal.

15. The method according to claim **1**, wherein said second metal is a solder ball made of an alloy of lead and tin, plated lead-free solder or other platable terminal metallurgies.

16. The method according to claim **1**, further comprising **[**the step of**]**:

removing said at least one conductive barrier layer from horizontal portions between said**[**recesses**]** *at least one recess*.

17. The method according to claim **16**, wherein said electroplated second metal acts as a mask for the removal of said at least one conductive barrier layer.

18. The method according to claim **1**, wherein said at least one metal feature is formed in said substrate.

19. The method according to claim **1**, wherein said insulating layer includes a layer of an oxide and a nitride and at least one layer of a polyimide.

20. The method of claim **19**, further comprising**[**the step of**]**:

forming a layer of at least one nitride or other passivation layer over the polyimide.

21. The method according to claim **1**, wherein said second metal is a solder ball.

22. A method for plating a second metal directly to a first metal, said method comprising**[**the steps of**]**:

providing a semiconductor substrate including at least one metal feature and at least one insulating layer covering said metal feature and said substrate;

forming at least one recess in said at least one insulating layer thereby exposing at least a portion of said metal feature;

forming at least one conductive barrier layer over said insulating layer and said exposed portion of said metal feature;

forming a plating seed layer of a first metal over said at least one barrier layer;

providing a pad in said at least one recess for preventing removal of portions of said seed layer in said at least one recess;

removing portions of said plating seed layer outside of said at least one recess;

removing said pad; and

electroplating a second metal to said plating seed layer in said recess without utilizing a *lithographic* mask.

23. The method of claim **22**, further comprising[the step of]:

utilizing a hard polishing pad to remove said seed layer outside of said recess.

24. A method for plating a second metal directly to a first metal, said method comprising:

providing a semiconductor substrate including at least one metal feature and at least one insulating layer covering said metal feature and said substrate;

forming at least one recess in said at least one insulating layer thereby exposing at least a portion of said metal feature;

forming at least one conductive barrier layer over said insulating layer and said exposed portion of said metal feature;

forming a plating seed layer of a first metal over said at least one barrier layer;

removing portions of said plating seed layer outside of said at least one recess; and

electroplating a second metal to said plating seed layer in said recess without utilizing a lithographic mask.

25. The method according to claim 24, wherein said metal feature is a metal last provided in said semiconductor substrate.

26. The method according to claim 24, wherein said conductive barrier is provided by sputter deposition of a layer of at least one nitride of tantalum on said insulating layer and said exposed portion of said metal feature and subsequent sputter deposition of a layer of tantalum on said tantalum nitride layer, such that the layer including the nitride of tantalum is in the α-phase.

27. The method according to claim 26, wherein said tantalum nitride layer is about 10 Å to about 1000 Å thick and said tantalum layer is about 500 Å to about 5000 Å thick.

28. The method according to claim 24, wherein said seed layer is formed by electrolytic or electroless plating of said first metal.

29. The method according to claim 28, wherein said seed layer is copper.

30. The method according to claim 29, wherein said copper is sputter coated on said conductive barrier layer.

31. The method according to claim 30, wherein said layer of tantalum is α-Ta/TaN layer.

32. The method according to claim 28, wherein said copper layer is about 1000 Å to about 20,000 Å thick.

33. The method according to claim 26, wherein said tantalum is alpha tantalum.

34. The method of claim 26, wherein said tantalum layer is TaN/α-Ta/TaN-laminate.

35. The method according to claim 24, wherein said seed layer outside of said recess is removed by chemical-mechanical polishing.

36. The method according to claim 24, wherein said barrier.

37. The method according to claim 24, wherein said second metal is a solder ball made of an alloy of lead and tin, plated lead-free solder or other platable terminal metallurgies.

38. The method according to claim 24, further comprising:

removing said at least one conductive barrier layer from horizontal portions between said at least one recess.

39. The method according to claim 38, wherein said electroplated second metal acts as a mask for the removal of said at least one conductive barrier layer.

40. The method according to claim 24, wherein said at least one metal feature is formed in said substrate.

41. The method according to claim 24, wherein said insulating layer includes a layer of an oxide and a nitride and at least one layer of a polyimide.

42. The method of claim 41 further comprising

forming a layer of at least one nitride or other passivation layer over the polyimide.

43. The method according to claim 24, wherein said second metal is a solder ball.

44. The method according to claim 22, wherein said metal feature is a metal last provided in said semiconductor substrate.

45. The method according to claim 22, wherein said conductive barrier is provided by sputter deposition of a layer of at least one nitride of tantalum on said insulating layer and said exposed portion of said metal feature and subsequent sputter deposition of a layer of tantalum on said tantalum nitride layer, such that the layer including the nitride of tantalum is in the α-phase.

46. The method according to claim 45, wherein said tantalum nitride layer is about 10 Å to about 1000 Å thick and said tantalum layer is about 500 Å to about 5000 Å thick.

47. The method according to claim 22, wherein said seed layer is formed by electrolytic or electroless plating of said first metal.

48. The method according to claim 47, wherein said seed layer is copper.

49. The method according to claim 48, wherein said copper is sputter coated on said conductive barrier layer.

50. The method according to claim 49, wherein said layer of tantalum is α-Ta/TaN layer.

51. The method according to claim 48, wherein said copper layer is about 1000 Å to about 20,000 Å thick.

52. The method according to claim 45, wherein said tantalum is alpha tantalum.

53. The method of claim 45, wherein said tantalum layer is TaN/α-Ta/TaN-laminate.

54. The method according to claim 22, wherein said portions of said seed layer outside of said recess are removed by chemical-mechanical polishing.

55. The method according to claim 22, wherein said barrier layer forms a conductor for said electroplating of said second metal.

56. The method according to claim 22, wherein said second metal is a solder ball made of an alloy of lead and tin, plated lead-free solder or other platable terminal metallurgies.

57. The method according to claim 22, further comprising the step of:

removing said at least one conductive barrier layer from horizontal portions between said at least one recess.

58. The method according to claim 57, wherein said electroplated second metal acts as a mask for the removal of said at least one conductive barrier layer.

59. The method according to claim 22, wherein said at least one metal feature is formed in said substrate.

60. The method according to claim 22, wherein said insulating layer includes a layer of an oxide and a nitride and at least one layer of a polyimide.

61. The method of claim 60, further comprising:

forming a layer of at least one nitride or other passivation layer over the polyimide.

62. The method according to claim 22, wherein said second metal is a solder ball.

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