

US00RE40854E

(19) **United States**
(12) **Reissued Patent**
Iwadare

(10) **Patent Number:** **US RE40,854 E**
(45) **Date of Reissued Patent:** **Jul. 14, 2009**

(54) **FAST CALCULATION APPARATUS FOR CARRYING OUT A FORWARD AND AN INVERSE TRANSFORM**

(75) Inventor: **Masahiro Iwadare**, Tokyo (JP)

(73) Assignee: **NEC Corporation**, Tokyo (JP)

(21) Appl. No.: **10/642,968**

(22) Filed: **Aug. 19, 2003**

Related U.S. Patent Documents

Reissue of:

(64) Patent No.: **5,218,561**
Issued: **Jun. 8, 1993**
Appl. No.: **07/712,888**
Filed: **Jun. 12, 1991**

(30) **Foreign Application Priority Data**

Jun. 12, 1990 (JP) 2-151662

(51) **Int. Cl.**
G06F 17/14 (2006.01)

(52) **U.S. Cl.** **708/400; 708/402**

(58) **Field of Classification Search** **708/400, 708/401, 402, 403, 404**

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,109,417 A 4/1992 Fielder et al.

FOREIGN PATENT DOCUMENTS

DE 3506912 A1 8/1986
DE 3621513 A1 1/1988

OTHER PUBLICATIONS

H. Nussbaumer, "Fast Multidimensional Discrete Cosine Transforms", IBM Technical Disclosure Bulletin, vol. 23, No. 5, Oct. 1980, pp. 1976-1981.*

H. Nussbaumer, "Improved Approach for the Computation of Multidimensional Cosine Transforms", IBM Technical Disclosure Bulletin, vol. 23, No. 10, Mar. 1981, pp. 4517-4521.*

Schiller, N., "Overlapping Block Transform Image Coding Preserving Equal Number of Samples and Coefficients", SPIE vol. 1001 Visual Communications and Image Processing 1988, pp. 834-839.*

Duhamel et al., "A DCT chip based on a new structured and computationally efficient DCT algorithm", Proceedings of the International Symposium on Circuits and Systems, New Orleans, May 1-3, 1990, New York, IEEE, US, vol. 1 Conf. 23, May 1, 1990, pp. 77-80.

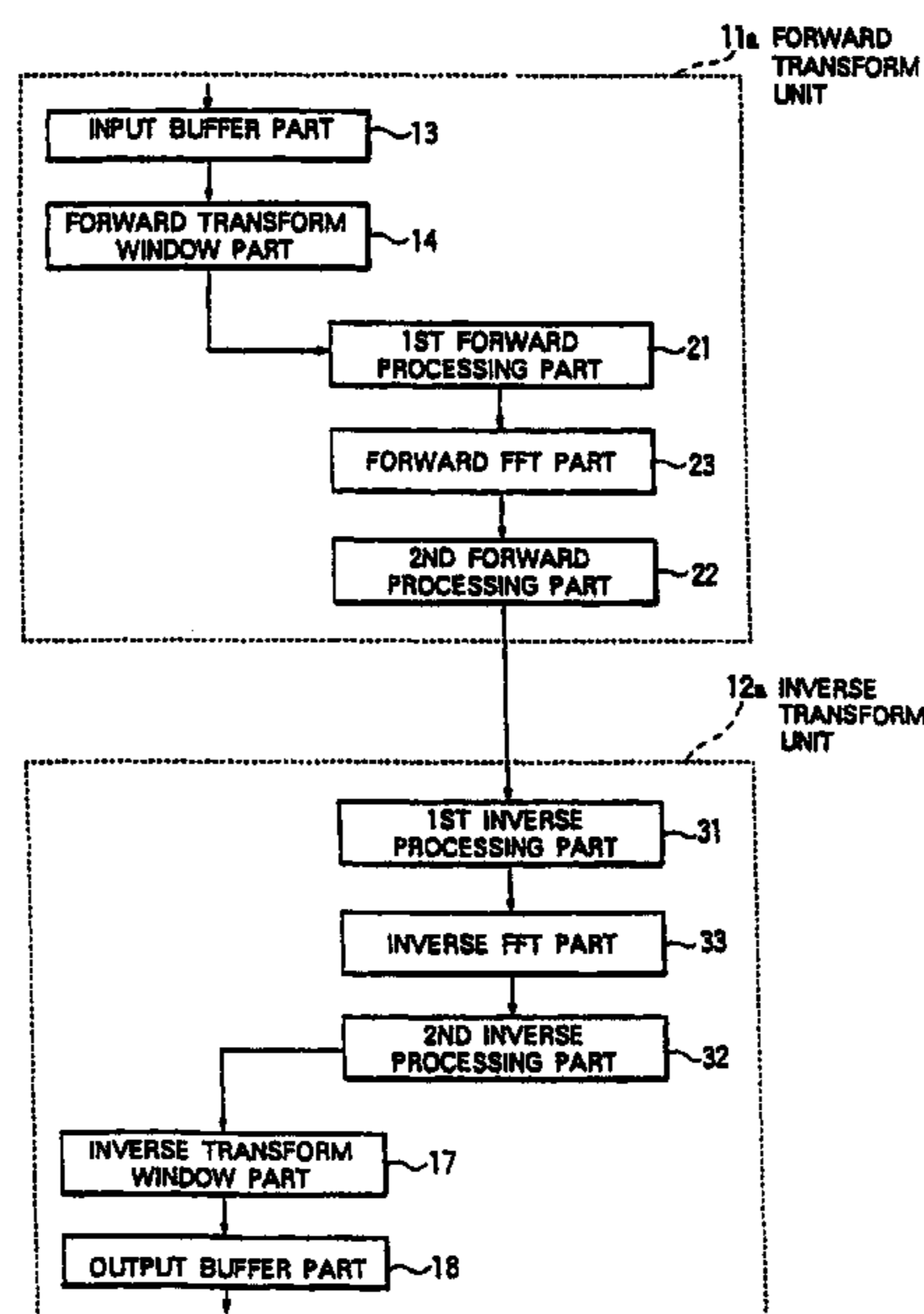
(Continued)

Primary Examiner—Chuong D Ngo
(74) *Attorney, Agent, or Firm*—Foley & Lardner LLP

(57) **ABSTRACT**

In an apparatus for carrying out a linear transform calculation on a product signal produced by multiplying a predetermined transform window function and an apparatus input signal, an FFT part (23) carries out fast Fourier transform on a processed signal produced by processing the product signal in a first processing part (21). As a result, the FFT part produces an internal signal which is representative of a result of the fast Fourier transform. A second processing part (22) processes the internal signal into a transformed signal which represents a result of the linear transform calculation. The apparatus is applicable to either of forward and inverse transform units (11, 12).

46 Claims, 7 Drawing Sheets



OTHER PUBLICATIONS

Henrique S. Malvar, "Lapped Transforms for Efficient Transform/Subband Coding", IEEE Transactions on Acoustics, Speech, and Signal Processing, vol. 38, No. 6 (Jun. 1990) pp. 969-978.

Madhally J. Narasimha and Allen M. Peterson, "On the Computation of the Discrete Cosine Transform", IEEE Transactions On Communications, vol. Com-26, No. 6 (Jun. 1978) pp. 934-936.

Thomas Duncan Lookabaugh, "Variable Rate and Adaptive Frequency Domain Vector Quantization of Speech" A Dissertation Submitted To The Department of Electrical Engineering and the Committee on Graduate Studies of Stanford University (Jun. 1988).

J.P. Princeton, A.W. Johnson and A.B. Bradley, "Subband/Transform Coding Using Filter Bank Designs Based on Time Domain Aliasing Cancellation", IEEE (1987) pp. 2161-2164.

* cited by examiner

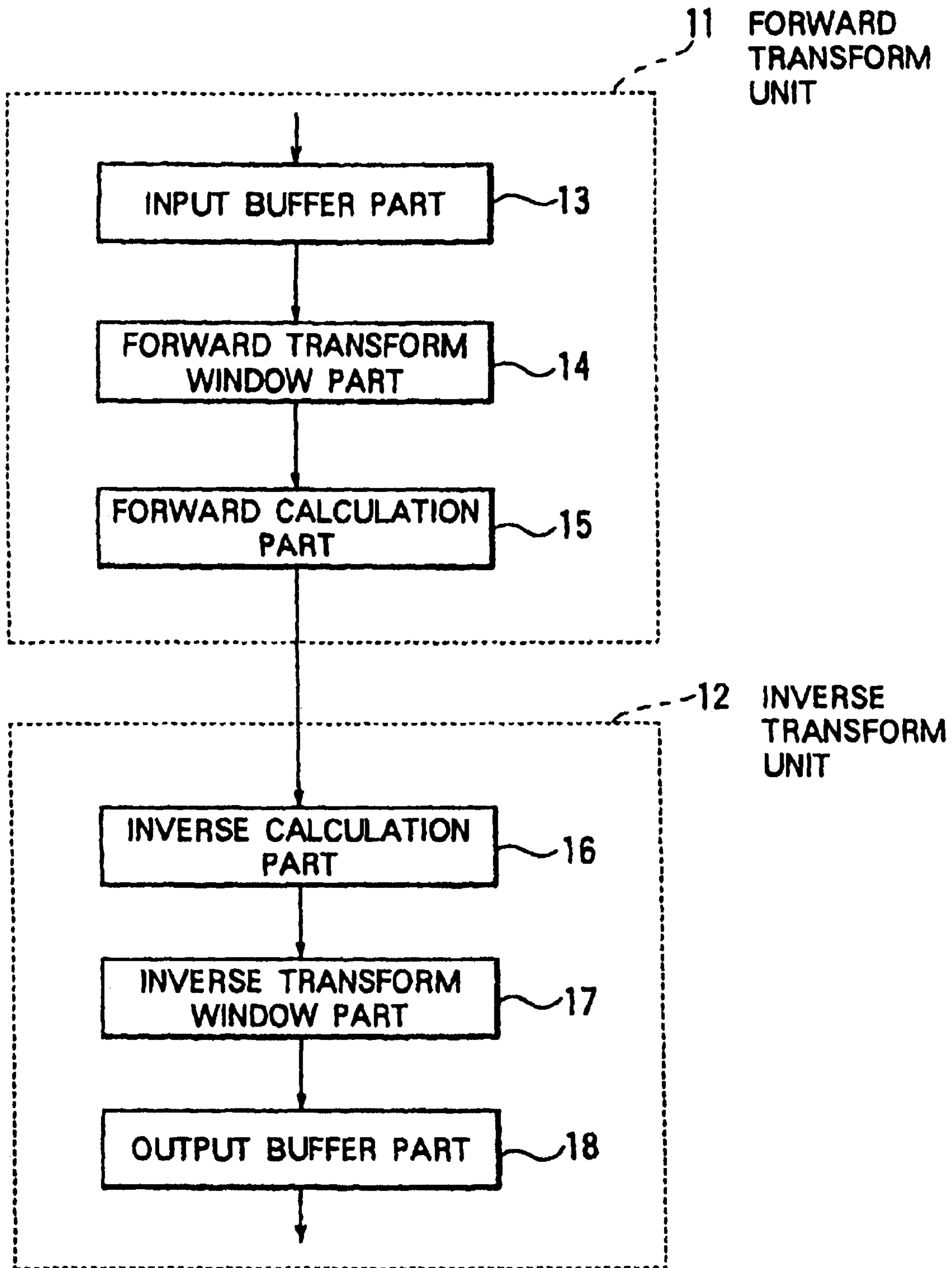


FIG. 1 PRIOR ART

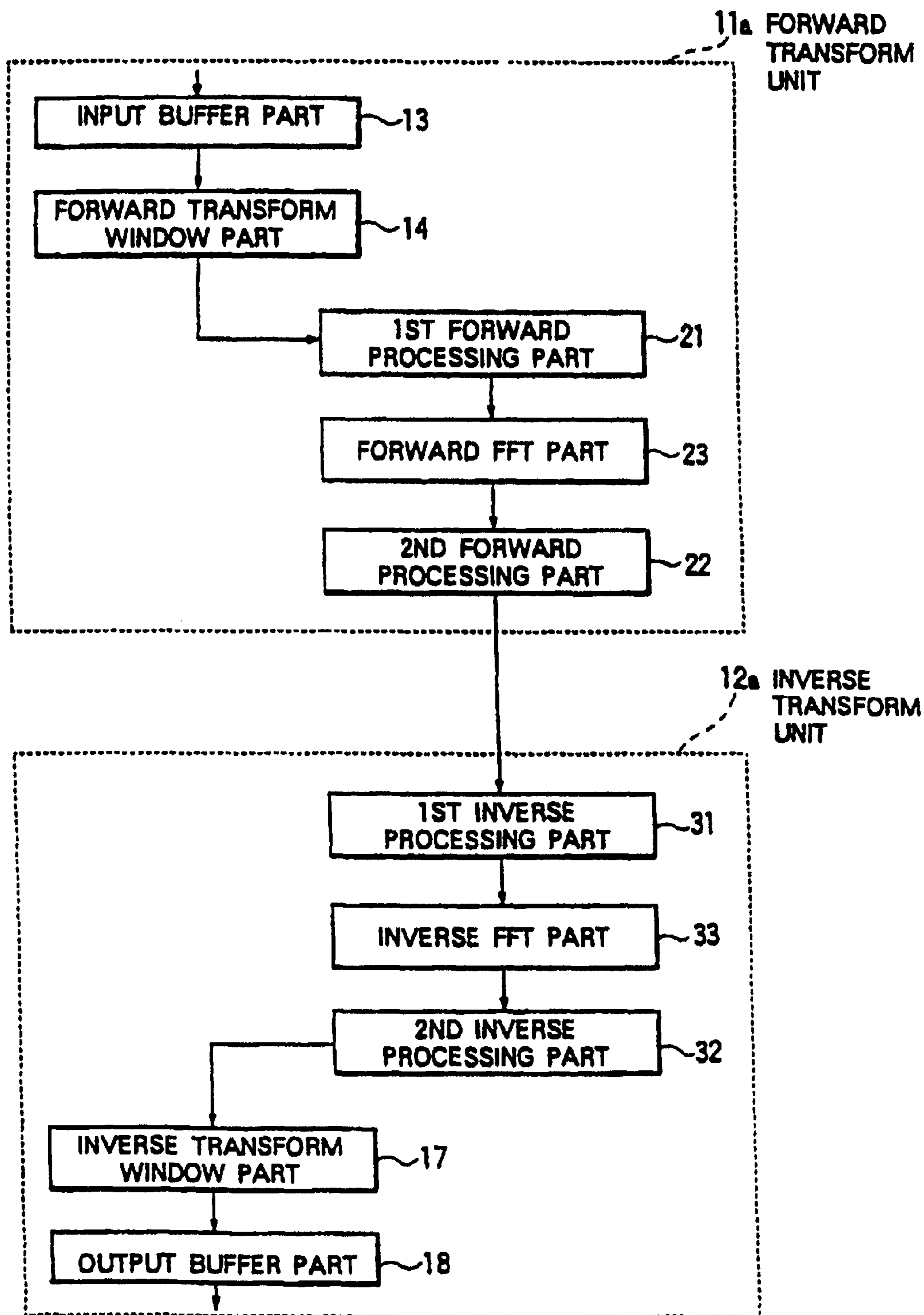


FIG. 2

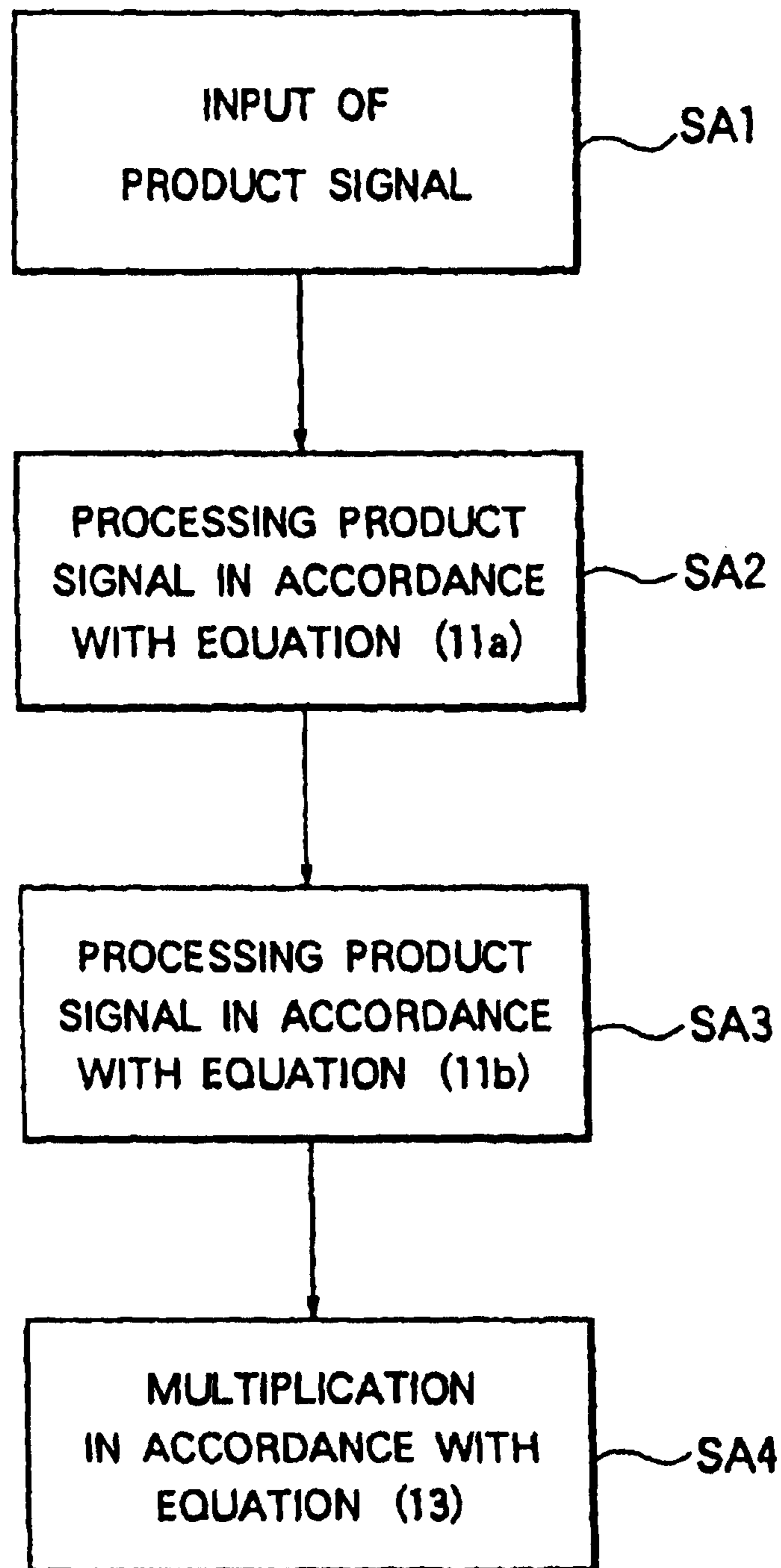


FIG. 3

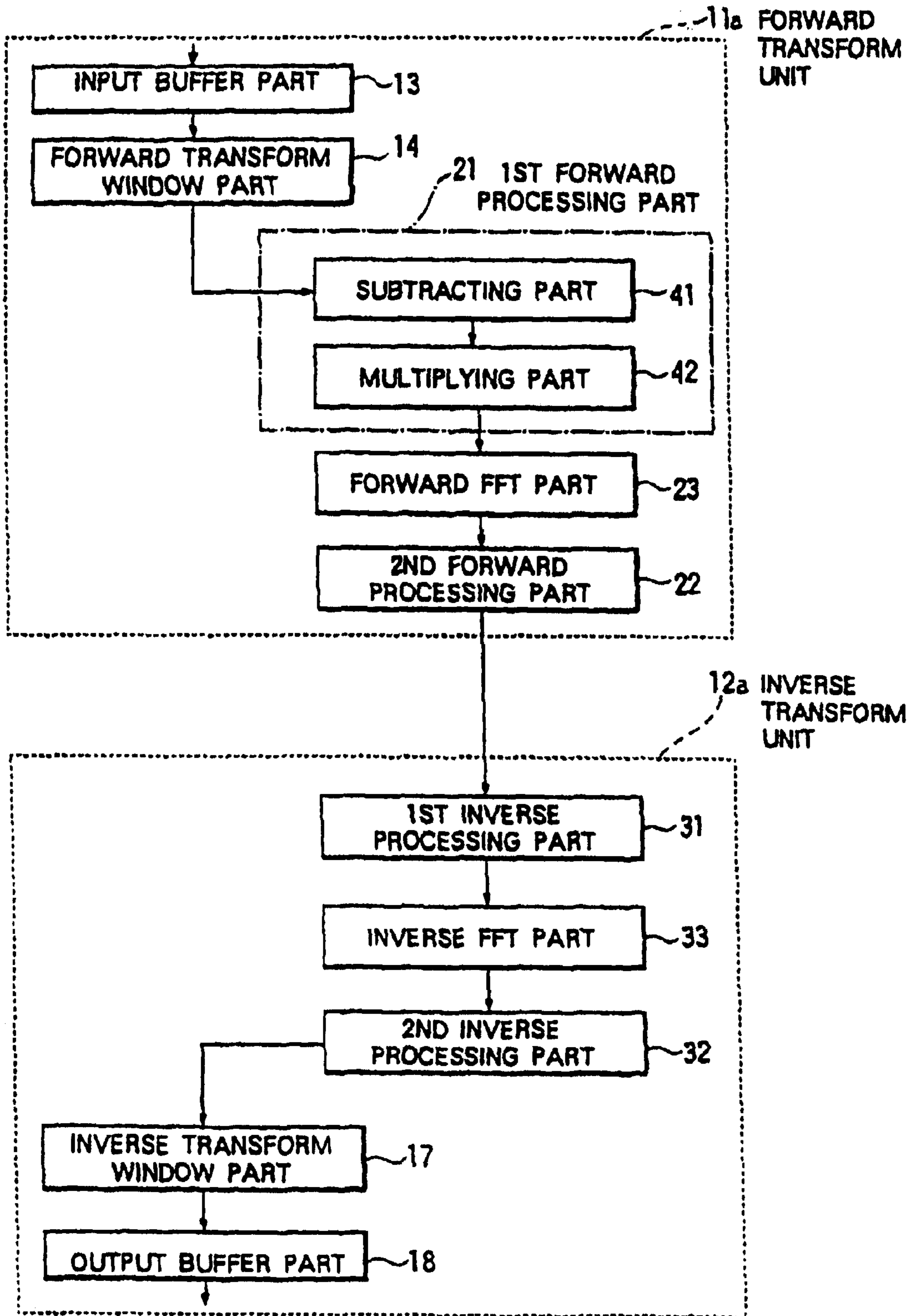


FIG. 4

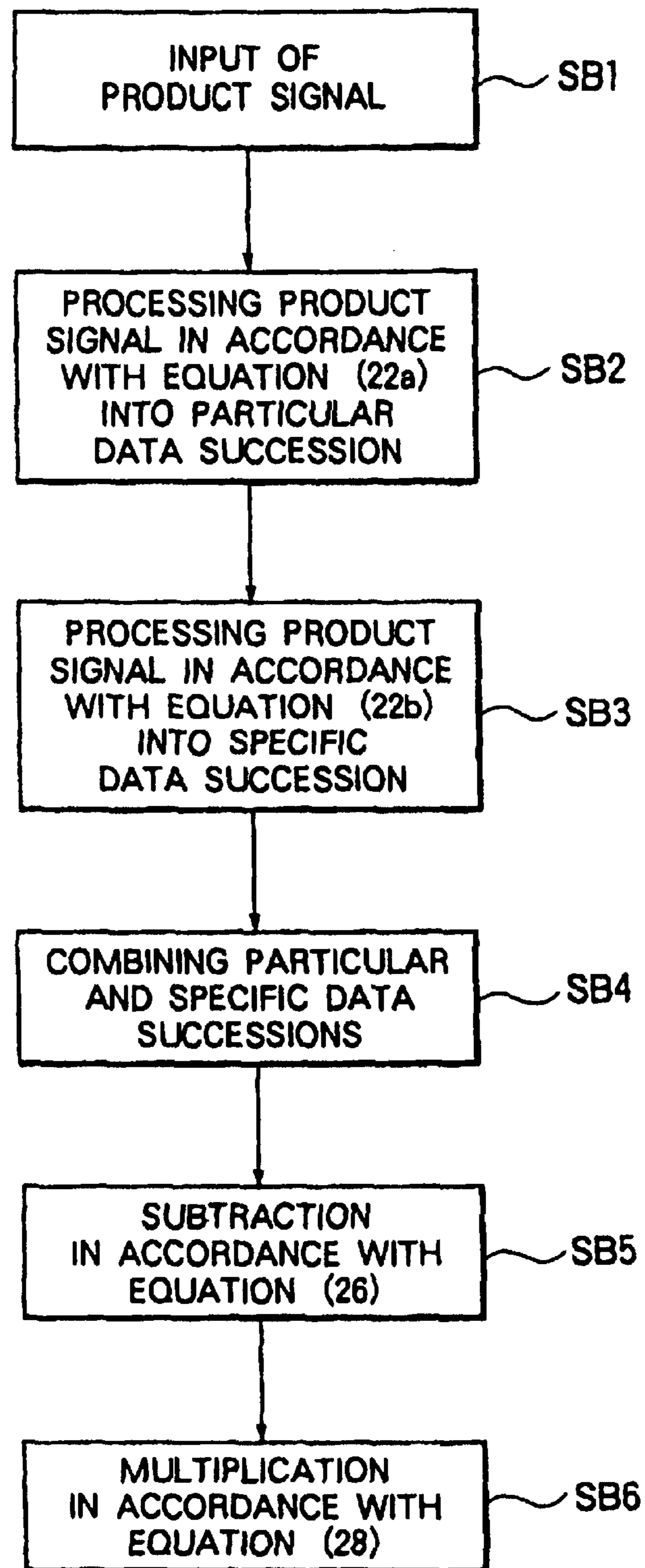


FIG. 5

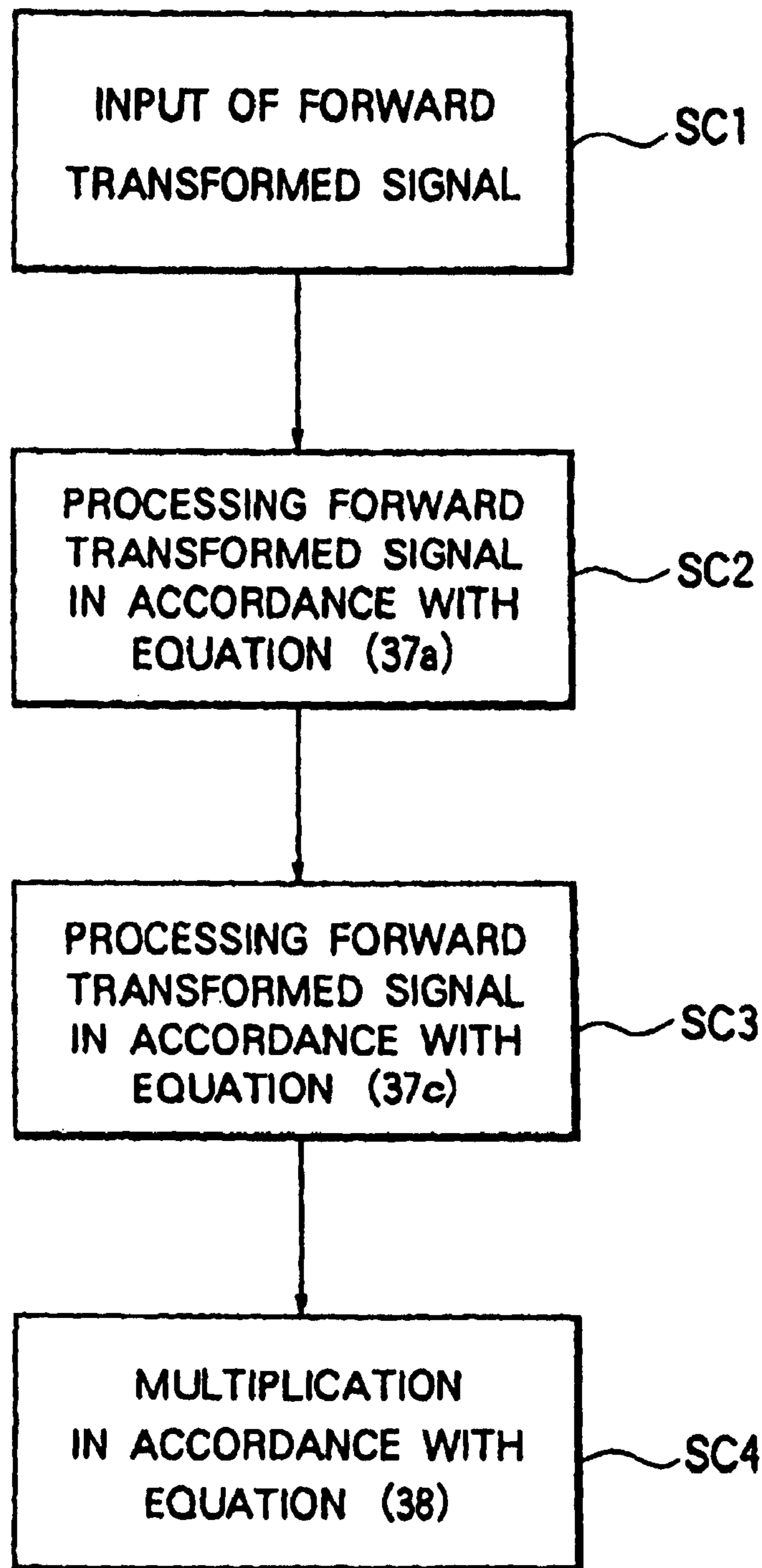


FIG. 6

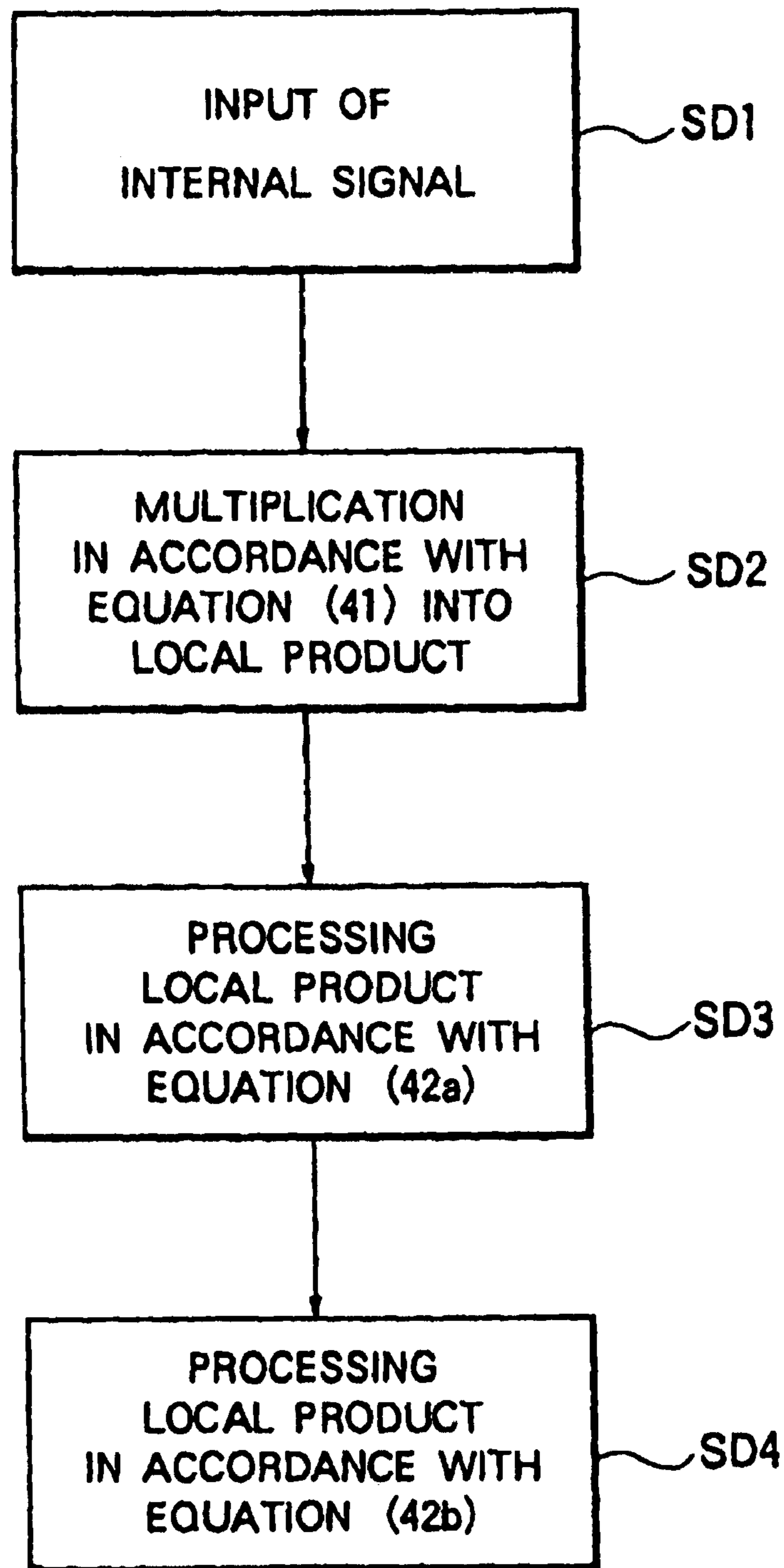


FIG. 7

**FAST CALCULATION APPARATUS FOR
CARRYING OUT A FORWARD AND AN
INVERSE TRANSFORM**

Matter enclosed in heavy brackets [] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

BACKGROUND OF THE INVENTION

This invention relates to a fast calculation apparatus included in each of a forward transform calculation apparatus and an inverse transform calculation apparatus.

A modified discrete cosine transform (hereinafter abbreviated to MDCT) apparatus is known as a linear transform apparatus for a digital signal such as an audio signal and a picture signal. In a conventional transform calculation apparatus, it is possible by the use of the MDCT technique to carry out a forward and an inverse transform calculation which are well known in the art.

The MDCT apparatus is described in detail in an article contributed by N. Schiller to the SPIE Vol. 1001 Visual Communications and Image Processing '88, pages 834-839, under the title of "Overlapping Block Transform for Image Coding Preserving Equal Number of Samples and Coefficients". The article will be described below.

In the MDCT technique, a forward transform equation and an inverse transform equation are given:

$$y(m, k) = \sum_{n=0}^{N-1} x(n)h(n)\cos [2\pi(k + 1/2)(n + n_0)/N] \quad (1)$$

and

$$xf(m, n) = 2f(n)/N \sum_{k=0}^{N-1} y(m, k)\cos [2\pi(k + 1/2)(n + n_0)/N], \quad (2)$$

wherein x represents an input signal, N represents a block length (N is multiple of 4), m represents a block number, h represents a forward transform window function, f represents an inverse transform window function, each of n and k represents an integer variable between 0 and $N-1$, both inclusive. Herein, n_0 is given as follows:

$$n_0 = N/4 + 1/2. \quad (3)$$

It is necessary in each of the forward and the inverse transform calculations to carry out a large number of multiplication times and addition times. This is because k is the integer between 0 and $(N-1)$, both inclusive. Accordingly, an increase in the block length N results in an increased number of times of each of the multiplication and the addition.

SUMMARY OF THE INVENTION

It is therefore an object of this invention to provide a forward transform calculation apparatus by which it is possible to reduce the number of times of multiplication and addition.

It is another object of this invention to provide an inverse transform calculation apparatus by which it is possible to reduce the number of times of the multiplication and the addition.

It is still another object of this invention to provide a calculation apparatus in which the number of times of the mul-

tiplication and the addition increases in proportion to only $N \log_2 N$, where N represents an integer.

It is yet another object of this invention to provide a calculation apparatus in which the number of times of the multiplication and the addition increases in proportion to $(N/2) \log_2(N/2)$, where N represents an integer.

Other object of this invention will become clear as the description proceeds.

According to an aspect of this invention, there is provided an apparatus for carrying out a forward transform calculation on an apparatus input signal. The apparatus includes multiplying means for multiplying a predetermined forward transform window function and the apparatus input signal to produce a multiplied signal and transform carrying out means for carrying out a linear forward transform on the product signal to produce a forward signal representative of a result of the linear forward transform. The transform carrying out means comprises first processing means connected to the multiplying means for processing the product signal into a processed signal, internal transform carrying out means connected to the first processing means for carrying out a forward fast Fourier transform on the processed signal to produce an internal signal representative of a result of the forward fast Fourier transform, and second processing means connected to the internal transform carrying out means for processing the internal signal into the forward transformed signal.

According to another aspect of this invention, there is provided an apparatus for carrying out an inverse transform calculation on an apparatus input signal. The apparatus includes transform carrying out means for carrying out a linear inverse transform on the apparatus input signal to produce an inverse signal representative of a result of the linear inverse transform and multiplying means for multiplying a predetermined inverse transform window function and the inverse signal to produce a product signal. The transform carrying out means comprises first processing means for processing the apparatus input signal into a processed signal, internal transform carrying out means connected to the first processing means for carrying out an inverse fast Fourier transform on the processed signal to produce an internal signal representative of a result of the inverse fast Fourier transform, and second processing means connected to the internal transform carrying out means for processing the internal signal into the inverse transformed signal.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a block diagram of a conventional calculation apparatus for successively carrying out a forward and an inverse transform;

FIG. 2 is a block diagram of a calculation apparatus according to a first embodiment of this invention;

FIG. 3 is a flow chart for use in describing operation of a first forward processing part included in the calculation apparatus of FIG. 2;

FIG. 4 is a block diagram of a calculation apparatus according to a second embodiment of this invention;

FIG. 5 is a flow chart for use in describing operation of a first forward processing part included in the calculation apparatus of FIG. 4;

FIG. 6 is a flow chart for use in describing operation of a first inverse processing part included in the calculation apparatus of FIG. 4; and

FIG. 7 is a flow chart for use in describing operation of a second inverse processing part included in the calculation apparatus of FIG. 4.

3

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 1, a conventional calculation apparatus will be described at first for a better understanding of the present invention. The conventional calculation apparatus is for successively carrying out a forward and an inverse transform and comprises forward and inverse transform units **11** and **12**.

The forward transform unit **11** comprises an input buffer part **13**, a forward transform window part **14**, and a forward calculation part **15**. The input buffer part **13** is for memorizing N samples of original signals $x(n)$, as an original data block. This means that the original data block has an original block length N . Responsive to the original signals $x(n)$, the forward transform window part **14** carries out multiplication between each of the original signals $x(n)$ and the forward transform window function $h(n)$ to produce a product signal $xh(n)$ as follows:

$$xh(n)=x(n)h(n). \quad (4)$$

Responsive to the product signal $xh(n)$, the forward calculation part **15** calculates the left-hand side of Equation (1) as follows:

$$y(m, k) = \sum_{n=0}^{N-1} xh(n) \cos [2\pi(k + 1/2)(n + n_0)/N]. \quad (5)$$

The calculation part produces the left-hand side as a forward transformed signal $y(m, k)$. It is necessary to carry out multiplication N^2 times and addition $N(N-1)$ times. This is because k is variable between 0 and $(N-1)$, both inclusive. Depending on the circumstances, each sample of the original signals $x(n)$ is herein called an apparatus input signal.

The inverse transform unit **12** comprises an inverse calculation part **16**, an inverse transform window part **17**, and an output buffer part **18**. The inverse calculation part **16** calculates the left-hand side of Equation (2) as follows:

$$x_t(m, n) = 2/N \sum_{k=0}^{N-1} y(m, k) \cos [2\pi(k + 1/2)(n + n_0)/N]. \quad (6)$$

The calculation part **16** produces the left-hand side as an inverse transformed signal $x_t(m, n)$. The inverse transform window part **17** multiplies the inverse transformed signal $x_t(m, n)$ and an inverse transform window function $f(n)$ into a product in accordance with:

$$x_f(m, n)=x_t(m, n)f(n). \quad (7)$$

The inverse transform window part **17** thereby produces a product signal $x_f(m, n)$ representative of the product.

The product signal is supplied to the output buffer part **18** whenever the multiplication is carried out by the inverse transform window part **17**. As a result, the output buffer part **18** memorizes a plurality of the product signals as a current and a previous data block at a time. The current data block corresponds to the original data block. The previous data block is previous to the current data block. Each of the current and the previous data blocks is divided into a former and a latter half block. The former half block comprises zeroth through $(N/2-1)$ -th product signals. The latter half block comprises $N/2$ -th through $(N-1)$ -th product signals.

4

As will be understood from the following equation, the output buffer part **18** carries out addition between the product signal $x_f(m, n)$ of the former half block of the current data block and the product signal $x_f(m-1, n)$ of the latter half block of the previous data block to produce a modified or reproduced signal $x'(n)$ of a modified half block having a modified block length which is a half of the original block length. The following equation is:

$$x'(n)=x_f(m-1, n+N/2)+x_f(m, n), \quad (8)$$

$$\text{when } 0 \leq n < N/2-1.$$

Simultaneously, the output buffer part **18** memorizes, as the latter half block, the second product signal $x_f(m, n)$ of the current data block. Each of the forward and the inverse transform window functions $h(n)$ and $f(n)$ can be given by Equation (9) on page 836 in the above-mentioned article.

The description will now proceed to an example of an algorithm which is applicable to a forward transform calculation apparatus according to this invention. Substituting Equation (3), Equation (5) is rewritten into:

$$y(m, k) = \sum_{n=0}^{N-1} xh(n) \cos [2\pi(k + 1/2)(n + n_0)/N] \quad (9)$$

$$= \sum_{n=0}^{N-1} xh(n) \cos [2\pi(k + 1/2)(n + N/4 + 1/2)/N]$$

$$= \sum_{n=N/4}^{5N/4-1} xh(n - N/4) \cos [2\pi(k + 1/2)(n + 1/2)/N]$$

In Equation (9), the cosine has a nature such that:

$$\cos [2\pi(k + 1/2)(n + 1/2)/N] = \quad (10)$$

$$\cos [2\pi(k + 1/2)((n - N) + 1/2 + N)/N] =$$

$$\cos [2\pi(k + 1/2)((n - N) + 1/2)/N + 2\pi(k + 1/2)N/N] =$$

$$-\cos [2\pi(k + 1/2)((n - N) + 1/2)/N]$$

When n is shifted by $(-N)$, the cosine has an argument shifted by $2\pi(k+1/2)$, namely, an odd integral multiple of π . In this event, the cosine has an absolute value unchanged and a sign inverted between positive and negative. Therefore, it is possible to delete the term $N/4$ in the argument of xh in the right-hand side of Equation (9) by shifting n by $(-N)$ with the sign of the product signal $xh(n)$ inverted.

Herein, the product signal is processed into particular and specific datum $x_2(n)$ which are represented as follows:

$$x_2(n)=-xh(n+3/N4), \quad (11a)$$

$$\text{when } 0 \leq n < N/4$$

and

$$x_2(n)=xh(n-N/4), \quad (11b)$$

$$\text{when } N/4 \leq n < N.$$

5

Therefore:

$$\begin{aligned}
 y(m, k) &= \sum_{n=0}^{N-1} x_2(n) \cos[2\pi(k+1/2)(n+1/2)/N] \\
 &= \text{real} \left[\sum_{n=0}^{N-1} x_2(n) \exp(-2\pi j(k+1/2)(n+1/2)/N) \right] \\
 &= \text{real} \left[\sum_{n=0}^{N-1} x_2(n) \times \right. \\
 &\quad \left. \exp(-2\pi j(k+1/2)/2N - 2\pi j(k+1/2)n/N) \right] \\
 &= \text{real} \left[\exp(-2\pi j(k+1/2)/2N) \times \right. \\
 &\quad \left. \sum_{n=0}^{N-1} x_2(n) \exp(-2\pi j(k+1/2)n/N) \right] \\
 &= \text{real} \left[\exp(-2\pi j(k+1/2)/2N) \times \right. \\
 &\quad \left. \sum_{n=0}^{N-1} x_2(n) \exp(-2\pi jn/2N - 2\pi jkn/N) \right] \\
 &= \text{real} \left[\exp(-2\pi j(k+1/2)/2N) \times \right. \\
 &\quad \left. \sum_{n=0}^{N-1} x_2(n) \exp(-2\pi jn/2N) \exp(-2\pi jkn/N) \right],
 \end{aligned} \tag{12}$$

where j represents an imaginary unit.

It will be assumed that:

$$x_3(n) = x_2(n) \exp(-2\pi jn/2N). \tag{13}$$

In this event:

$$y(m, k) = \text{real} \left[\exp(-2\pi j(k+1/2)/2N) \times \sum_{n=0}^{N-1} x_3(n) \exp(-2\pi jkn/N) \right]. \tag{14}$$

Herein, Equation (14) is divided into a front part and a rear part which represents execution of a fast Fourier transform (hereinafter abbreviated to FFT) at a point N of a specific signal $x_3(n)$. The FFT is represented by Equation (15) which is given below.

Accordingly, Equation (16) is given from Equation (14).

$$x_f(m, k) = \sum_{n=0}^{N-1} x_3(n) \exp(-2\pi jkn/N) \tag{15}$$

and

$$y(m, k) = \text{real}[\exp(-2\pi j(k+1/2)/2N)x_f(m, k)]. \tag{16}$$

It is therefore possible to obtain the result of Equation (5).

The multiplications are required N times before execution of the FFT, at most $N \log_2 N$ times for executing the FFT, and N times after execution of the FFT. As a result, the multiplication is carried out the number of times which is substantially equal to $N \log_2 N$ if N is great. The number of times of the addition is equal to $2N \log_2 N$. Accordingly, it is possible to reduce the number of times of the multiplication and the addition as compared with the conventional calculation apparatus.

6

The description will proceed to an example of an algorithm which is applicable to an inverse transform calculation apparatus according to this invention. Substituting Equation (3), Equation (6) is rewritten into:

$$\begin{aligned}
 x_t(m, n) &= 2/N \sum_{k=0}^{N-1} y(m, k) \cos[2\pi(n+n_0)(k+1/2)/N] \\
 &= 2/N \sum_{k=0}^{N-1} y(m, k) \cos[2\pi(n+N/4+1/2)(k+1/2)/N] \\
 &= 2/N \text{real} \left[\sum_{k=0}^{N-1} y(m, k) \times \exp(2\pi j(n+N/4+1/2)(k+1/2)/N) \right] \\
 &= 2/N \text{real} \left[\sum_{k=0}^{N-1} y(m, k) \times \exp(2\pi j(n+N/4+1/2)/2N + \right. \\
 &\quad \left. 2\pi j(n+N/4+1/2)k/N) \right] \\
 &= 2/N \text{real} \left[\exp(2\pi j(n+N/4+1/2)/2N) \times \right. \\
 &\quad \left. \sum_{k=0}^{N-1} y(m, k) \exp(2\pi j(n+N/4+1/2)k/N) \right] \\
 &= 2/N \text{real} \left[\exp(2\pi j(n+N/4+1/2)/2N) \times \right. \\
 &\quad \left. \sum_{k=0}^{N-1} y(m, k) \exp(2\pi j(N/4+1/2)k/N + 2\pi jnk/N) \right] \\
 &= 2/N \text{real} \left[\exp(2\pi j(n+N/4+1/2)/2N) \times \right. \\
 &\quad \left. \sum_{k=0}^{N-1} y(m, k) \exp(2\pi j(N/4+1/2)k/N) \exp(2\pi jnk/N) \right].
 \end{aligned} \tag{17}$$

The following equations are introduced:

$$y_2(m, k) = y(m, k) \exp[2\pi j(N/4+1/2)k/N] \tag{18}$$

and

$$y_3(m, k) = \sum_{k=0}^{N/2-1} y_2(m, k) \exp(2\pi jnk/N). \tag{19}$$

Equation (19) represents the inverse FFT for the signal $y_2(m, k)$. Substituting Equations (18) and (19) in Equation (17):

$$x_t(m, n) = 2/N \text{real}[\exp(2\pi j(n+N/4+1/2)/2N)y_3(m, n)]. \tag{20}$$

It is therefore possible to obtain the result of Equation (6).

The multiplication is carried out the number of times which is substantially equal to $N \log_2 N$. The number of times of the addition is equal to $2N \log_2 N$. Accordingly, it is possible to reduce the number of times of the multiplication and the addition as compared with the conventional apparatus.

The description will now proceed to another example of the algorithm that is applicable to the forward transform calculation apparatus according to this invention. With p substituted for n , Equation (9) is rewritten into:

$$y(m, k) = \sum_{p=N/4}^{5N/4-1} xh(p - N/4) \cos [2\pi(k + 1/2)(p + 1/2)/N]. \quad (21)$$

It is possible to delete the term $N/4$ in the argument of xh in the right-hand side of Equation (21) by shifting p by $(-N)$ with the sign of the product signal $xh(p)$ inverted.

Herein, the product signal is processed into the particular and the specific data $x_2(p)$ which are represented as follows:

$$x_2(p) = -xh(p + 3N/4), \quad (22a) \quad 15$$

when $0 \leq p < N/4$

and

$$x_2(p) = xh(p + N/4), \quad (22b) \quad 20$$

when $N/4 \leq p < N$.

Therefore:

Therefore:

$$y(m, k) = \sum_{p=0}^{N-1} x_2(p) \cos [2\pi(k + 1/2)(p + 1/2)/N] \quad (23) \quad 30$$

In Equation (23), the cosine has a nature such that:

$$\cos [2\pi(k + 1/2)(p + 1/2)/N] = \cos [-2\pi(k + 1/2)(p + 1/2)/N] = \quad (24) \quad 35$$

$$\cos [2\pi(k + 1/2)((N - p - 1/2) - N)/N] =$$

$$\cos [2\pi(k + 1/2)((N - 1 - p) + 1/2)/N - 2\pi(k + 1/2)(N/N)] =$$

$$-\cos [2\pi(k + 1/2)((N - p - 1) + 1/2)/N] \quad 40$$

When $(N-1-p)$ is substituted for p , the cosine has an absolute value unchanged and a sign inverted between positive and negative. When p separated into an even and an odd number, Equation (23) is rewritten into:

$$y(m, k) = \sum_{p=0}^{N/2-1} x_2(2p) \cos [2\pi(k + 1/2)(2p + 1/2)/N] + \quad (25)$$

$$\sum_{p=0}^{N/2-1} x_2(N - 1 - 2p) \cos [2\pi(k + 1/2) \times (N - 1 - 2p + 1/2)/N]$$

$$= \sum_{p=0}^{N/2-1} [x_2(2p) - x_2(p - 1 - 2p)] \times$$

$$\cos [2\pi(k + 1/2)(2p + 1/2)/N] \quad 55$$

It is assumed that:

$$x_3(p) = x_2(2p) - x_2(N - 1 - 2p), \quad (26) \quad 65$$

when $0 \leq p \leq N/2 - 1$.

In this event:

$$y(m, k) = \sum_{n=0}^{N/2-1} x_3(n) \cos [2\pi(k + 1/2)(2n + 1/2)/N] \quad (27)$$

$$= \text{real} \left[\sum_{n=0}^{N/2-1} x_3(n) \exp(-2\pi j(k + 1/2)(2n + 1/2)/N) \right]$$

$$= \text{real} \left[\sum_{n=0}^{N/2-1} x_3(n) \times$$

$$\exp(-2\pi j(k + 1/2)/2N - 2\pi j(k + 1/2)2n/2) \right]$$

$$= \text{real} \left[\exp(-2\pi j(k + 1/2)/2N) \times$$

$$\sum_{n=0}^{N/2-1} x_3(n) \exp(-2\pi j(k + 1)n/N) \right]$$

$$= \text{real} \left[\exp(-2\pi j(k + 1/2)/2N) \times$$

$$\sum_{n=0}^{N/2-1} x_3(n) \exp(-2\pi jn/N - 2\pi jk2n/N) \right]$$

$$= \text{real} \left[\exp(-2\pi j(k + 1/2)/2N) \times$$

$$\sum_{n=0}^{N/2-1} x_3(n) \exp(-2\pi jn/N) \exp(-2\pi jkn/(N/2)) \right]$$

It is assumed that:

$$x_4(p) = x_3(p) \exp(-2\pi jp/N). \quad (28)$$

In this event:

$$y(m, k) = \quad (29)$$

$$\text{real} \left[\exp(-2\pi j(k + 1/2)/2N) \times \sum_{p=0}^{N/2-1} x_4(p) \exp(-2\pi jkp/(N/2)) \right]$$

Herein, Equation (14) is divided into a front part and a rear part which represents execution of the FFT at $N/2$ of $x_4(p)$. The FFT is represented by Equation (30) which is given below. Accordingly, Equation (31) is given from Equation (29).

$$xf(m, k) = \sum_{p=0}^{N/2-1} x_4(p) \exp[-2\pi jkp/(N/2)] \quad (30)$$

$$y(m, k) = \text{real} [\exp(-2\pi j(k + 1/2)/2N) \times f(m, k)] \quad (31)$$

It is therefore possible to obtain the result of Equation (5).

The multiplication is carried out the number of times which is substantially equal to $(N/2) \log_2 (N/2)$ if N is great. The total number of the addition and the subtraction is equal to $N/2$ for $x_3(p)$ and to $N \log_2 (N/2)$ for FFT. The number of

the addition is substantially equal to $N \log_2(N/2)$ if N is great. Accordingly, it is possible to reduce the number of times of the multiplication and the addition as compared with the conventional calculation apparatus.

Since the FFT is carried out at $N/2$ points, $y(m, n)$ is obtained in a case where k is variable between 0 and $N/2-1$, both inclusive. In Equation (24), p and k are symmetrical with one another. Using the symmetric nature of the cosine with respect to k , Equation (23) is rewritten into:

$$\begin{aligned} y(m, k) &= \sum_{n=0}^{N-1} x_2(n) \cos [2\pi(k+1/2)(n+1/2)/N] \\ &= \sum_{n=0}^{N-1} -x_2(n) \cos [2\pi(N-1-k+1/2)(n+1/2)/N] \\ &= -y(m, N-1-k). \end{aligned} \quad (32)$$

Therefore, $y(m, k)$ is obtained in another case where k is variable between $N/2$ and $N-1$, both inclusive.

The description will proceed to another example of the algorithm that is applicable to the inverse transform calculation apparatus according to this invention. Substituting Equation (3) with p substituted for n , Equation (6) is rewritten into:

$$\begin{aligned} xt(m, n) &= 2/N \sum_{k=0}^{N-1} y(m, k) \cos [2\pi(p+p_0)(k+1/2)/N] \\ &= 2/N \sum_{k=0}^{N-1} y(m, k) \cos [2\pi(p+N/4+1/2)(k+1/2)/N]. \end{aligned} \quad (33)$$

For convenience of the equation, it will be assumed that:

$$xt_2(m, p) = xt(m, p-N/4). \quad (34)$$

In this event:

$$xt_2(m, p) = 2/N \sum_{k=0}^{N-1} y(m, k) \cos [2\pi(p+1/2)(k+1/2)/N] = 2/ \quad (35)$$

$$\begin{aligned} N \left[\sum_{k=0}^{N/2-1} y(m, 2k) \cos(2\pi(p+1/2)(2k+1/2)/N) + \sum_{k=0}^{N/2-1} y(m, N-1-2k) \times \cos(2\pi(p+1/2)(N-1-2k+1/2)/N) \right] \\ = 2/N \left[\sum_{k=0}^{N/2-1} (y(m, 2k) - y(m, N-1-2k)) \times \cos(2\pi(p+1/2)(2k+1/2)/N) \right]. \end{aligned}$$

Substituting Equation (31):

$$xt_2(m, p) = 2/N \left[\sum_{k=0}^{N/2-1} 2y(m, 2k) \cos(2\pi(p+1/2)(2k+1/2)/N) \right]. \quad (36)$$

Herein, $y_2(m, k)$ is represented as follows:

$$y_2(m, k) = y(m, 2k), \quad (37a)$$

$$\text{when } 0 \leq k < N/4$$

$$y_2(m, k) = -y(m, k), \quad (37b)$$

$$\text{when } N/4 \leq k < N/2.$$

Using Equation (32), Equation (37b) is represented as follows:

$$y_2(m, k) = -y(m, N-1-2k), \quad (37c)$$

$$\text{when } N/4 \leq k < N/2.$$

Equation (35) is rewritten into:

$$xt_2(m, p) = \quad (38)$$

$$4/N \operatorname{real} \left[\sum_{k=0}^{N/2-1} y_2(m, k) \times \exp(2\pi j(p+1/2)(2k+1/2)/N) \right]$$

$$= 4/N \operatorname{real} \left[\sum_{k=0}^{N/2-1} y_2(m, k) \times \exp(2\pi j(p+1/2)/2N + 2\pi j(p+1/2)2k/N) \right]$$

$$= 4/N \operatorname{real} \left[\exp(2\pi j(p+1/2)/2N) \times \sum_{k=0}^{N/2-1} y_2(m, k) \exp(2\pi j(2p+1)k/N) \right]$$

$$= 4/N \operatorname{real} \left[\exp(2\pi j(p+1/2)/2N) \times \sum_{k=0}^{N/2-1} y_2(m, k) \exp(2\pi jk/N + (2\pi jpk/(N/2))) \right]$$

$$= 4/N \operatorname{real} \left[\exp(2\pi j(p+1/2)/2N) \times \sum_{k=0}^{N/2-1} y_2(m, k) \exp(2\pi jk/N + (2\pi jpk/(N/2))) \right]$$

$$= 4/N \operatorname{real} \left[\exp(2\pi j(p+1/2)/2N) \times \sum_{k=0}^{N/2-1} y_2(m, k) \exp(2\pi jk/N + (2\pi jpk/(N/2))) \right]$$

$$= 4/N \operatorname{real} \left[\exp(2\pi j(p+1/2)/2N) \times \sum_{k=0}^{N/2-1} y_2(m, k) \exp(2\pi jk/N + (2\pi jpk/(N/2))) \right]$$

It is assumed that:

$$y_3(m, k) = y_2(m, k) \exp(2\pi jk/N) \quad (39)$$

$$y_4(m, p) = \sum_{k=0}^{N/2-1} y_3(m, k) \exp[2\pi jpk/(N/2)] \quad (40)$$

Equation (40) represents an inverse FFT for $y_3(m, k)$. Substituting Equations (39) and (40) into Equation (38):

$$xt_2(m, n) = 4/N \operatorname{real} [\exp(2\pi j(n+1/2)/2N) y_4(m, n)]. \quad (41)$$

In order to convert $xt_2(m, n)$ to $xt(m, n)$, it is assumed from Equations (20), (24), and (32) that:

$$xt(m, 3N/4-1-n) = xt(m, 3N/4+n) \quad (42a)$$

$$= -xt_2(m, n)$$

$$\text{when } 0 \leq n < N/4$$

It is therefore possible to obtain the result of Equation (6).

11

The multiplication is carried out the number of times which is substantially equal to $(N/2) \log_2 (N/2)$. The addition is carried out the number of times which is substantially equal to $N \log_2 (N/2)$. Accordingly, it is possible to reduce the number of times of the multiplication and the addition as compared with the conventional calculation apparatus.

Referring to FIG. 2, the description will be directed to a calculation apparatus according to a first embodiment of this invention. The calculation apparatus comprises similar parts designated by like reference numerals. The forward transform window part 14 produces, as the product signal, a succession of zeroth through $(3N/4-1)$ th and $(3N/4)$ th through $(N-1)$ th product data. The forward transform window part 14 will be referred to as a multiplying arrangement.

The forward transform unit 11a further comprises first forward processing, second forward processing, and forward FFT parts 21, 22, and 23. The first forward processing part 21 is connected to the forward transform window part 14 and is for processing the product signal into a processed signal.

Referring to FIG. 3 together with FIG. 2, the description will be made as regards operation of the first forward processing part 21. At a first stage SA1, the first forward processing part 21 is supplied with the product signal from the forward transform window part 14. The first stage SA1 proceeds to a second stage SA2 at which the first forward processing part 21 processes the $(3N/4)$ th through the $(N-1)$ th product data into a succession of zeroth through $(N/4-1)$ th particular data having a negative polarity or sign in common. In other words, the zeroth through the $(N/4-1)$ th product data are processed in accordance with Equation (11a). The first forward processing part 21 for carrying out the second stage SA2 will be referred to as a particular processing arrangement.

The second stage SA2 proceeds to a third stage SA3 at which the first forward processing part 21 processes the zeroth through the $(3N/4-1)$ th product data into a succession of $(N/4)$ th through $(3N/4-1)$ th specific data having a positive polarity or sign in common. In other words, the $(N/4)$ th through the $(N-1)$ th product data are processed in accordance with Equation (11b). The first forward processing part 21 for carrying out the third stage SA3 will be referred to as a specific processing arrangement.

The third stage SA3 proceeds to a fourth stage SA4 at which the first forward processing part 21 multiplies $\exp[-2\pi j n / (2n)]$ and each of the $(3N/4)$ th through the N -th particular and the zeroth through the $(3N/4-1)$ th specific data in accordance with Equation (13) to produce the processed signal. The first forward processing part 21 for carrying out the fourth stage SA4 will be referred to as a calculating arrangement.

Returning to FIG. 2, the forward FFT part 23 is connected to the first forward processing part 21 and is for carrying out a linear forward FFT on the processed signal in accordance with Equation (15) to produce an internal signal representative of a result of the forward FFT. The forward FFT part 23 is herein referred to as an internal transform carrying out arrangement.

The second forward processing part 22 is connected to the forward FFT part 23 and is for processing the internal signal into the forward transformed signal in accordance with Equation (16). More particularly, the second forward processing part 22 multiplies the internal signal and $[-2\pi j (k+1/2) / 2N]$ into a local product, namely, a real part, to make the forward transformed signal represent the local product. In this event, the second forward processing part 22 will be referred to as an internal multiplying arrangement. A combination of the first forward processing, the second forward

12

processing, and the forward FFT parts 21, 22, and 23 will be referred to as a transform carrying out arrangement.

Continuing reference to FIG. 2, the description will proceed to the inverse transform unit 12a. The inverse transform unit 12 comprises first inverse processing, second inverse processing, and inverse FFT parts 31, 32, and 33. The first inverse processing part 31 is connected to the second forward processing part 22 and is for processing the forward transformed signal into a processed signal.

The first inverse processing part 31 is supplied with the forward transformed signal as an apparatus input signal. The forward transformed signal is a succession of zeroth through $(N-1)$ th apparatus input data.

The first inverse processing part 31 carries out multiplication between the zeroth through the $(N-1)$ th apparatus input data and $\exp[2\pi j (N/4+1/2)k/N]$ in accordance with Equation (18) into a first product to make the processed signal represent the first product. In this event, the first inverse processing part 31 will be referred to as a first multiplying arrangement.

The inverse FFT part 33 is connected to the first inverse processing part 31 and is for carrying out a linear inverse FFT on the processed signal in accordance with Equation (19) to produce an internal signal representative of a result of the inverse FFT. The internal signal is a succession of zeroth through $(N-1)$ th internal data. In this event, the inverse FFT part 33 is herein referred to as an internal transform carrying out arrangement.

The second inverse processing part 32 is connected to the inverse FFT part 33 and is for carrying out multiplication between the zeroth through the $(N-1)$ th internal data and $2\exp[-2\pi j (n+N/4+1/2)/(2N)]$ in accordance with Equation (20) into a second product, namely, a real part, to make the inverse transformed signal represent the second product. In this event, the second inverse processing part 32 will be referred to as a second multiplying arrangement.

The second inverse processing part 32 is further connected to the inverse transform window part 17. The inverse transformed signal is sent from the second inverse processing part 32 to the inverse transform window part 17.

Referring to FIG. 4, the description will be directed to a calculation apparatus according to a second embodiment of this invention. The calculation apparatus comprises similar parts designated by like reference numerals. The forward transform window part 14 produces, as the product signal, a succession of zeroth through $(3N/4-1)$ th and $(3N/4)$ th through $(N-1)$ th product data. The forward transform window part 14 will be referred to as a multiplying arrangement.

The first forward processing part 21 comprises subtracting and multiplying parts 41 and 42. The subtracting part 41 is connected to the forward transform window part 14 and is for producing a local signal in response to the product signal. The multiplying part 42 is connected to the subtracting part 41 and is for producing the processed signal in response to the local signal.

Referring to FIG. 5 together with FIG. 4, the description will be made as regards operation of the first forward processing part 21. At a first stage SB1, the subtracting part 41 is supplied with the product signal from the forward transform window part 14. The first stage SB1 proceeds to a second stage SB2 at which the subtracting part 41 processes the zeroth through the $(N/4-1)$ th product data into a succession of $(3N/4)$ through N th particular data having a negative polarity in common. In other words, the zeroth through the $(N/4-1)$ th product data are processed in accordance with Equation (22a). The subtracting part 41 for carrying out the second stage SB2 will be referred to as a particular processing arrangement.

The second stage SB2 proceeds to a third stage SB3 at which the subtracting part 41 processes the zeroth through the $(3N/4-1)$ th product data into a succession of zeroth through $(N/4)$ th specific data having a positive polarity in common. In other words, the $(N/4)$ th through the $(N-1)$ th product data are processed in accordance with Equation (22b). The subtracting part 41 for carrying out the third stage SB3 will be referred to as a specific processing arrangement.

The third stage SB3 proceeds to a fourth stage SB4 at which the subtracting part 41 combines the particular and the specific data successions into a succession of zeroth through $(N-1-2p)$ th and $2p$ th through $(N-1)$ th combined data. When the fourth stage SB3 is carried out, the subtracting part 41 will be referred to as a combining arrangement.

The fourth stage SB4 proceeds to a fifth stage SB5 at which the subtracting part 41 subtracts the $(N-1-2p)$ th combined datum from the $2p$ th combined datum in accordance with Equation (26) to produce a difference and the local signal that is representative of the difference. The subtracting part 41 for carrying out the fifth stage SB5 will be referred to as a subtracting arrangement.

The fifth stage SB5 proceeds to a sixth stage SB6 at which the multiplying part 42 carries out multiplication between $\exp(-2\pi j p/N)$ and the local signal in accordance with Equation (28) to produce an internal product to make the processed signal represent the internal product. The multiplying part 42 will be referred to as an internal multiplying arrangement.

Returning to FIG. 4, the forward FFT part 23 is connected to the multiplying part 42 and is for carrying out the linear forward FFT on the processed signal in accordance with Equation (30) to produce an internal signal representative of a result of the forward FFT. The forward FFT part 23 is herein referred to as an internal transform carrying out arrangement.

The second forward processing part 22 is connected to the forward FFT part 23 and is for processing the internal signal into the forward transformed signal in accordance with Equation (31). More particularly, the second forward processing part 22 carries out multiplication between the internal signal and $[-2\pi j(k+1/2)/(2N)]$ into a local product, namely, a real part, to make the forward transformed signal represent the local product. In this event, the second forward processing part 22 will be referred to as an internal multiplying arrangement. A combination of the first forward processing, the second forward processing, and the forward FFT parts 21, 22, and 23 will be referred to as a transform carrying out arrangement.

Referring to FIG. 6 together with FIG. 4, operation of the first inverse processing part 31 will be described at first. At a first stage SC1, the first inverse processing part 31 is supplied with the forward transformed signal from the second forward processing part 22. The first stage SC1 proceeds to a second stage SC2 at which the first inverse processing part 31 processes the $2k$ th apparatus input datum into a k th particular datum. In other words, the forward transformed signal is processed in accordance with Equation (37a). In this event, the first inverse processing part 16 will be referred to as a particular processing arrangement.

The second stage SC2 proceeds to a third stage SC3 at which the first inverse processing part 31 processes the $(2k+1)$ th apparatus input datum into a $(N-1-k)$ th specific datum. In other words, the forward transformed signal is processed in accordance with Equation (37c). In this event, the first inverse processing part 16 will be referred to as a specific processing arrangement.

The third stage SC3 proceeds to a fourth stage SC4 at which the first inverse processing part 31 carries out multi-

plication between $\exp(2\pi j k/N)$ and each of the k th particular and the $(N-1-k)$ th specific data in accordance with Equation (38) into the processed signal. In this event, the first inverse processing part 16 will be referred to as a calculation arrangement.

In FIG. 4, the inverse FFT part 33 carries out the linear inverse FFT on the processed signal in accordance with Equation (40) to produce an internal signal representative of a result of the inverse FFT. The inverse FFT part 23 will be referred to as an internal transform carrying out arrangement.

Referring to FIG. 7 together with FIG. 4, the description will be directed to operation of the second inverse processing part 32. The inverse FFT part 23 produces, as the internal signal, a succession of zeroth through $(p-1)$ th and p th through $(N/2-1)$ th internal data. At a first stage SD1, the second inverse processing part 32 is supplied with the internal signal from the inverse FFT part 23.

The first stage SD1 proceeds to a second stage SD2 at which the second inverse processing part 32 carries out multiplication between the p th internal datum and the $\exp[2\pi j(p+1/2)/(2N)]$ in accordance with Equation (41) into a local product to make the inverse transformed signal represent the local product. The local product is a succession of zeroth through $(N/4-1)$ th and $(N/4)$ th through $(N/2-1)$ th product data. In this event, the second inverse processing part 32 will be referred to as a multiplying arrangement.

The second stage SD2 proceeds to a third stage SD3 at which the second inverse processing part 32 processes the zeroth through the $(N/4-1)$ th product data in accordance with Equation (42a) into a first succession of $(3N/4-1)$ th through $(N/2)$ th particular data in a descending order and a second succession of $(3N/4)$ th through N th particular data in ascending order. The particular data of the first and the second successions have a first polarity in common. In this event, the second inverse processing part 32 will be referred to as a particular processing arrangement.

The third stage SD3 proceeds to a fourth stage SD4 at which the second inverse processing part 32 processes the $(N/4)$ th through the $(N/2-1)$ th product data in accordance with Equation (42b) into a first succession of zeroth through $(N/4-1)$ th specific data in an ascending order and a second succession of $(N/2-1)$ th through $(N/4)$ th specific data in a descending order. The specific data of the first and the second successions have a second polarity in common. The second polarity is different from the first polarity. In this event, the second inverse processing part 32 will be referred to as a specific processing arrangement.

While the present invention has thus far been described in connection with only a few embodiment thereof, it will readily be possible for those skilled in the art to put this invention into practice in various other manners. For example, the block length N may be equal to 256 or 512.

What is claimed is:

1. An apparatus for carrying out a forward *modified discrete cosine* transform comprising:

an input signal;

a multiplier, said multiplier multiplying a predetermined forward transform window function and said input signal and outputting as a result a product signal;

transform carrying out means connected to said multiplier for carrying out a linear forward *modified discrete cosine* transform on said product signal and for outputting a forward *modified discrete cosine* transformed signal representative of said linear forward *modified discrete cosine* transform, wherein said transform carrying out means further comprises:

15

a first processing device connected to receive said product signal from said multiplier, said first processing device outputting a processed signal;
 means connected to said first processing device for receiving said processed signal and carrying out a forward fast Fourier transform on said processed signal and outputting an internal signal representative of said forward fast Fourier transform; and
 a second processing device connected to receive said internal signal from said means for carrying out a forward fast Fourier transform, said second processing device processing said internal signal and outputting as a result said forward *modified discrete cosine* transformed signal.

2. An apparatus as recited in claim 1, wherein said product signal produced by said multiplier, is a succession of zeroth through (N/4-1)th and (N/4)th through (N-1)th product data, where N represents an integral multiple of four;

said first processing device includes a particular processing means connected to said multiplier for processing said zeroth through said (N/4-1)th product data into a succession of (3N/4) through Nth particular data having a first polarity in common;

said first processing device further includes a specific processing means connected to said multiplier for processing said (N/4)th through said (N-1)th product data into a succession of zeroth through (3N/4-1)th specific data having a second polarity in common, said second polarity being different from said first polarity; and

a calculating means is connected to said particular processing means, said specific processing means, and said means for carrying out a forward fast Fourier transform, for calculating said processed signal by using a predetermined signal and each of said (3N/4) through said Nth particular and said zeroth through said (3N/4-1)th specific data.

3. An apparatus as recited in claim 2, wherein said predetermined signal represents $\exp(-2\pi jn/(2N))$, and said calculating means multiplies said $\exp(-2\pi jn/(2N))$ and each of said (3N/4) through said Nth particular data and said zeroth through the (3N/4-1)th specific data to produce said processed signal, where j represents an imaginary unit, n being variable between 0 and N-1, both inclusive.

4. An apparatus as recited in claim 2, wherein said calculating means comprises:

combining means connected to said particular and said specific processing means for combining said particular and said specific data successions into a succession of zeroth through (N-1-2p)th and 2pth through (N-1)th combined data, where p is variable between 0 and N/2-1, both inclusive;

a subtractor connected to said combining means, said subtractor subtracting said (N-1-2p)th combined datum from said 2pth combined datum to produce a difference and output a local signal representative of said difference; and

internal multiplying means connected to said subtractor and said means for carrying out a forward fast Fourier transform, for multiplying a predetermined signal with said local signal into an internal product to make said processed signal represent said internal product.

5. An apparatus as recited in claim 4, wherein said predetermined signal represents $\exp(-2\pi jp/N)$, and said internal multiplying means multiplies said $\exp(-2\pi jp/N)$ and said local signal to produce said processed signal, where j represents an imaginary unit, p being variable between 0 and N-1, both inclusive.

16

6. An apparatus as recited in claim 1, wherein said internal signal is a succession of zeroth through (K-1)th and kth through (N/2-1)th internal data, where N represents an integral multiple of four, k being variable between 0 and N-1, both inclusive, and wherein said second processing device includes internal multiplying means connected to said means for carrying out a forward fast Fourier transform, for multiplying said kth internal datum and $\exp(-2\pi j(k+1/2)/(2N))$ into a local product to make said forward transformed signal represent said local product, where j represents an imaginary number.

7. An apparatus for carrying out an inverse *modified discrete cosine* transform comprising:

an input signal *comprising a modified discrete cosine transformed signal*;

transform carrying out means for carrying out a linear inverse *modified discrete cosine* transform on said input signal and for outputting an inverse *modified discrete cosine* transformed signal representative of a result of said linear inverse *modified discrete cosine* transform;

a multiplier connected to said transform carrying out means, said multiplier multiplying a predetermined inverse transform window function and said inverse *modified discrete cosine* transformed signal to produce a product signal; wherein said transform carrying out means comprises:

a first processing device which receives said input signal and outputs a processed signal;

internal transform carrying out means connected to said first processing device for carrying out an inverse fast Fourier transform on said processed signal and for outputting as a result of said inverse fast Fourier transform an internal signal; and

a second processing device connected to said internal transform carrying out means to receive said internal signal and output as a result of processing said internal signal said inverse *modified discrete cosine* transformed signal.

8. An apparatus as recited in claim 7, said input signal being a succession of zeroth through (N-1)th apparatus input data, where N represents an integral multiple of four, wherein said first processing device includes a first multiplier, said multiplier multiplying said zeroth through said (N-1)th apparatus input data and $\exp(2\pi(N/4+1/2)k/N)$ and outputting as a result a first product, said processed signal representing said first product, where j represents an imaginary unit, k being variable between 0 and N-1, both inclusive.

9. An apparatus as recited in claim 7, said internal transform carrying out means producing, as said internal signal, a succession of zeroth through (N-1)th internal data, where N represents an integral multiple of four, wherein said second processing device includes a second multiplier connected to said internal transform carrying out means, said multiplier multiplying said zeroth through said (N-1)th internal data and $\exp(-2\pi j(n+N/4+1/2)/(2N))$ into a second product, said inverse transformed signal representing said second product, where j represents an imaginary unit, n being variable between 0 and N-1, both inclusive.

10. An apparatus as recited in claim 7, wherein said input signal is a succession of zeroth through (N/2-1)th apparatus input data, where N represents an integral multiple of four;

said first processing device includes a particular processing means for processing said 2kth apparatus input datum into a kth particular datum, where k is variable between 0 and N/2-1, both inclusive and a specific pro-

17

cessing means for processing said (2k+1)th apparatus input datum into a (N-1-k)th specific datum; and a calculating means connected to said particular and said specific processing means for calculating said processed signal by using a predetermined signal and each of said kth particular and said (N-1-k)th specific data.

11. An apparatus as recited in claim 10, wherein said predetermined signal represents $\exp(2\pi jk/N)$, where j represents an imaginary unit, and said calculating means multiplies said predetermined signal and said kth particular datum.

12. An apparatus as recited in claim 7, said internal transform carrying out means producing, as said internal signal, a succession of zeroth through (p-1)th and pth through (N/2-1)th internal data, where N represents an integral multiple of four, p being variable between 0 and (N/2-1), both inclusive, wherein said second processing device comprises:

a multiplier connected to said internal transform carrying out means, said multiplier multiplying said pth internal datum and $\exp(2\pi j(p+1/2)/2N)$ resulting in a local product to make said inverse transformed signal represent said local product, j representing an imaginary unit, said local product being a succession of zeroth through (N/4-1)th and (N/4)th through (N/2-1)th product data;

a particular processing means connected to said multiplier for processing said zeroth through said (N/4-1)th product data into a first succession of [(3N/4-1)] (3N/4-1)th through (N/2)th particular data in a descending order and a second succession of (3N/4)th through Nth particular data in an ascending order, said particular data of said first and said second successions having a first polarity in common; and

a specific processing means connected to said multiplier for processing said (N/4)th through (N/2-1)th product data into a first succession of zeroth through (N/4-1)th specific data in an ascending order and a second succession of (N/2-1)th through (N/4)th specific data in a descending order, the specific data of said first and said second successions having a second polarity in common, said second polarity being different from said first polarity.

13. The apparatus of claim 1 wherein said input signal is an audio signal.

14. The apparatus of claim 1 wherein said modified discrete cosine transformed signal has a block length N of 512.

15. The apparatus of claim 1 wherein said transform carrying out means calculates fewer than N^2 multiplications.

16. The apparatus of claim 1 wherein said transform carrying out means calculates fewer than $N(N-1)$ additions.

17. The apparatus of claim 1 wherein said processed signal is formed by multiplying said input signal by a predetermined factor.

18. The apparatus of claim 17 wherein said modified discrete cosine transformed signal comprises said internal signal representative of said forward fast Fourier transform multiplied by a second predetermined factor.

19. The apparatus of claim 7 wherein said modified discrete cosine transformed signal is a transformed audio signal.

20. The apparatus of claim 7 wherein said modified discrete transformed signal has a block length N of 512.

21. The apparatus of claim 7 wherein said transform carrying out means calculates fewer than N^2 multiplications to carry out said inverse discrete cosine transform.

22. The apparatus of claim 21 wherein said transform carrying out means calculates fewer than $N(N-1)$ additions to carry out said inverse discrete cosine transform.

18

23. The apparatus of claim 7 wherein said processed signal comprises said input signal multiplied by a predetermined factor.

24. The apparatus of claim 23 wherein said inverse modified discrete cosine transform signal comprises said internal signal representative of said inverse forward fast Fourier transform multiplied by a second predetermined factor.

25. An apparatus for carrying out an inverse transform comprising:

an input signal $y(m,k)$;

transform carrying out means for carrying out a linear inverse transform $xt(m,n)$ on said input signal $y(m,k)$ and for outputting an inverse transformed signal representative of a result of said linear inverse transform, said linear inverse transform being defined by:

$$xt(m, n) = 2/N \sum_{k=0}^{N-1} y(m, k) \cos[2\pi(n + n_0)(k + 1/2)/N]$$

where m represents a block number, n represents a sample number, N represents a block length and k is an integer between 0 and N-1;

a multiplier connected to said transform carrying out means, said multiplier multiplying a predetermined inverse transform window function and said inverse transformed signal to produce a product signal; wherein said transform carrying out means comprises:

a first processing device which receives said input signal $y(m,k)$ and outputs a processed signal, said processed signal comprising a product signal formed by multiplying said input signal $y(m,k)$ by a predetermined factor; internal transform carrying out means connected to said first processing device for carrying out an inverse fast Fourier transform on said processed signal and for outputting as a result of said inverse fast Fourier transform an internal signal; and

a second processing device connected to said internal transform carrying out means to receive said internal signal and output as a result of processing said internal signal said inverse transformed signal.

26. The apparatus of claim 17 wherein N is 512.

27. The apparatus of claim 17 wherein said transform carrying out means calculates fewer than N^2 multiplications.

28. The apparatus of claim 19 wherein said transform carrying out means calculates fewer than $N(N-1)$ additions.

29. An apparatus for carrying out an inverse transform comprising:

a transformed discrete audio input signal having a block size (N) of 512;

transform carrying out means for carrying out a linear inverse transform on said input signal by calculating fewer than N^2 multiplications and fewer than $N(N-1)$ additions, and for outputting an inverse transformed signal representative of a result of said linear inverse transform;

a multiplier connected to said transform carrying out means, said multiplier multiplying a predetermined inverse transform window function and said inverse transformed signal to produce a product signal; wherein said transform carrying out means comprises: a first processing device which receives said input signal and outputs a processed signal;

internal transform carrying out means connected to said first processing device for carrying out an inverse fast

19

Fourier transform on said processed signal and for outputting as a result of said inverse fast Fourier transform an internal signal; and

a second processing device connected to said internal transform carrying out means to receive said internal signal and output as a result of processing said internal signal said inverse transformed signal.

30. An apparatus for carrying out a forward transform comprising:

an input signal $x(n)$;

a multiplier for multiplying a predetermined forward transform window function and said input signal $x(n)$ to produce a product signal to produce a product signal $xh(n)$;

transform carrying out means connected to said multiplier for carrying out a linear forward transform on said product signal $xh(n)$ and for outputting a forward transformed signal $y(m,k)$ representative of a result of said forward transform, said linear forward transform being defined by;

$$y(m, k) = \sum_{n=0}^{N-1} xh(n) \cos [2\pi(k + 1/2)(n + n_0)/N]$$

where m represents a block number, n represents a sample number, N represents a block length and k is an integer between 0 and $N-1$;

wherein said transform carrying out means comprises:

a first processing device which receives said product signal $xh(n)$ and outputs a processed signal, said processed signal comprising a product signal formed by multiplying said product signal $xh(n)$ by a predetermined factor;

internal transform carrying out means connected to said first processing device for carrying out a forward fast Fourier transform on said processed signal and for outputting as a result of said forward fast Fourier transform an internal signal; and

a second processing device connected to said internal transform carrying out means to receive said internal signal and output as a result of processing said internal signal said forward transformed signal.

31. An apparatus for carrying out a forward transform comprising:

an input signal having a block size (N) of 512;

a multiplier for multiplying a predetermined forward transform window function and said input signal to produce a product signal; and

transform carrying out means connected to said multiplier for carrying out a linear forward transform on said product signal by calculating fewer than N^2 multiplications and fewer than $N(N-1)$ additions, and for outputting a forward transformed signal representative of a result of said linear forward transform;

wherein said transform carrying out means comprises:

a first processing device which receives said product signal and outputs a processed signal;

internal transform carrying out means connected to said first processing device for carrying out a forward fast Fourier transform on said processed signal and for outputting as a result of said forward fast Fourier transform an internal signal; and

a second processing device connected to said internal transform carrying out means to receive said internal

20

signal and output as a result of processing said internal signal said forward transformed signal.

32. An apparatus for carrying out a forward modified discrete cosine transform comprising:

an input signal;

a multiplier, said multiplier multiplying a predetermined forward transform window function and said input signal and outputting as a result a product signal; and

transform carrying out means connected to said multiplier for carrying out a linear forward modified discrete cosine transform on said product signal and for outputting a forward modified discrete cosine transformed signal representative of said linear forward modified discrete cosine transform, wherein said transform carrying out means comprises:

a first processing device connected to receive said product signal having N samples, N being an integer, from said multiplier, said first processing device outputting a processed signal having M samples, M being an integer different from N ;

means connected to said first processing device for receiving said processed signal and for carrying out a forward fast Fourier transform on said processed signal, and for outputting an internal signal representative of said forward fast Fourier transform; and

a second processing device connected to receive said internal signal from said means for carrying out a forward fast Fourier transform, said second processing device processing said internal signal and outputting as a result said forward modified discrete cosine transformed signal.

33. The apparatus as claimed in claim 32, wherein M is smaller than N .

34. The apparatus as claimed in claim 32, wherein M is equal to $N/2$.

35. An apparatus for carrying out an inverse modified discrete cosine transform comprising:

an input signal having M samples, M being an integer;

transform carrying out means carrying out a linear inverse modified discrete cosine transform on said input signal and for outputting an inverse modified discrete cosine transformed signal having M samples representative of said linear inverse modified discrete cosine transform; and

a multiplier connected to said transform carrying out means, said multiplier multiplying a predetermined inverse transform window function and said linear inverse modified discrete cosine transformed signal to produce a product signal having N samples, N being an integer different from M , wherein said transform carrying out means comprises:

a first processing device which receives said input signal, said first processing device outputting a processed signal;

internal transform carrying out means connected to said first processing device for carrying out an inverse fast Fourier transform on said processed signal as a result of processing said inverse fast Fourier transform an internal signal; and

a second processing device connected to said internal transform carrying out means to receive said internal signal and output as a result of processing said inverse modified discrete cosine transformed signal.

36. The apparatus as claimed in claim 35, wherein M is smaller than N .

21

37. The apparatus as claimed in claim 35, wherein M is equal to $N/2$.

38. An apparatus for carrying out a forward transform comprising:

an input signal $x(n)$;

a multiplier for multiplying a predetermined forward transform window function and said input signal $x(n)$ to produce a product signal $xh(n)$; and

transform carrying out means connected to said multiplier for carrying out a linear forward transform on said product signal $xh(n)$ and for outputting a forward transformed signal $y(m,k)$ representative of a result of said forward transform, said linear forward transform being defined by;

$$y(m, k) = \sum_{n=0}^{N-1} xh(n) \cos [2\pi(k + 1/2)(n + n_0)/N]$$

where m represents a block number, n represents a sample number, N represents a block length and k is an integer between 0 and $N-1$;

wherein said transform carrying out means comprises:

a first processing device which receives said product signal $xh(n)$ having N samples and outputs a processed signal having M samples, M being an integer different from N , said processed signal comprising a product signal formed by multiplying said product signal $xh(n)$ by a predetermined factor;

internal transform carrying out means connected to said first processing device for carrying out a forward fast Fourier transform on said processed signal and for outputting as a result of said forward fast Fourier transform an internal signal; and

a second processing device connected to said internal transform carrying out means to receive said internal signal and output as a result of processing said internal signal said forward transformed signal.

39. The apparatus as claimed in claim 38, wherein M is smaller than N .

40. The apparatus as claimed in claim 38, wherein M is equal to $N/2$.

41. An apparatus for carrying out an inverse transform comprising:

an input signal $y(m,k)$ having M samples, M being an integer;

transform carrying out means for carrying out a linear inverse transform on said input signal $y(m,k)$ and for outputting an inverse transformed signal $xt(m,n)$ representative of a result of said linear inverse transform, said linear inverse transform being defined by:

$$xt(m, n) = 2/N \sum_{k=0}^{M-1} y(m, k) \cos [2\pi(n + n_0)(k + 1/2)/N]$$

where m represents a block number, n represents a sample number, N represents a block length and k is an integer between 0 and $N-1$;

a multiplier connected to said transform carrying out means, said multiplier multiplying a predetermined inverse transform window function and said inverse

22

transformed signal $xt(m,n)$ to produce a product signal having N samples, N being an integer different from M ;

wherein said transform carrying out means comprises:

a first processing device which receives said input signal $y(m,k)$ and outputs a processed signal, said processed signal comprising a product signal formed by multiplying said input signal $y(m,k)$ by a predetermined factor; internal transform carrying out means connected to said first processing device for carrying out an inverse fast Fourier transform on said processed signal and for outputting as a result of said inverse fast Fourier transform an internal signal; and

a second processing device connected to said internal transform carrying out means to receive said internal signal and output as a result of processing said internal signal said inverse transformed signal.

42. The apparatus as claimed in claim 41, wherein M is smaller than N .

43. The apparatus as claimed in claim 41, wherein M is equal to $N/2$.

44. An apparatus for carrying out an inverse transform comprising:

an input signal $y(m,k)$ having M samples, M being an integer;

transform carrying out means for carrying out a linear inverse transform on said input signal $y(m,k)$ and for outputting an inverse transformed signal $xt(m,n)$ representative of a result of said linear inverse transform, said linear inverse transform $xt(m,n)$ being determined using the sum:

$$\sum_{k=0}^{M-1} y(m, k) \cos [2\pi(n + n_0)(k + 1/2)/N]$$

where m represents a block number, n represents a sample number, N represents a block length and k is an integer between 0 and $M-1$;

a multiplier connected to said transform carrying out means, said multiplier multiplying a predetermined inverse transform window function and said inverse transformed signal $xt(m,n)$ to produce a product signal having N samples, N being an integer different from M ;

wherein said transform carrying out means comprises:

a first processing device which receives said input signal $y(m,k)$ and outputs a processed signal, said processed signal comprising a product signal formed by multiplying said input signal $y(m,k)$ by a predetermined factor; internal transform carrying out means connected to said first processing device for carrying out an inverse fast Fourier transform on said processed signal and for outputting as a result of said inverse fast Fourier transform an internal signal; and

a second processing device connected to said internal transform carrying out means to receive said internal signal and output as a result of processing said internal signal said inverse transformed signal.

45. The apparatus as claimed in claim 44, wherein M is smaller than N .

46. The apparatus as claimed in claim 44, wherein M is equal to $N/2$.