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(54) **LOW POWER CIRCUIT WITH PROPER SLEW RATE BY AUTOMATIC ADJUSTMENT OF BIAS CURRENT**

(75) Inventors: **Hiromi Nanba**, Tokyo (JP); **Tohru Mizutani**, Kawasaki (JP); **Makoto Ikeshita**, Kawasaki (JP); **Masato Takeyabu**, Sapporo (JP)

(73) Assignee: **Fujitsu Limited**, Kawasaki (JP)

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H03K 5/12 (2006.01)

(52) **U.S. Cl.** **327/170**; 379/538

(58) **Field of Classification Search** 327/94–96, 327/170, 336–339, 345, 379–382, 401, 538, 327/545, 561, 541; 341/122–124; 326/17, 326/22, 26, 30–33; 323/209, 312

See application file for complete search history.

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Primary Examiner—Linh My Nguyen
(74) *Attorney, Agent, or Firm*—Arent Fox LLP

(57) **ABSTRACT**

An evaluation circuit **16** repeats processing in which an output VD thereof is reset, there is obtained repeatedly given times a difference between sampled output voltages Vo of a replica circuit **11**R when respective times t**1** and t**2** have elapsed after a voltage Vi is step-inputted to the replica circuit **11**R, and the differences are successively summed. A comparator circuit **20** compares a difference cumulation voltage VD with a reference voltage VS. A bias adjustment circuit **15** steps up the bias currents of the replica circuit **11**R and an adjusted circuit **11** at every this given times if VD>VS, and ceases the adjustment if VD<VS.

20 Claims, 12 Drawing Sheets

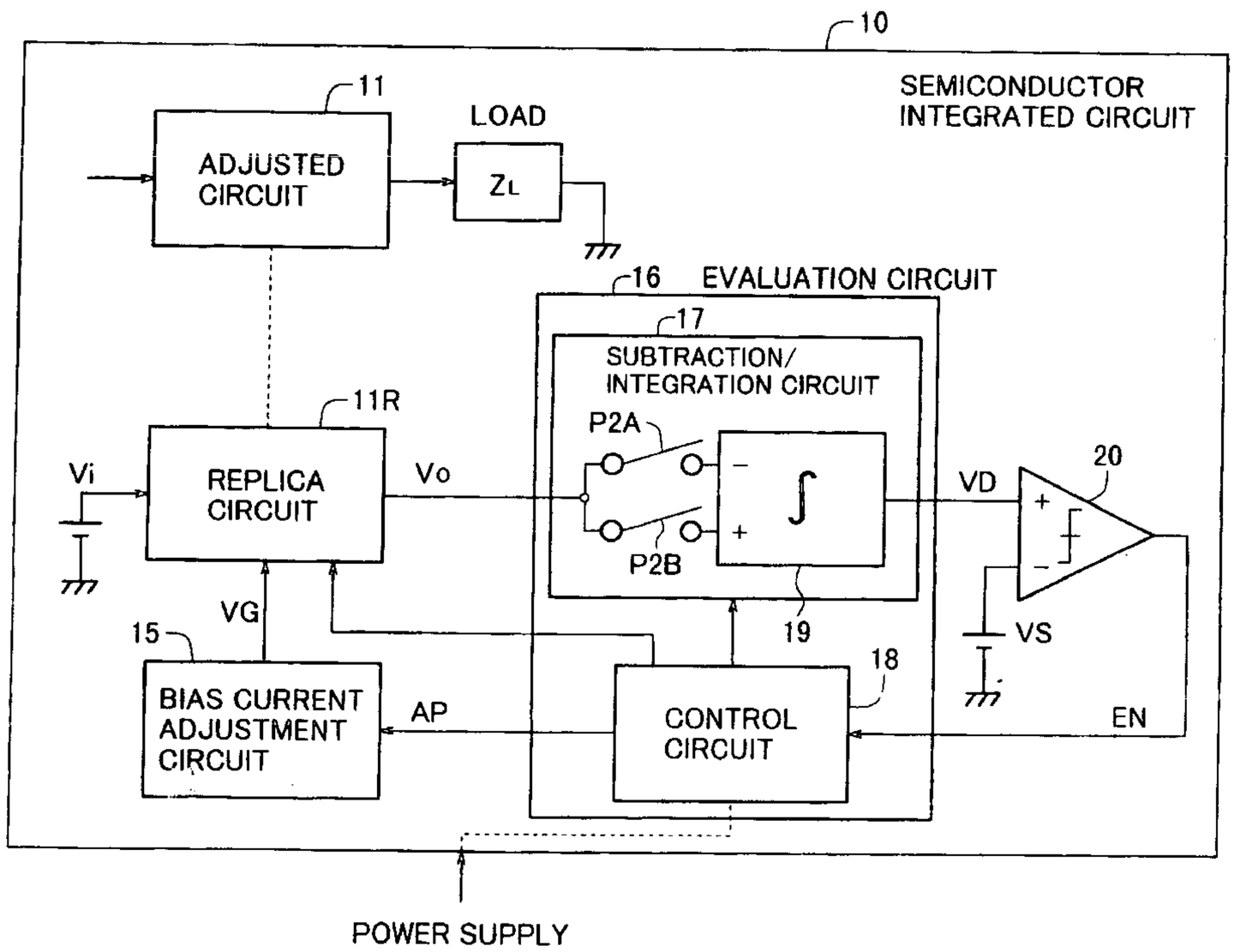


FIG. 1

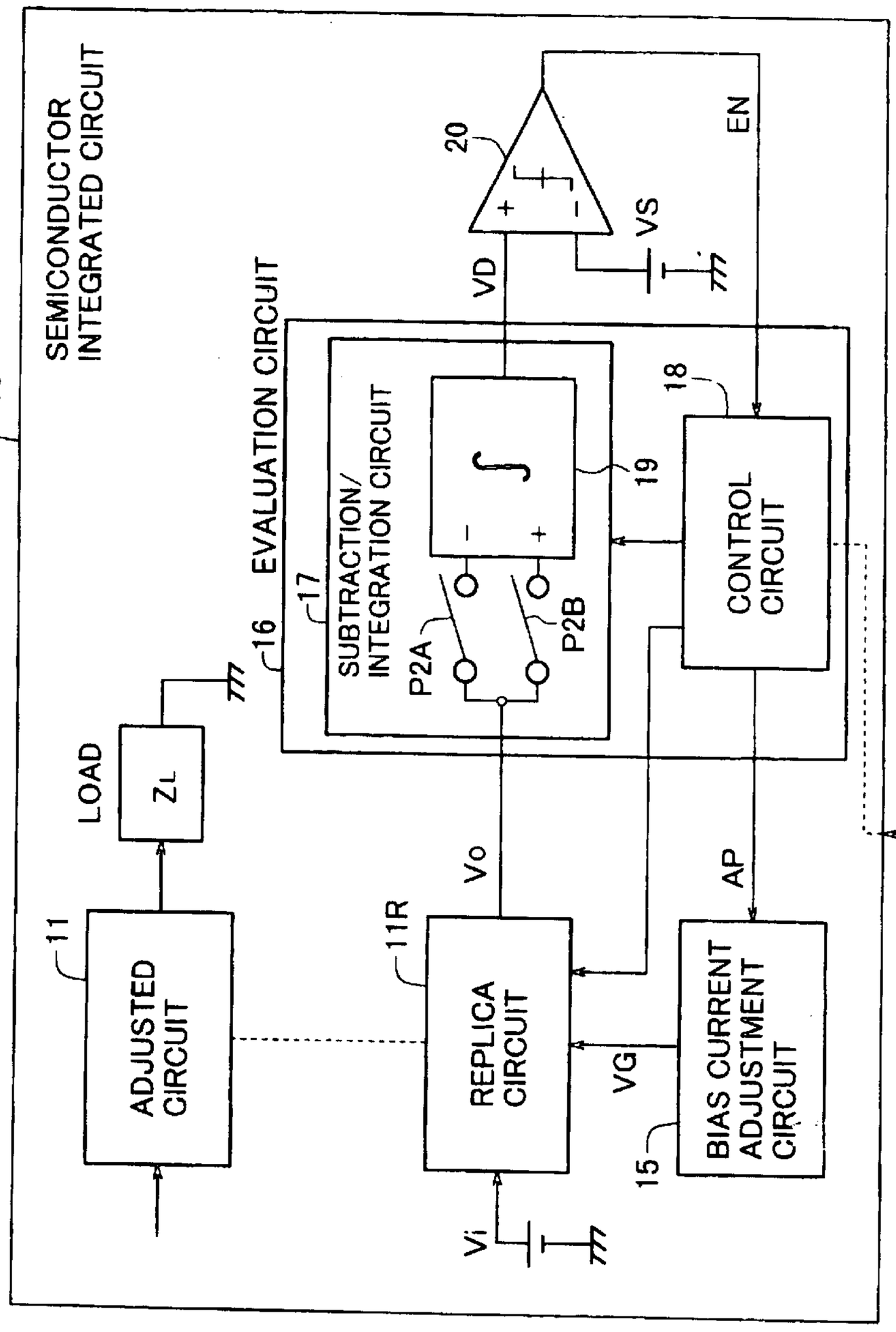

10
SEMICONDUCTOR INTEGRATED CIRCUIT
LOAD
Z_L
11
ADJUSTED CIRCUIT
16
EVALUATION CIRCUIT
17
SUBTRACTION/ INTEGRATION CIRCUIT
P2A
P2B
20
VD
VS
EN
18
CONTROL CIRCUIT
19
V_O
11R
REPLICA CIRCUIT
V_i
VG
15
BIAS CURRENT ADJUSTMENT CIRCUIT
AP
POWER SUPPLY

FIG. 2

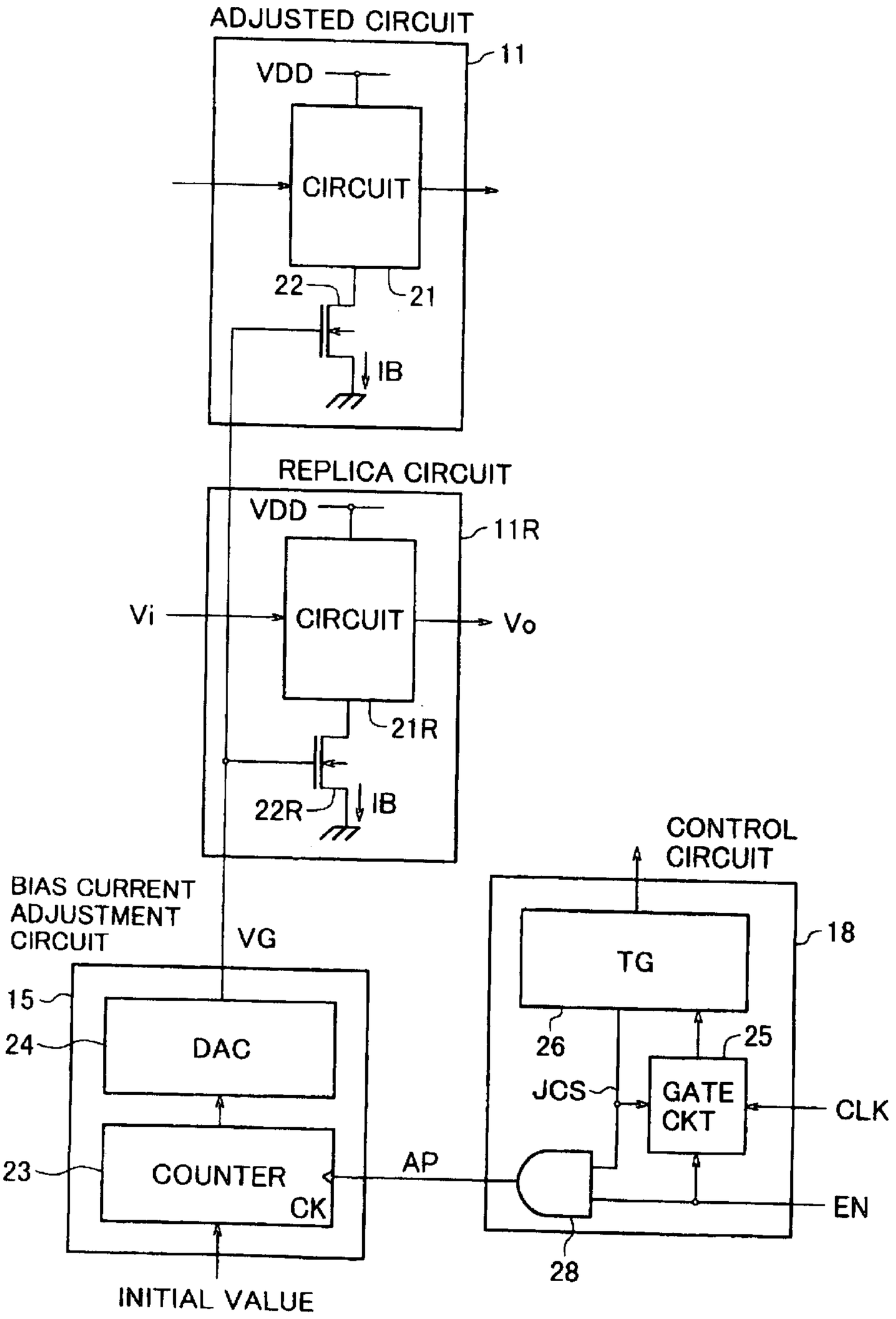
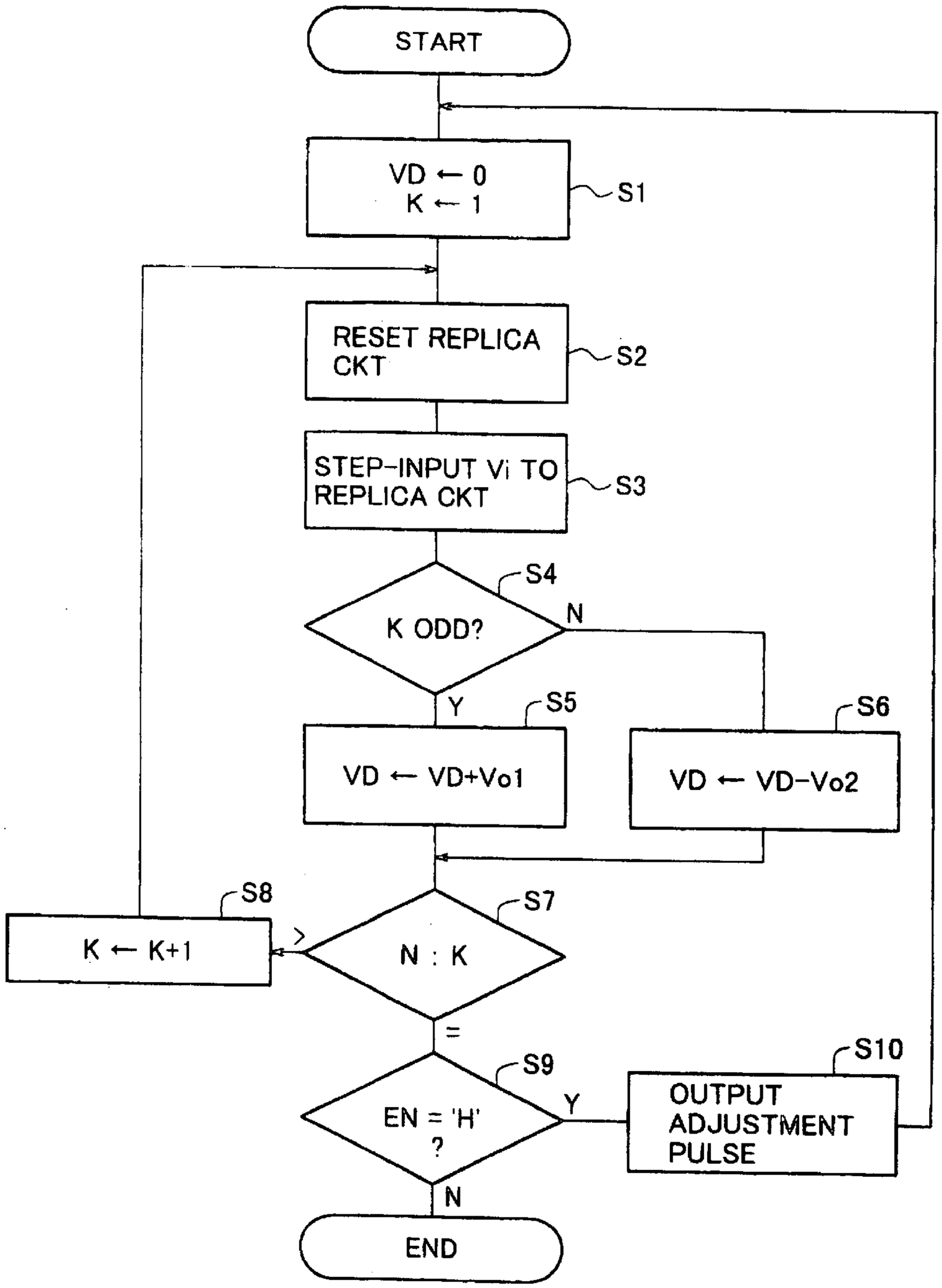

ADJUSTED CIRCUIT
11
VDD
CIRCUIT
22
21
IB
REPLICA CIRCUIT
VDD
11R
Vi
CIRCUIT
Vo
21R
22R
IB
CONTROL CIRCUIT
BIAS CURRENT ADJUSTMENT CIRCUIT
VG
18
TG
15
24
DAC
26
25
JCS
GATE CKT
CLK
23
COUNTER
CK
AP
EN
28
INITIAL VALUE

FIG.3


START
VD ← 0
K ← 1
S1
RESET REPLICA CKT
S2
STEP-INPUT Vi TO REPLICA CKT
S3
S4
K ODD?
N
Y
S5
VD ← VD+Vo1
S6
VD ← VD-Vo2
S8
K ← K+1
>
S7
N : K
=
S9
EN = 'H' ?
Y
S10
OUTPUT ADJUSTMENT PULSE
N
END

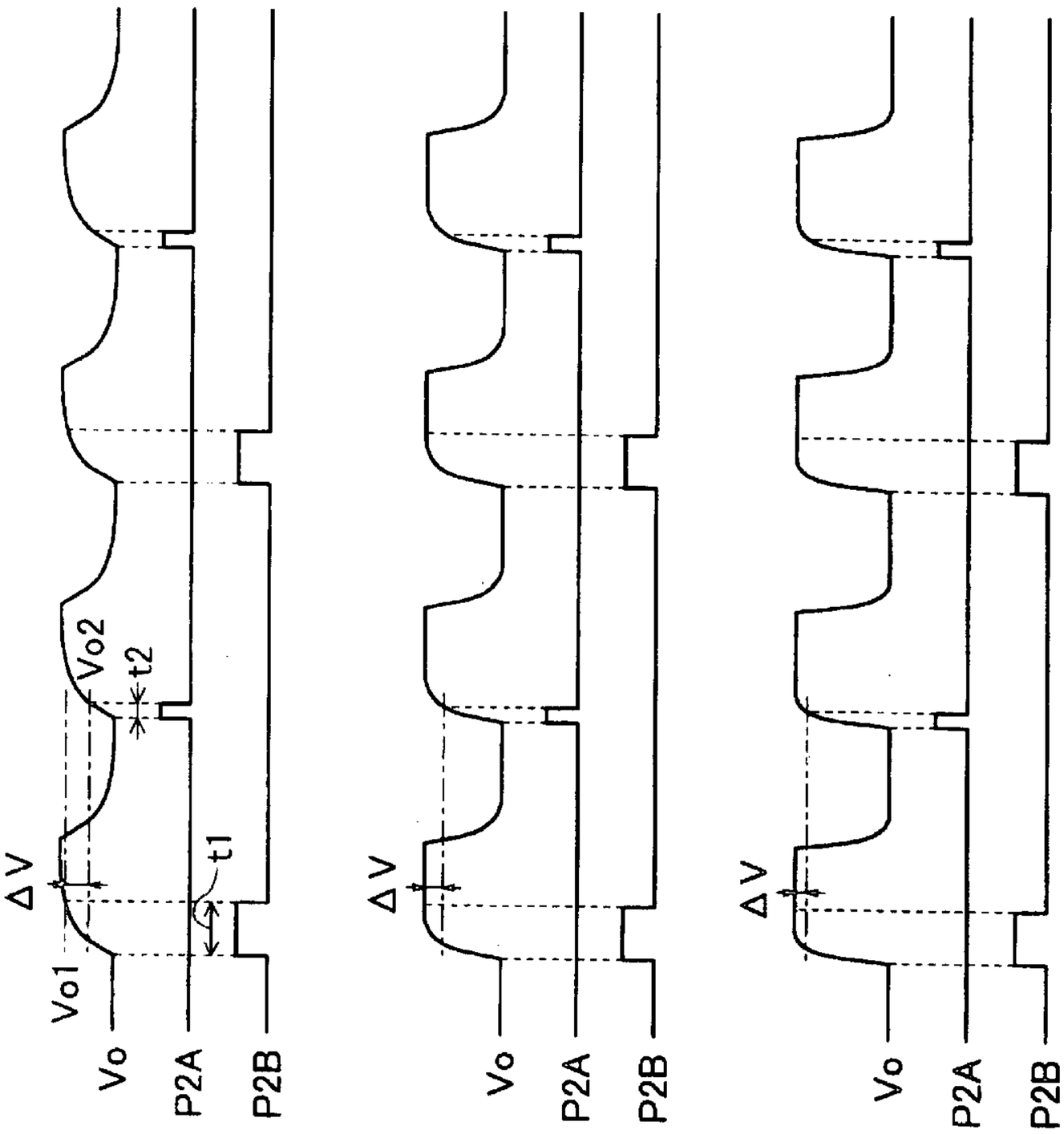


FIG.4(A)

FIG.4(B)

FIG.4(C)

FIG.5(A)

FIG.5(B)

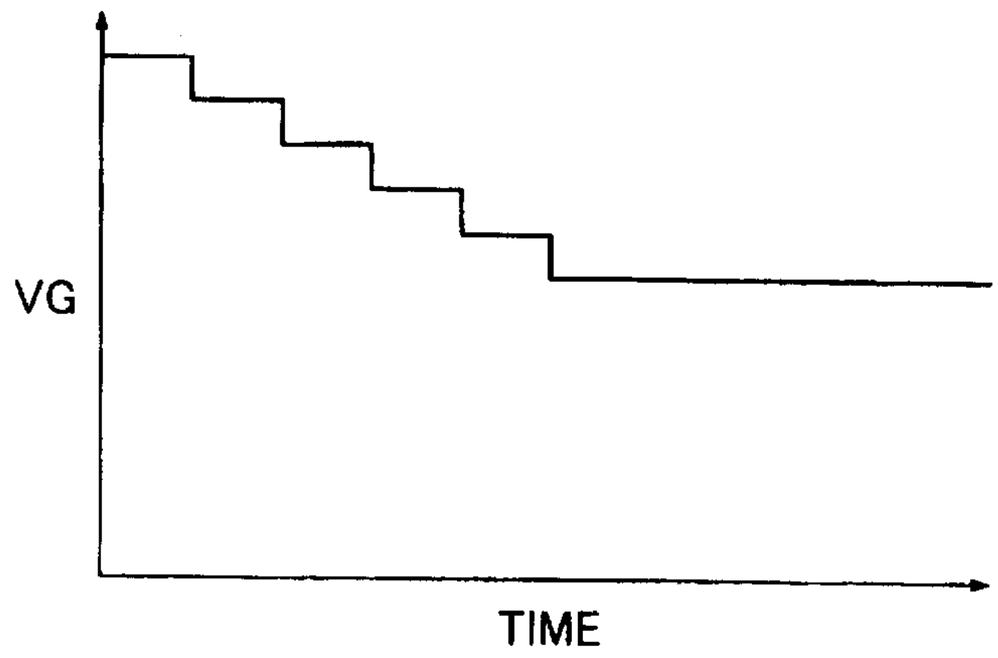


FIG.5(C)

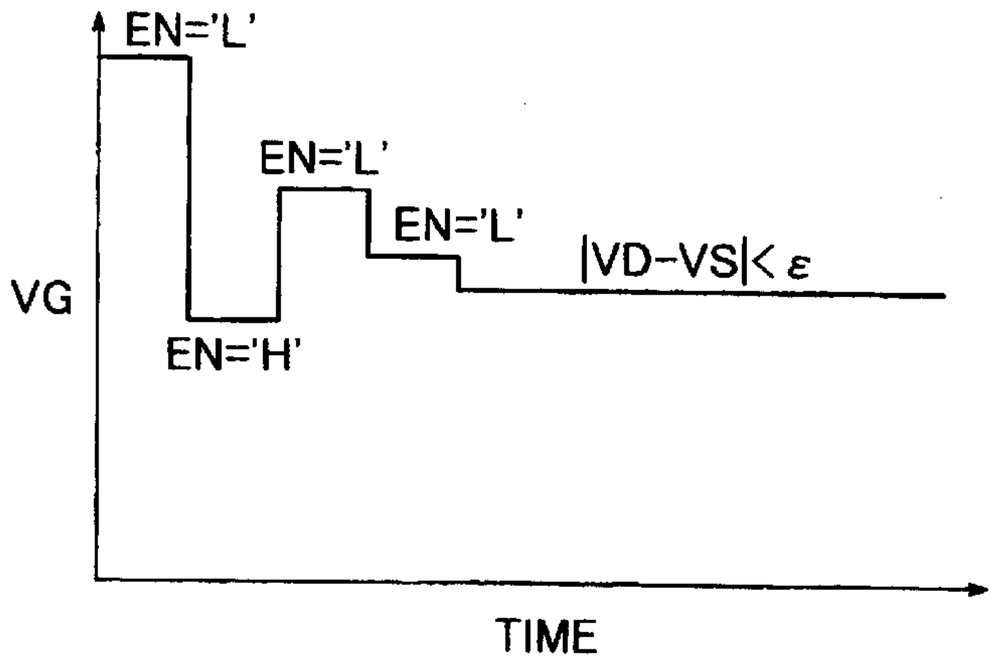


FIG.6

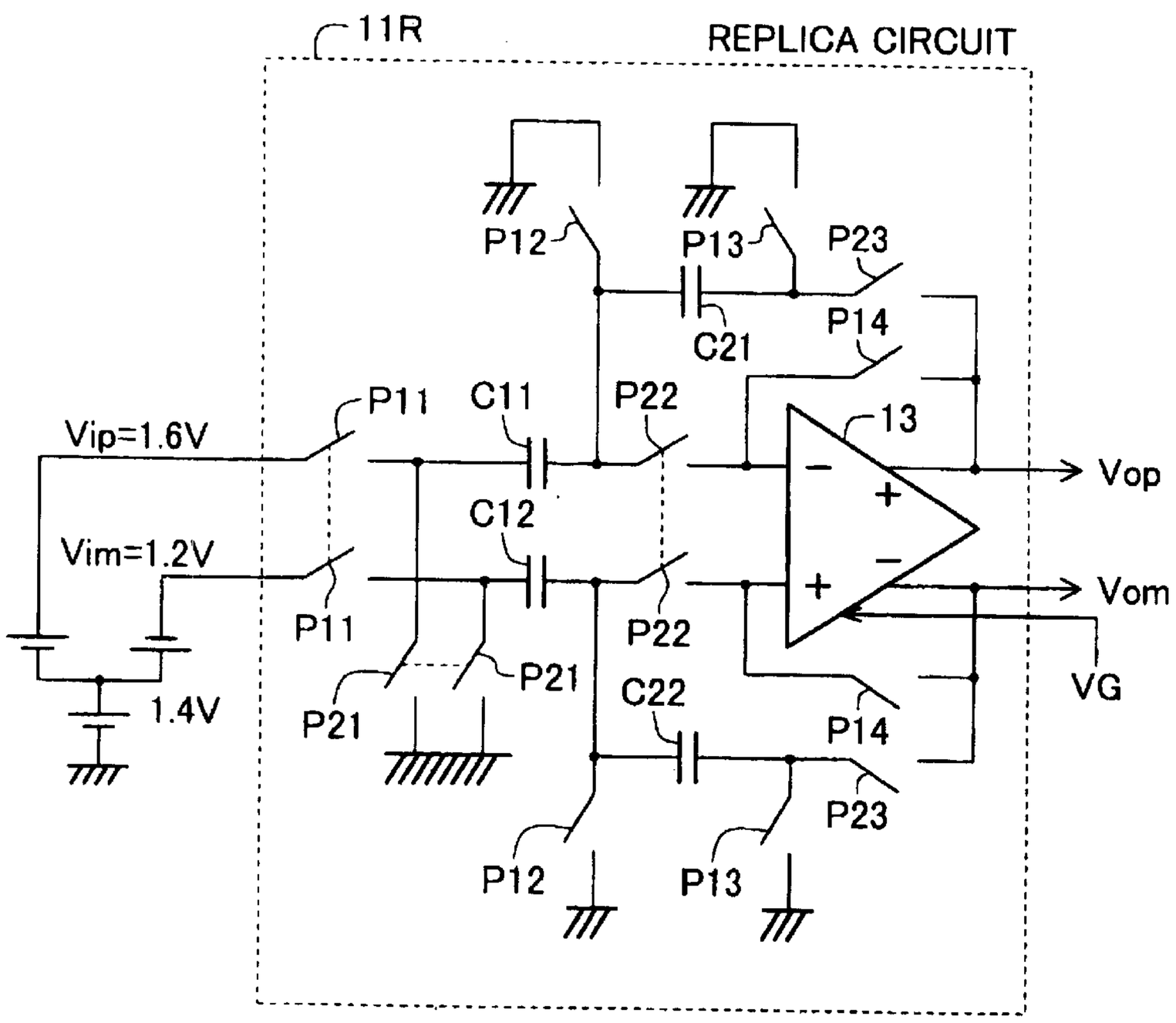

11R
REPLICA CIRCUIT
P12
P13
P23
C21
P14
P11
C11
P22
13
Vip=1.6V
Vop
C12
Vim=1.2V
Vom
P11
P22
P21
P21
C22
VG
1.4V
P14
P23
P12
P13

FIG.7

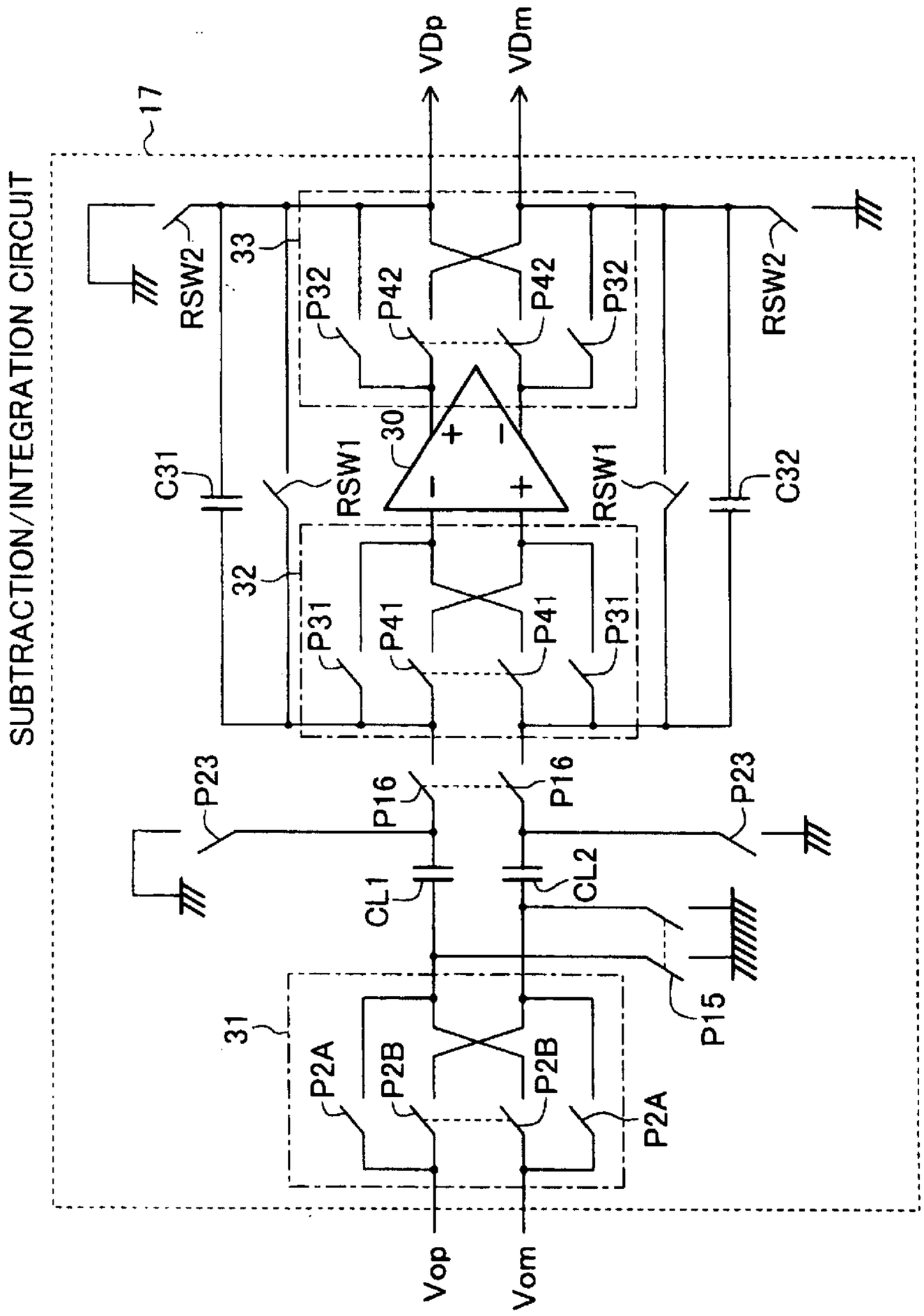

SUBTRACTION/INTEGRATION CIRCUIT
17
T
VDp
VDm
RSW2
33
P32
P42
P42
P32
RSW2
30
C31
RSW1
RSW1
C32
32
P31
P41
P41
P31
P23
P16
P16
P23
CL1
CL2
5
P15
31
P2A
P2B
P2B
P2A
Vop
Vom

FIG.8

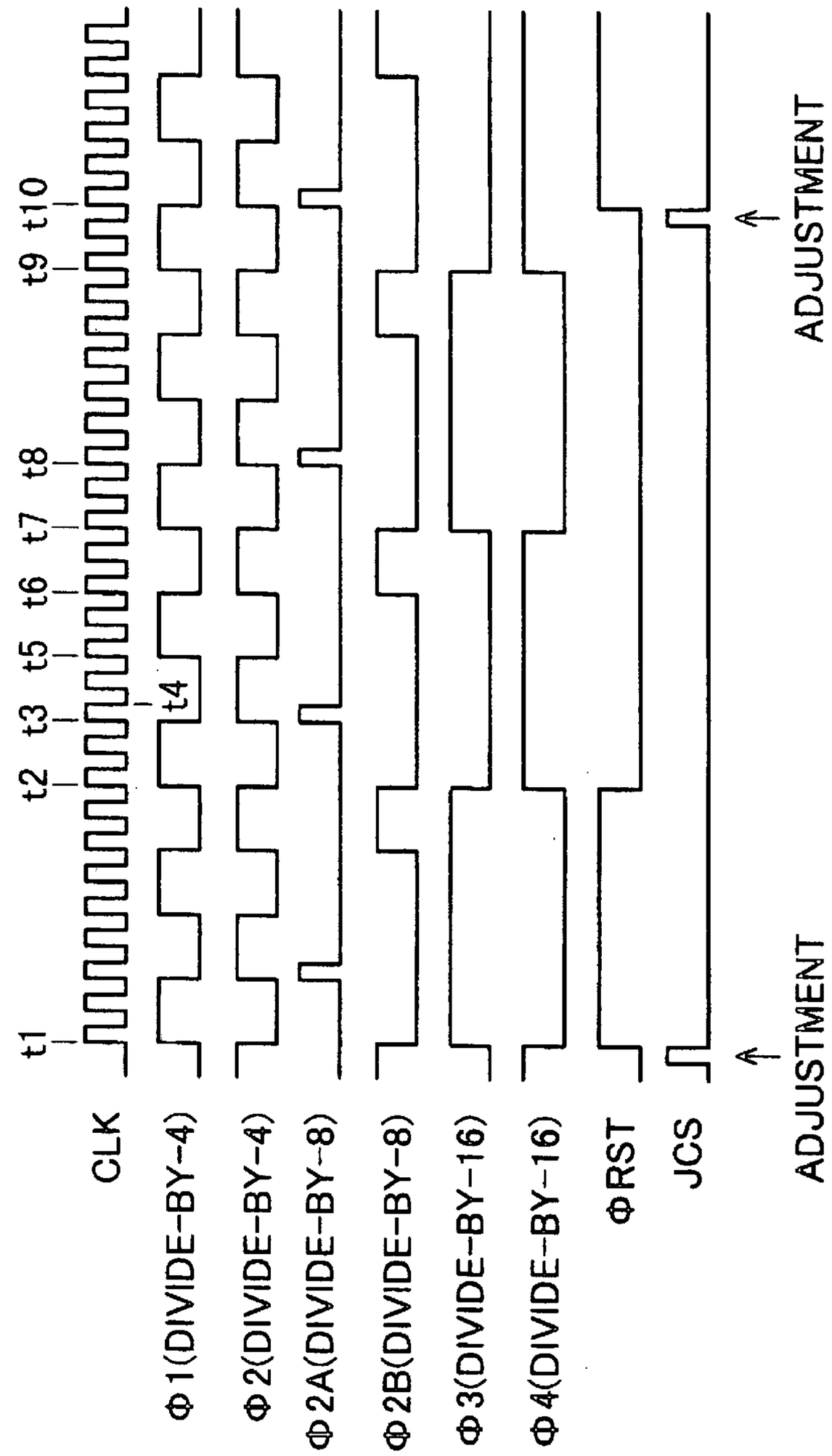

t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
CLK
Φ1(DIVIDE-BY-4)
Φ2(DIVIDE-BY-4)
Φ2A(DIVIDE-BY-8)
Φ2B(DIVIDE-BY-8)
Φ3(DIVIDE-BY-16)
Φ4(DIVIDE-BY-16)
ΦRST
JCS
ADJUSTMENT
ADJUSTMENT

FIG.9
prior art

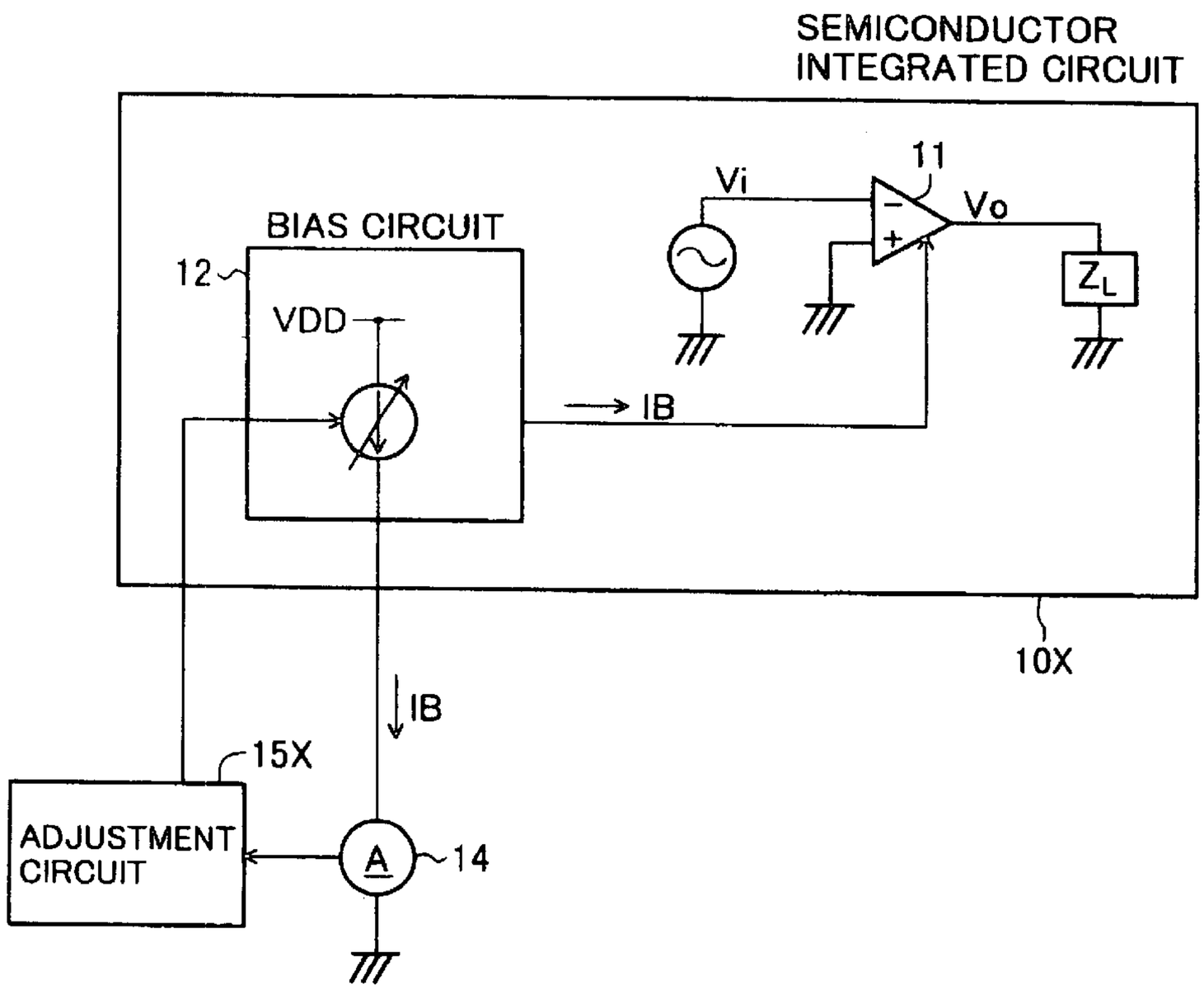


FIG.10
prior art

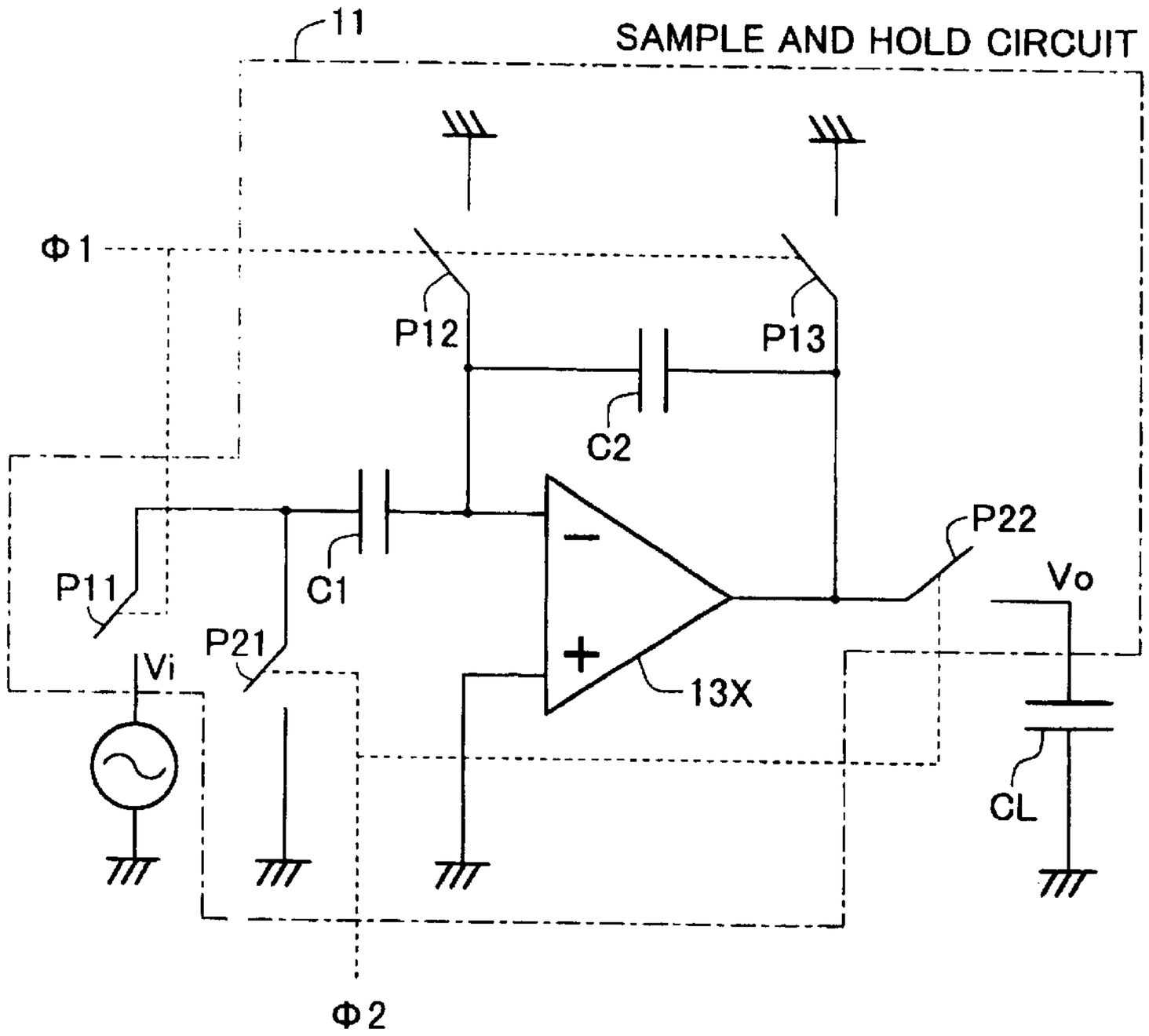


FIG.11
prior art

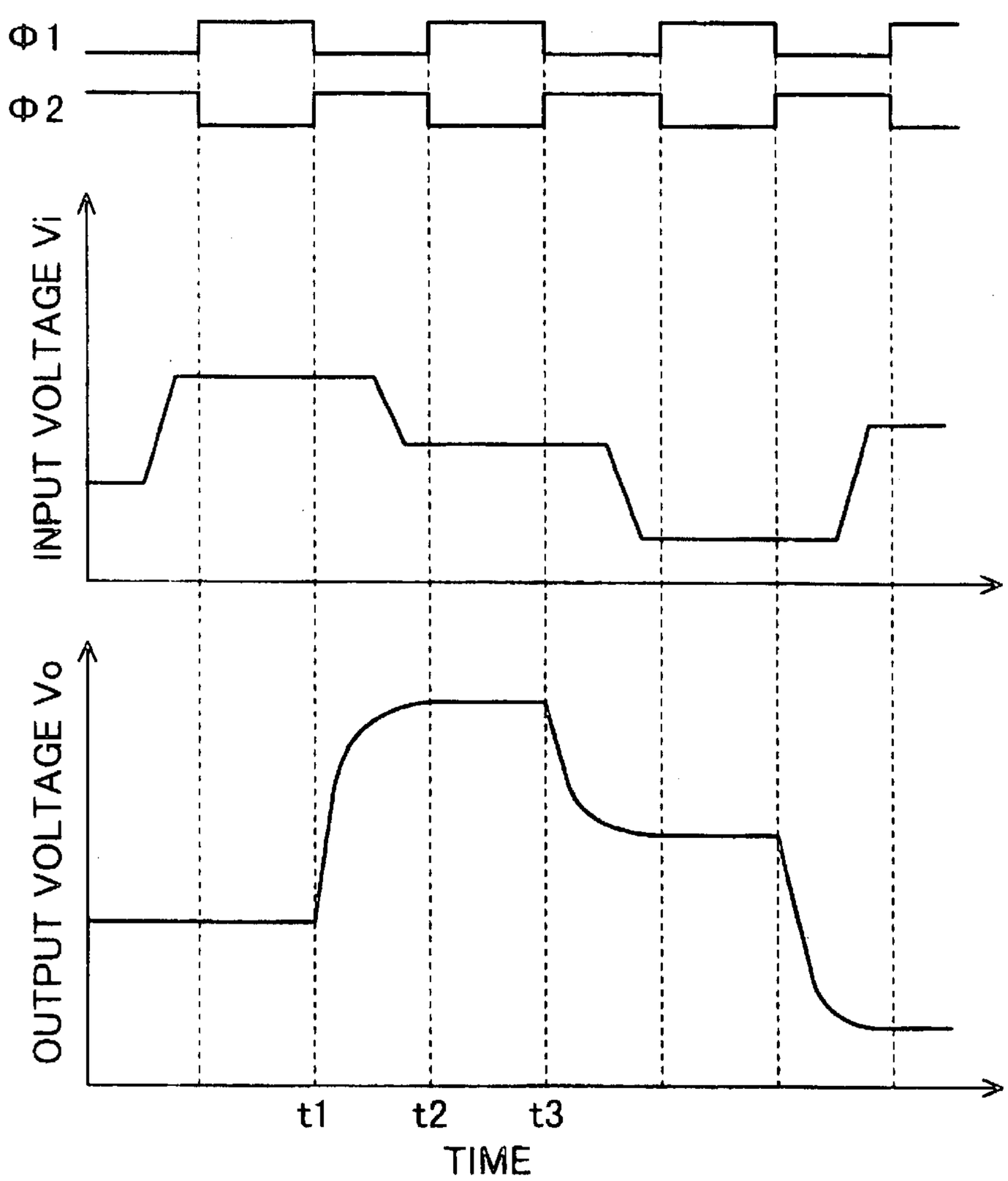
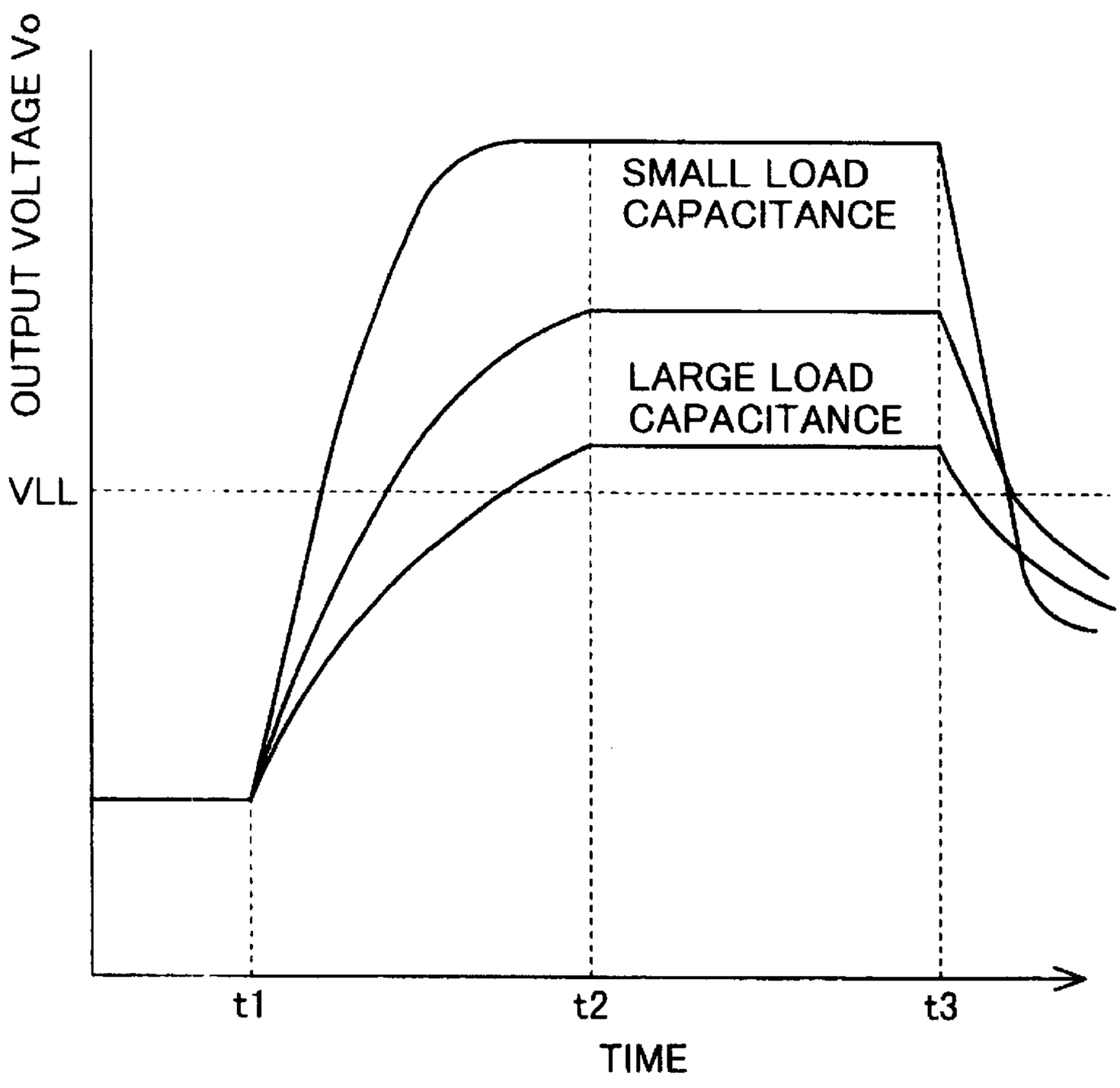


FIG.12
prior art



LOW POWER CIRCUIT WITH PROPER SLEW RATE BY AUTOMATIC ADJUSTMENT OF BIAS CURRENT

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor integrated circuit including an adjusted circuit a slew rate (an amount of change in output voltage per unit time for step input) of whose output is dependent on a bias current and a circuit automatically adjusting the value of the bias current to achieve low power with proper slew rate.

2. Description of the Related Art

FIG. **9** is an illustration of bias adjustment to a prior art semiconductor integrated circuit **10**X including an adjusted circuit **11** whose slew rate is dependent on a bias current IB.

To the adjusted circuit **11**, the bias current IB is provided from a bias current **12**. The output of the adjusted circuit **11** is connected to another circuit not shown or an output terminal of the semiconductor integrated circuit **10**X and a load impedance measured at the output of the adjusted circuit **11** is Z_L.

FIG. **10** shows a sample and hold circuit as an adjusted circuit **11** of FIG. **9**, which is a combination of a switched capacitor circuit and an operational amplifier **13**X. FIG. **10** shows a case where the load impedance can be approximated by a capacitance CL. FIG. **11** are waveform diagrams showing operation of the circuit of FIG. **10**.

The switches of FIG. **10** are controlled by two phase clocks ϕ**1** and ϕ**2** shown in FIG. **11**, wherein a high and a low of each clock correspond to ON and OFF of switches controlled by the clock. The switches P**11**, P**12** and P**13** are is controlled by the clock ϕ**1** and switches P**21** and P**22** are controlled by the clock ϕ**2**.

The input and output voltages of the adjusted circuit **11** are denoted by Vi and Vo, respectively. When the clock ϕ**1** is high, the both ends of a integrating capacitor C**2** are grounded to be reset and a sampling capacitor C**1** is simultaneously charged with the input voltage Vi. The electric charge Q**1** charged on the sampling capacitor C**1** is C**1**×Vi. Thus, when the clock ϕ**2** goes high, the electric charge Q**1** is transferred to the integrating capacitor C**2** and if a sufficient settling time is given, the electric charge Q**2** and if a sufficient settling time is given, the electric charge Q**2** of the integrating capacitor C**2** becomes C**2**×Vo. Since Q**1**=Q**2**, a relation to Vo=(C**1**/C**2**)Vi holds.

When the adjusted circuit **11** is operated with a high speed clock signal, unless the adjusted circuit **11** has a sufficient drive ability for the load capacitance CL, the slew rate is insufficient and Vo<(C**1**/C**2**)Vi, whereby a necessary output amplitude will not be obtained.

In design, the bias current IB to be provided to the operational amplifier **13**X is determined such that a necessary slew rate can be obtained under the worst conditions of a power supply voltage, temperature and a deviation in circuit element characteristics occurring in fabrication process. Besides, there are taken into consideration a variation in drive ability of the operational amplifier **13**X in company with a variation in the bias current IB and a variation in the capacitance CL.

In ordinary case, however, the worst conditions does not occur, thereby resulting in excessive power consumption.

FIG. **12** shows the output voltages Vo, with respect to time between t**1** and t**3** of FIG. **11**, of adjusted circuits **11** under different conditions fabricated on the basis of the same design. In FIG. **12**, VLL denotes the lowest limit value of a necessary output voltage Vo for ensuring a normal operation of the adjusted circuits **11** under the worst conditions.

Referring back to FIG. **9**, in order to solve the problem of excessive power consumption, a configuration was adopted in the prior art in which a bias circuit **12** capable of adjusting the bias current IB is incorporated in the semiconductor integrated circuit **10**X, a bias current IB having the same value as the bias current IB provided to the adjusted circuit **11** is taken out from the bias circuit **12** to the outside and measured with an ammeter **14**, and such a trimming adjustment is performed that the bias current IB is adjusted by an adjustment circuit **15**X to make the bias current IB within a given range. This adjustment is performed in the final stage of a fabrication process of the semiconductor integrated circuit **10**X.

However, since characteristic variations in load impedance and a variation in load impedance caused by variations in power supply voltage and temperature are not taken into consideration, the bias current BI has to be determined assuming that the load impedance has the maximum value, leading to insufficient reduction in power consumption. Further, since adjustment operation for the bias current IB is necessary in fabrication process of the semiconductor integrated circuit **10**X, the cost increases.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a semiconductor integrated circuit capable of achieving more of power consumption of a circuit, whose slew rate is dependent on a bias current, without adjusting the bias current thereof prior to product shipment.

In one aspect of the present invention, there is provided a semiconductor integrated circuit comprising: a replica circuit of an adjusted circuit whose slew rate is dependent on a bias current; and a bias current automatic adjustment circuit; wherein the replica circuit is repeatedly operated for adjustment. This automatic adjustment circuit comprises: an evaluation circuit; a comparator circuit; and a bias adjustment circuit.

In the evaluation circuit, processing is repeated, wherein the processing includes: resetting an output thereof; obtaining a difference between first and second values of an output of the replica circuit given times, the first and second value being responsive ones at respective times when first and second time intervals has elapsed after a given value having been step-inputted to the replica circuit; and successively summing the differences. In the comparator circuit, a value obtained by the successively summing is compared with a reference value. The bias adjustment circuit changes the bias current of the replica circuit and the adjusted circuit according to a comparison result of the comparator circuit at every given times.

According to this semiconductor integrated circuit, since even if there are variations in bias current and output load of adjusted circuit due to variations in fabrication process, power supply and environmental temperature, the bias current is automatically and properly adjusted coping with the variations, and low power consumption can be realized. Further, a parasitic capacitance of circuit elements of the automatic adjustment circuit exerts no adverse influence on

a main signal system including the adjusted circuit, and in addition automatic adjustment of the bias current of the adjusted circuit can be performed without ceasing operation of the main signal system in parallel thereto. Still further, there is no need to perform bias current adjustment operation at the final stage of fabrication of the semiconductor integrated circuit, thereby enabling reduction in cost thereof.

Other aspects, objects, and the advantages of the present invention will become apparent from the following detailed description taken in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a semiconductor integrated circuit including an adjusted circuit whose slew rate is dependent on a bias current and a bias current automatic adjustment circuit, of one embodiment according to the present invention;

FIG. **2** is a block diagram showing a structural example of part of FIG. **1**;

FIG. **3** is a flow chart showing a control sequence of the control circuit of FIG. **1**;

FIGS. **4**(A) to **4**(C) are diagrams each showing a waveform of an output voltage Vo and on/off waveforms of switches P**2**A and P**2**B of FIG. **1**;

FIGS. **5**(A) to **5**(C) are graphs showing changes over time in output value of the bias current adjustment circuit when automatically adjusting a bias current by step-up, step-down and dichotomizing search methods, respectively;

FIG. **6** is a diagram showing a structural example of the replica circuit of FIG. **1**;

FIG. **7** is a diagram showing a structural example of the subtraction/integration circuit of FIG. **1**;

FIG. **8** is a timing chart showing a reference clock CLK, control signals provided to the switches of FIGS. **6** and **7** and a judgment cycle signal JCS of FIG. **2**;

FIG. **9** is an illustration of bias adjustment to a prior art semiconductor integrated circuit including an adjusted circuit whose slew rate is dependent on a bias current;

FIG. **10** is a diagram showing a sample and hold circuit as an adjusted circuit of FIG. **9**, which is a combination of a switched capacitor circuit and an operational amplifier;

FIG. **11** are waveform diagrams showing operation of the circuit of FIG. **10**; and

FIG. **12** is a waveform diagram of output voltages Vo, with respect to time between t**1** and t**3** of FIG. **11**, of adjusted circuits under different conditions fabricated on the basis of the same design.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the drawings, wherein like reference characters designate like or corresponding parts throughout several views, preferred embodiments of the present invention are described below.

First Embodiment

FIG. **1** is a block diagram of a semiconductor integrated circuit **10** including an adjusted circuit **11** whose slew rate is depending on a bias current and a bias current automatic adjustment circuit.

The output of the adjusted circuit **11** is connected to another circuit not shown or an output terminal of the semiconductor integrated circuit **10**, and a load impedance measured at the output of the adjusted circuit **11** is Z_L. In the semiconductor integrated circuit **10**, there is formed a replica circuit **11**R which is substantially the same as the adjusted circuit **11**. In order to increase the degree of the sameness as the adjusted circuit **11**, the replica circuit **11**R is formed in the proximity of the adjusted circuit **11**. Bias current with the same value flow through the adjusted circuit **11** and the replica circuit **11**R, respectively, and their current value can be adjusted by a bias current adjustment circuit **15**. An evaluation circuit **16** connected to the output of the replica circuit **11**R is designated such that a load impedance measured at the output of the replica circuit **11**R is almost equal to that of the adjusted circuit **11**.

The evaluation circuit **16** is provided with a subtraction/integration circuit **17** and a control circuit **18**, and the subtraction/integration circuit **17** is provided with switches P**2**A and P**2**B and an integration circuit **19**.

The switch P**2**A is connected between the output of the replica circuit **11**R and the inverting input of the integration circuit **10**, and the switch P**2**B is connected between the output of the replica circuit **11**R and the non-inverting input of the integration circuit **19**. The integration circuit **19** has the inverting input and non-inverting input, and successively sums up values each proportional to a difference between a signal provided to the non-inverting input and a signal provided to the inverting input to output the sum as a difference cumulation voltage VD. The reason for the successive summing is to increase precision of bias current adjustment. That is, an individual difference is extremely small, which makes direct comparative evaluation within an allowable error difficult, and therefore the cumulation of the differences is adopted.

The difference cumulation voltage VD is provided to the inverting input of a comparator **20** and a reference voltage VS is provided to the non-inverting input thereof. An enable signal EN outputted from the comparator **20** is high when VS>VS while being low when VD<VS.

The control circuit **10** provides a timing signal to the replica circuit **11**R and the subtraction/integration circuit **17** to operate the circuits cyclically as will be described later, and if the enable signal EN is high, that is VD>VS, after the subtraction/integration circuit **17** repeats an operation N times, then the control circuit **18** provides a pulse of an adjustment signal AP to a bias current adjustment circuit **15**. The bias current adjustment circuit **15** responds to this pulse and adjusts, by one step, the bias current of the replica circuit **11**R and adjusted circuit **11** in a direction in which the value of the bias current converges to the optimal value.

FIG. **2** is a block diagram showing a structural example of part of FIG. **1**.

In the adjusted circuit **11**, a circuit **21** and FET **22** are connected in series between a power supply potential VDD and ground. A circuit **21**R and an FET **22**R of the replica circuit **11**R correspond to a circuit **21** and an FET **22**, respectively, of the adjusted circuit **11**.

The bias current adjustment circuit **15** is provided with a counter **23** and a D/A converter **24** to which the count of the counter **23** is provided, and the output of the D/A converter **24** is provided to the gates of the FETs **22** and **22**R as a gate voltage VG. Into the FETs **22** and **22**R, a bias current IB according to the value of the gate voltage VG flows. As the gate voltage VG rises, the bias current IB increases with the result of a higher slew rate of the circuits **21** and **21**R.

In the control circuit **18**, a clock CLK is provided through a gate circuit **25** to a timing generation circuit **26**. The timing

generation circuit **26** generates a timing signal for the replica circuit **11**R and the subtraction/integration circuit **17** on the bases of the clock CLK. The timing generation circuit **26** further generates a judgment cycle signal JCS whose pulse cycle is equal to a comparative judgment cycle (a cycle of judging as K=N at the step S**7** of FIG. **3**), and provides it to one input of an AND gate **28**. The enable signal EN is provided to the other input of the AND gate **28**, and while the enable signal EN is high, pulses of the judgment cycle signal JCS are provided through the AND gate **28** to the clock input CK of the counter **23** as an adjustment signal AP. After power is turned on, the gate circuit **25** enters into a through state for the clock CLK and this-state is latched at a flip-flop thereof. When the enable signal EN is low at a rise of a pulse of the judgment cycle signal JCS, then the flip-flop is reset to enter into a cutoff state for the clock CLK, and operation of the control circuit **18** ceases, that is, a bias current automatic adjustment operation has been completed.

FIG. **3** is a flow chart showing a control sequence of the control circuit **18** of FIG. **1**. FIGS. **4**(A) to **4**(C) each show waveforms of the output voltage Vo and on/off waveforms of the switches P**2**A and P**2**B of FIG. **1**. In the following description, characters in parenthesis denotes step identification of FIG. **3**.

(S**1**) The integration circuit **19** is caused to reset, and thereby its output VD becomes 0 V. Further, an internal counter K is caused to load an initial value of 1 and the counter **23** of FIG. **2** is caused to load an initial value.

(S**2**) The replication circuit **11**R is caused to reset, and thereby its output voltage Vo becomes 0 V.

(S**3**) The replica current **11**R is caused to receive an input voltage stepping up to Vi. Thereby, the output voltage Vo rises as shown in FIG. **4**(A) for example.

(S**4**) If the counter K indicates an odd number, then the process goes to step **5**, or else the process goes to step S**6**.

(S5) The switch P**2**B is caused to keep an ON state as shown in FIG. **4**(A) till a time t**1** elapses after the input voltage of the replica circuit **11**R being stepped up to Vi, and the integration circuit **19** is caused to add a value Vo**1** of the output voltage Vo to the VD when the switch P**2**B transits from ON to OFF. Thereafter, the process goes to step S**7**.

(S**6**) The switch P**2**A is caused to keep an ON state as shown in FIG. **4**(A) till a time t**2** elapses after the input voltage of the replica circuit **11**R being stepped up to Vi, and the integration circuit **19** is caused to subtract a value Vo**2** of the output voltage Vo from the VD when the switch P**2**A transits from ON to OFF.

(S**7**) If N>K, then the process goes to step S**8**, and if N=K, then the process goes to step **9**.

(S**8**) The value of the counter K is incremented by 1, and the process returns to step S**2**.

Each time the processing of steps S**1** to S**8** has been repeated twice, ΔV=Vo**1**−Vo**2** is added to VD. In general, a value proportional to a voltage difference ΔV is added to VD.

(S**9**) The judgment cycle signal JCS of FIG. **2** rises, and at this time if the enable signal EN is high ('H'), that is, VD>VS, then the process goes to step S**10**, or else the clock CLK is not provided to the timing generation circuit **26** in FIG. **2** to cease operation of the control circuit **18**. In the latter case, no pulse of the adjustment signal AP is provided to the counter **23** to fix the output of the counter **23**, and therefore both the gate voltage VG and the bias current IB are also fixed. Thereby, automatic adjustment of the bias current is completed.

(S**10**) in FIG. **2**, a pulse of the judgment cycle signal JCS passes through the AND gate **28** and is provided to the clock input CLK of the counter **23** as a pulse of the adjustment signal AP. Then, the process returns to step Si.

When values of the gate voltage VG corresponding to the waveforms of the output voltage Vo of FIGS. **4**(A) to **4**(C) are denoted by VG**1**, VG**2** and VG**3**, respectively, a relation VG**1**<VG**2**<VG**3** holds. That is, the value of the bias current **1**B is larger in the case of FIG. **4**(B) than in the case of FIG. **4**(B), and the value of the bias current **1**B is larger in the case of FIG. **4**(C) than in the case of FIG. **4**(B). As the value of the bias current **1**B is larger, the rise time of the output voltage Vo is shorter and the voltage differences ΔV is smaller, and therefore the value VD obtained by cumulating ΔVo over N times is also smaller. Since power consumption increases with decrease in the value of VD, a proper value of VD at which excessive power consumption can be prevented and the adjusted circuit **11** normally operates is obtained in advance, which is adopted as a reference voltage VS.

The gate voltage VG changes stepwise as shown in FIG. **5**(A) in response to pulses of the adjustment signal AP.

Since according to the present embodiment, the bias current automatic adjustment circuit as described above is provided to the adjusted circuit **11** in the semiconductor integrated circuit **10**, the bias current of the adjusted circuit **11** is properly and automatically adjusted in response to variations in the bias current and the output load of the adjusted circuit **11** occurring by variations in fabrication process, power supply voltage and environmental temperature, which enables realization of low power consumption. Furthermore, since no necessity arises of bias current adjustment at the final stage of fabrication process of the semiconductor integrated circuit **10**, it is possible to reduce cost. Moreover, since the replica circuit **11**R is provided corresponding to the adjusted circuit **11** and automatic adjustment is performed using the output thereof, the parasitic capacitance of circuit elements of the automatic adjustment circuit exerts no adverse influence on a main signal system, and in addition automatic adjustment of the bias current of the adjusted circuit **11** can be performed without ceasing operation of the main signal system in parallel thereto.

Note that other methods may be adopted in order to converge the bias current **1**B. For example, the counter **23** may be replaced with a down counter, and the reference voltage VS and the difference cumulation voltage VD are provided to the non-inverting input and inverting input, respectively, of the comparator **20** of FIG. **1**. In this case, the gate voltage VG changes as shown in FIG. **5**(B). Further, the counter **23** and the AND gate **28** of FIG. **2** may not be employed with using a dichotomizing search method in which the gate voltage VG is changed as shown in FIG. **5**(C) depending on the sign of the enable signal EN each time a pulse of the adjustment cycle signal JCS is provided and this processing is repeated till the absolute value of the difference between the difference cumulation voltage VD and the reference voltage VS becomes less than a given value ϵ.

FIG. **6** and **7** respectively show structural examples of the replica circuit **11**R and the subtraction/integration circuit **17** of FIG. **1**. These circuits are of a complementary input/output type. FIG. **8** shows the clock CLK, control signals provided to the circuits of FIGS. **6** and **7** and the judgment cycle signal JCS of FIG. **2**. FIG. **8** shows a case where the value N of FIG. **3** is 4.

The replica circuit **11**R is a sample and hold circuit which is a combination of a switched capacitor circuit and a

complementary input/output operational amplifier **13**, and analogous to the adjusted circuit **11** of FIG. **10**. Switches of FIG. **6** are denoted by the same reference characters as those of the corresponding switches of FIG. **10**. In the circuit of FIG. **6**, there are provided switches P**14** and P**23** which are not provided in the circuit of FIG. **10**.

The switches P**14** are for short-circuiting between the inverting input and the non-inverting output and between the non-inverting input and the inverting output of the operational amplifier **13** to let the complementary input/output of the operational amplifier **13** be of the same potential, for example, 1.4 V, and the offset thereof be 0 V when resetting the replica circuit **11**R. The switches P**22** and P**23** are for separating the inputs and outputs of the operational amplifier **13** from integrating capacitors C**21** and C**22** to enable to reset the integrating capacitors C**21** and C**22** to the ground potential with switches P**12** and P**13** being on, which is different from the same input and output potential of the operational amplifier **13** when resetting the replica circuit **11**R.

The switches P**11** to P**14** are subjected to on/off control by a clock ϕ**1** of FIG. **8** obtained by dividing the frequency of the clock CLK by 4, and these switches are turned on when the clock ϕ**1** is high. The switches P**21** and P**23** are subjected to on/off control by a clock ϕ**2** in opposite phase from the clock ϕ**1**, and these switches are turned on when the clock ϕ**2** is high. Sampling capacitors C**11** and C**12** are of the same capacitance and correspond to the sampling capacitor C**1** of FIG. **10**. The integrating capacitors C**21** and C**22** are of the same capacitance and correspond to the integrating capacitor C**2** of FIG. **10**.

To the replica circuit **1**R, for example, Vip=16 V and Vim=1.2 V as complementary input signals are provided.

Since operation of the circuit of FIG. **6** can be understood with ease from operation of FIG. **10** described above, description thereof is omitted.

The subtraction/integration circuit **17** of FIG. **7** is analogous to the replica circuit **11**R of FIG. **6**. A complementary input/output operational amplifier **30**, a polarity changeover circuit **31**, switches P**15**, sampling capacitors CL**1**, CL**2**, integrating capacitors C**31** and C**32**, and a polarity changeover circuit **32** correspond to the operational amplifier **30**, the switches P**11** and P**21**, the capacitors C**11**, C**12**, C**21** and C**22**, and the switches P**22**, respectively, of FIG. **6**. The polarity changeover circuit **31** in which the switches P**2**A and P**2**B are connected in parallel and cross connection enables addition/subtraction on electric charges. The sampling capacitors CL**1** and CL**2** or the sampling capacitors CL**2** and CL**1** are charged with the output voltages Vop and Vom, respectively, in a state where the switch P**23** is on and the switches P**15** and P**16** is off, and next the electric charges are transferred to the integrating capacitors C**31** and C**32**, whereby addition or subtraction are performed on cumulated electric charges on the integrating capacitors C**31** and C**32**.

Capacitances of the sampling capacitors CL**1** and CL**2** are determined such that a load impedance measured at the output of the circuit of FIG. **6** is almost equal to the load impedance ZL of FIG. **1**.

The electric charges of the sampling capacitors CL**1** and CL**2** are transferred to the integrating capacitors C**31** and C**32** by turning off the switch P**23** and turning on the switches P**15** and P**16** in a state where the polarity changeover circuits **32** and **33** are in parallel or cross connection.

The polarity changeover circuits **32** and **33** are for canceling offset voltages with each other. That is, a polarity of an offset voltage added to the integrating capacitors C**31** and C**32** when electric charges on the sampling capacitors CL**1** and CL**2** are transferred to the respective integrating capacitors C**31** and C**32** with the polarity changeover circuits **32** and **32** in parallel connection is opposite from a polarity of an offset voltage added to the integrating capacitors C**31** and C**32** when electric charges on the sampling capacitors CL**1** and CL**2** are transferred to the respective integrating capacitors C**31** and C**32** with the polarity changeover circuits **32** and **33** in cross connection, and therefore the offset voltages are canceled with each other.

Reset switches RSW**1** and RSW**2** are for resetting electric charges on the integrating capacitors C**31** and C**32**.

The switches P**2**A and P**2**B are controlled by the respective clocks ϕ**2**A and ϕ**2**B of FIG. **8**. The switches P**15** and P**16** are controlled by the clock ϕ**1** of FIG. **8** together with the switches P**11** to P**14** of FIG. **6**. The switch P**23** are controlled by the clock ϕ**2** of FIG. **8** together with the switches P**21** to P**23** of FIG. **6**. Switches P**31** and P**32** are controlled by a clock ϕ**3** of FIG. **8**. Switches P**41** and P**42** are controlled by a clock ϕ**4** of FIG. **8**. The reset switches RSW**1** and RSW**2** are controlled by a clock ϕRST of FIG. **8**. A high and a low of switch control clocks of FIG. **8** correspond to On and OFF, respectively, of the switches controlled by the corresponding clocks.

The voltage difference between the complementary output voltages VDp and VDm corresponds to the difference cumulation voltage V of FIG. **1**, and is compared with the reference voltage VS as the comparator **20** (FIG. **1**).

Next, description will be given of operation of the circuit of FIG. **7** with reference to FIG. **8**.

(t**1** to t**2**) The reset switches RSW**1** and RSW**2** are on and the subtraction/integration circuit **17** is reset, that is, electric charges on the integrating capacitors C**31** and C**32** are reset.

(t**2** to t**9**) The reset switches RSW**1** and RSW**2** are off. In a time interval between t**2** and t**7**, the switches P**41** and P**42** are on and the switches P**31** and P**32** are off, while in the next time interval between t**7** and t**9**, the conversion arises.

Details in the time interval between t**2** and t**7** are as follows:

(t**3** to t**4**) The switches P**2**A are on, the switches P**2**B are off, the switches P**15** and P**16** are off, and the switches P**23** are on, and thereby the sampling capacitors CL**1** and CL**2** are charged with the respective output voltages Vop and Vom. At t**4**, the switches P**2**A are turned off, and the output voltages Vop and Vom at this time are held on the sampling capacitors CL**1** and CL**2**.

(t**5** to t**6**) The switches P**23** are off, the switches P**15** and P**16** are on, and thereby electric charges on the sampling capacitors CL**1** and CL**2** are transferred to the respective integrating capacitors C**31** and C**32**.

(t**6** to t**7**) The switches P**2**A are off, the switch P**2**B are on, the switches P**15** and P**16** are off, the switches P**23** are on, and thereby the sampling capacitors CL**1** and CL**2** are charged with the respective output voltages Vom and Vop. At t**7**, the switches P**2**B are turned off, and the output voltages Vom and Vop at this time are held on the respective sampling capacitors CL**1** and CL**2**.

Details in a time interval between t**7** and t**10** are as follows:

(t**7** to t**8**) The switches P**23** are off, the switches P**15** and P**16** are on, and thereby electric charges on the sampling capacitors CL**1** and CL**2** are transferred to the respective integrating capacitors C**31** and C**32**.

In a time interval from t**8** to **10**, operations similar to those in the time form t**3** to t**8** are performed. Immediately prior

to resetting of the integrating capacitors C**31** and C**32** at t**10**, a pulse of the judgment cycle signal JCS is outputted from the timing generation circuit **26** of FIG. **2**.

By such operation, the operation described with reference to FIG. **1** are performed.

Although a preferred embodiments of the present invention has been described , it is to be understood that the invention is not limited thereto and that various changes and modifications may be made without departing from the spirit and scope of the invention.

For example, bias current automatic adjustment may be performed not only when power is turned on, but also at every predetermined intervals, when the system is reset, or when temperature or a power supply voltage falls outside a given range. Further, the adjusted circuit **11** may be any one as far as the slew rate thereof is dependent on its bias current.

What is claimed is:

1. A semiconductor integrated circuit comprising:

an adjusted circuit in which a first bias current flows, a slew rate of said adjusted circuit being dependent on said first bias current;

a replica circuit of said adjusted circuit in which a second bias current flows, a value of said second bias current being substantially equal to that of said first bias current;

an evaluation circuit configured to repeat a cycle of processing, said cycle of processing including:

resetting an output thereof;

obtaining a difference between first and second voltages at given times, said first voltage being one at an output of said replica circuit at a time when a first time interval has elapsed after a given voltage having been step-inputted to said replica circuit, said second value being one at said output of said replica circuit at a time when second time interval has elapsed after a voltage equal to said given voltage having been step-inputted to said replica circuit, said second time interval being different from said first time interval; and

successively summing said differences;

a comparator circuit for comparing a value obtained by said successively summing with a reference value; and

a bias adjustment circuit for changing said second bias current according to a comparison result of said comparator circuit at every said given times.

2. The semiconductor integrated circuit of claim **1**, wherein said evaluation circuit comprises:

a subtraction/integration circuit integrating, as said successively summing, each difference between said first voltage and said second voltage; and

a control circuit;

wherein said control circuit is configured to repeat the steps of:

(1) resetting said subtraction/integration circuit;

(2) repeating part of said cycle of processing at said given times, said part of said cycle of processing including:

resetting said replica circuit;

next step-inputting said given voltage to said replica circuit;

next providing said first voltage to said subtraction/integration circuit after or till said first time interval has elapsed from said step-inputting;

next resetting said replica circuit;

next step-inputting said voltage equal to said given voltage to said replica circuit; and

next providing said second voltage to said subtraction/integration circuit after or till said second time interval has elapsed from said previous step-inputting.

3. The semiconductor integrated circuit of claim **2**,

wherein said bias adjustment circuit is configured to step up said second bias current in response to judgment that a value obtained by said successively summing is larger than said reference value by said comparator circuit,

wherein said control circuit is configured to cease operation **[**of said bias adjustment circuit**]** *thereof* in response to judgment that said value obtained by said successively summing is smaller than said reference value.

4. **[**The semiconductor integrated circuit of claim **3**, wherein said replica circuit has an inverting output and a non-inverting output, wherein said subtraction/integration circuit comprises:

an operation amplifier circuit having an inverting input, a non-inverting input, an inverting output and a non-inverting output;

a first integrating capacitor connected between said inverting input and non-inverting output of said operational amplifier circuit;

a second integrating capacitor connected between said non-inverting input and inverting output of said operational amplifier circuit;

a reset switching circuit for resulting electric charges on said first and second integrating capacitors;

first and second sampling capacitors; and

a switching circuit for selectively charging said first and second sampling capacitors or said second and first sampling capacitors by said inverting output and non-inverting output, respectively, of said replica circuit, and thereafter transferring electric charges on said first and second sampling capacitors to said first and second integrating capacitors, respectively**]** *The semiconductor integrated circuit of claim 2,*

wherein said bias adjustment circuit is configured to step down said second bias current in response to judgment that a value obtained by said successively summing is smaller than said reference value by said comparator circuit, and

wherein said control circuit is configured to cease operation thereof in response to judgment that said value obtained by said successively summing is larger than said reference value.

5. **[**The semiconductor integrated circuit of claim **4**, wherein said subtraction/integration circuit further comprising:

a first polarity changeover circuit for connecting first ends of said first and second integrating capacitors to respective said inverting and non-inverting inputs of said operational amplifier circuit to change into a parallel connection state, or connecting said first ends of said first and second integrating capacitors to respective said non-inverting and inverting inputs of said operational amplifier circuit to change into a cross connection state, selectively; and

a second polarity changeover circuit for connecting second ends of said first and second integrating capacitors to respective said non-inverting and inverting outputs of said operational amplifier circuit to change into a parallel connection state, or connecting aid second ends of said first and second integrating capacitors to respective said inverting and non-inverting inputs of said

operational amplifier circuit to change into a cross connection state, selectively] *The semiconductor integrated circuit of claim 2,*

wherein said bias adjustment circuit is configured to step down said second bias current in response to judgment that a value obtained by said successively summing is smaller than said reference value by said comparator circuit, and step up said second bias current in response to judgment that said value obtained by said successively summing is larger than said reference value by said comparator circuit,

wherein said control circuit is configured to cease operation thereof in a case where an absolute value of a difference between said value obtained by said successively summing and said reference value is smaller than a given value.

6. [The semiconductor integrated circuit of claim **5**, wherein said control circuit alternately repeats a first period for causing both said first and second polarity changeover circuits to be in said parallel connection state and a second period for causing both said first and second polarity changeover circuits to be in said cross connection state, and performs said processing in said step (2) once in each of said first and second periods.] *The semiconductor integrated circuit of claim 3,*

wherein said replica circuit has an inverting output and a non-inverting output,

wherein said subtraction/integration circuit comprises:

an operational amplifier circuit having an inverting input, a non-inverting input, an inverting output and a non-inverting output;

a first integrating capacitor connected between said inverting input and non-inverting output of said operational amplifier circuit;

a second integrating capacitor connected between said non-inverting input and inverting output of said operational amplifier circuit;

a reset switching circuit for resetting electric charges on said first and second integrating capacitors;

first and second sampling capacitors; and

a switching circuit for selectively charging said first and second sampling capacitors or said second and first sampling capacitors by said inverting output and non-inverting output, respectively, of said replica circuit, and thereafter transferring electric charges on said first and second sampling capacitors to said first and second integrating capacitors, respectively.

7. The semiconductor integrated circuit of claim **6**, wherein said [adjusted circuit comprises an operational amplifier circuit,] *subtraction/integration circuit further comprises:*

a first polarity changeover circuit for connecting first ends of said first and second integrating capacitors to respective said inverting and non-inverting inputs of said operational amplifier circuit to change into a parallel connection state, or connecting said first ends of said first and second integrating capacitors to respective said non-inverting and inverting inputs of said operational amplifier circuit to change into a cross connection state, selectively; and

a second polarity changeover circuit for connecting second ends of said first and second integrating capacitors to respective said non-inverting and inverting outputs of said operational amplifier circuit to change into a parallel connection state, or connecting aid second ends of said first and second integrating capacitors to respective said inverting and non-inverting inputs of said operational amplifier circuit to change into a cross connection state, selectively.

8. The semiconductor integrated circuit of claim [**1**, wherein said adjusted circuit comprises an operational amplifier circuit.] *7, wherein said control circuit alternately repeats a first period for causing both said first and second polarity changeover circuits to be in said parallel connection state and a second period for causing both said first and second polarity changeover circuits to be in said cross connection state, and performs said processing in said step (2) once in each of said first and second periods.*

9. The semiconductor integrated circuit of claim [**8**, wherein said adjusted circuit further comprises a switched capacitor circuit connected to an input stage of said operational amplifier circuit.] *1, wherein said adjusted circuit comprises an operational amplifier circuit.*

10. The semiconductor integrated circuit of claim **2**, [wherein said bias adjustment circuit is configured to step down said second bias current in response to judgment that a value obtained by said successively summing is smaller than said reference by said comparator circuit, and

wherein said control circuit is configured to cease operation of said bias adjustment circuit in response to judgment that said value obtained by said successively summing is larger than said reference value.] *wherein said adjusted circuit comprises an operational amplifier circuit.*

11. The semiconductor integrated circuit of claim [**10**] *3*, wherein said adjusted circuit comprises an operational amplifier circuit.

12. The semiconductor integrated circuit of claim [**11**, wherein said adjusted circuit further comprises a switched capacitor circuit connected to an input stage of said operational amplifier circuit] *4, wherein said adjusted circuit comprises an operational amplifier circuit.*

13. The semiconductor integrated circuit of claim [**2**, wherein said bias adjustment circuit is configured to step down said second bias current in response to judgment that a value obtained by said successively summing is smaller than said reference value by said comparator circuit, and step up said second bias circuit in response to judgment that said value obtained by said successively summing is larger than said reference value by said comparator circuit,

wherein said control circuit is configured to cease operation of said bias adjustment circuit in a case where an absolute value of a difference between said value obtained by said successively summing and said reference value is smaller than a given value.] *5, wherein said adjusted circuit comprises an operational amplifier circuit.*

14. The semiconductor integrated circuit of claim [**13**] *6*, wherein said adjusted circuit comprises an operational amplifier circuit.

15. The semiconductor integrated circuit of claim [**2**] *7*, wherein said adjusted circuit comprises an operational amplifier circuit.

16. The semiconductor integrated circuit of claim [**15**, wherein said adjusted circuit further comprises a switched capacitor circuit connected to an input stage of said operational amplifier circuit.] *8, wherein said adjusted circuit comprises an operational amplifier circuit.*

17. The semiconductor integrated circuit of claim [**3**, wherein said adjusted circuit comprises an operational amplifier circuit.] *9, wherein said adjusted circuit further comprises a switched capacitor circuit connected to an input stage of said operational amplifier circuit.*

18. The semiconductor integrated circuit of claim **[17]** *10*, wherein said adjusted circuit further comprises a switched capacitor circuit connected to an input stage of said operational amplifier circuit.

19. The semiconductor integrated circuit of claim **[4**, wherein said adjusted circuit comprises an operational amplifier circuit.**]** *11, wherein said adjusted circuit further comprises a switched capacitor circuit connected to an input stage of said operational amplifier circuit.*

20. The semiconductor integrated circuit of claim **[5**, wherein said adjusted circuit comprises an operational amplifier circuit.**]** *12, wherein said adjusted circuit further comprises a switched capacitor circuit connected to an input stage of said operational amplifier circuit.*

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