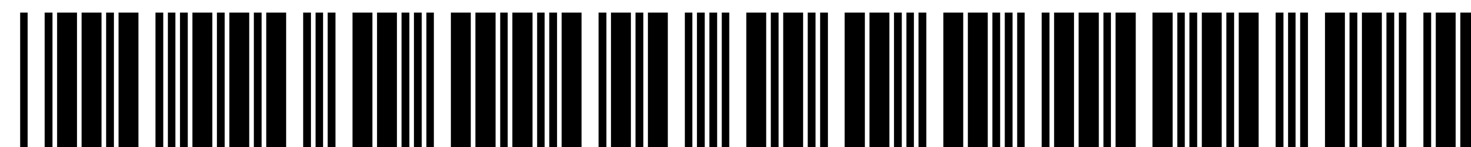

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(12) **Reissued Patent**
Cha

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(54) **PROGRAM CIRCUIT**

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G11C 16/34 (2006.01)

(52) **U.S. Cl.** **365/189.07**; 365/185.22; 365/189.08

(58) **Field of Classification Search** 365/185.09
See application file for complete search history.

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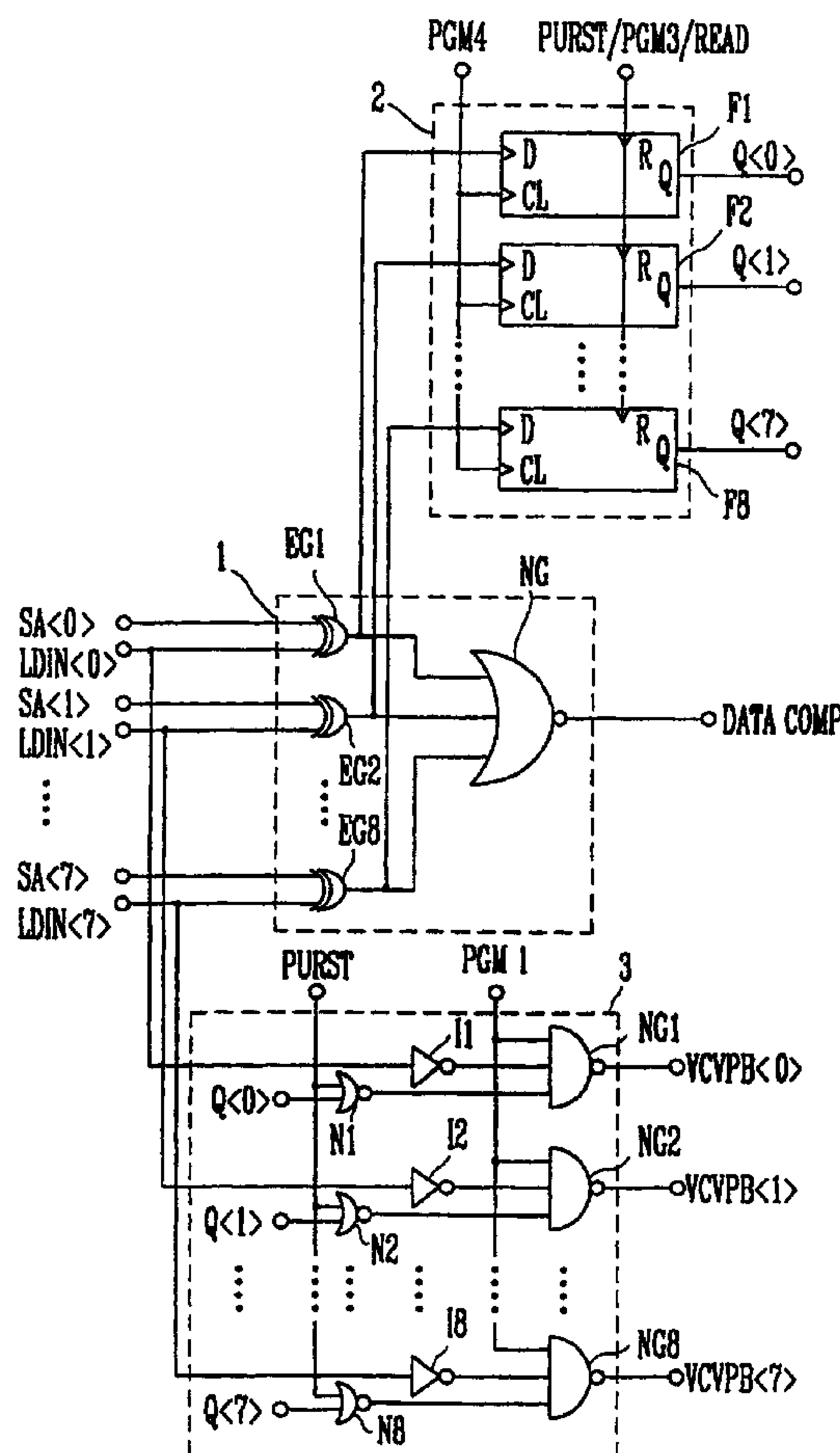
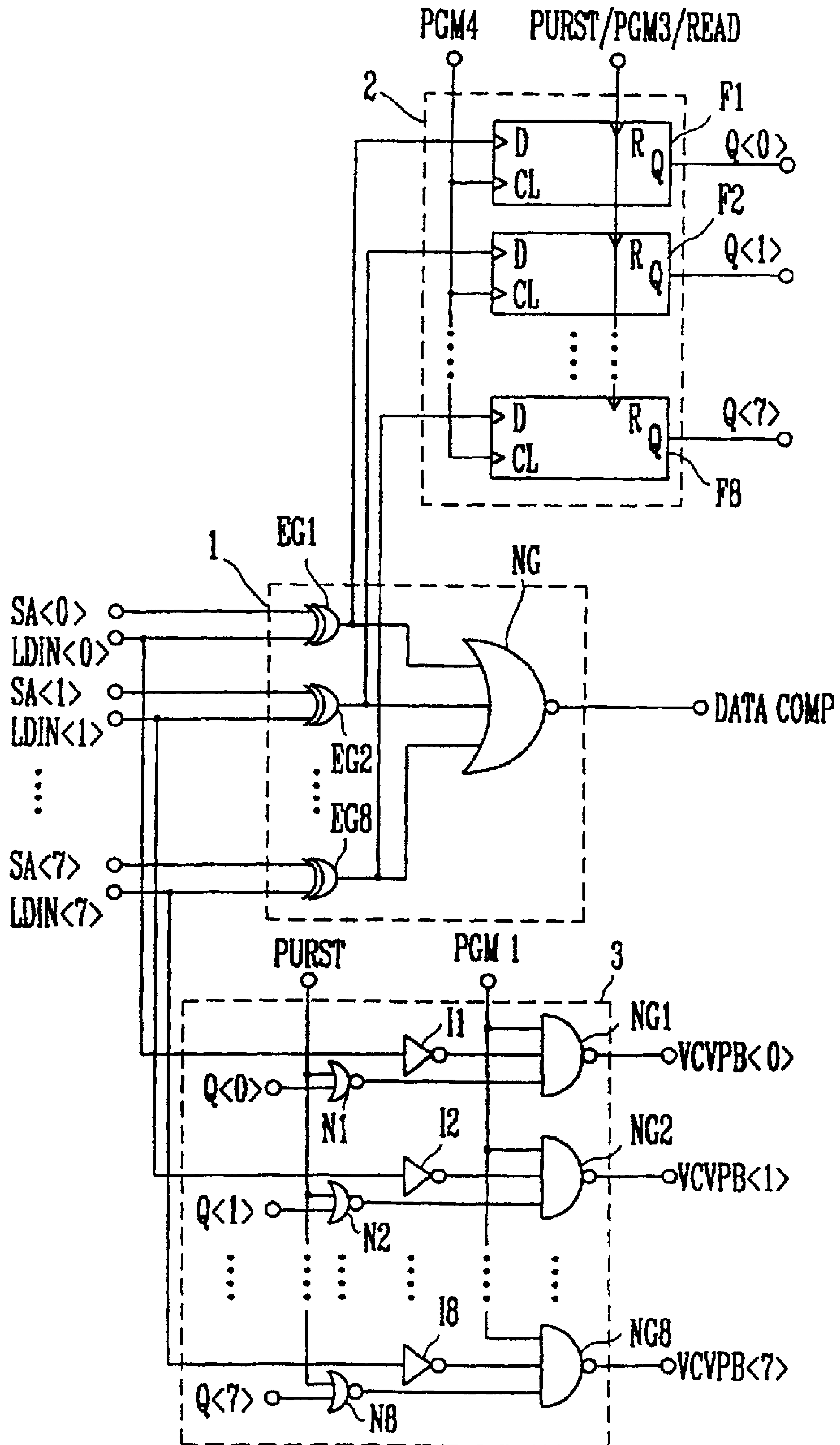
(57) **ABSTRACT**

The program circuit according to the present invention can apply a program voltage to the only memory cells which are not programmed during a re-programming operation, thus, the present invention can be prevent a lowering of reliability of the memory cell due to a continued supply of a program bias voltage.

20 Claims, 1 Drawing Sheet

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F1
D
CL
R
Q
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F2
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F8
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EG1
NG
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I8
NG8
VCVPB<7>
Q<7>
N8

PROGRAM CIRCUIT

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

This application is a Reissue application of U.S. patent application Ser. No. 08/882,835, filed on Jun. 26, 1997, now U.S. Pat. No. 5,930,179.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a program circuit and, more particularly, to a program circuit which can prevent a lowering of reliability occurring during the process of verifying the programmed data.

2. Description of the Prior Arts

Generally, a flash memory device has functions of electrical program and erasure. The flash memory device also performs a verification operation so as to confirm whether the memory cell has been programmed or erased or not after completion of the programming or the erasure operation. At this time, if there are memory cells in which a programming or erasure operation has not completed, re-programming or re-erasure operation is performed again.

In a conventional flash memory device, however, a program bias voltage is applied to a memory cell which is already programmed during a re-programming operation, thus the already programmed memory cell is damaged. This is because the program bias voltage of high voltage is applied to the memory cell, therefore, charge is trapped at the tunnel oxide film of the memory. As a result, reliability of the memory cell is degraded.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a program circuit which can apply a program bias voltage only to the memory cell which is not programmed during a re-programming operation.

To achieve the object described above, a program circuit according to the present invention comprises a comparator for comparing output data of a data input buffer with output data of a sense amplifier bit by bit and for outputting a re-program operation signal if the data are different each other, a data latch circuit for latching the comparing results of the output data of the data input buffer and the output data of the sense amplifier, and a control circuit for generating a high voltage for receiving the output data of the data input buffer and the data latched at the data latch circuit, respectively and for outputting a signal for applying a program bias voltage to a memory cell which has not been programmed in response to a power-up reset signal and program state signal.

The comparator includes a plurality of exclusive gates to which output data of the data input buffer and output data of the sense amplifier, respectively, and a NOR gate for logically combining the output signals of the exclusive NOR gates.

The data latch circuit has a plurality of flip-flops, each flip-flop has a data input terminal to which comparing results of the output data of the data input buffer and the output data of the sense amplifier, a clock signal input terminal to which a program state signal, and a reset signal input signal to which power-up reset signal/program state signal/read mode signals are inputted.

The control circuit for generating a high voltage includes a plurality of NOR gates to which output data of the data latch circuit and a power-up reset signal are inputted, respectively, a plurality of inverters to which output data of the data input buffer is inputted; and a plurality of NAND gates to which the output signals of the NOR gates, the output signals of the inverters and the program state signal are inputted, respectively.

BRIEF DESCRIPTION OF THE DRAWING

Other objects and advantages of the present invention will be understood by reading the detailed explanation of the embodiment with reference to the accompanying drawing in which:

FIGURE is a circuit diagram for explaining a program circuit according to the present invention.

DESCRIPTION OF THE INVENTION

The accompanying drawing is a circuit diagram for explaining a program circuit according to the present invention.

The program circuit according to the present invention is consisted of a comparator **1**, a data latch circuit **2**, and a control circuit for generating a high voltage **3**, and added to the flash memory device.

The comparator **1** comprises of a plurality of exclusive NOR gates EG**1** through EG**8** to which output data LDIN**0** through LDIN**7** of a data input buffer and output data SA**0** through SA**7** of a sense amplifier are inputted, respectively. Also, the comparator **1** comprises a NOR gate NG to which output signals of the exclusive NOR gates EG**1** through EG**8** are inputted. The NOR gate NG outputs logical combination signals via an output terminal DATA COMP.

The data latch circuit **2** is consisted of a plurality of flip-flops F**1** through F**8**. Each of flip-flops F**1** through F**8** comprises a data input terminal D to which an output signal of one of the exclusive NOR gates EG**1** through EG**8**, a clock signal input terminal CL to which a program state signal PGM**4** is inputted, and a reset signal input terminal R to which a power-up reset signal/program state signal/read mode signals PURST/PGM**3**/READ are inputted.

The control circuit for generating a high voltage **3** comprises a plurality of NOR gates N**1** through N**8** to which output data Q**0** through Q**7** of the flip-flops F**1** through F**8** and the power-up reset signal PURST are inputted, respectively, a plurality of inverters I**1** through I**8** to which the output data LDIN**0** through LDIN**7** of data input buffer are inputted, respectively, and a plurality of NAND gates NG**1** through NG**8** to which output signals of the NOR gates N**1** through N**8**, output signals of the inverters I**1** through I**8** and the program state signal PGM**1**, respectively. The plurality of NAND gates NG**1** through NG**2** output signals VCVPB**0** through VCVPB**7**, respectively.

An operation of the program circuit will be now explained below.

For example, in case where a verification operation is performed after data "10011000" of 8 bits inputted through the data input buffer was programmed into the memory cell, the data "10011000" is inputted to the exclusive NOR gates EG**1** through EG**8** via one input terminal, respectively, and the data read from the memory cell, that is, the data SA**0** through SA**7** outputted from the sense amplifier are inputted to the exclusive NOR gates EG**1** through EG**8** via other input terminal, respectively.

At this time, assume that the data SA**0** through SA**7** outputted from the sense amplifier is "11011100". Then,

since data SA1 and SA5 which are the second bit and the sixth bit, respectively, are different *from* each other, the data outputted via the output terminals of the exclusive NOR gates EG1 through EG8 become "10011000". As a result, the output of the NOR gate NG is maintained at a low level, and a re-programming operation is performed. At the same time, the data "101111011" outputted via the output terminals of the exclusive NOR gates EG1 through EG8 is latched to the flip-flops F1 through F8 respectively depending on the input of the program state signal PGM4, and the output signals Q0 through Q7 of the flip-flops F1 through F8 are inputted to the NOR gates N1 through N8, respectively. For reference only, before the data ["101111011"] *"10111011"* is inputted to the data latch circuit 2, the flip-flops F1 through F8 are maintained at the state in which the data of "0" is latched by the input of the power-up reset signal PURST. Thereafter, the data "10011000" outputted from the flip-flops F1 through F8 are inputted to the NOR gates N1 through N8 of the control circuit for generating high voltage 3 respectively, and the output data "1001100" of the data input buffer is inputted to the inverters I1 and I8, respectively.

At this time, signals at a low level are outputted from only the output terminals VCVPB1 and VCVPB5 of the NAND gates NG2 and NG6 by the power-up reset signal PURST inputted with a low level and the program state signal PGM1 inputted with a high level. Therefore, a programming bias voltage is again applied to only the memory cells which are corresponded to the second and the sixth bits, respectively.

As mentioned above, the program circuit according to the present invention can apply a program voltage to only the memory cells which are not programmed during a re-programming operation. Therefore, the present invention can be prevent a lowering of reliability of the memory cell due to a continued supply of a program bias voltage.

The foregoing description, although described in its preferred embodiments with a certain degree of particularity, is only illustrative of the principle of the present invention. It is to be understood that the present invention is not to be limited to the preferred embodiment disclosed and illustrated herein. Accordingly, all expedient variations that may be made within the scope and spirit of the present invention are to be encompassed as further embodiments of the present invention.

What is claimed is:

1. A program circuit comprising:

a comparator for comparing output data of a data input buffer with output data of a sense amplifier bit by bit, and for outputting a re-program operation signal if the data are different from each other;

a data latch circuit for latching the comparing results of the output data of said data input buffer and the output data of said sense amplifier;

a control circuit for generating a high voltage for receiving the output data of said data input buffer and the data latched at said data latch circuit, respectively, and for outputting a signal for applying a program bias voltage to a memory cell which has not been completely programmed in response to a power-up reset signal and program state signal.

2. The program circuit as claimed in claim 1, wherein said comparator includes a plurality of exclusive-NOR gates to which output data of said data input buffer and output data of said sense amplifier, respectively, and a NOR gate for logically combining the output signals of said exclusive-NOR gates.

3. The program circuit as claimed in claim 1, wherein said data latch circuit includes a plurality of flip-flops, each flip-flop having a data input terminal to which comparing results of the output data of said data input buffer and the output data of said sense amplifier, a clock signal input terminal to which a program state signal and a reset signal input signal to which power-up reset signal/program state signal/read mode signals are inputted.

4. The program circuit as claimed in claim 1, wherein said control circuit for generating a high voltage includes a plurality of NOR gates to which output data of said data latch circuit and a power-up reset signal are inputted, respectively; a plurality of inverters to which output data of said data input buffer is inputted; and a plurality of NAND gates to which the output signals of said NOR gates, the output signals of said inverters and the program state signal are inputted, respectively.

5. The program circuit as claimed in claim 1, wherein said comparator includes eight exclusive-NOR gates to compare the output data of said data input buffer and the output data of said sense amplifier.

6. A semiconductor device, comprising:

a plurality of memory cells;

an input component coupled to the memory cells and configured to program the memory cells;

a comparator to determine whether first information of the input component has been properly programmed into the memory cells, the comparator having a logic gate to output a first signal to indicate whether or not a reprogramming operation is needed, wherein the first information is N bits of data;

a controller coupled to the comparator and configured to output a second signal to initiate reprogramming of M number of the memory cells, where M is less than N,

wherein the comparator compares the first information of the input component with second information read from the memory cells,

wherein N is eight and the input component is configured to transmit a byte of information at a time to the memory cells, and

wherein the comparator includes a plurality of XNOR gates having first and second input ports, the first input ports being configured to receive the first information and the second input ports being configured to receive the second information, wherein outputs of the XNOR gates indicate whether the first information and the second information are the same.

7. The device of claim 6, wherein the comparator includes N number of the XNOR gates.

8. The device of claim 6, wherein the comparator further includes:

a logic gate coupled to the outputs of the XNOR gates, the logic gate configured to output the second signal; and

a data latch circuit for latching the compared results of the comparator.

9. The device of claim 6, further comprising:

a sense amplifier coupled to the memory cells, wherein the sense amplifier provides the second information to the second input ports of the XNOR gates.

10. The device of claim 9, further comprising:

a latch configured to receive information relating to the first information of the input component.

11. The device of claim 10, wherein the latch receives the outputs of the XNOR gates.

12. The device of claim 11, wherein the latch includes N number of flip-flops to receive the outputs of the XNOR gates.

13. The device of claim 10, wherein the information received by the latch is the first information of the input component.

14. The device of claim 10, wherein an output of the latch is transmitted to the controller.

15. The device of claim 14, wherein the first information of the input component is transmitted to the controller.

16. The device of claim 15, wherein the first information and the output of the latch are eight bits of data, respectively, where the controller outputs eight signals in response to receipt of the first information and the output of the latch, the eight signals having one or more signals of first type to initiate reprogramming of corresponding one or more memory cells that have not been properly programmed and one or more of signals of second type to disable reprogramming of corresponding one or more memory cells that have been properly programmed.

17. A non-volatile semiconductor device, comprising:

a plurality of memory cells;

a sense amplifier coupled to the memory cells to read information written into the memory cells;

an input data buffer coupled to the memory cells and configured to transmit N bits of information at a time into the memory cells;

a comparator having a plurality of logic gates to compare bit-by-bit first information of the input data buffer with second information of the sense amplifier and output a reprogram operation signal if the first information and the second information are different;

a data latch circuit coupled to outputs of one or more of the logic gates of the comparator; and

a controller having a plurality of logic gates and being configured to receive the first information of the input data buffer and outputs of the data latch circuit, and output a signal for applying a program bias voltage to any memory cell that has not been properly programmed.

18. The non-volatile device of claim 17, wherein the plurality of logic gates of the controller include a first set of logic gates of N numbers corresponding to the N bits of information programmed into the memory cells, the first set of logic gates being configured to output a high voltage signal for any bit of information that has not been properly programmed into the memory cells.

19. The non-volatile device of claim 18, wherein the signal for applying the program bias voltage is a low voltage signal.

20. A non-volatile semiconductor device, comprising:

a plurality of memory cells;

a sense amplifier coupled to the memory cells;

an input data buffer coupled to the memory cells and configured to write N bits of information at a time into the memory cells;

a comparator having N number of XNOR gates corresponding to the N bits of information being written into the memory cells, the comparator being configured to compare bit-by-bit N bits of first information of the input data buffer with N bits of second information of the sense amplifier and output a rewrite operation signal if any bit of the first information and the second information is different from each other;

a data latch circuit coupled to the comparator to receive outputs of the XNOR gates; and

a controller having a plurality of logic gates and being configured to receive the first information of the input data buffer and outputs of the data latch circuit, and configured to output a signal for applying a bias voltage to any memory cell that has not been properly written,

wherein the plurality of logic gates of the controller include a first set of logic gates of N numbers corresponding to the N bits of information written into the memory cells, the first set of logic gates being configured to output a high voltage signal for any bit of information that has not been properly written into the memory cells.

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