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(54) **STACKABLE FLEX CIRCUIT IC PACKAGE AND METHOD OF MAKING SAME**

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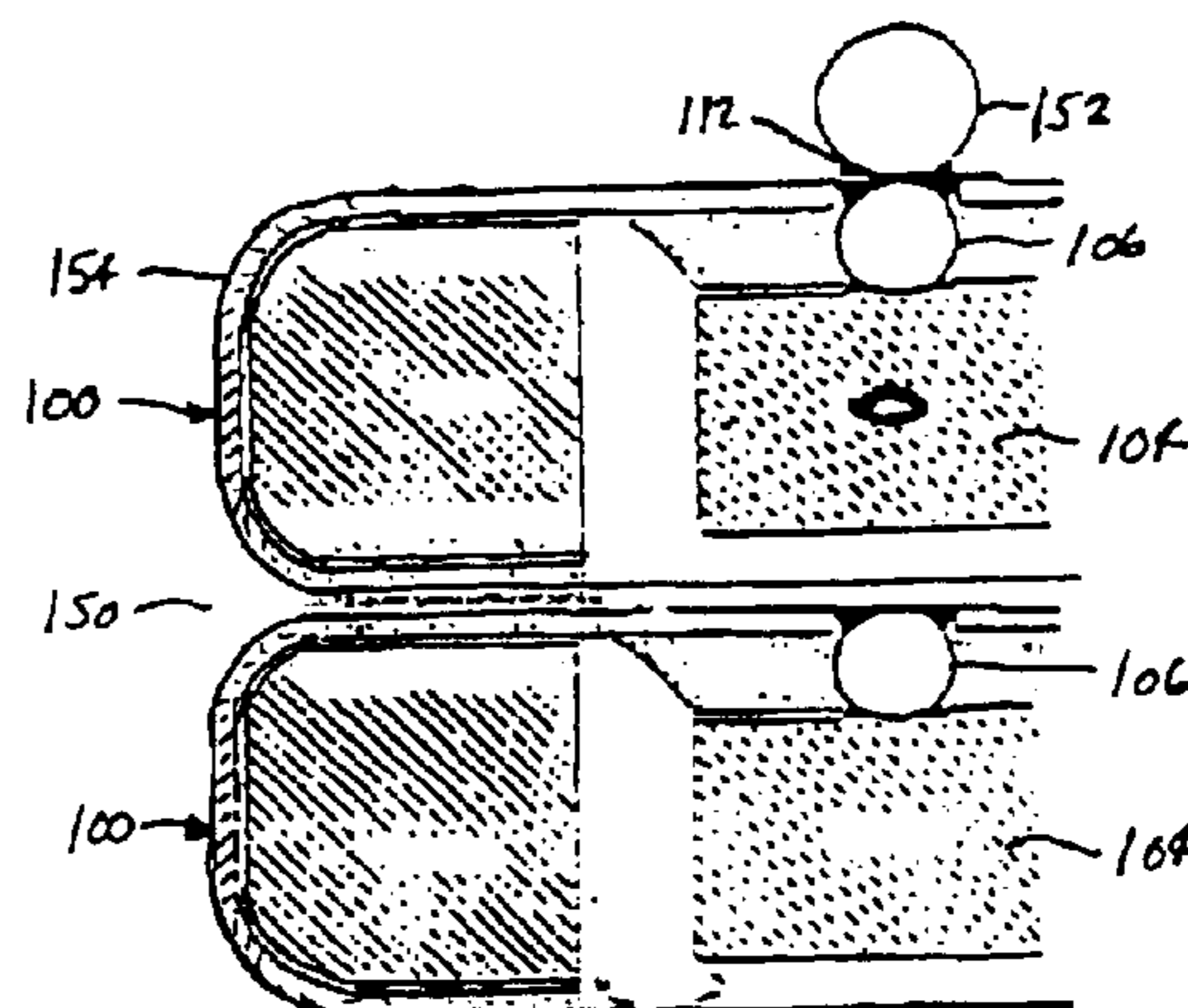
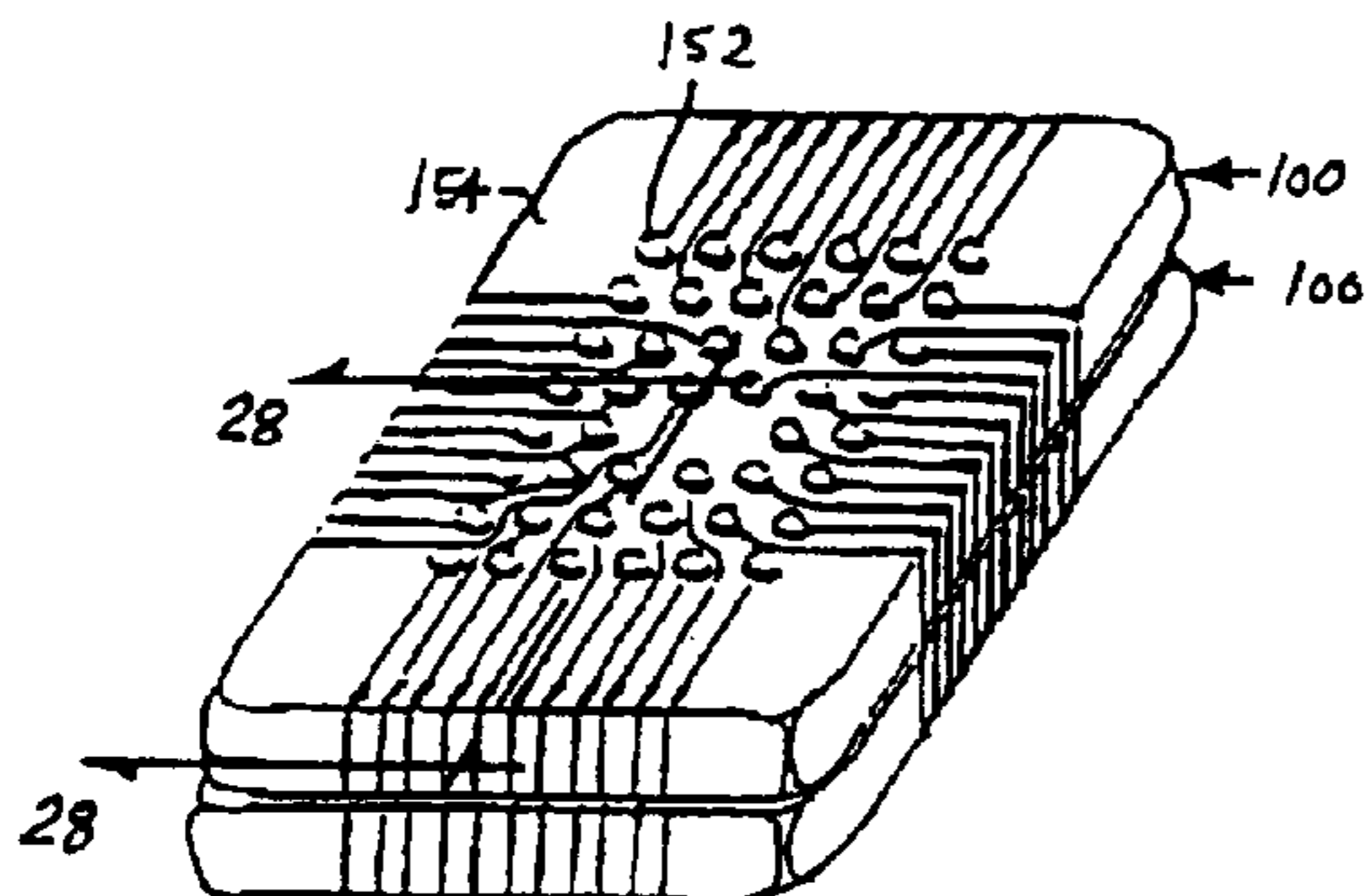
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(57) **ABSTRACT**

A stackable flex circuit IC package includes a flex circuit comprised of a flexible base with a conductive pattern thereon, and wrapped around at least one end portion of a frame so as to expose the conductive pattern at the edge portion. An IC device is mounted within a central aperture in the frame, and is electrically coupled to the conductive pattern. The IC device is sealed in place within the frame with epoxy. A stack of the IC packages is assembled by disposing a conductive epoxy of anisotropic material between the conductive patterns at the edge portions of adjacent IC packages. Application of pressure in a vertical or Z-axis direction between adjacent IC packages completes electrical connections between the individual conductors of the conductive patterns of adjacent IC packages to interconnect the IC packages of the stack, while at the same time maintaining electrical isolation between adjacent conductors within each of the conductive patterns. The IC devices may comprise bare memory chips electrically coupled to the conductive pattern by wire bonds which are encapsulated in the epoxy together with the chip. Alternatively, where the IC devices comprise ball grid array (BGA) devices, such as chip scale packages, μ BGAs, flip chips, or the like, the matrix of balls or other conductive elements on the device are disposed within apertures ablated through the flexible base of the flex circuit where they are soldered to the conductive pattern. A method of making the stackable flex circuit IC package secures the frame onto the flex circuit so that the flex circuit is wrapped around at least one end of the frame, secures the IC device to the flex circuit within the opening in the frame, electrically couples the IC device to the conductive pattern on the flex circuit, either by wire bonding in the case of a bare chip or by soldering the matrix of balls or other conductive elements to the conductive pattern of the flex circuit in the case of a BGA device, and then encapsulates the device with epoxy. A stack of the IC packages is formed by placing anisotropic conductive epoxy between the exposed conductive patterns of adjacent IC packages and pressing the IC packages together.

20 Claims, 7 Drawing Sheets



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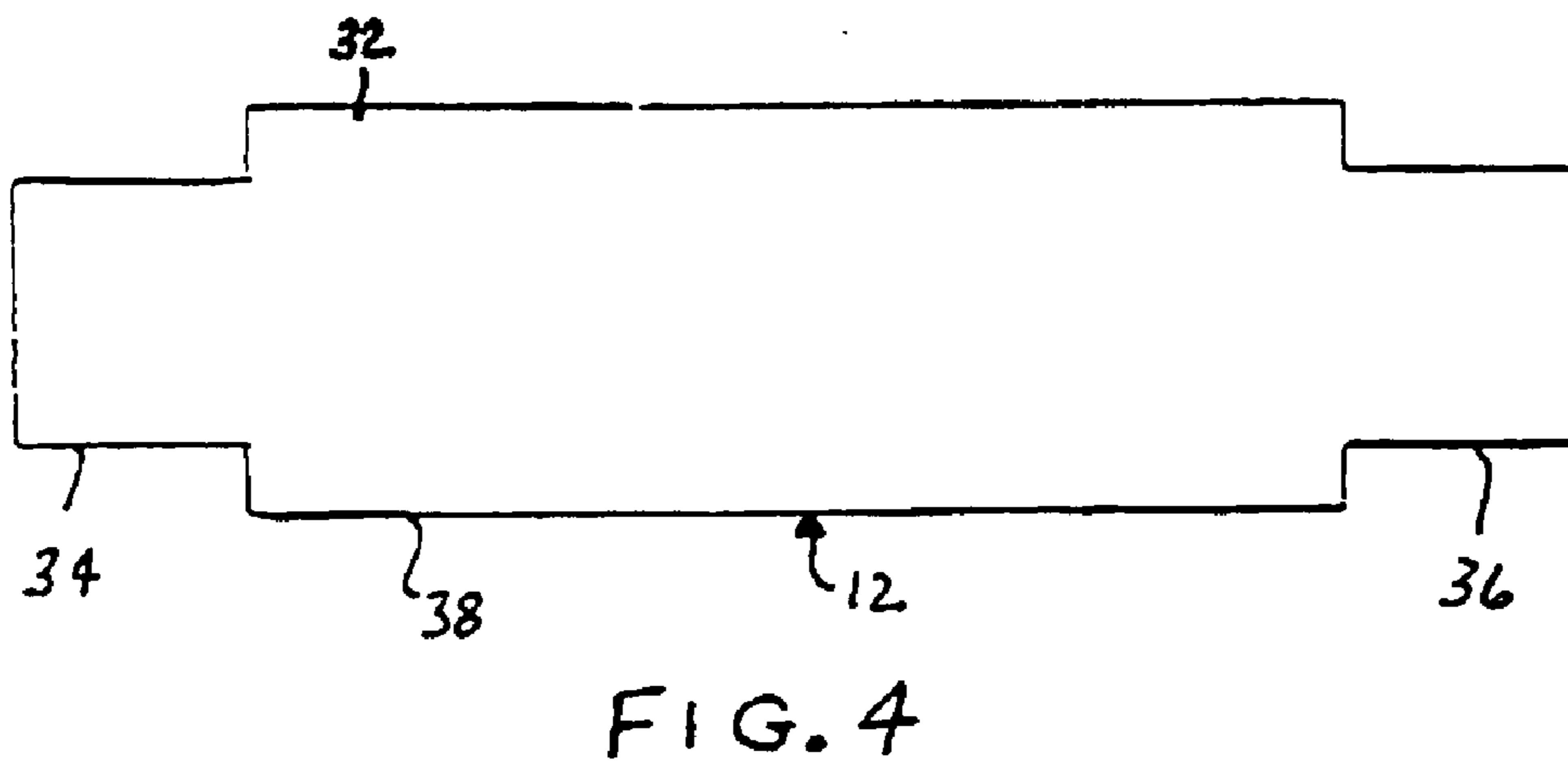
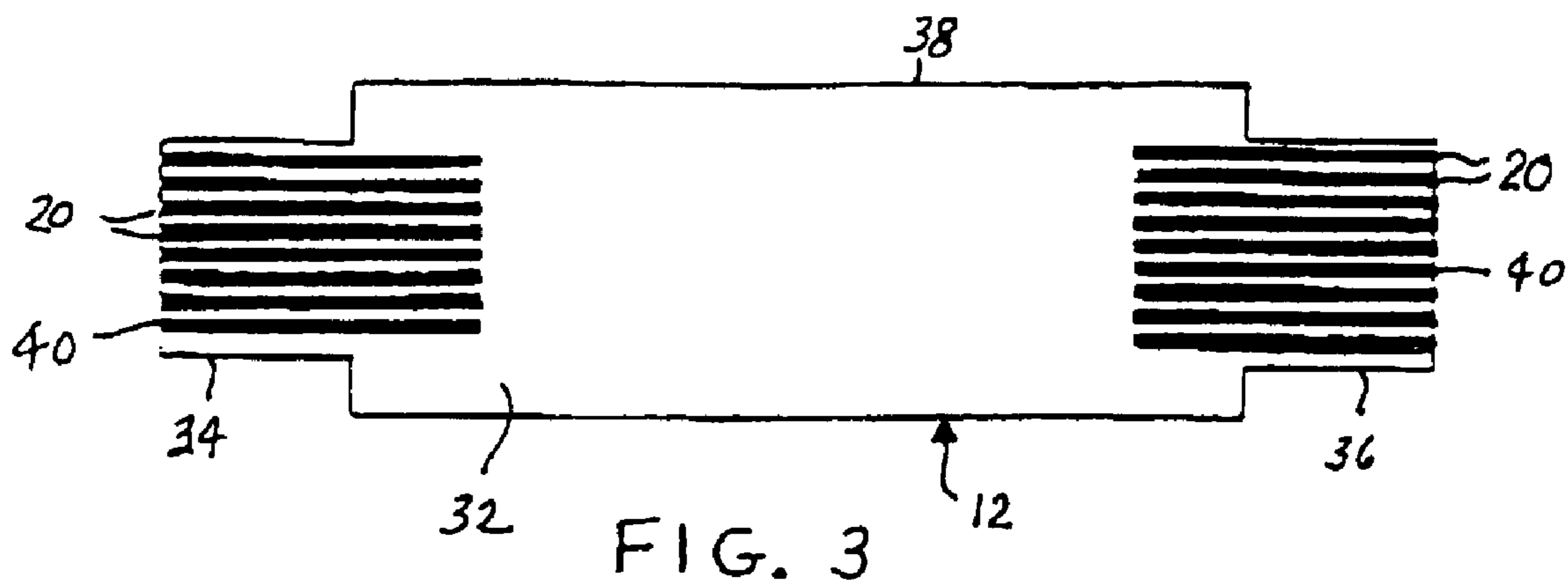
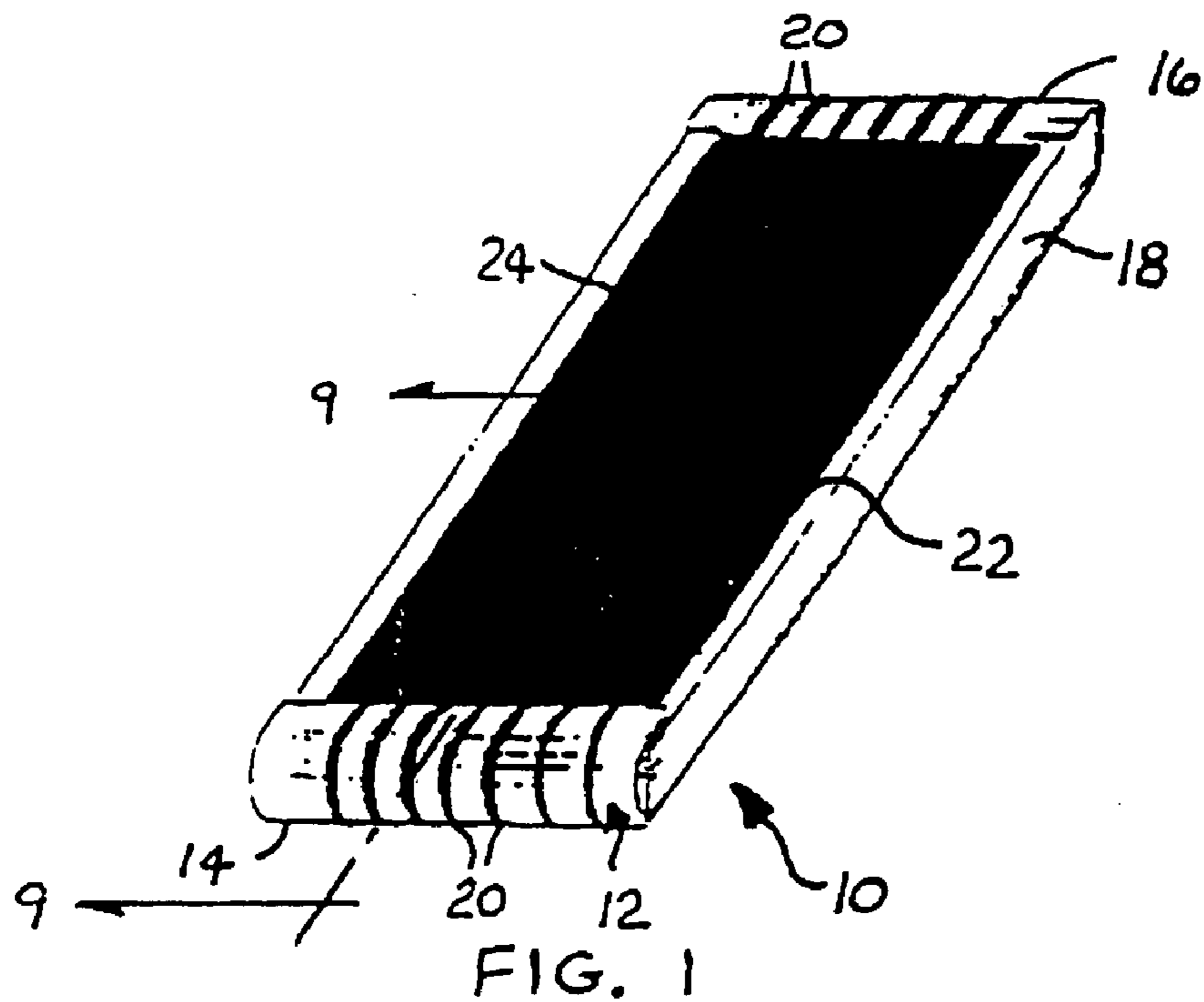
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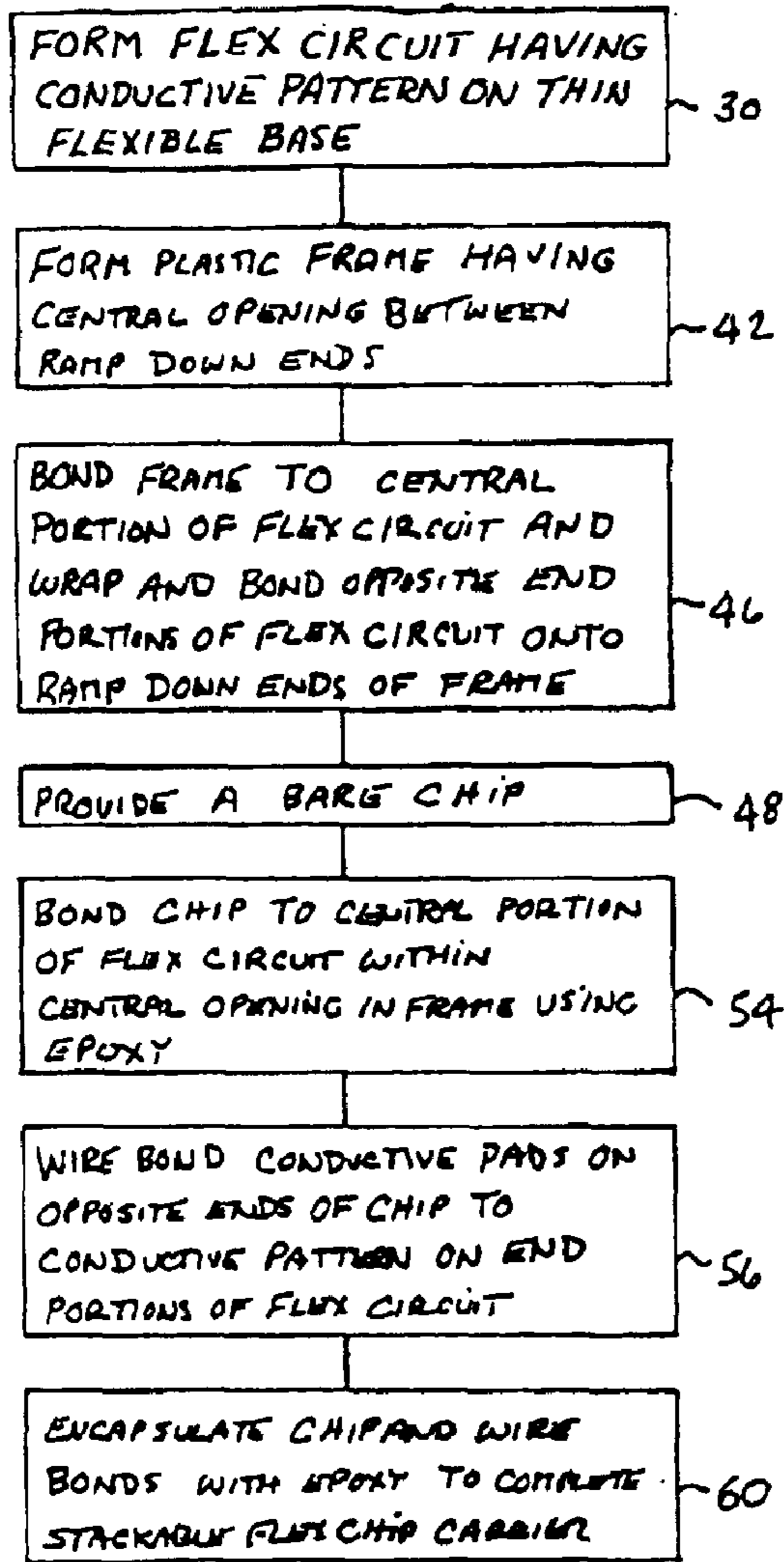


FIG. 2

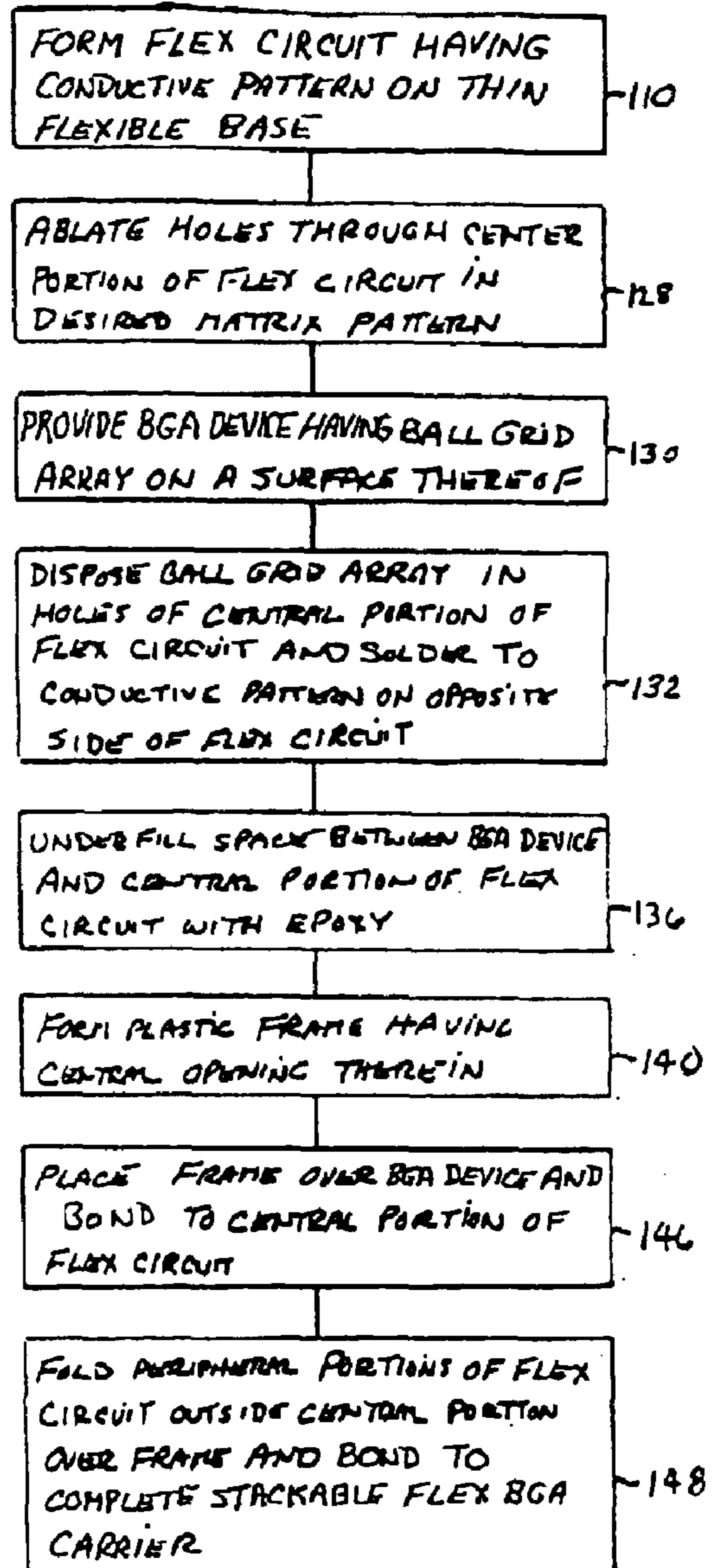
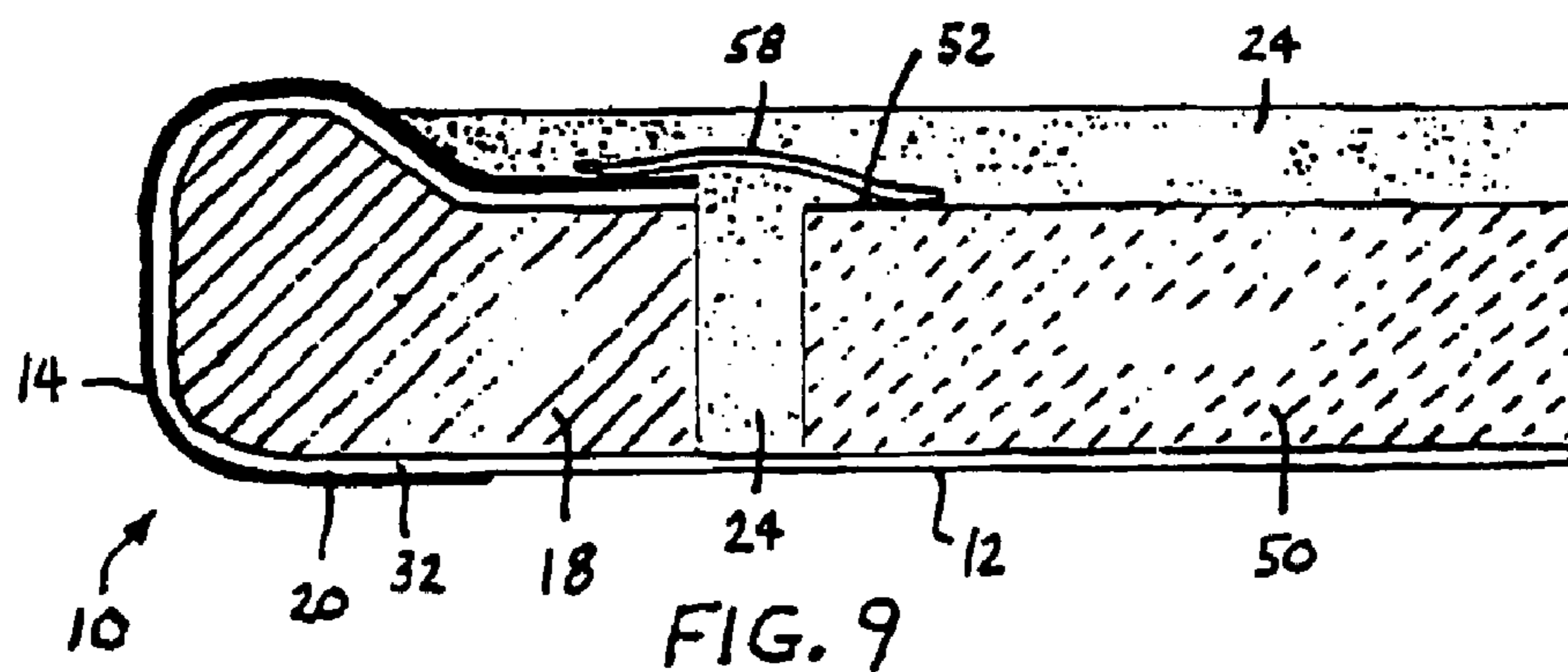
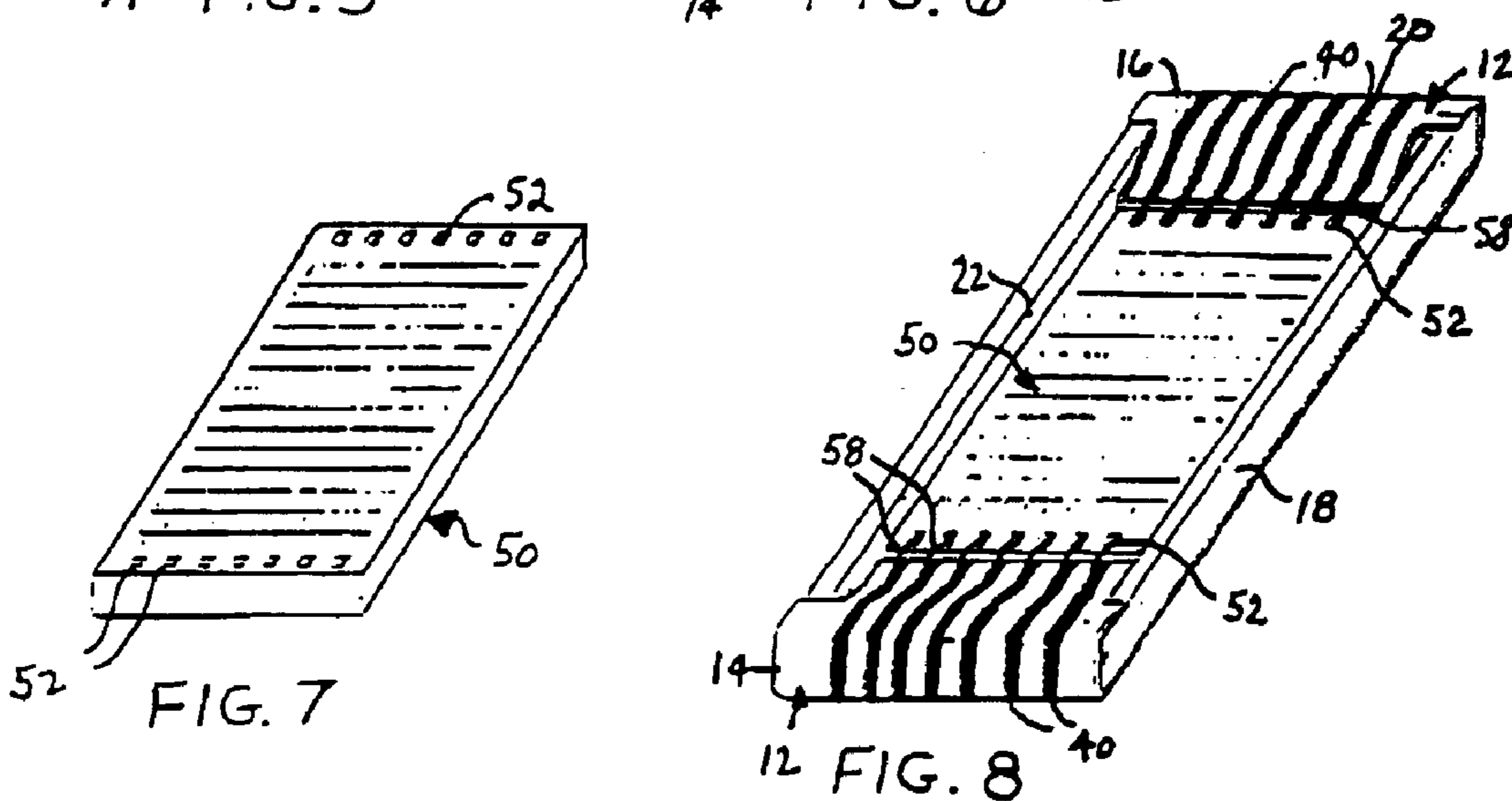
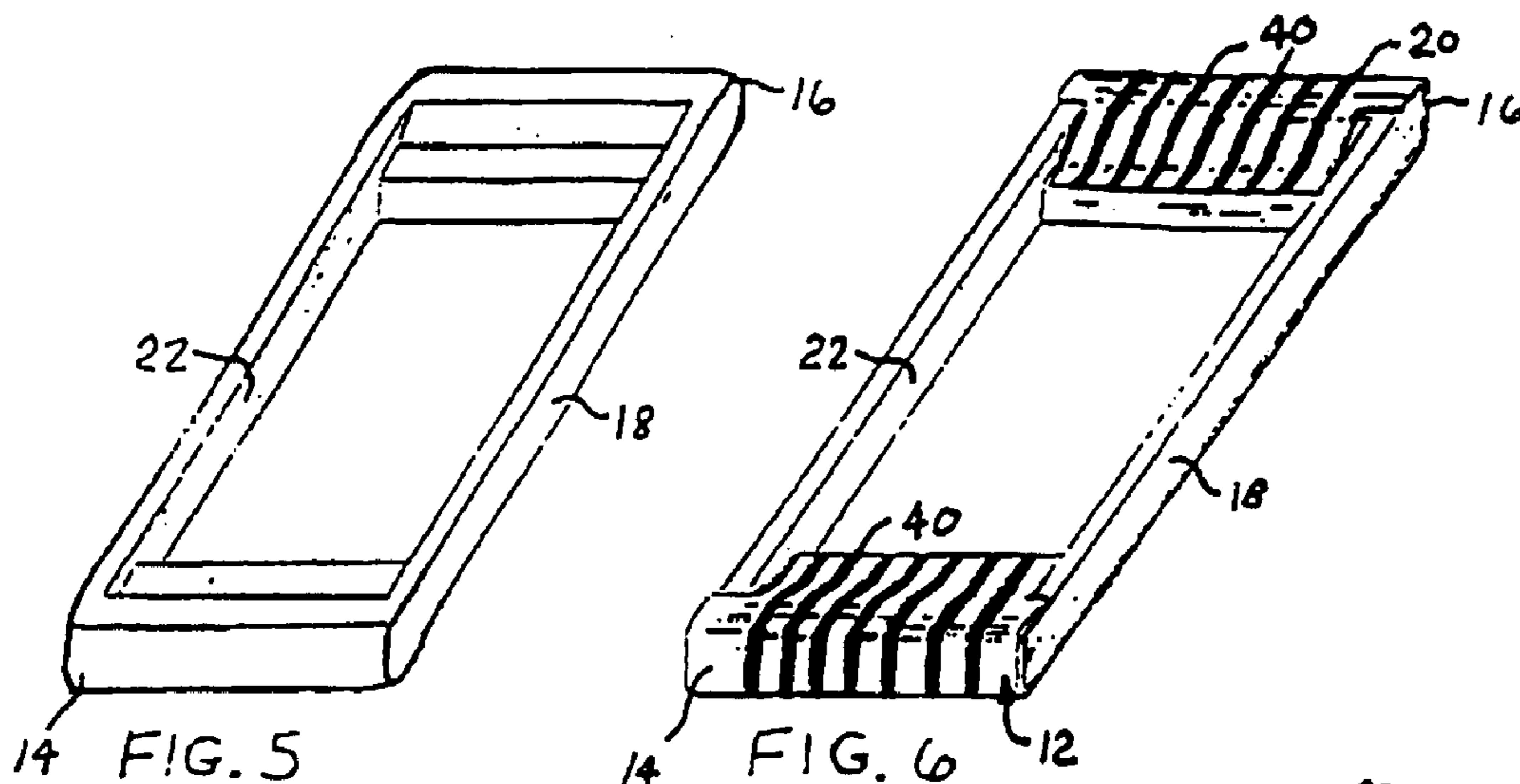
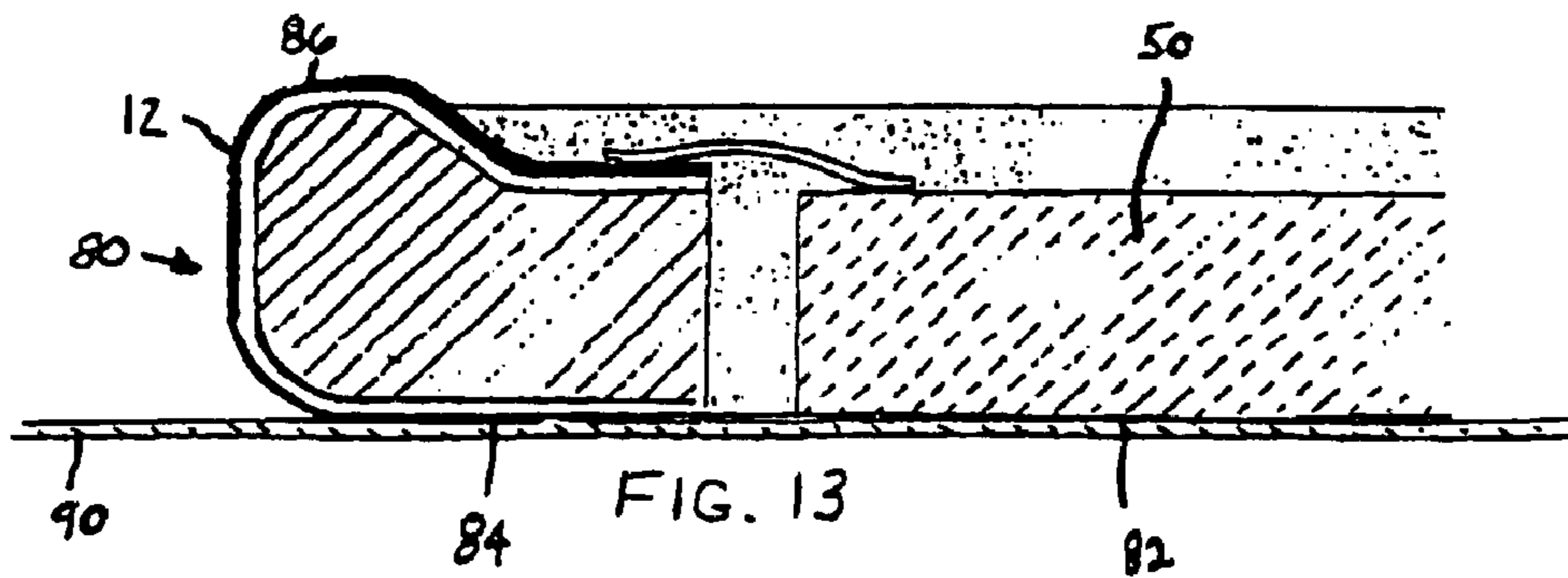
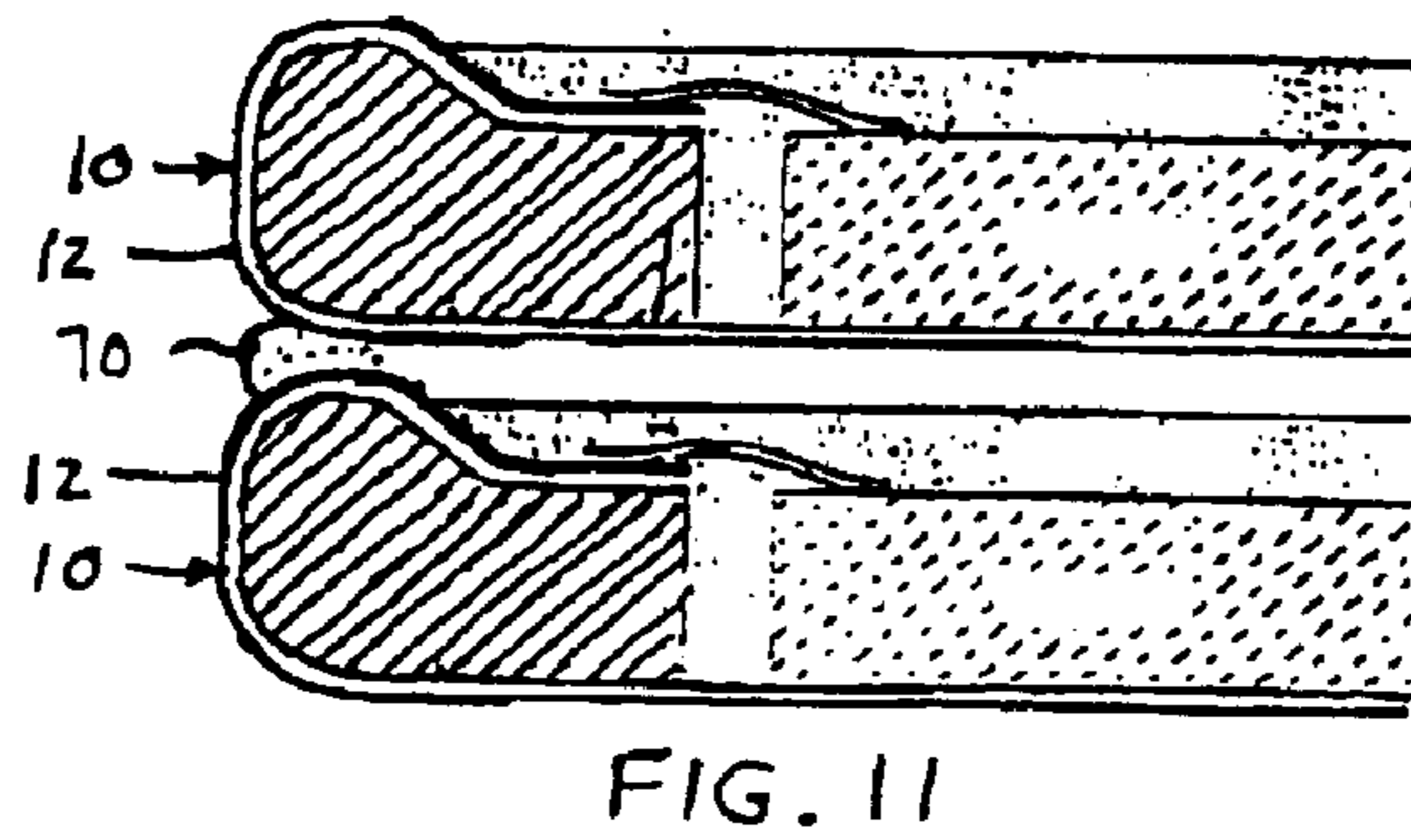
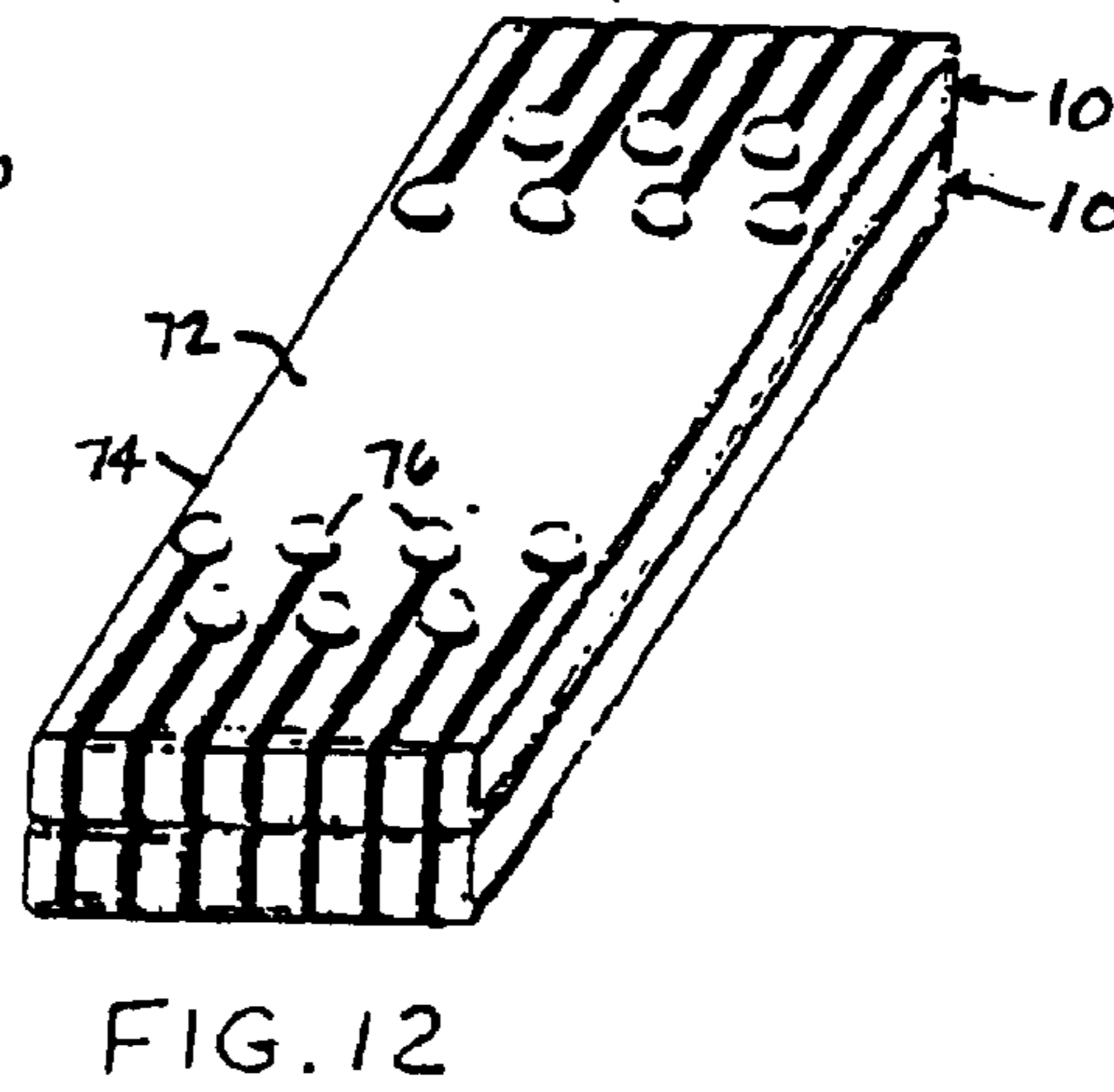
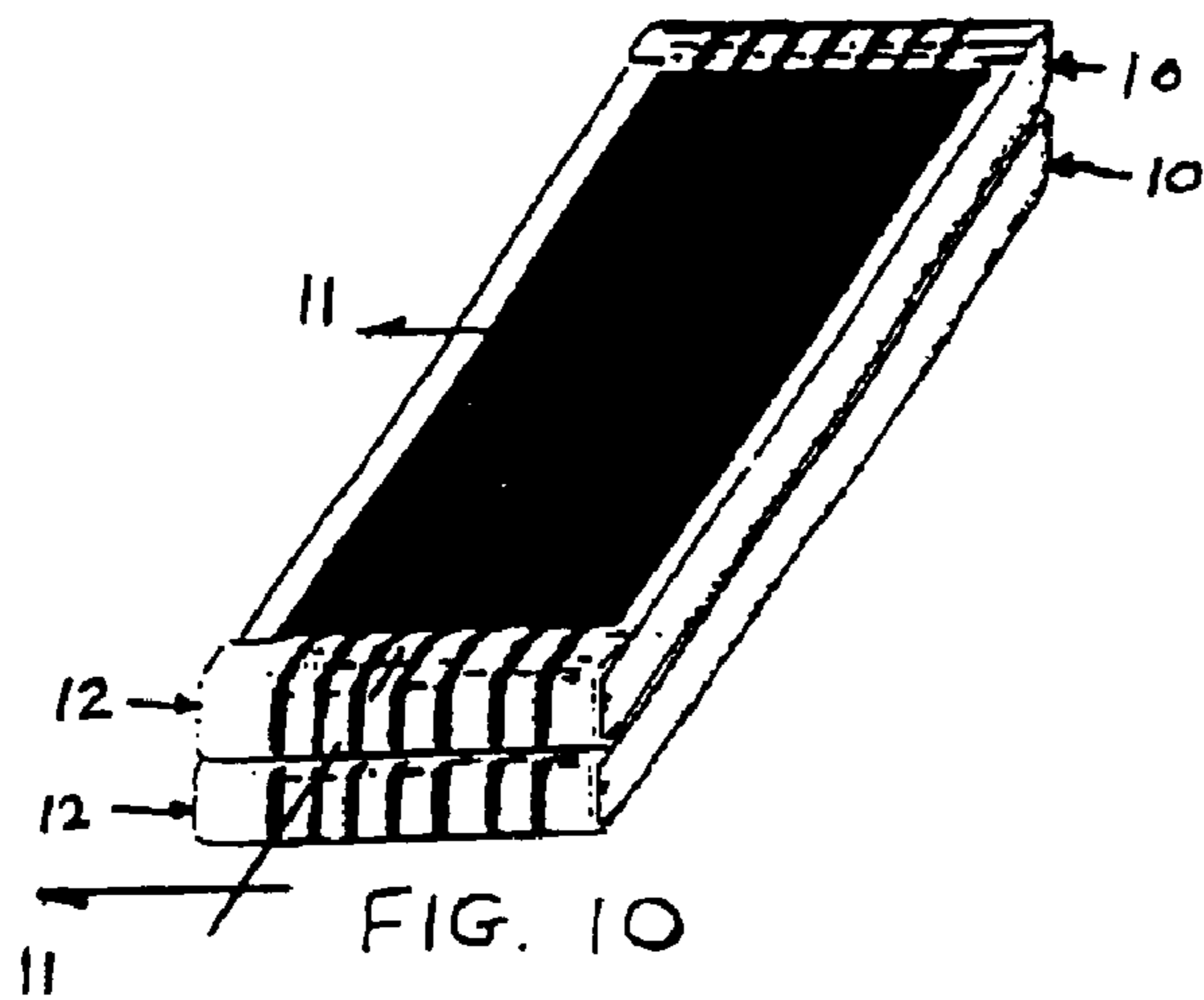
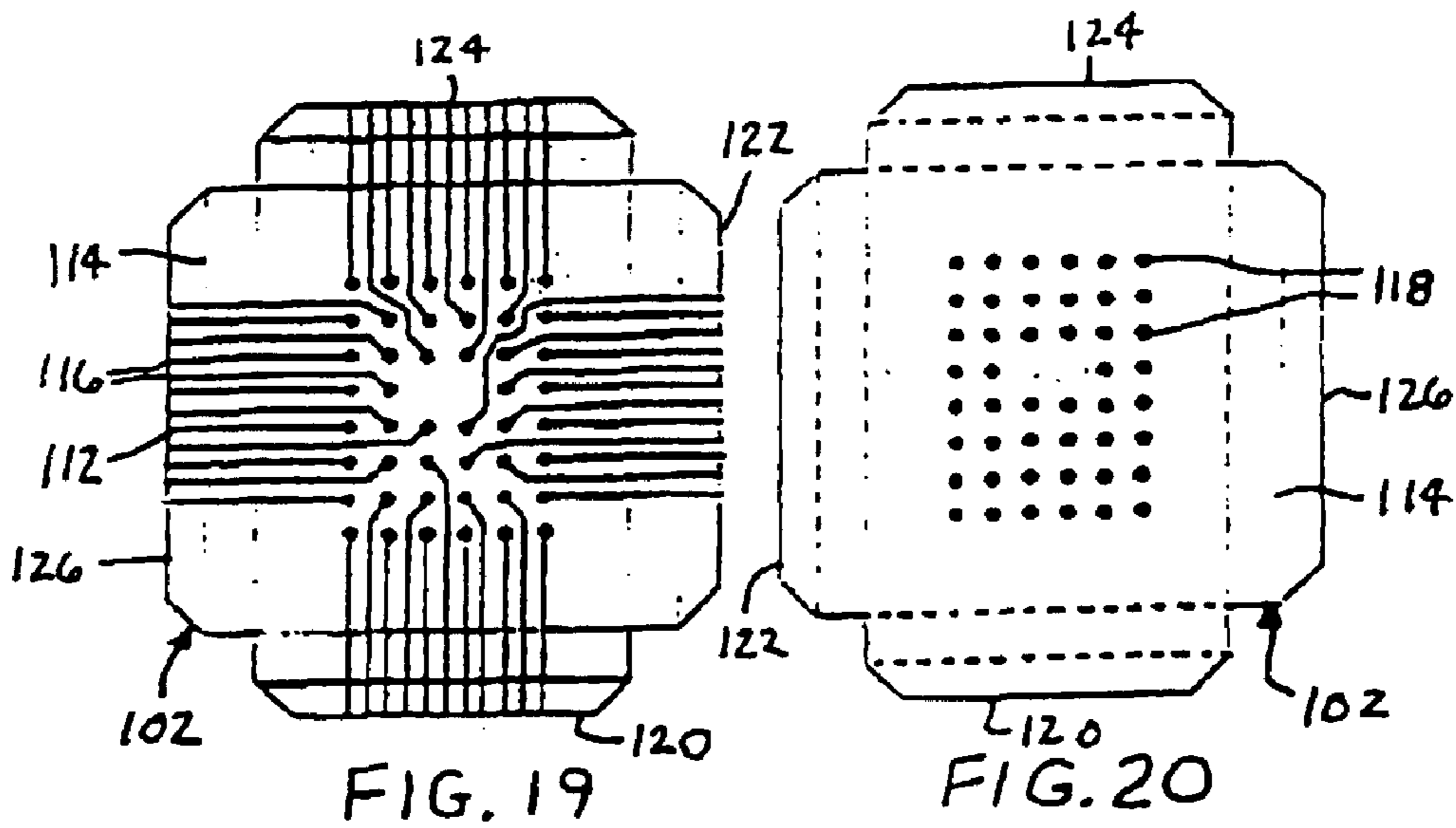
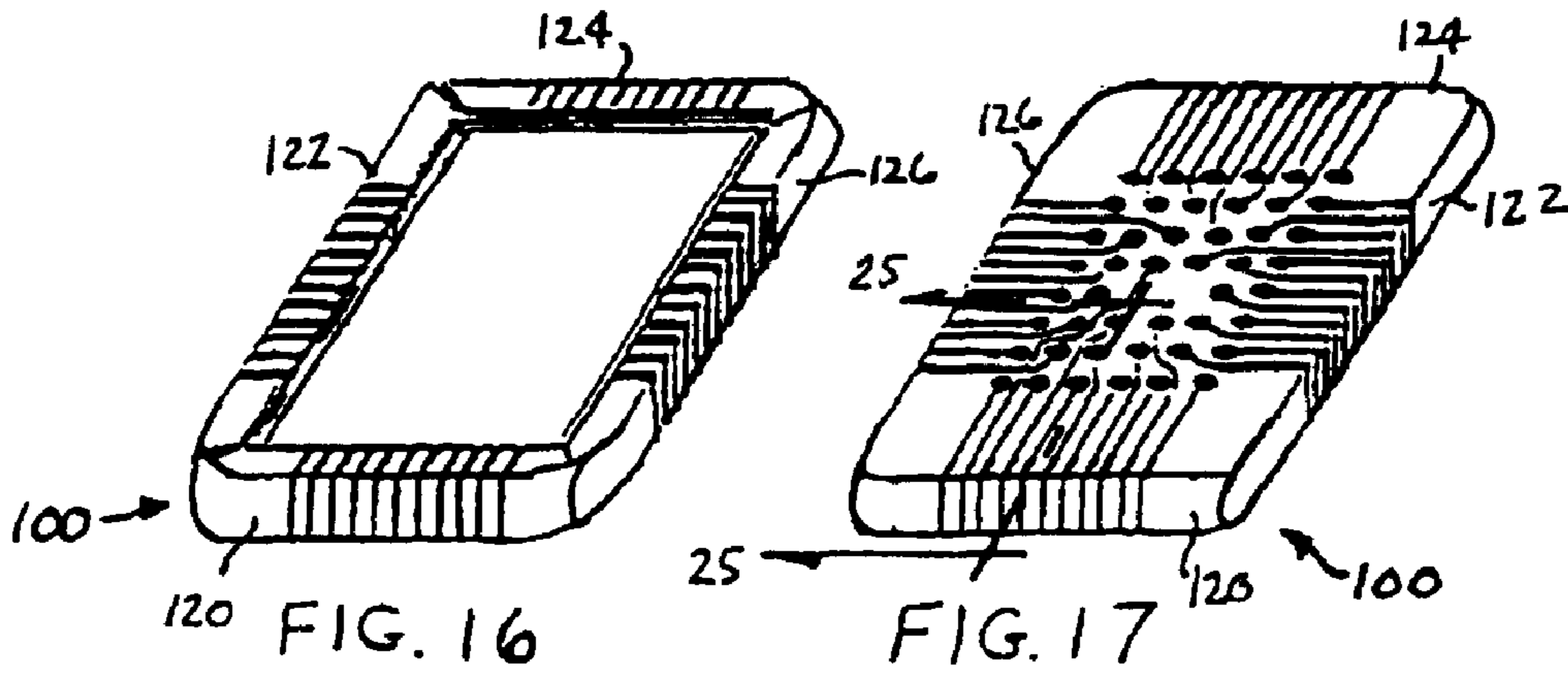
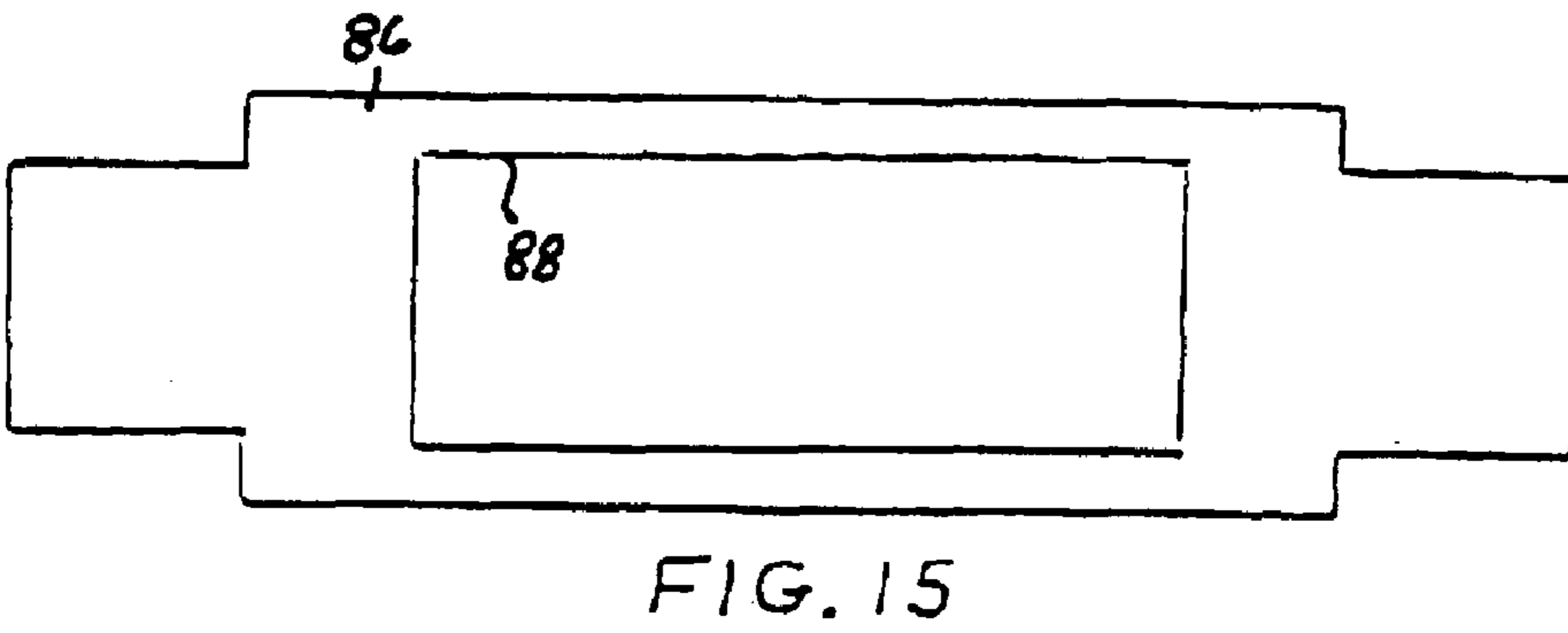
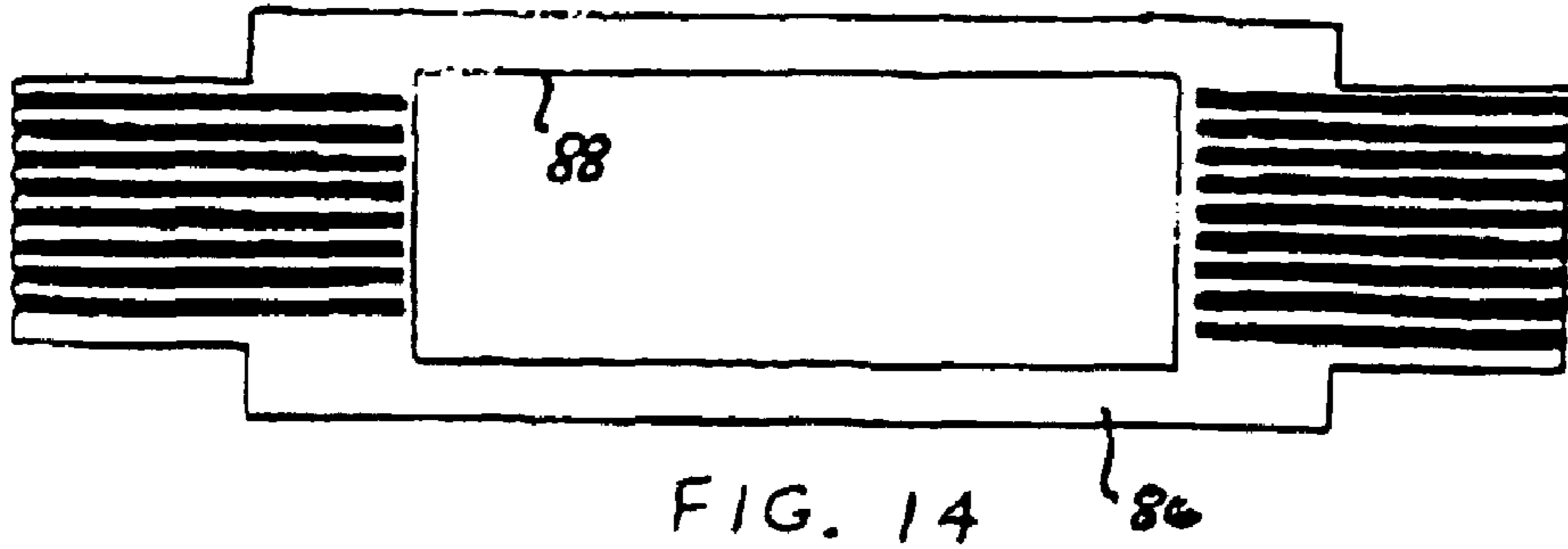
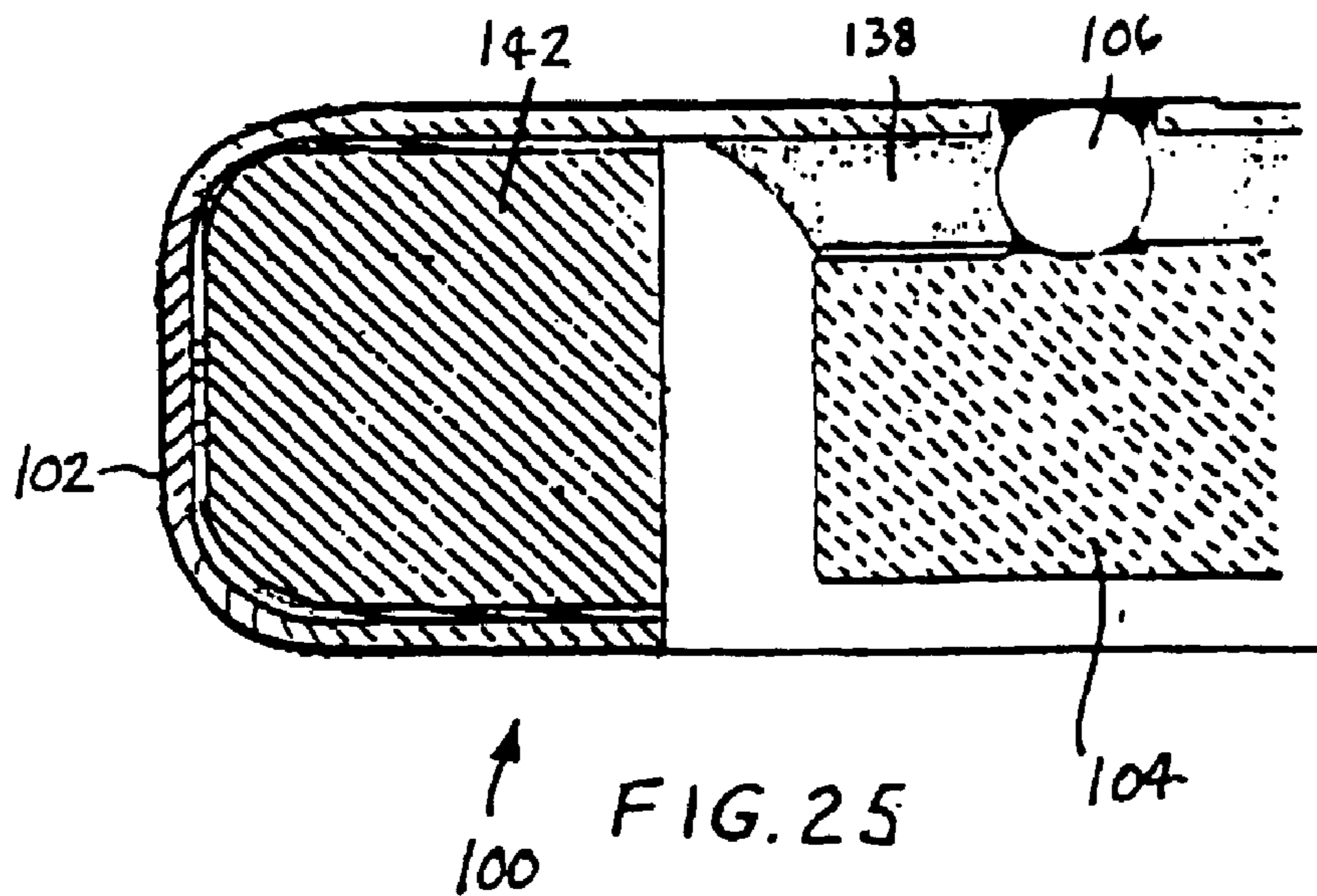
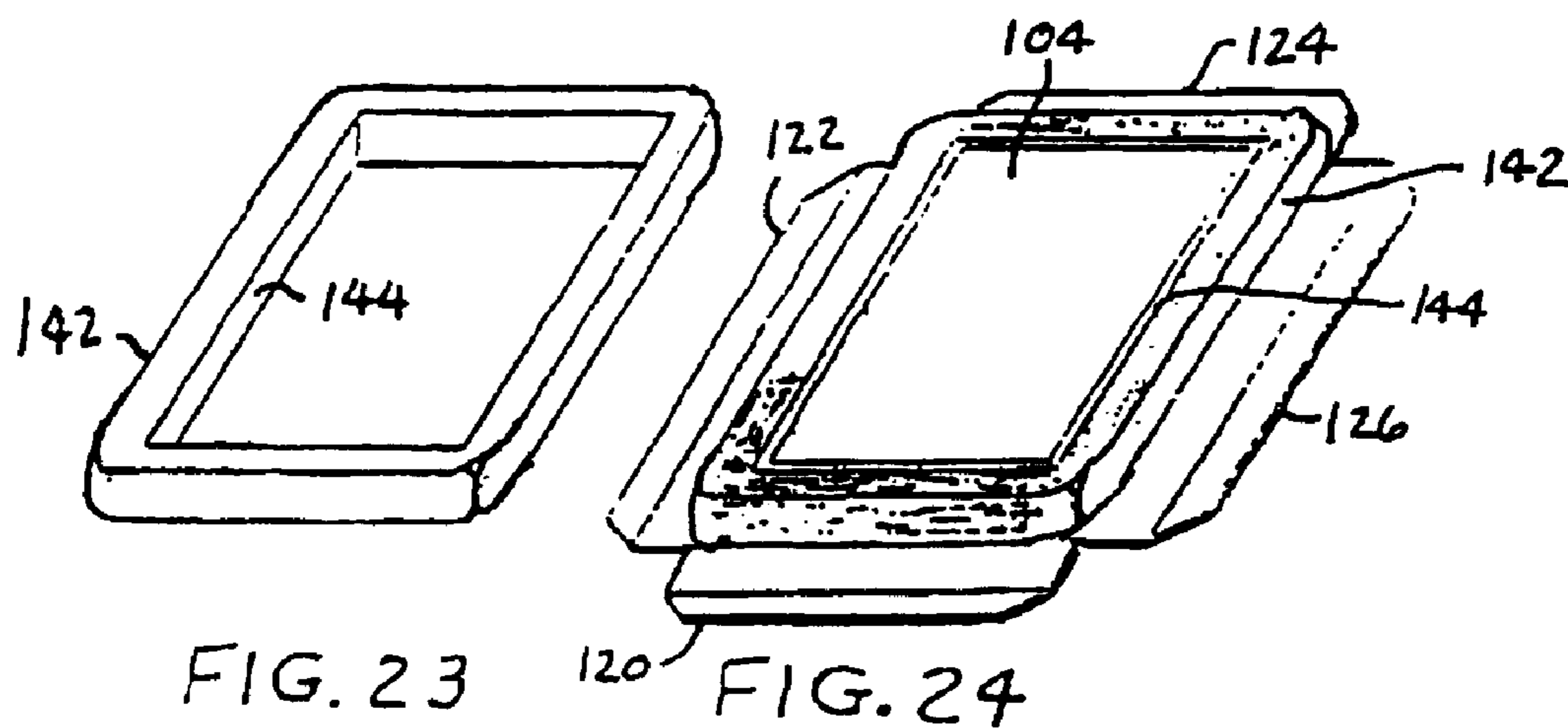
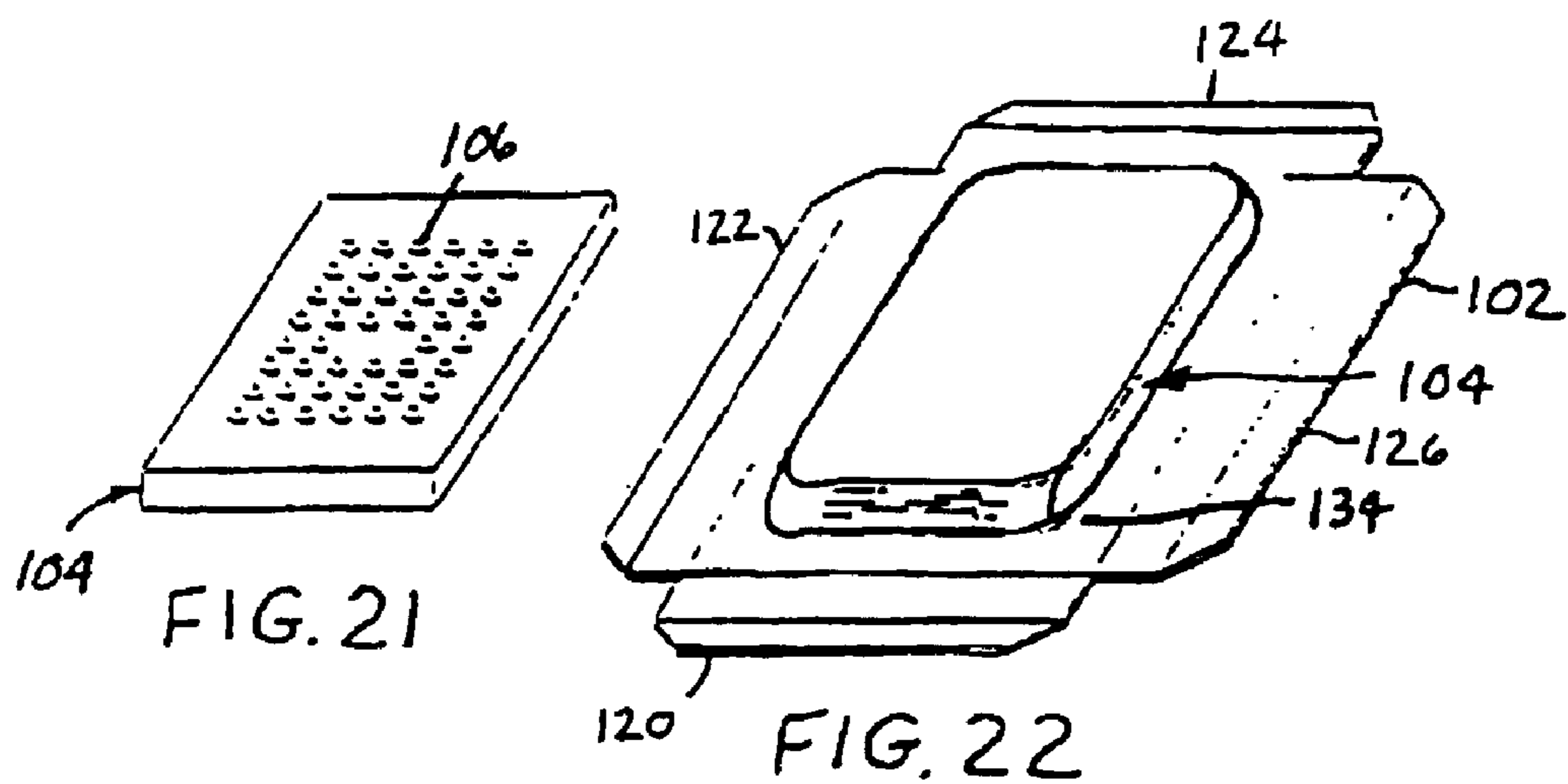


FIG. 18









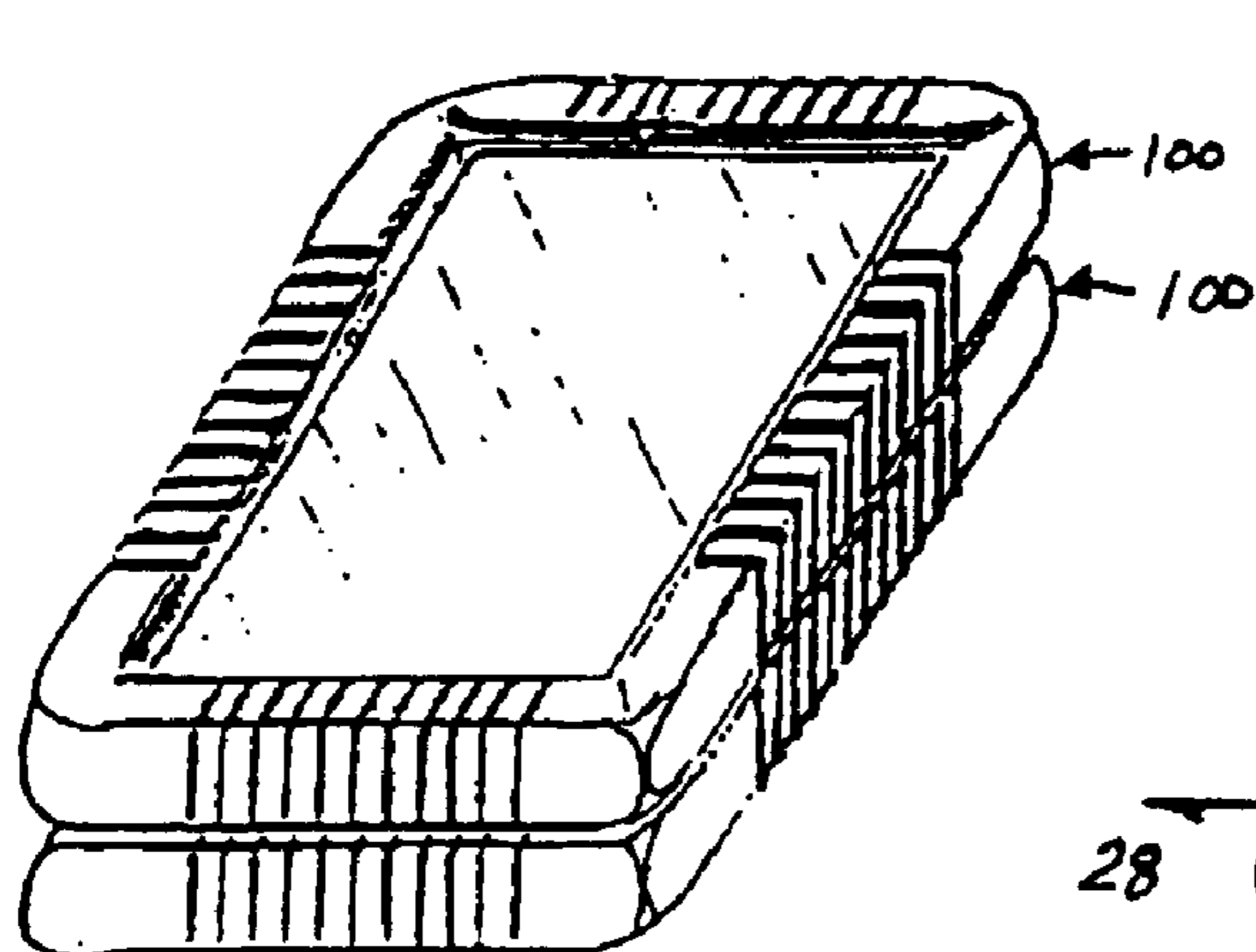


FIG. 26

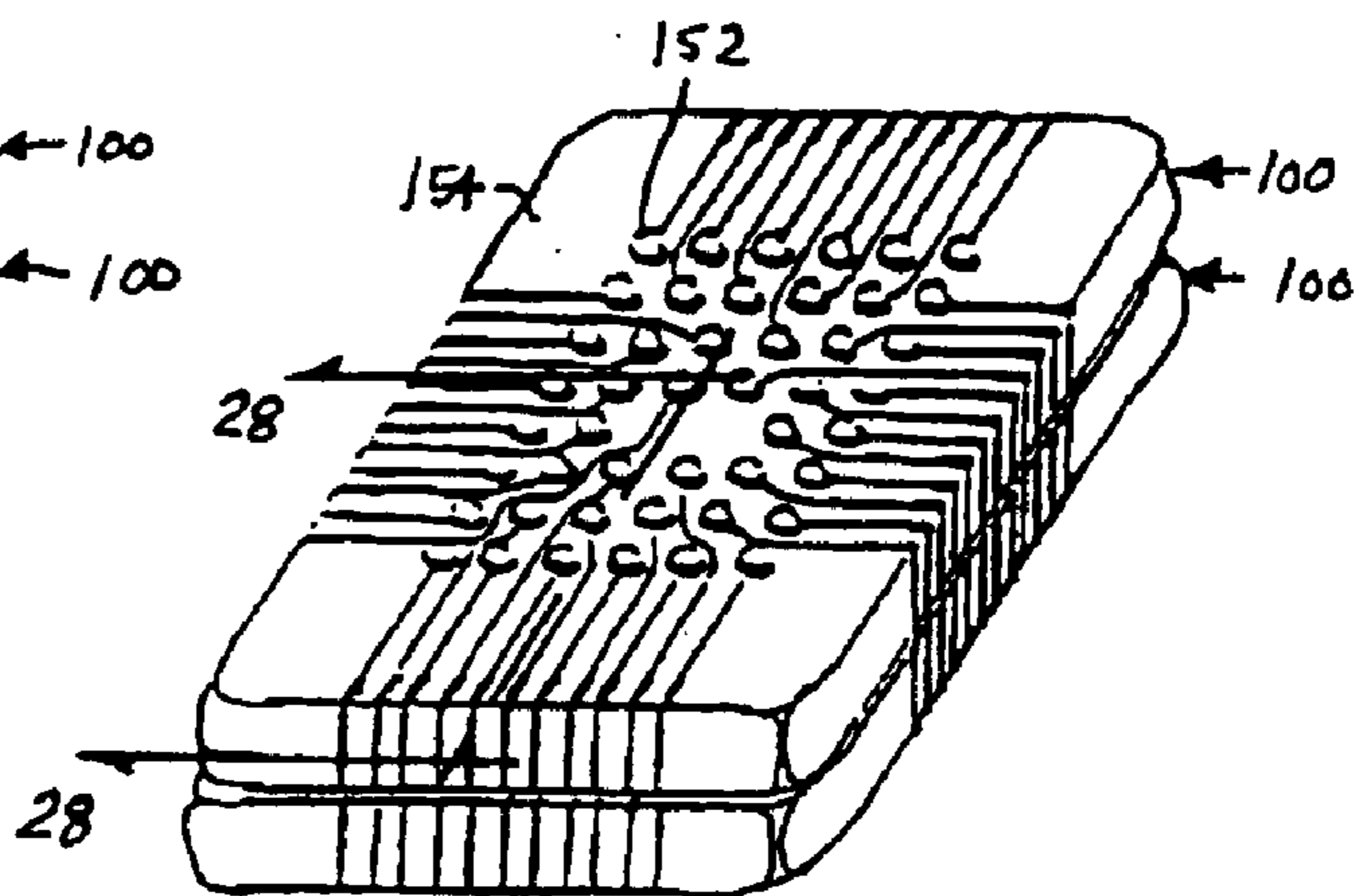


FIG. 27

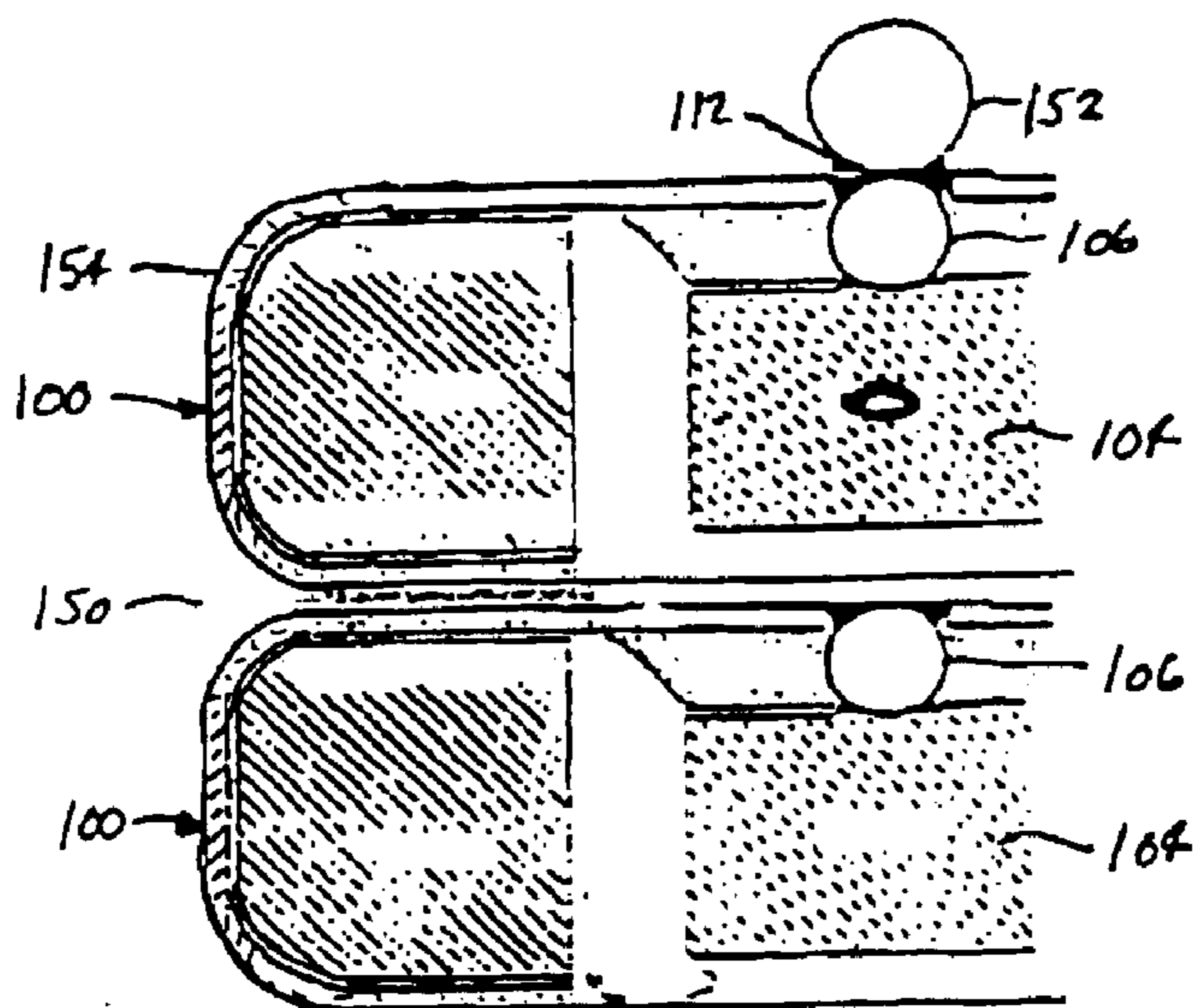


FIG. 28

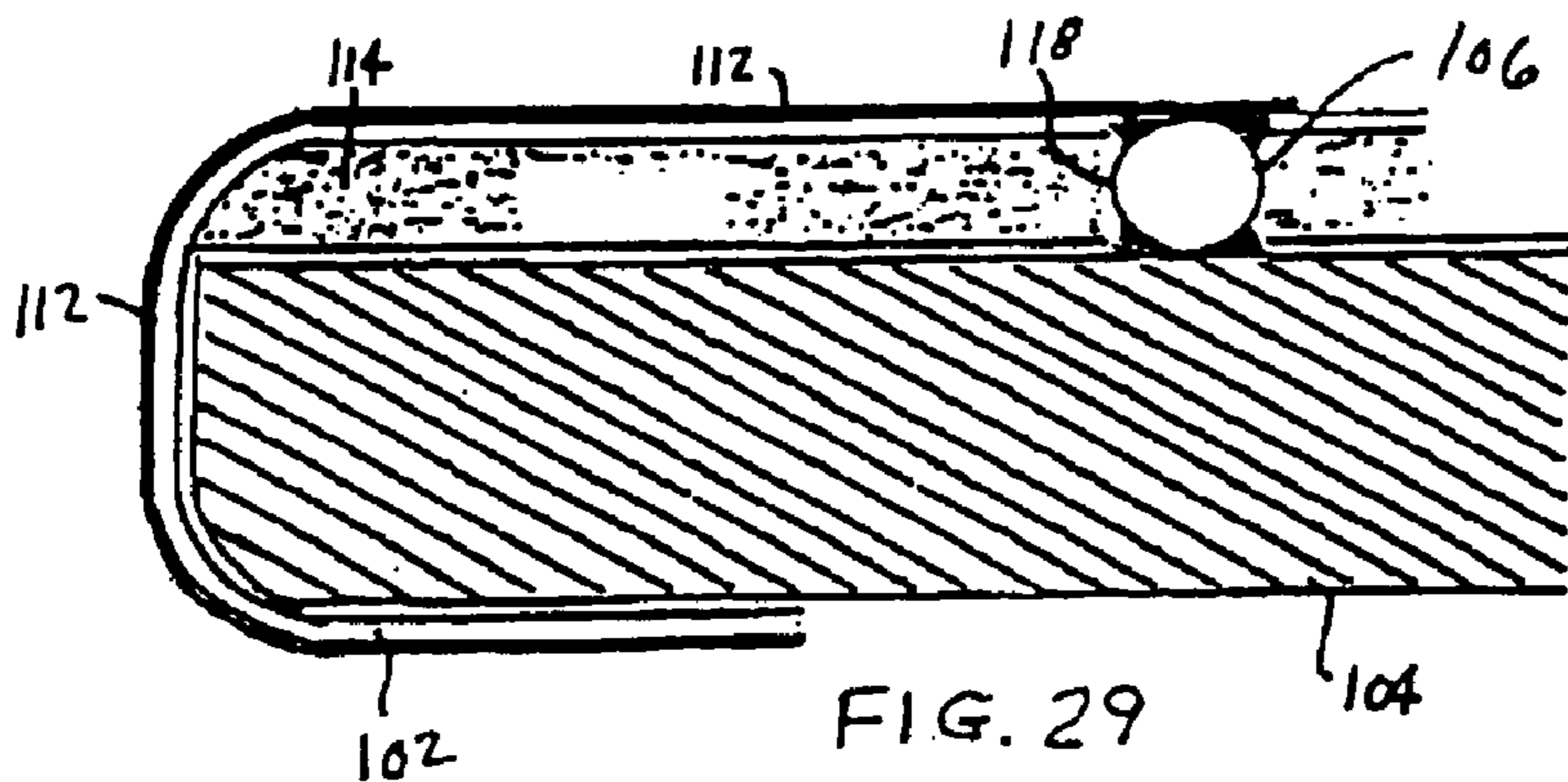


FIG. 29

STACKABLE FLEX CIRCUIT IC PACKAGE AND METHOD OF MAKING SAME

Matter enclosed in heavy brackets [] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

This is a division of Ser. No. 09/305,584 filed May 5, 1999 *now U.S. Pat. No. 6,323,060.*

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to stacks in which a plurality of integrated circuit (IC) packages arranged in a stack are electrically connected in a desired fashion, and to methods of making such stacks.

2. History of the Prior Art

Various common approaches are used to increase memory capacity on a circuit board. Larger memory IC devices such as chips can be used, if available. The size of the circuit board can be increased in order to hold more IC chips. Vertical plug-in boards can be used to increase the height of the mother board. The memory devices can be stacked in pancake style (sometimes referred to as 3D packaging or Z-Stacking). The Z-Stacking approach interconnects from 2 to as many as 8 chips in a single component which can be mounted on the "footprint" of a single package device. This approach is the most volumetrically efficient. Package chips in TSOP (thin small outline package) or LCC (leadless chip carrier) form have been used for stacking, and are perhaps the easiest to use. Bare chips or dies have also been used, but the process for forming a stack thereof tends to be complex and not well adapted to automation.

In forming a stack of IC chips such as memory chips, the chips must be formed into a stack and at the same time must be electrically interconnected in the desired fashion. Typically, the chips, which are mounted within packages therefor, have most of the electrical contacts thereof coupled in common or in parallel to contacts on a supporting substrate, and several unique contacts which are coupled individually to the substrate to the exclusion of the other chips. The prior art includes various different arrangements for electrically interconnecting the IC chips in a stack. For example, electrical conductors which may comprise thin film metal on an insulating base may be disposed perpendicular to the planes of the planar chips so as to connect those conductors on each chip which are exposed through openings in an insulating layer. Where the chip packages are assembled into a stack, electrical connections may be accomplished by lead frames or solder strips extending along the sides of the stack and attached to the electrical contacts of the chips.

Another common technique for providing the desired electrical interconnections in a chip stack is to form a stack of chips having bonding pads disposed on the chips adjacent the outer edges thereof. After assembling the stack of chips, the chip edges are ground flat and polished before sputtering an insulating layer thereon. The bonding pads on the edges of the chips are masked during the sputtering process to avoid covering them with the insulating layer. Next, a metal layer is sputtered onto the entire edge of the stack in conjunction with photomasking which forms conductive traces of the metal layer in desired locations for connecting the bonding pads.

Further examples of vertical stacks of IC chips and various methods of making such stacks are provided by U.S.

Pat. Nos. 4,956,694, 5,313,096 and 5,612,570, which patents are commonly assigned with the present application. U.S. Pat. Nos. 5,612,570, which issued Mar. 18, 1997 and is entitled CHIP STACK AND METHOD OF MAKING THE SAME, describes a chip stack and a method for making the same in which chip packages are first assembled by mounting plastic packaged chips or thin, small outline package chips (TSOPs) within the central apertures of thin, planar frames having a thickness similar to the thickness of the packaged chip. Leads at opposite ends of the package are soldered to conductive pads on the upper surface of the surrounding frame. Each frame also has other conductive pads on the upper and lower surface thereof adjacent the outer edges of the frame, which are coupled to the conductive pads that receive the leads of the packaged chip by conductive traces and vias. A chip stack is then formed by stacking together a plurality of the chip packages and dipping the upper edges of the stack into molten solder to solder together the conductive pads adjacent the outer edges of the frames. The conductive pads adjacent the outer edges of the frame can be interconnected in a stair step arrangement, and pads on opposite sides of each frame can be coupled in offset fashion using vias, in order to achieve desired electrical interconnections of the various chips.

A still further example is provided by copending application Ser. No. 08/935,216, filed Sep. 22, 1987 and entitled CHIP STACK AND METHOD OF MAKING SAME. Such application, which is commonly assigned with the present application, describes formation of a stack of ball grid array IC packages by assembling a ribbon-like structure of thin, planar bases, each with plural terminals and an interconnecting conductive pattern thereon, and with the bases electrically interconnected by flex circuits extending therebetween. A different IC package is mounted on each base by soldering the balls of a ball grid array thereon to the terminals of the base. The bases alternate in orientation, so that alternate IC packages are joined to the tops and bottoms of the bases. The resulting arrangement is then folded over on itself, with IC packages being joined to adjacent bases using adhesive. The resulting chip stack is mounted on a substrate by soldering the balls of the ball grid array at the underside of the lowermost base at the bottom of the stack to the substrate. The conductive patterns on the bases and the interconnecting flex circuits form conductive pads which contact selected terminals of the various IC packages as the pads extend in alternating fashion through the stack between opposite sides of the stack.

A still further example is provided by copending application Ser. No. 08/971,499, filed Nov. 17, 1997 and entitled METHOD OF MAKING CHIP STACKS. Such application, which is commonly assigned with the present application, describes the making of a chip stack which begins with the formation of a plurality of panels having apertures therein and conductive pads on opposite sides thereof. Solder paste is deposited on the conductive pads prior to mounting plastic packaged IC chips within each of the apertures in each of the panels so that opposite leads thereof reside on the conductive pads at opposite sides of the apertures. The plural panels are then assembled into a stack, such as by use of a tooling jig which aligns the various panels and holds them together in compressed fashion. The assembled panel stack is heated so that the conductive paste solders the leads of the packaged chips to the conductive pads and interfacing conductive pads of adjacent panels together, to form a panel stack comprised of a plurality of chip package stacks. Following cleaning of the panel stack to remove solder flux residue, the individual chip package stacks are separated from the panel stack by

cutting and breaking the stack. Score lines across the top-most panel and transverse slots within remaining panels therebelow result in the formation of strips of chip package stacks when longitudinal cuts are made through the panel stack. The remaining portions of the uppermost panel within such strips are then snapped along the score lines thereof to separate the individual chip package stacks from the strips.

A still further example is provided by copending application Serial No. 09/073,254, filed May 5, 1998 and entitled CHIP STACK AND METHOD OF MAKING SAME. Such application, which is commonly assigned with the present application, describes a stackable carrier made from plural layers of Kapton or other plastic material, and which may be made using conventional flex circuit techniques. The stackable carrier has a central opening, a plurality of stacking apertures extending through the thickness thereof between opposite surfaces of the carrier and a conductive pattern therein which extends between the central opening and the stacking apertures. An IC device is mounted within the central opening, and is electrically coupled to the conductive pattern such as by wire bonding or by soldering a ball grid array or other arrangement of contacts on the device directly to the conductive pattern, and is encapsulated therein with potting compound using conventional chip-on-board encapsulation technology, to form a single layer integrated circuit element. Conductive elements such as metallic balls are inserted into the stacking apertures, and are mounted therein using solder or conductive epoxy, so as to electrically contact the conductive pattern and form a stackable IC package. A stack of the IC packages is assembled by arranging a stack of the packages so that the metallic balls which protrude from a surface of each package are inserted into the stacking apertures of an adjacent package, where they are electrically and mechanically secured by solder or conductive epoxy. Balls mounted within the stacking apertures of a lowermost one of the IC packages protrude from the bottom surface thereof, so that the completed stack forms a ball grid array product.

The various arrangements and methods described in the patents and patent applications noted above have been found to provide IC package stacks and methods which are advantageous and which are suited for many applications. Nevertheless, the provision of further alternative arrangements and methods would be advantageous. In particular, it would be advantageous to provide IC package stacks and methods of making such stacks which utilize available materials and known process techniques, including particularly flex circuit technology. The assembly of such stacks should lend itself to automated production methods, and thus be competitive with other stacking approaches.

BRIEF SUMMARY OF THE INVENTION

The foregoing objects and features are achieved in accordance with the invention by an IC package stack and method of making the same which uses available materials and known process techniques and in which automated production methods can be used. A stackable flex circuit IC package in accordance with the invention includes an IC device and a flex circuit comprised of a flexible base with a conductive pattern disposed thereon. The IC device is mounted within a central aperture in a frame, and the flex circuit is wrapped around at least one end portion of the frame so as to expose the conductive pattern thereat. The IC device is electrically coupled to the conductive pattern. The conductive pattern of the flex circuit is comprised of a plurality of spaced-apart conductors. A stack of the stackable flex circuit IC packages may be formed, and the plurality of

spaced-apart conductors of the flex circuits of adjacent IC packages are electrically coupled, such as by use of anisotropic conductive epoxy. By pressing the adjacent IC packages together, the conductive epoxy forms connections between the adjacent IC packages in a vertical or Z-axis direction while maintaining the spaced-apart conductors of the conductive pattern within each flex circuit electrically isolated from one another.

When the IC devices comprise bare chips, the chip is electrically coupled to the conductive pattern of the flex circuit using wire bonds coupled between conductive pads of the chip and the conductive pattern of the flex circuit. A potting compound is applied to encapsulate the chip and the wire bonds within the frame. Alternatively, the IC devices may comprise BGA (Ball Grid Array) devices, such as chip scale packages, μ BGAs, flip chips, and the like, in which event an array of ball contacts or other conductive elements of the BGA device are disposed within apertures, formed such as by ablation, through the flexible base of the flex circuit. The balls of the grid pattern are soldered to the conductive pattern of the flex circuit to accomplish the electrical coupling. A potting compound is used to underfill a space between the surface of the chip having the ball grid array of contacts and the flexible base of the flex circuit.

Where the stackable flex circuit IC package has a bare chip mounted within a central aperture in the frame, the frame may be of elongated configuration with opposite ends of the flex circuit being mounted on the opposite step down ends of the frame so as to extend thereover and expose the conductive pattern at each of such opposite ends of the frame. Where a stack of the IC packages is assembled, a lowermost one of the packages in the stack may be provided with a plurality of contacts on the conductive pattern at each of the opposite ends to facilitate coupling and electrical interconnection of the stack to a substrate board. Within each IC package, the flex circuit extends across the central aperture in the frame, and the IC device is secured thereto within the aperture. Alternatively, in order to provide a thinner IC package, the flex circuit may be provided with a central aperture therein in the region of the central aperture in the frame. The IC device is disposed in the central aperture of the flex circuit so that a bottom surface of the IC device is generally coplanar with an adjacent lower surface of the flex circuit opposite the frame.

Where the IC package is formed using a BGA device, a central portion of the flex circuit has a plurality of holes ablated or otherwise formed therethrough in an array which corresponds with an array of conductive elements on the device. The conductive pattern is formed on the flex circuit so as to extend between the holes and four opposite edges of the flex circuit. After securing the frame to the flex circuit and the device to the flex circuit and mounting the device within the central aperture in the frame, the array of balls or other conductive elements at the bottom of the device are soldered to the conductive pattern on the flex circuit, with the balls disposed within the apertures in the flex circuit. The four opposite sides of the flex circuit are then wrapped over and bonded such as by adhesive to the frame, exposing the conductive pattern at the four edges of the frame. Upon stacking such IC packages, conductive epoxy such as anisotropic conductive epoxy is applied to the exposed conductive pattern at the four sides of the frame, and the application of pressure between adjacent IC packages completes the electrical interconnections between the individual conductors of the conductive pattern of adjacent IC packages.

A method of making a stackable flex circuit IC package in accordance with the invention includes the steps of provid-

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ing a flex circuit with a conductive pattern thereon and providing a frame having an opening therein. The frame is secured onto the flex circuit so that the flex circuit is wrapped around at least one end of the frame to expose the conductive pattern at the at least one end. An IC device is secured to the flex circuit within the opening in the frame, and the device is electrically coupled to the conductive pattern on the flex circuit. The device is then encapsulated with epoxy. The flex circuit may be formed by sputtering or otherwise depositing a conductive layer on a layer of thin flexible base, followed by etching of the layer to form a desired conductive pattern. Where a bare chip is used, the electrical interconnection is accomplished by wire bonding the conductive pads of the chip to the conductive pattern of the flex circuit. In that event, the wire bonds are encapsulated as part of the step of encapsulating the chip with epoxy.

Where the IC package uses a BGA device, the step of providing a flex circuit includes forming a matrix of holes through the flexible base to the conductive pattern of the flex circuit. The ball grid array or other conductive elements of the device are disposed within the matrix of holes and coupled to the conductive pattern such as by soldering. A space between the circuit and the device is underfilled with epoxy. Thereafter, a frame having an opening therein is placed over the chip and is attached to the flex circuit, such as by adhesive. The opposite edges of the flex circuit are then folded over the frame and are bonded, again such as by adhesive.

DESCRIPTION OF THE FIGURES

A detailed description of the invention will be made with reference to the accompanying drawings, in which:

FIG. 1 is a perspective view of a stackable flex circuit IC package in accordance with the invention;

FIG. 2 is a block diagram of the successive steps of a method of making the IC package of FIG. 1;

FIG. 3 is a top view of a flex circuit used in the IC package of FIG. 1;

FIG. 4 is a bottom view of the flex circuit of FIG. 3;

FIG. 5 is a perspective view of a frame used in the IC package of FIG. 1;

FIG. 6 is a perspective view of the frame of FIG. 5 with the flex circuit of FIG. 3 mounted thereon;

FIG. 7 is a perspective view of a bare memory chip or die used in the IC package of FIG. 1;

FIG. 8 is a perspective view similar to that of FIG. 6 but with the chip of FIG. 7 mounted within a central opening in the frame and electrically coupled by wire bonds to the conductive pattern of the flex circuit;

FIG. 9 is a sectional view of a portion of the IC package of FIG. 1 taken along the lines 9—9 thereof.

FIG. 10 is a perspective view of a stack of two of the IC packages of FIG. 1;

FIG. 11 is a sectional view of a portion of the stack of FIG. 10 taken along the line 11—11 thereof;

FIG. 12 is an inverted perspective view of the stack of FIG. 10 showing the manner in which the lowermost IC package is provided with an array of contacts for mounting the stack on a substrate board;

FIG. 13 is a sectional view similar to the view of FIG. 9 but showing an alternative arrangement of an IC package in which the IC device extends into a central aperture within the flex circuit;

FIG. 14 is a top view of a flex circuit used in the IC package of FIG. 13;

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FIG. 15 is a bottom view of the flex circuit of FIG. 14;

FIG. 16 is a perspective view of a stackable flex circuit IC package in accordance with the invention, which utilizes a BGA (Ball Grid Array) device;

FIG. 17 is an inverted perspective view of the IC package of FIG. 16;

FIG. 18 is a block diagram of the successive steps of a method of making the IC package of FIG. 16;

FIG. 19 is a top view of a flex circuit used in the IC package of FIG. 16;

FIG. 20 is a bottom view of the flex circuit of FIG. 19;

FIG. 21 is a perspective view of a BGA device used in the IC package of FIG. 16;

FIG. 22 is a perspective view of the BGA device of FIG. 21 as it is mounted on the flex circuit of FIG. 19;

FIG. 23 is a perspective view of a frame used in the IC package of FIG. 16;

FIG. 24 is a perspective view similar to the view of FIG. 22 but with the frame of FIG. 23 mounted on the flex circuit together with the BGA device of FIG. 21;

FIG. 25 is a sectional view of the IC package of FIG. 16 taken along the line 25—25 of FIG. 17;

FIG. 26 is a perspective view of a stack of two of the IC packages of FIG. 16;

FIG. 27 is an inverted perspective view of the stack of FIG. 26;

FIG. 28 is a sectional view of a portion of the stack of FIG. 26 taken along the line 28—28 of FIG. 27; and

FIG. 29 is a sectional view of an alternative embodiment of a IC package in accordance with the invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 depicts a stackable flex circuit IC package 10 in accordance with the invention. The IC package 10 includes a flex circuit 12 mounted on and wrapped around opposite ends 14 and 16 of an elongated frame 18. The flex circuit 12 includes a conductive pattern 20 thereon which is exposed at the opposite ends 14 and 16 of the frame 18. This facilitates electrical interconnection between adjacent IC packages when a stack of the IC packages 10 is formed, as described hereafter. The chip package 10 includes an IC device such as a memory chip or die which is hidden from view in FIG. 1 and which is shown and described in FIG. 7 hereafter. The memory chip is mounted within a central aperture 22 within the frame 18 where it is encapsulated by a quantity of potting compound in the form of epoxy 24.

FIG. 2 shows the successive steps of a method of making the IC package 10. In a first such step 30, the flex circuit 12 is formed by depositing a conductive layer of metal and then etching the layer of metal to form the conductive pattern 20, on a thin flexible base 32. FIG. 3 is a top view of the flex circuit 12, while FIG. 4 is an opposite bottom view of the flex circuit 12. As shown in FIGS. 3 and 4, the flex circuit 12 is of elongated configuration with opposite end portions 34 and 36 that are slightly narrower than an intermediate portion 38 therebetween. The flex circuit 12 is made using conventional flex circuit techniques. The base 32 is made of material such as Kapton or polyimide and is thin and flexible. Typically, the base 32 is several mils thick or less. The base 32 exists principally for the purpose of supporting the conductive pattern 20 thereon. The conductive pattern 20 comprises a thin layer of adhesiveless copper which is formed on the base 32 such as by sputtering. The layer of

copper, which can have a thickness ranging from just a few microns to as much as 25 microns, is etched to form individual conductors which are spaced apart by very small distances such as a few mils. A pitch of 4 mils between the individual conductors is possible. This greatly increases the routing density. As shown in FIG. 3, the conductive pattern 20 is comprised of parallel, spaced-apart arrays of the individual conductors 40 at the opposite end portions 34 and 36 of the flex circuit 12.

While the flex circuit 12 is shown and described as having the conductive pattern 20 on only one side of the flexible base 32, the conductive pattern can be placed on both sides where desired to achieve various chip package configurations. As described hereafter, a laser can be used to ablate holes through the base 32 which covers portions of the conductive pattern 20. When the base 32 is ablated through, the copper of the conductive pattern 20 reflects the laser so as to be unaffected thereby.

As shown in FIG. 2, a second step 42 comprises forming the frame 18. As shown in FIG. 5, the frame 18 is of elongated configuration between the opposite ends 14 and 16 thereof and has the central aperture 22 therein. The opposite ends 14 and 16 are of ramp down configuration. In the present example, the frame 18 is molded from high temperature heat resistant plastic.

In a third step 46 of the method of FIG. 2, the frame 18 is bonded on the intermediate portion 38 of the flex circuit 12, and the end portions 34 and 36 are wrapped around and bonded to the ramp down ends of the frame 18 at the opposite ends 14 and 16 thereof. The bonding is accomplished using adhesive. The adhesive can be coated on the parts to be bonded, or a transfer adhesive can be used. The result is shown in FIG. 6. With the end portions 34 and 36 of the flex circuit 12 wrapped around and bonded to the ramp down ends of the frame 18, the conductive pattern 20 at the end portions 34 and 36 of the flex circuit 12 is exposed at the ends 14 and 16 of frame 18. This facilitates electrical interconnection of the conductive patterns 20 of adjacent IC packages 10 when a stack of the chip packages 10 is formed. It also provides for electrical interconnection of an IC device to the conductive pattern 20, as described hereinafter in connection with FIGS. 8 and 9.

In a fourth step 48 of the method of FIG. 2, an IC device in the form of a bare memory chip or die 50 is provided. The chip 50, which is shown in FIG. 7, is of conventional configuration and has a plurality of terminals in the form of conductive pads 52 at opposite ends of an upper surface thereof.

In a fifth step 54 of the method of FIG. 2, the chip 50 is bonded to the intermediate portion 38 of the flex circuit 12 within the central opening or aperture 22 in the frame 18, using epoxy. This disposes the conductive pads 52 of the chip 50 adjacent the individual conductors 40 of the conductive pattern 22 at the opposite ends 14 and 16 of the flex circuit 12.

In a sixth step 56 of the method of FIG. 2, the conductive pads 52 of the chip are wire bonded to the conductors 40 of the conductive pattern 20 at the ends 14 and 16 of the flex circuit 12, to electrically couple the chip 50 to the conductive pattern 20. FIGS. 8 and 9 show the resulting wire bonds 58. The wire bonds 58 may be formed by wedge bonding gold or aluminum wire.

In a seventh step 60 of the method of FIG. 2, the chip 50 and the wire bonds 58 are encapsulated with the epoxy 24 shown in FIG. 1. The epoxy 24 covers the chip 50 and the wire bonds 58, and extends down around the peripheral

edges of the chip 50 to seal the chip 50 in place within the frame 18. The sectional view of FIG. 9 shows the manner in which the epoxy 24 covers and encapsulates the chip 50 and the wire bonds 58. This completes the stackable flex IC package 10.

It will be appreciated by those skilled in the art that the stackable flex circuit IC package 10 utilizes readily available materials and well developed process techniques. The essence of the IC package 10 is the flex circuit 12 which routes connections from the chip 50 to peripheral positions at the ends 14 and 16 of the frame 18, allowing the IC package 10 to be stacked. FIG. 10 shows a stack of two of the IC packages 10. Because the conductive pattern 20 of the flex circuit 12 is exposed at the ends 14 and 16 of the frame 18 of each IC package 10, electrical interconnections between the conductive patterns 20 of the adjacent IC packages 10 is readily accomplished using conductive epoxy. Such epoxy also joins the IC packages 10 together within the stack. While the stack shown in FIGS. 10-12 is comprised of two of the IC packages 10, greater numbers of the IC packages 10 can be stacked by joining together each adjacent pair of the packages 10 in the manner described hereafter.

FIG. 11 shows a quantity of conductive epoxy 70 placed between the conductive patterns 20 of the flex circuits 12 of the two different IC packages 10 of the stack. The conductive epoxy 70, which contains conductive polymer particles, is an anisotropic material which becomes conductive in a Z-axis or vertical direction when pressure is applied thereto. To assemble the stack of IC packages 10, the conductive epoxy 70 is applied between the adjacent conductive patterns 20 at both ends 14 and 16 of the IC packages 10. The epoxy comes in liquid or sheet form. The IC packages 10 are then pressed together, as heat is applied. After the epoxy is cured, the IC packages 10 are bonded together and the heat and pressure may be removed. In addition to bonding, the epoxy forms electrical connections in the vertical or Z-axis direction between the individual conductors 40 of the conductive patterns 20 of the adjacent IC packages 10. However, because of the anisotropic nature of the conductive epoxy 70, electrical connections are not made in the lateral or horizontal direction. Consequently, the conductors 40 within each conductive pattern 20 remain electrically isolated from each other. There is no bridging between the conductors 40 in spite of the close pitch. This is advantageous over solder which tends to bridge between adjacent conductors and which requires a higher temperature.

To enable the stack of IC packages 10 shown in FIG. 10 to be mounted on and electrically coupled to a substrate board, the lowermost one of the IC packages 10 is provided at a lower surface thereof with a plurality of contacts. This is shown in FIG. 12 in which a bottom surface 72 of a lowermost one 74 of the IC packages 10 is provided with an array of contacts 76 thereon. The contacts 76 are electrically coupled to the conductors 40 of the conductive pattern 20 at the opposite ends 14 and 16 of the lowermost one 74 of the IC packages 10. The contacts 74 are coupled, such as by soldering, to mating contacts on the surface of a substrate board (not shown) to mount the stack of IC packages 10 and electrically couple such IC packages 10 to the substrate board.

FIG. 13 shows a variation of the IC package 10 which allows the IC package to be made somewhat thinner. An IC package 80 as shown in FIG. 13 is similar to the IC package 10 shown in FIGS. 1-12, except that the chip 50 thereof extends to the bottom of the central aperture 22 within the frame 18 and a lower surface 82 of the chip 50 is coplanar

with a lower surface **84** of the flex circuit **12** at the bottom of the frame **18**. This eliminates the thickness of that portion of the central or intermediate portion **38** of the flex circuit **12** which resides beneath the chip **50**, in the IC package **10**.

FIGS. **14** and **15** are top and bottom views, respectively, of a flex circuit **86** used in the IC package **80** of FIG. **13**. The flex circuit **86** is like the flex circuit **12** of the IC package **10**, except for the presence of a central aperture **88** therethrough. The flex circuit **86** is mounted on and glued to the frame **18** including the opposite ends **14** and **16** thereof in the manner previously described in connection with the IC package **10**. With the flex circuit **86** mounted on the frame **18** in this fashion, the resulting package is open to the bottom thereof through the central aperture **22** of the frame **18** and the central aperture **88** in the flex circuit **86**. To mount the chip **50** so that the lower surface **82** thereof is coplanar with the lower surface **84** of the flex circuit **12** at the frame **18**, a piece of Kapton tape **90** is placed across the lower surface **84** of the flex circuit **86** so as to cover the central aperture **88**. The chip **50** is then lowered into place onto the Kapton tape **90** and is electrically coupled such as by wire bonding to the flex circuit **86**. The epoxy **24** is then deposited over and around the chip **50**, in the manner previously described. When this is completed so as to mount the chip **50** within the central aperture **22** and the frame **18**, the Kapton tape **90** is removed.

FIGS. **16** and **17** are upper and lower perspective views, respectively, of a stackable flex circuit IC package **100** for a IC package of the type having conductive elements protruding therefrom, according to the present invention. FIG. **18** is a block diagram of the successive steps of a method of making the IC package **100**. FIGS. **19** and **20** are top and bottom views of a flex circuit **102** used in the IC package **100**. FIG. **21** is a perspective view of an IC device **104** which may be used in the IC package **100**. In the present example, the IC device **104** is a BGA device in the form of a μ BGA package having a matrix of balls **106** on a surface thereof. However, other BGA devices with protruding contacts, such as chip scale packages or flip chips, can be used in the IC package **100**.

FIG. **18** shows the successive steps of a method of making the IC package **100**. In a first step **110**, the flex circuit **102** shown in FIGS. **19** and **20** is formed. A layer of conductive metal, such as copper, is deposited on a thin flexible base **114** and is etched to form a conductive pattern **112**. The conductive pattern **112** of the flex circuit **102** includes a plurality of separated conductors **116**, in the manner of the flex circuit **12** of the IC package **10**. However, in the case of the flex circuit **102**, each of the conductors **116** is routed to one of an array or grid of apertures **118** formed so as to extend through the thin flexible base **114**. In addition, the conductive pattern **112** formed by the conductors **116** extends to four opposite end portions **120**, **122**, **124** and **126** of the thin flexible base **114**. The apertures **118** may be ablated through the thin flexible base **114** using a laser. After the apertures **118** are ablated with the laser, the copper of the conductors **116** reflects the laser, and is unaffected by the laser. The array or grid of apertures **118** corresponds to the balls **106** on the BGA device **104** so as to receive the balls **106** therein when the BGA device **104** is mounted on the flex circuit **102**, as described hereafter. Ablation of the holes or apertures **118** through the center portion of the thin flexible base **114** of the flex circuit **102** is set forth as a second step **128** in the method of FIG. **18**. In a following third step **130**, the BGA device **104** is provided.

In a fourth step **132** of the method of FIG. **18**, the array of balls **106** of the BGA device **104** are disposed in the

apertures **118** in the flex circuit **102** and are soldered to the conductive pattern **112** on the opposite side of the flex circuit **102**. This is accomplished by placing the BGA device **104** over the bottom surface of the flex circuit **102** shown in FIG. **20**, so that the balls **106** of the BGA device **104** extend through the apertures **118** and into contact with the conductive pattern **112** on the opposite side of the flex circuit **102**. Coating the balls **106** with solder paste or flux prior to placement of the chip package **104** on the flex circuit **102**, followed by the application of heat, effects soldering of the balls **106** to the conductive pattern **112**.

As previously described, the conductive pattern **112** is comprised of the individual conductors **116** as shown in FIG. **19**. With the BGA device **104** mounted on the flex circuit **102**, the individual balls **106** are soldered to contacts at the ends of the conductors **116**. In this manner, the BGA device **104** is electrically coupled to parts of the conductive pattern **112** at the end portions **120**, **122**, **124** and **126** of the thin flexible base **114** of the flex circuit **102**.

FIG. **22** shows the BGA device **104** as so mounted on the flex circuit **102** and with the balls **106** thereof soldered to the conductive pattern **112**. With the BGA device **104** thus mounted, a relatively small space **134** exists between a surface of the BGA device **104** and the flex circuit **102**. This is because the balls **106** are larger than the thickness of the flexible base **114**. In a fifth step **136** of the method of FIG. **18**, the space **134** is underfilled with epoxy. The underfilled epoxy **138** is shown in the sectional view of FIG. **25**.

As an alternative to soldering the balls **106** to the conductive pattern **112** and then underfilling with epoxy, an anisotropic adhesive can be used. The adhesive is spread on the flex circuit **102**, and the BGA device **104** is then placed thereon and cured. This connects the balls **106** to the circuit **102** and bonds the BGA device **104** to the flex circuit.

In a sixth step **140** of the method of FIG. **18**, a frame **142** is provided. The frame **142** has a central aperture **144** therein. As in the case of the frame **18** of the IC package **10**, the frame **142** may be made from heat resistant plastic. In a seventh step **146** of the method of FIG. **18**, the frame **142** is placed over the IC package **104** and is attached to the central portion of the flex circuit **102** with adhesive. This is shown in FIG. **24**.

In an eighth and final step **148** of the method of FIG. **18**, the end portions **120**, **122**, **124** and **126** of the thin flexible base **114** of the flex circuit **102** are folded over the frame **142** and are secured in place with adhesive, to complete the stackable flex circuit IC package **100**. The completed IC package **100** is shown in FIGS. **16** and **17**. All four of the opposite edge portions of the IC package **100** expose the conductive pattern **112** thereat, in preparation for electrical coupling thereof to the conductive pattern of an adjacent IC package **100** when a stack of the IC packages **100** is formed.

FIGS. **26** and **27** show a stack of two of the IC packages **100**. As in the case of the stack of FIG. **10** which is comprised of a pair of the IC packages **10**, the stack of FIGS. **26** and **27** employs conductive epoxy and the application of pressure to form vertical or Z-axis conductive paths between the conductors **116** of adjacent portions of the conductive patterns of the IC packages **100**. The conductive epoxy is applied to the conductive pattern **112** at each of the end portions **120**, **122**, **124** and **126** of the thin flexible base **114** of the conductive pattern **112**.

FIG. **28** is a sectional view of a portion of the stack of IC packages **100** shown in FIGS. **26** and **27**. As shown in FIG. **28**, a quantity of conductive epoxy **150** is placed between adjacent portions of the IC packages **100**. Upon application

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of heat and pressure to the epoxy, vertical or Z-axis conductive pads are formed between the conductors 116 within the adjacent conductive patterns 112 of the IC packages 100. As shown in FIG. 28, conductive balls 152 may be soldered to portions of the conductive pattern 112 opposite the balls 106 of the IC package 104 in a lowermost one 154 of the IC packages 100. This facilitates mounting and electrical inter-connection of the stack of FIGS. 26 and 27 on a substrate board.

FIG. 29 is a sectional view of a variation of the stackable flex circuit IC package 100 in which the frame 142 is eliminated. This arrangement is particularly useful in cases where the IC device 104 is relatively large and the opposite top and bottom surfaces thereof are parallel. In such instances, the opposite edges of the IC device 104 function as the frame, with the end portions 120, 122, 124 and 126 of the thin flexible base 114 of the conductive pattern 112 being folded over and secured by adhesive thereto. The central portion of the flex circuit 102 is provided with the apertures 118 in the manner previously described, so that the balls 106 of the BGA device 104 are soldered to the conductive pattern 112 upon mounting of the IC package 104. The space between the flex circuit 102 and the BGA device 104 is underfilled with epoxy in the manner previously described.

The arrangement of FIG. 29 is best employed in cases where the opposite surfaces of the IC device are parallel to each other. For non-parallel surfaces, a frame can be molded to fit the chip, and is used in forming the IC package.

While the stackable flex circuit IC packages described herein have a single IC device mounted therein, it will be apparent that packages can be assembled with more than one IC device therein. In such instances, the plural IC devices can be interconnected using multilayered flex circuits. Also, transposer layers can be made as an integral part of the flex circuit of each carrier or as separate boards between carriers when stacking carriers.

While the invention has been shown with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention.

I claim:

1. A stackable integrated circuit chip package, comprising:

a flex circuit comprising:

a flexible base; and

a conductive pattern disposed on the flexible base;

a frame defining a central opening and opposed top and bottom surfaces, the flex circuit being wrapped around at least a portion of and secured to the frame such that the, conductive pattern defines a first portion which extends over a portion of the bottom surface of the frame and a second portion which extends over a portion of the top surface of the frame; and

an integrated circuit device disposed within the opening of the frame and secured to the flexible base of the flex circuit, the integrated circuit device being electrically connected to the conductive pattern;

the first and second portions of the conductive pattern each being electrically connectable to another component.

2. The chip package of claim 1 further in combination with a second stackable integrated circuit chip package identically configured to the chip package, the first portion of the conductive pattern of the second chip package being electrically connected to the second portion of the conductive pattern of the chip package to form a chip stack.

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3. The chip stack of claim 2 wherein the first portion of the conductive pattern of the second chip package is electrically connected to the second portion of the conductive pattern of the chip package through the use of an anisotropic conductive epoxy.

4. The chip package of claim 1 wherein:

the integrated circuit device comprises a bare die; and the bare die is electrically connected to the second portion of the conductive pattern via at least one conductive wire.

5. The chip package of claim 4 wherein:

the top surface of the frame defines at least one ramp which is recessed relative to the remainder thereof;

a portion of the second portion of the conductive pattern extends over the ramp; and

the bare die is electrically connected via the conductive wire to the portion of the second portion of the conductive pattern which extends over the ramp.

6. The chip package of claim 5 further comprising a potting compound encapsulating the bare die and the at least one conductive wire within the central opening of the frame.

7. The chip package of claim 1 wherein:

the integrated circuit device comprises a BGA device including a body having an array of contacts disposed thereon;

the flexible base of the flex circuit includes a plurality of apertures extending therethrough to the first portion of the conductive pattern; and

the contacts of the BGA device are disposed within respective ones of the apertures and electrically connected to the first portion of the conductive pattern.

8. The chip package of claim 7 wherein the contacts are electrically connected to the first portion of the conductive pattern via solder.

9. The chip package of claim 7 further comprising a potting compound underfilling a gap defined between the body of the BGA device and the flexible base of the flex circuit.

10. The chip stack of claim 1 wherein the flexible base extends across and completely covers one end of the central opening within the frame.

11. A chip stack comprising:

at least first and second stackable integrated circuit chip packages, each of which comprises:

a flex circuit comprising:

a flexible base; and

a conductive pattern disposed on the flexible base; a frame defining a central opening, the flex circuit being wrapped around at least a portion of and secured to the frame such that the conductive pattern defines a first portion which extends over a portion of the bottom surface of the frame and a second portion which extends over a portion of the top surface of the frame; and

an integrated circuit device disposed within the opening of the frame and secured to the flexible base of the flex circuit, the integrated circuit device being electrically connected to the conductive pattern;

the first portion of the conductive pattern of the second chip package being electrically connected to the second portion of the conductive pattern of the first chip package.

12. The chip stack of claim 11 wherein the first portion of the conductive pattern of the first chip package is electrically connected to the second portion of the conductive pattern of the second chip package-via an anisotropic epoxy.

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13. The chip stack of claim 11 wherein the second chip package includes a plurality of contacts on the first portion of the conductive pattern thereof to facilitate electrical connection to a substrate board.

14. A stackable integrated circuit chip package, comprising: 5

a flex circuit comprising:

a flexible base having a central aperture therein; and
a conductive pattern disposed on the flexible base;

a frame defining a central opening and opposed top and bottom surfaces, the flex circuit being wrapped around at least a portion of and secured to the frame such that the conductive pattern defines a first portion which extends over a portion of the bottom surface of the frame and a second portion which extends over a portion of the top surface of the frame; and 10

an integrated circuit device disposed within the central aperture of the flexible base and the central opening of the frame, the integrated circuit device being electrically connected to the conductive pattern; 15

the first and second portions of the conductive pattern each being electrically connectable to another component.

15. The chip package of claim 14 further in combination with a second stackable integrated circuit chip package identically configured to the chip package, the first portion of the conductive pattern of the second chip package being electrically connected to the second portion of the conductive pattern of the chip package to form a chip stack. 20

16. The chip stack of claim 15 wherein the first portion of the conductive pattern of the second chip package is electrically connected to the second portion of the conductive pattern of the chip package through the use of an anisotropic conductive epoxy. 25

17. The chip package of claim 14 wherein:

the integrated circuit device comprises a bare die; and

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the bare die is electrically connected to the second portion of the conductive pattern via at least one conductive wire.

18. The chip package of claim 17 wherein:

the top surface of the frame defines at least one ramp which is recessed relative to the remainder thereof;

a portion of the second portion of the conductive pattern extends over the ramp; and

the bare die is electrically connected via the conductive wire to the portion of the second portion of the conductive pattern which extends over the ramp.

19. The chip package of claim 18 further comprising a potting compound partially encapsulating the bare die and the at least one conductive wire within the central aperture of the flexible base and the central opening of the frame.

20. A stacked integrated circuit module comprising:

a first ball grid array package having a first major surface and a second major surface and emergent from the second major surface there being a first matrix of balls, the first ball grid array package containing an integrated circuit chip; 25

a second ball grid array package having a first major surface and a second major surface and containing an integrated circuit chip, the second ball grid array package being disposed in a stacked disposition above the first ball grid array package;

a flex circuit connected on one side to the first matrix of balls of the first ball grid array package and connected on the other side to a second matrix of balls for the module the flex circuit further comprising a first portion and a second portion with the first and second portions being coplanarly disposed above the first major surface of the first ball grid array package and below the second major surface of the second ball grid array package, the first and second portions being electrically connected to the second ball grid array package. 30

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : RE 39,628 E
APPLICATION NO. : 10/900073
DATED : May 15, 2007
INVENTOR(S) : Harlan R. Isaak

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page, Item (73) Assignee: please change "Stakick Group, L.P." to --Staktek Group L.P.--

Signed and Sealed this

Third Day of July, 2007

A handwritten signature in black ink on a light gray dotted background. The signature reads "Jon W. Dudas" in a cursive style.

JON W. DUDAS

Director of the United States Patent and Trademark Office