US00RE38820E

(19) **United States**

(12) **Reissued Patent**

Dejager et al.

(10) **Patent Number: US RE38,820 E**

(45) **Date of Reissued Patent: Oct. 11, 2005**

(54) **MULTI-PROTOCOL PACKET FRAMING OVER AN ISOCHRONOUS NETWORK**

(75) Inventors: **Gregory L. Dejager**, San Jose, CA (US); **Erik R. Swenson**, San Jose, CA (US)

(73) Assignee: **Negotiated Data Solutions LLC**, Chicago, IL (US)

(21) Appl. No.: **09/285,303**

(22) Filed: **Jul. 2, 1998**

Related U.S. Patent Documents

Reissue of:

(64) Patent No.: **5,533,018**
Issued: **Jul. 2, 1996**
Appl. No.: **08/361,603**
Filed: **Dec. 21, 1994**

(51) **Int. Cl.**[7] **H04L 12/52**

(52) **U.S. Cl.** **370/352**; 370/395.5

(58) **Field of Search** 370/352, 395.5, 370/403, 461, 465

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,619,505	A	11/1971	Melle	375/110
3,835,260	A	9/1974	Prescher et al.	379/237
3,988,716	A	10/1976	Fletcher et al.	370/100.1
4,150,404	A	4/1979	Tercic et al.	380/22
4,220,816	A	9/1980	Howells et al.	370/24

(Continued)

FOREIGN PATENT DOCUMENTS

EP	0131662	1/1985
EP	0318332	5/1989
JP	A1254035	10/1989
JP	A1297926	12/1989
JP	A5175977	7/1993
WO	WOA88055233	7/1988
WO	WOA8911183	11/1989

OTHER PUBLICATIONS

U.S. Appl. No. 07/969,916 filed Nov. 1992 to Edem et al.*

"ISO/IEC 3309" International Standard, reference No. ISO/IEC 3309:1991(E), 1991 6 pgs.*

"ATM User–Network Interface Specification: Version 3.0", Technical Committee of the ATM Forum, pp. iii–103.*

"IEEE Standards For Local & Metropolitan Area Networks", Prepared by IEEE 802.9a Editor, unapproved IEEE Standards Draft, Jul. 25, 1994, pp. i–289.*

(Continued)

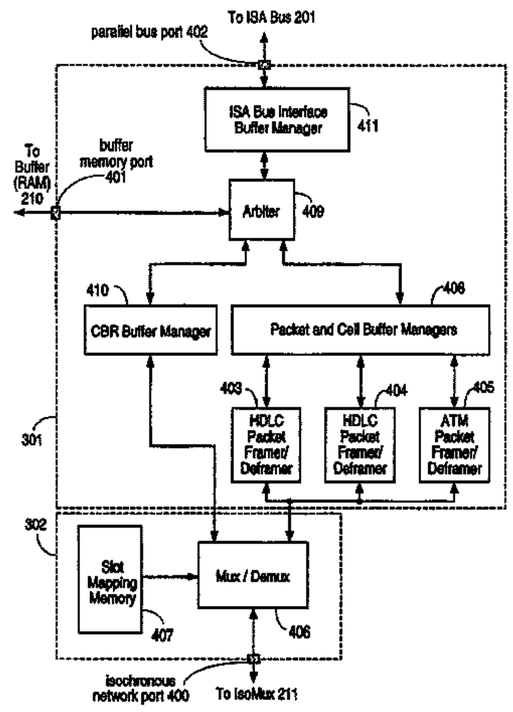
Primary Examiner—Salvatore Cangialosi

(74) *Attorney, Agent, or Firm*—Loudermilk & Associates

(57) **ABSTRACT**

An integrated circuit has an isochronous network port for receiving isochronous information from an isochronous network. To allow the integrated circuit to receive information packaged in accordance with two different packaging protocols (for example, HDLC and ATM), the integrated circuit includes a first framer/deframer circuit for deframing information packaged in accordance with a first packaging protocol (for example, HDLC) and a second framer/deframer circuit for deframing information packaged in accordance with a second packaging protocol (for example, ATM). A circuit switch is provided to cause incoming data to be deframed by the appropriate framer/deframer circuit depending on which slot of the network frame contained the information. Once deframed, a buffer manager controls storing of the information in a circular ring buffer in an external memory. A device residing on a host bus coupled to the integrated circuit may then read the information from the circular ring buffer via a parallel bus port of the integrated circuit. Information may also pass in the opposite direction from the parallel bus port, through a buffer memory port to the buffer memory, and from the buffer memory through the buffer memory port, through an appropriate framer/deframer circuit, through the isochronous network port, and onto the network.

97 Claims, 4 Drawing Sheets



U.S. PATENT DOCUMENTS

4,258,434	A	3/1981	Glowinski et al.	370/60
4,347,527	A	8/1982	Lainez	358/310
4,359,770	A	11/1982	Suzuka	370/105.3
4,412,324	A	10/1983	Glowinsky et al.	370/58.1
4,419,765	A	12/1983	Wycoff et al.	455/38.3
4,429,405	A	1/1984	Bux et al.	375/89
4,445,213	A	4/1984	Baugh et al.	370/94.1
4,449,248	A	5/1984	Leslie et al.	455/38.3
4,472,802	A	9/1984	Pin et al.	370/108
4,484,218	A	11/1984	Boland et al.	358/86
4,530,088	A	7/1985	Hamstra et al.	370/110.1
4,543,652	A	9/1985	Amada et al.	370/66
4,547,880	A	10/1985	De Vita et al.	370/67
4,549,292	A	10/1985	Isaman et al.	370/85.15
4,556,970	A	12/1985	Flanagin et al.	370/60
4,577,312	A	3/1986	Nash	370/84
4,577,315	A	3/1986	Otsuka	455/38.3
4,580,276	A	4/1986	Andruzzi, Jr. et al.	375/269
4,587,650	A	5/1986	Bell	340/825.05
4,637,014	A	1/1987	Bell et al.	340/825.05
4,656,592	A	4/1987	Spaanenburg et al.	364/490
4,674,082	A	6/1987	Flanagin et al.	370/60
4,677,611	A	6/1987	Yanosy, Jr. et al.	370/85
4,715,002	A	12/1987	Vernon et al.	364/422
4,726,018	A	2/1988	Bux et al.	370/85.5
4,759,010	A	7/1988	Murata et al.	370/66
4,766,590	A	8/1988	Hamada et al.	370/56
4,766,591	A	8/1988	Huang	370/60
4,769,813	A	9/1988	Lenart	370/60
4,771,417	A	9/1988	Maxwell et al.	370/296
4,771,426	A	9/1988	Rattlingourd et al.	375/120
4,782,485	A	11/1988	Gollub	370/118
4,800,560	A	1/1989	Aoki et al.	370/108
4,807,224	A	2/1989	Naron et al.	370/94.1
4,811,367	A	3/1989	Tajika	370/108
4,825,435	A	4/1989	Admundsen et al.	370/85.1
4,837,799	A	6/1989	Prohs et al.	379/224
4,845,609	A	7/1989	Lighthart et al.	395/275
4,847,613	A	7/1989	Sakurai et al.	340/825.21
4,858,232	A	8/1989	Diaz et al.	370/85.7
4,866,704	A	9/1989	Bergman	370/85.4
4,872,157	A	10/1989	Hemmady et al.	370/60
4,876,683	A	10/1989	Suzuki	370/97
4,897,831	A	1/1990	Negi et al.	370/296
4,907,260	A	3/1990	Prohs et al.	379/224
4,920,483	A	4/1990	Pogue et al.	395/425
4,930,127	A	5/1990	Abaziou et al.	370/110.4
4,931,250	A	6/1990	Greszczuk	375/8
4,954,988	A	9/1990	Robb	365/189.02
4,959,774	A	9/1990	Davis	364/200
4,961,188	A	10/1990	Lau	370/94.2
4,964,121	A	10/1990	Moore	370/100.1
4,977,582	A	12/1990	Nichols et al.	375/118
4,985,891	A	1/1991	Fujiwara et al.	370/110.1
4,993,026	A	2/1991	Yamashita	370/100.1
5,001,707	A	3/1991	Kositpaiboon et al.	370/94.1
5,007,045	A	4/1991	Tsuzuki	370/94.1
5,014,247	A	5/1991	Albachten, III et al.	365/230.05
5,018,136	A	5/1991	Gollub	370/60.1
5,020,058	A	5/1991	Holden et al.	370/109
5,020,132	A	5/1991	Nazarenko et al.	455/17
5,041,924	A	8/1991	Blackborow et al.	360/69
5,058,110	A	10/1991	Beach et al.	370/85.6
5,065,398	A	11/1991	Takashima	370/94.1
5,067,149	A	11/1991	Schneid et al.	379/224
5,084,872	A	1/1992	Le Cucq et al.	370/85.1
5,095,494	A	3/1992	Takahashi et al.	375/10
5,103,446	A	4/1992	Fischer	370/85.1
5,119,373	A	6/1992	Fredricsson et al.	370/85.15
5,121,382	A	6/1992	Yang et al.	370/296
5,128,930	A	7/1992	Nazarenko et al.	370/60
5,134,611	A	7/1992	Steinka et al.	370/79
5,138,440	A	8/1992	Radice	370/110.1
5,140,587	A	8/1992	Mueller et al.	370/85.15
5,146,455	A	9/1992	Goke et al.	370/66
5,163,148	A	11/1992	Walls	395/600
5,164,938	A	11/1992	Jurkevich et al.	370/60
5,179,554	A	1/1993	Lomicka et al.	370/85.13
5,189,414	A	2/1993	Tawara	340/825.5
5,200,952	A	4/1993	Bernstein et al.	370/79
5,202,899	A	4/1993	Walsh	375/8
5,206,863	A	4/1993	Nazarenko et al.	371/37.1
5,208,807	A	5/1993	Gass et al.	370/60.1
5,212,724	A	5/1993	Nazarenko et al.	371/37.1
5,214,648	A	5/1993	Lespagnol et al.	370/85.15
5,229,998	A	7/1993	Weisser	370/108
5,251,207	A	10/1993	Abensour et al.	370/60.1
5,283,786	A	2/1994	Hoff et al.	379/85.13
5,305,306	A	4/1994	Spinney et al.	370/296
5,305,317	A	4/1994	Szczepanek	370/85.5
5,311,114	A	5/1994	Sambamurthy et al.	370/296
5,315,588	A	5/1994	Kajiwara et al.	370/60.1
5,361,261	A	11/1994	Edem et al.	370/85.3
5,375,121	A	12/1994	Nishino et al.	370/94.2
5,410,535	A	4/1995	Yang et al.	370/13
5,453,984	A	9/1995	Mueller	370/85.13
5,504,738	A	4/1996	Sambamurthy et al.	370/296
5,533,018	A	7/1996	DeJager et al.	370/60.1
5,594,734	A	1/1997	Worsley et al.	370/395
5,648,956	A	7/1997	Sambamurthy et al.	370/296
5,761,292	A	6/1998	Wagner et al.	379/93.09

OTHER PUBLICATIONS

A disclosure of a communication system was presented at the IEEE 802.9, Standards Meeting on Nov. 8–12, 1992. The pages entitled: "Multi–Media Applications are Ready".

"ATM Overview," National Semiconductor Corp., ATM Overview F–Fred Device, Aug. 1993, entire booklet.

"DP839XX Isochronous Time Slot Exchanger (IsoTSX™)," Revision 0.8, bearing the date Oct. 29, 1992 and DP839XX Isochronous Ethernet Physical Layer isoPHY™ Revision 1.1, bearing the date Oct. 1992, were disclosed to IBM.

DP839XX Isochronous Ethernet Physical Layer Iso–PHY™, Revision 2.1, bearing the date Dec. 1992 and DP839XX Isochronous Time Slot Exchanger, Revision 1.0, bearing the date Dec. 13, 1992, were disclosed to IBM and Ericsson.

DP839XX Isochronous Ethernet Physical Layer Iso–PHY™, Revision 3.0, bearing the date Dec. 1992 and Isochronous Time Slot Exchanger (IsoTSX™ Workbook, Revision 1.2, bearing the date Feb. 16, 1993, was disclosed to Luxcom, Inc. of Fremont, California.

"DP8390 Network Interface Controller: An Introductory Guide", Local Area Network Databook, National Semiconductor Corp., pp. 1–206 to 1–213, 1992 Edition.

"DP83950A Repeater Interface Controller," Local Area Network Databook, National Semiconductor Corp., pp. 3–3 to 3–73, 1992 Edition.

DP83950EB at IEEE 802.3, Multi–Port Repeater Evaluation Kit, Local Area Network Databook, National Semiconductor Corp., pp. 75–87, 1992 Edition.

"DP83932B Systems–Oriented Network Interface Controller", Local Area Network Databook, National Semiconductor Corp., pp. 1–288 to 1–383, 1992 Edition.

"Exchangeable Card Architecture Specification," Release 1.00, bearing the date Dec. 20, 1991, pp. 7, 20 and 22.

"Fiber Distributed Data Interface (FDDI)—Token Ring Media Access Control (MAC)," American National Standard for Information System—Document ANSI X3.139, 1987.
Gallagher, C.A., "IEEE 802.9: A Multi–Service Lan Interface," Second IEEE National Conference on Telecommunications, Apr. 1989, York GB, pp. 173–178.
HMUX ERS "FDDI–II Hybrid Multiplexor (HMUX)," Rev. 2.4, Mar. 25, 1991.
IBM—On or about Nov. 1, 1991, IBM Corporation provided a "Task Order and appendix". A copy of pp. 6 and 7 of the Task Order and appendix titled, Isoethernet Project Local Cluster Controller Version 1.2.
"IBM's Multimedia Venture: Oppurtunity for its Hardware?," vol. 38, No. 1930, p. 1, Sep. 21, 1992.
"IEEE 802.3, Draft Supplement to IEEE Std 802.3 DSMA/CD Access Method and Physical Layer Specifications," Institute of Electrical and Electronics, Nov. 15, 1989.
"IEEE 802.9, Draft Standard Integrated Services (IS) LAN Interface at the MAC and PHY Layers," Institute of Electrical and Electronics, Nov. 1992.
"Integrated PBX Systems, An NCC State of the Art Report," The National Computer Centre Limited, 1987.
Irube et al., "Integrated Information and Communication System for Business Networks," Hitachi Review 40(3):241–247, 1991.
"ISDN Basic Rate Interface System Design Guide," Telenetworks document, Aug. 1989.
"ISDN Primary Rate Interface System Design Guide," Telenetworks document, Jul. 1989.
"IsoEnet Transforms LANs and WANs Into Interactive Multimedia Tools," Brian Edem et al., Computer Technology Review, Winter 1992, 3 pgs. "ISO/IEC 3309" International Standard, ref. No. ISO/IEC 3309; 1991 (E), 1991, 7 pgs.
"Local Area Network Databook" published by National Semiconductor, pp. 1–3 to 1–9, 1–242 to 1–248, 5–3 to 5–7.
Martini et al., "Real–Time Traffic in FDDI–II, Packet Switching vs. Circuit Switching," IEEE Infocom 1991, vol. 3, Apr. 1991, Bal Harbour, U.S., pp. 1413–1420.
"National Proposes Isochronous Ethernet," *Electronic News*, vol. 38, No. 1940, p. 19, Nov. 30, 1992.
"PCMCIA Socket Services Interface Specification," Draft 2.00b, bearing the date Jul. 17, 1992.
Ross, F.E. et al., FDDI—A Lan Among Mans, Computer Communications Review, vol. 20, No. 3, Jul. 1990, New York, U.S., pp. 16–31.
Shimizu, H. et al., "IVDLAN Standardization and Development," IEICE Transactions, vol. E74, No. 9, Sep. 1991, Tokyo, JP, pp. 2696–2702.
"Token–Ring Network Architecture Reference," pp. 5–1 through 5–28 and pp. 5–10 and 5–17.
"VersaNet™ An Ethernet Extension for Isochronous Communications," bearing the date Aug. 14, 1992 is a paper sent to National Semiconductor Corp. from Condor Systems, Inc. of San Jose, CA on Aug. 18, 1992.
Wirbel, Loring, "Scheme for Fast Ethernet Proposed," appears to be a newspaper article; date of article is uncertain, but is believed to be prior to Mar. 1993.
Wong, David., "Second Generation 10Base T Silicon Solutions," IRE Wescon Convention Record, vol. 35, Nov. 1991, No. Hollywood, Ca. pp. 238–242.

* cited by examiner

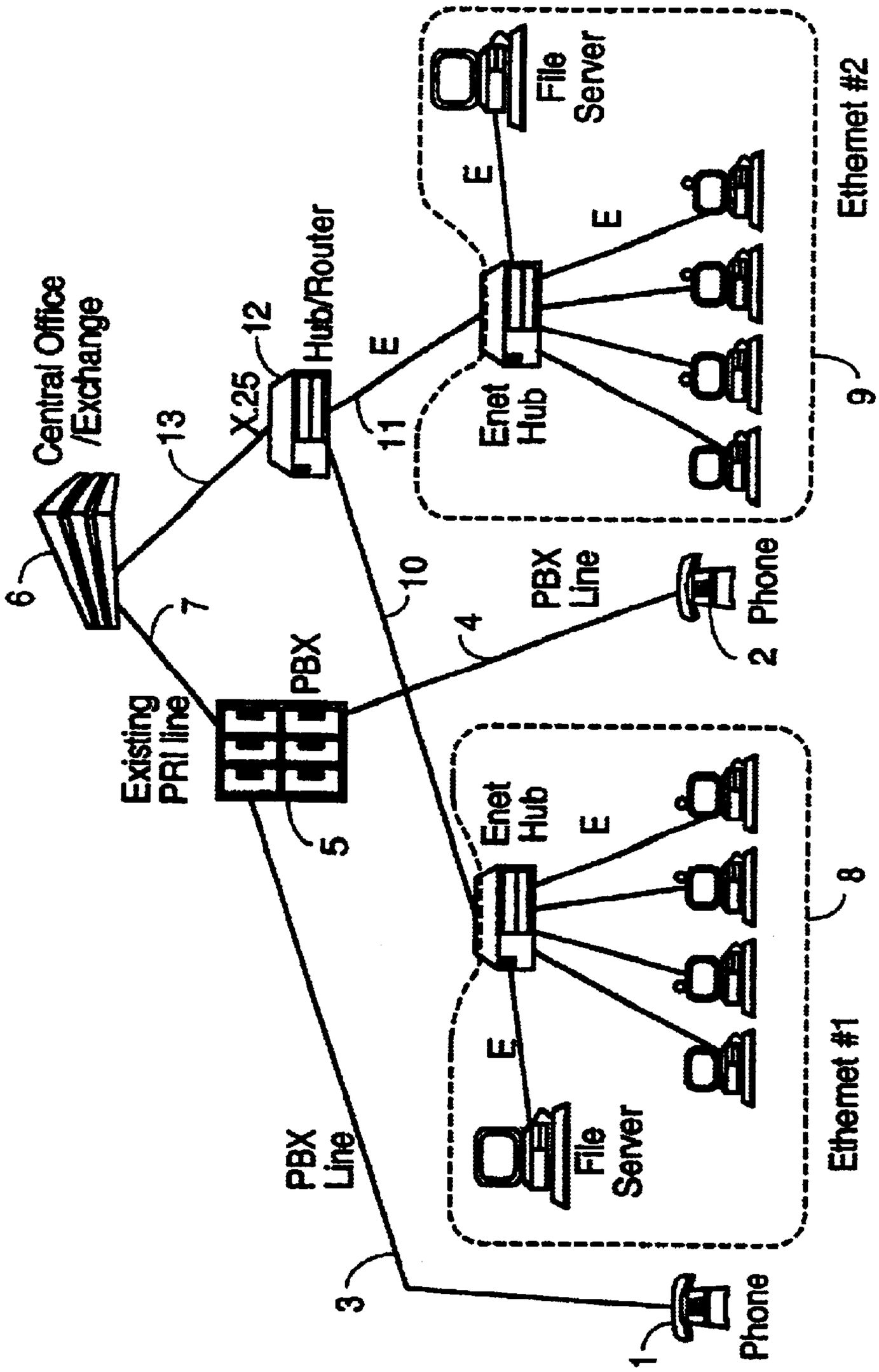


FIG. 1
(Prior Art)

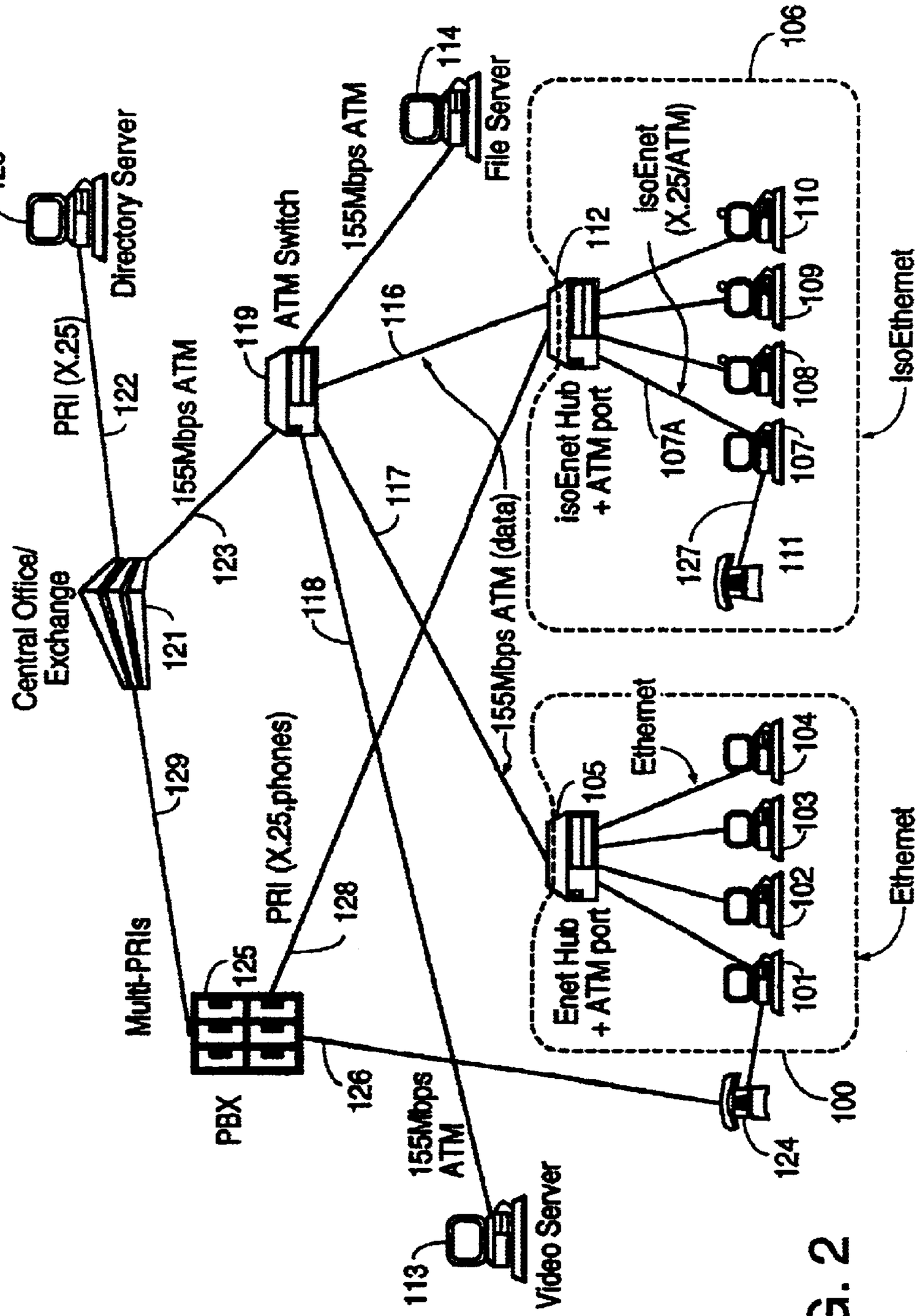

120
Directory Server
PRI (X.25)
122
Central Office/
Exchange
121
Multi-PRIs
129
125
PBX
126
155Mbps ATM
123
155Mbps ATM
119
ATM Switch
114
File Server
116
117
118
PRI (X.25,phones)
128
155Mbps ATM (data)
155Mbps
ATM
113
Video Server
106
112
IsoEnet
(X.25/ATM)
110
109
108
107A
107
127
111
isoEnet Hub
+ ATM port
IsoEthernet
105
Ethernet
104
103
102
101
Enet Hub
+ ATM port
Ethernet
124
100

FIG. 2

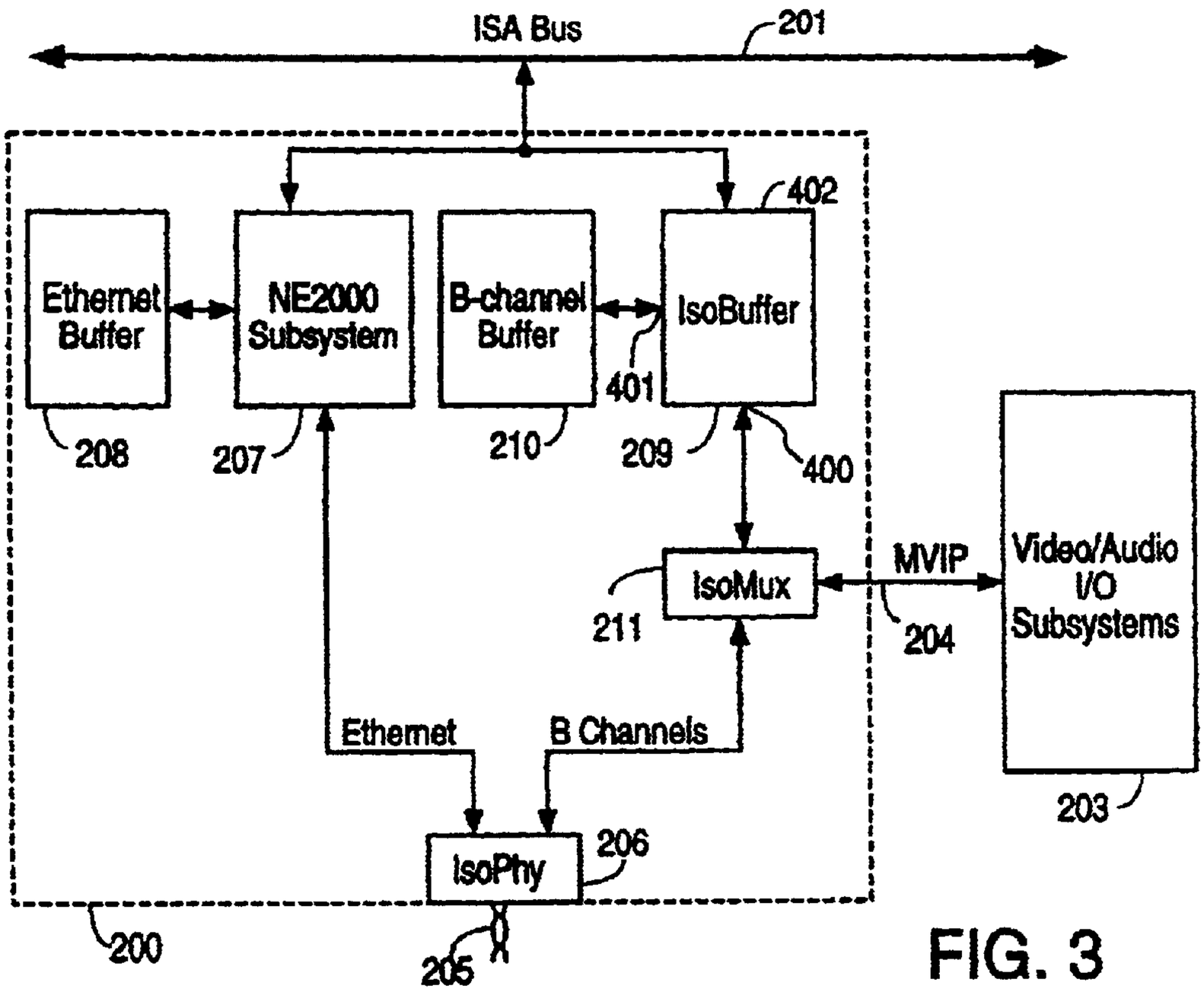

ISA Bus
201
402
Ethernet Buffer
NE2000 Subsystem
B-channel Buffer
IsoBuffer
401
208
207
210
209
400
IsoMux
211
MVIP
204
Video/Audio I/O Subsystems
203
Ethernet
B Channels
IsoPhy
206
200
205

FIG. 3

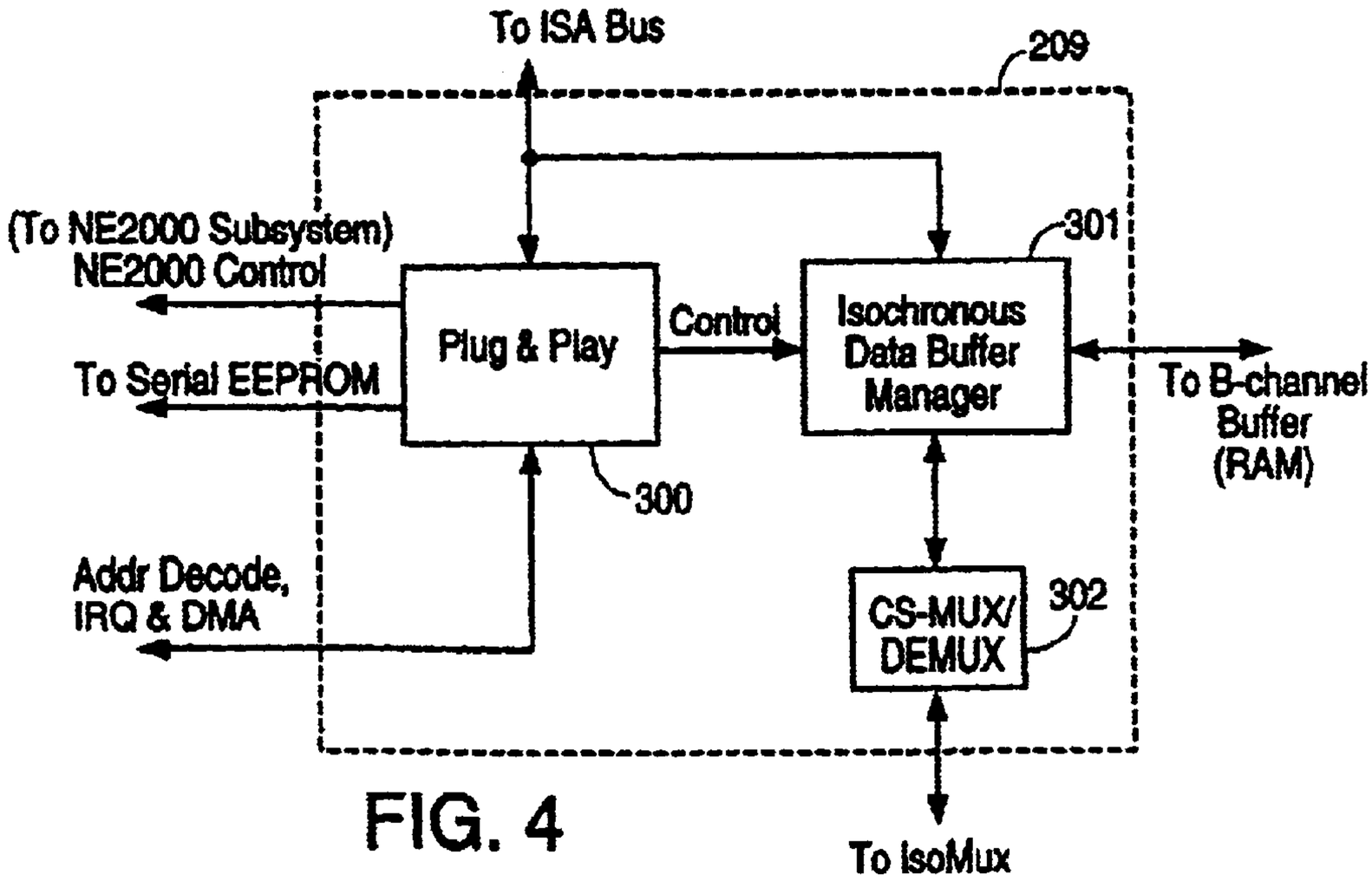

To ISA Bus
209
(To NE2000 Subsystem)
NE2000 Control
301
Plug & Play
Control
Isochronous Data Buffer Manager
To Serial EEPROM
To B-channel Buffer (RAM)
300
Addr Decode, IRQ & DMA
CS-MUX/ DEMUX
302
To IsoMux

FIG. 4

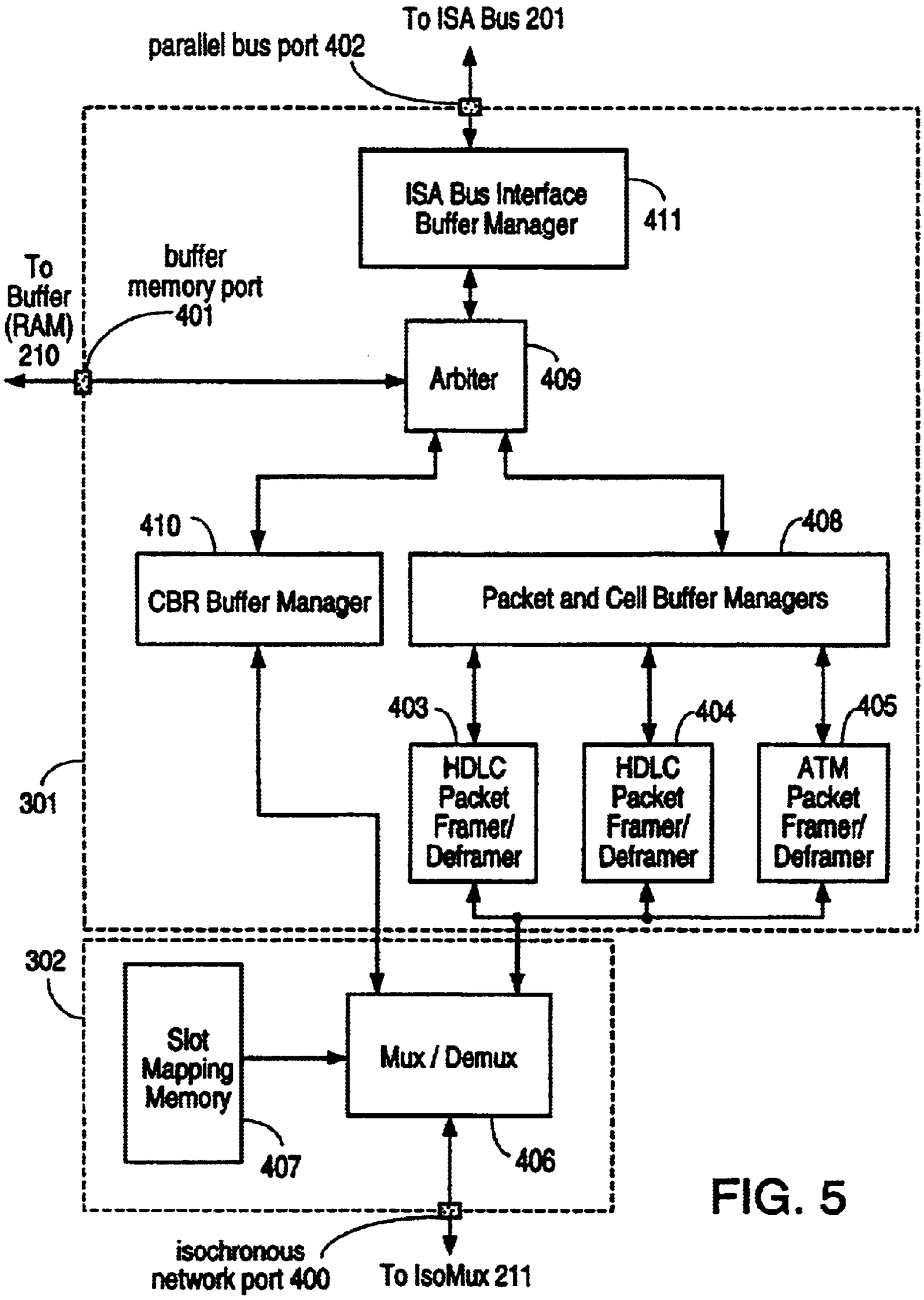

To ISA Bus 201
parallel bus port 402
ISA Bus Interface Buffer Manager
411
To Buffer (RAM) 210
buffer memory port 401
Arbiter
409
410
CBR Buffer Manager
408
Packet and Cell Buffer Managers
403
404
405
HDLC Packet Framer/ Deframer
HDLC Packet Framer/ Deframer
ATM Packet Framer/ Deframer
301
302
Slot Mapping Memory
407
Mux / Demux
406
isochronous network port 400
To IsoMux 211

FIG. 5

MULTI-PROTOCOL PACKET FRAMING OVER AN ISOCHRONOUS NETWORK

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

CROSS REFERENCE TO MICROFICHE APPENDIX

The microfiche appendix, which is a part of the present disclosure, entails one sheet of microfiche having a total of ninety-two (92) frames. The microfiche appendix contains RTL code and schematics of a specific embodiment of an integrated circuit in accordance with the present invention. A portion of the disclosure of this patent document contains material which is subject to copyright protection. The copyright owner has no objection to the facsimile reproduction by anyone of the patent document or the patent disclosure, as it appears in the Patent and Trademark Office patent files or records, but otherwise reserves all copyright rights whatsoever.

FIELD OF THE INVENTION

This invention relates to isochronous networks.

BACKGROUND INFORMATION

Ethernet is a well known network protocol. See the IEEE specification 802.3 (the subject matter of which is incorporated herein by reference) for further background information on Ethernet. Ethernet is well suited for transferring large packets of information at spaced intervals. Information may, for example, be accumulated into a large packet and then sent in a relatively large packet from one Ethernet node to another Ethernet node. Ethernet can therefore be said to be a "bursty" network protocol.

Some types of information, such as the information in a typical telephone conversation, do not lend themselves to being accumulated over time and then being transmitted as a single large packet. In a telephone conversation, speech information should be passed from speaker to listener without significant delay because the listener may use that speech information to formulate a response. Accordingly, there is not time for large packets of information to be accumulated. Frequent transmissions of small packets of information over the network is required. Ethernet is not well suited to this "nonbursty" type of information transfer.

There are, however, communication protocols (called isochronous protocols) which are suited for communication of such "nonbursty" information. Circuit switching and time division multiplexing (TDM) techniques are employed to divide a communication medium into a number of consecutive frames, each frame including a number of time slots. A first telephone conversation may, for example, be allocated a first slot of each frame whereas a second telephone conversation may be allocated a second slot of each frame. Because telephone information for each conversation is received each frame, the "nonbursty" information of the telephone conversations is communicated without significant delay.

Isochronous networks may also be made to carry "bursty" information. Telephone companies use an information framing protocol known as "HDLC" to frame information ("bursty" and/or "nonbursty") for isochronous communication over a standard digital telephone line (an example of

which is Primary Rate ISDN or "PRI"). HDLC is part of a more encompassing protocol called "X.25" See the document ISO/IEC 3309, 1991 (the subject matter of which is incorporated herein by reference) for additional information on the HDLC protocol.

FIG. **1** (Prior Art) shows an interconnection of networks. Telephone information passes to and from telephones **1** and **2** over PBX (Private Branch Exchange) lines **3** and **4**, respectively, to a local PBX **5**. The local PBX **5** is coupled to a central office/exchange **6** (typically operated by a telephone company) via one or more PRI lines **7**. "Nonbursty" telephone conversation information passes over this structure.

"Bursty" information such as video information and large computer files, on the other hand, passes over another structure. A first Ethernet network **8** having a plurality of workstations and a file server and an Ethernet hub is coupled to a second Ethernet network **9** via two Ethernet lines **10**, **11** and an Ethernet hub/router **12**. The file server of a network may, for example, store video data which can be accessed and displayed by the workstations of the network. Lines **10** and **11** are logically two different Ethernet lines. Hub/router **12** is coupled to the central office/exchange **6** via an isochronous link **13** such as a PRI line. Information is passed over link **13** using the HDLC protocol. The dots on selected workstations indicate video cameras.

A video camera of a workstation in the first Ethernet network can therefore capture video information and store that information in the file server of the first Ethernet network **8**. A workstation in the second Ethernet network **9** can then access that information over Ethernet lines **10** and **11** via hub/router **12** and display that information. A workstation can also receive HDLC packaged "bursty" information (such as the yellow pages in graphic form) from the central office/exchange **6** via isochronous link **13**.

There exists, however, another information packaging protocol known as asynchronous transfer mode (hereinafter "ATM"). See the document "ATM User-Network Interface Specification", Version 3.0 (the subject matter of which is incorporated herein by reference) for additional information on the ATM protocol. Although it is envisioned that ATM will eventually replace HDLC, it is likely that significant numbers of ATM and HDLC data communication services will coexist for a significant period of time. It would therefore be desirable to provide network node hardware capable of both ATM and HDLC communication. Furthermore, a user using the structure of FIG. **1** would likely have a telephone on his/her desk in addition to a workstation. Accordingly, a PBX line would extend onto the user's desk for coupling to the telephone and an Ethernet line would also extend onto the user's disk for coupling to the workstation. It would be desirable to eliminate one of these two lines so that the workstation could receive both "bursty" Ethernet information and "nonbursty" telephone information over a single line.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** (Prior Art) is a diagram showing an interconnection of Ethernet networks.

FIG. **2** is a diagram showing an isoENET network coupled to an Ethernet network in accordance with an embodiment of the present invention.

FIG. **3** is a simplified block diagram of an expansion card for coupling an ISA parallel bus to an isochronous network in accordance with an embodiment of the present invention.

FIG. **4** is a simplified block diagram of an integrated circuit disposed on the expansion card of FIG. **3** in accordance with an embodiment of the present invention.

FIG. **5** is a more detailed block diagram illustrating a part of the integrated circuit of FIG. **4** in accordance with an embodiment of the present invention.

SUMMARY

An integrated circuit has an isochronous network port for receiving isochronous information from an isochronous network. To allow the integrated circuit to receive information packaged in accordance with two different packaging protocols (for example, HDLC and ATM), the integrated circuit includes a first protocol packet framer/deframer circuit for deframing information packaged in accordance with a first packaging protocol (for example, HDLC) and a second protocol packet framer/deframer circuit for deframing information packaged in accordance with a second packaging protocol (for example, ATM). A circuit switch is provided to steer incoming information to the appropriate packet framer/deframer circuit depending on which slot of the network frame carried the information.

In some embodiments, the information received from the network is stored in an external memory after being deframed. A buffer manager circuit may be provided on the integrated circuit to manage a circular inbound ring buffer of information in the external memory. A device, such as a CPU, residing on a host bus coupled to the integrated circuit may then read the information stored in the circular ring buffer via a parallel bus port of the integrated circuit. An arbiter circuit on the integrated circuit determines whether information from the framer/deframer circuit will be written to the external memory or whether the device on the host bus will read information from the external memory. In some embodiments, the integrated circuit includes a slot mapping memory which contains a map of which packet framer/deframer should be used for which slot. The slot mapping memory can be programmed from the host bus of the integrated circuit via the parallel bus port.

If information from the host bus is to be transmitted over the network, the information is written into the external buffer memory via the parallel bus port and the buffer memory port. The information is then framed by the appropriate packet framer/deframer circuit and is supplied to the isochronous network port of the integrated circuit via the circuit switch. The buffer manager circuit of the integrated circuit determines how the information is written into an outbound buffer of the external memory from the host parallel bus port and how that information is later read out of the outbound buffer and supplied to the packet framer/deframer circuit. The arbiter determines whether information received from the parallel bus port will be written into the external memory or whether information from the external memory will be supplied to the packet framer/deframer circuit for framing and transmission on the isochronous bus.

Other associated structures and methods are also disclosed.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

An isochronous network specified by IEEE 802.9a (herein after referred to as "isoENET") provides for transmission of both "nonbursty" and "bursty" information over a single Ethernet-compatible network. See the documents U.S. patent application Ser. No. 07/970,329 entitled "Frame-Based Transmission of Data"; IEEE specification 802.9a; and "IsoEnet Transforms LANs And WANs Into Interactive Multimedia Tools", National Semiconductor Corporation, by Brian Edem et al., 1992 (the subject matter of all three documents is incorporated herein by reference) for further information on the IsoENET isochronous network.

In an isoENET network, the information being transmitted is broken up into a plurality of frames of information by a plurality of synchronization pulses. In addition to dedicated. Ethernet bandwidth, each frame contains 96 slots (also called "B-channels"). To transfer "bursty" information, multiple of these slots are filled with the bursty information. Several consecutive frames may be largely dedicated to the transfer of a burst of information whereas subsequent frames (after the burst) may carry no "bursty" information. To transfer "nonbursty" information, on the other hand, one slot of each successive frame may carry a small amount of "nonbursty" information. Accordingly, information from both a telephone and a workstation can be transferred over an isochronous network which is compatible with Ethernet.

FIG. **2** shows an example of an interconnection of networks and services which may be typical in the future. Network **100** is one Ethernet network of the large installed base of Ethernet networks in use today. At least some of these installed Ethernet networks are likely to still be operating in the future. Ethernet network **100** involves four workstations **101–104** and an Ethernet hub **105**. The workstations are coupled to the hub via corresponding Ethernet lines which function as one logical wire.

Network **106** is an isoENET network which is capable of isochronous information transfer and is also compatible with the installed base of Ethernet networks. IsoENET network **106** includes four workstations **107–110**, a telephone **111**, and an isoENET hub **112**. Because isoENET is capable of transmitting "nonbursty" telephone conversation information, telephone **111** is coupled to the isoENET network via workstation **107**.

Video information (for example, MPEG encoded video) for display by the workstations of the two networks is stored in this example in a video server **113**. Programs for use by the workstations of the two networks are stored in this example in a file server **114**. The servers **113** and **114** are coupled to the two networks **100** and **106** via high speed 155 Mbps (megabits per second) fiber optic links **115–118** and an ATM switch **119**. Accordingly, video information may be packaged in ATM format and transmitted from the video server **113** in "bursty" fashion over 155 Mbps link **118**, 155 Mbps link **116**, and isoENET line **107**A to workstation **107**.

A directory server **120** which supplies information in HDLC format may be provided by a telephone company. Directory server **120** is coupled to a central office/exchange **121** via a PRI line **122**. The central office/exchange **121** is coupled to the ATM switch via a 155 Mbps link **123**. Accordingly, information (such as yellow page graphic information) may be packaged in HDLC format and transmitted from the directory server **120** in "bursty" fashion over PRI line **122**, 155 Mbps link **123**, 155 Mbps link **116**, and isoENET line **107**A to workstation **107**. Workstation **107** therefore is an isoENET node capable of communicating using both ATM and HDLC protocols. The structure of workstation **107** is described in further detail later.

Because network **100** is a standard Ethernet network which does not support "nonbursty" telephone conversation information, a telephone **124** associated with workstation **101** is not coupled to a workstation of network **100** but rather is coupled to a PBX **125** via a PBX line **126**. Because network **106** is an isoENET network, telephone **111** transmits and receives "nonbursty" telephone conversation information via PBX-like line **127**, isoENET line **107**A, and PRI line **128**. PBX **125** is coupled to the central office/exchange **121** via multiple PRI lines **129**.

FIG. **3** is a block diagram illustrating an expansion card **200** disposed inside workstation **107**. See the document "HydraPro isoENET ISA Card Project Requirement Specification", National Semiconductor Corporation, 1994, (the subject matter of which is incorporated herein by reference) for additional information regarding a specific embodiment of expansion card **200**. Although FIG. **2** shows workstations as being the isoENET and Ethernet nodes, it is to be understood that any suitable equipment may serve as isoENET and Ethernet nodes. Personal computers, printers, and other peripherals may serve as nodes. The term "workstation" is used in a nonlimiting sense only as an illustrative example.

In FIG. **3**, the expansion card **200** is coupled via a card edge connector (not shown) to the ISA parallel bus **201** on the motherboard of the workstation **107**. Video/audio I/O subsystems **203** are coupled to card **200** via a MVIP (Multi-Vendor Integration Protocol) bus **204**. Video/audio I/O subsystems **203** may, for example, include a video camera, speakers, a microphone, and a video compressor/decompressor for compressing data output from the video camera for transmission on the MVIP bus **204** and for decompressing compressed video data received from the MVIP bus **204**. The MVIP bus is a known parallel isochronous bus used for moving isochronous data from one card to another card.

IsoENET line **107**A of FIG. **2** actually is in this embodiment a twisted pair of physical wires **205**. The block **206** of FIG. **3** labeled isoPhy is an integrated circuit which performs the functions of level shifting and buffering the isoENET network signals on physical wires **205** as well as separating or combining Ethernet and B-channel data. See U.S. patent application Ser. No. 07/969,916 entitled "Network For Data Communication With Isochronous Capability" (the subject matter of which is incorporated herein by reference) for additional information on isoPhy block **206**. An Ethernet subsystem integrated circuit **207** as well as an Ethernet buffer **208** are disposed in the Ethernet data path between isoPhy block **206** and ISA bus **201**. These parts perform the standard Ethernet MAC (Media Access Control) function and manage transmit and receive packet buffers. An integrated circuit **209** labeled isoBuffer, a B-channel buffer **210**, and a multiplexer/demultiplexer **211** labeled isoMux is disposed in the B-channel data path between isoPhy block **206** and ISA bus **201**.

FIG. **4** is a logical block diagram illustrating the contents of the isoBuffer integrated circuit **209** of FIG. **3**. See the document "isoBuffer Specification", National Semiconductor Corporation, 1994 (the subject matter of which is incorporated herein by reference) for additional details on a specific embodiment of integrated circuit **209**. Integrated circuit **209** includes a plug and play block **300**, an isochronous data buffer manager block **301**, and a circuit switch multiplexer/demultiplexer block **302**. At system boot, the central processing unit (not shown) of the workstation which is coupled to ISA bus **201** determines the needs and functions of card **200** via resource data stored in an EEPROM (not shown) on the card in accordance with the Microsoft Plug and Play Specification. Plug and play block **300** controls the EEPROM, decodes I/O addresses on the ISA bus, provides hardware chip selects for other chips on card **200**, and routes interrupt requests to the appropriate IRQ lines of the ISA bus.

FIG. **5** is a block diagram illustrating blocks **301** and **302** of FIG. **4** in greater detail. Information received from network wires **205** of FIG. **3** is received into the isoBuffer integrated circuit **209** on an isochronous network port **400**, proceeds through the isoBuffer as explained in further detail below, and is written to external buffer memory **210** via a buffer memory port **401**. The CPU of the workstation can later access that information in external buffer memory **210** so that the information is read from buffer **210**, passes through buffer memory port **401**, and passes onto the ISA bus **201** via a parallel bus port **402**. Information can also flow in the opposite direction such that information to be transmitted on network wires **205** is written by the CPU into the external buffer memory **210** via parallel bus port **402** and buffer memory port **401**. This information is later read from the external buffer memory **210** and output onto network wires **205** via buffer memory port **401** and isochronous network port **400**.

To allow workstation **107** (see FIG. **2**) to receive and transmit information packaged in both HDLC and ATM protocols, isoBuffer integrated circuit **209** includes two HDLC packet framer/deframer circuits **403** and **404**, an ATM packet framer/deframer circuit **405**, a multiplexer/demultiplexer **406**, and a slot mapping memory **407**. Packet framer/deframer circuits are known in the art. See the document "ATM OVERVIEW F-Fred Device-DP83372/R-Fred Device DP83382", National Semiconductor Corporation, 1993 (the subject matter of which is incorporated herein by reference) for additional information pertaining to a packet framer/deframer circuit. A packet may, for example, consist of a handful to several thousand bytes of information. (Although a "framer/deframer" circuit does not really "frame" or "deframe" information but rather "packetizes" or "depacketizes" information, the term "packetizer/depacketizer" is not is used herein because the term "packetizer" is not commonly used in the industry.)

Assume for illustrative purposes that isoENET frames are to be received from wires **205** of FIG. **3**, that the first slot of each frame contains a byte of a packet framed in accordance with the HDLC protocol, and that the second slot in each frame contains a byte of a packet framed in accordance with the ATM protocol. First, a 256 by 4-bit receive portion of the slot mapping memory **407** is initialized by the workstation CPU from the ISA bus **201** so that the contents of each of the 256 memory locations of memory **407** indicates which of the packet framer/deframer circuits is to be used to deframe a corresponding one of the 256 slots of a frame. The first memory location of memory **407** is programmed to contain a value indicating that a HDLC packet framer/deframer circuit is to be used to frame or deframe information for the first slot whereas the second memory location is programmed to contain a value indicating that the ATM packet framer/deframer circuit is to be used to frame or deframe information for the second slot.

After this initialization of the slot mapping memory **407**, a channel counter (not shown) of circuit switch multiplexer/demultiplexer block **302** provides addresses to the receive portion of the slot mapping memory **407**. Initially, the channel counter outputs a value which addresses the first memory location of the receive portion of memory **407**. Because the first memory location of memory **407** was initialized to contain data which causes multiplexer/demultiplexer circuit **406** and HDLC packet framer/deframer circuit **404** to perform packet deframing, the first slot of the isoENET frame is deframed by HDLC packet framer/deframer circuit **404**. After the information from the first slot is received, the channel counter is incremented. At the start of the second slot, the receive portion of memory **407** is read using the incremented count value output from the channel counter for the memory address. Because the second memory location of memory **407** was initialized to

contain data which causes multiplexer/demultiplexer circuit **406** and ATM packet framer/deframer circuit **405** to perform packet deframing, the second slot of the isoENET frame is deframed by ATM packet framer/deframer circuit **405**. After the information from the second slot is received, the channel counter is again incremented. Deframing of each successive slot of the isoENET frame proceeds in like fashion. The channel counter is reset by the rising edge of the frame synchronization signal received on wires **205** at the end of the frame. As an incoming packet is deframed, it is stored in a dedicated location in buffer **210**.

When information is being written into buffer RAM **210** from one of the packet framer/deframer circuits, a buffer manager in block **408** of the integrated circuit determines where in memory **210** that information is written so that a separate receive ring buffer is maintained in memory **210** for each packet framer/deframer. The location and size of each ring buffer is set from the ISA bus by writing control registers in block **408**. Four control registers are associated with each packet framer/deframer circuit: a control register defining the beginning location of the ring buffer in physical memory **210**, a control register defining the ending location of the ring buffer in physical memory **210**, a control register defining where in memory **210** the next incoming packet is to be written, and a control register defining where in memory **210** the oldest packet unread by the CPU is located. After an entire packet has been received and deframed by the appropriate packet framer/deframer circuit, the CPU is signalled via the ISA bus **201** that packet reception is complete. The CPU can then commence in the transfer of the packet data stored in buffer **210** to system memory via the ISA bus **201**.

The block **408** actually includes two independent buffer managers. Each buffer manager is coupled to an associated packet framer/deframer circuit. Two HDLC packet framer/deframer circuits **403** and **404** are provided in the specific embodiment in order to support a specific video conferencing method. The present invention is not, however, limited to require two packet framer/deframers for the same protocol.

In some embodiments, block **408** also includes circuitry for managing a "receive cell buffer" in memory **210**. The receive cell buffer can be used as a receptacle for ATM cells (a "cell" is an ATM construct and is 53 bytes of ATM information). When an ATM cell is received that is not part of a packet of information being written into a receive ring buffer, the ATM cell may be stored in the receive cell buffer. These stored ATM cells can then be accessed later via the ISA bus **201**. Such ATM cells may, for example, be intermittently transmitted ATM cells which indicate the status of a conference call when the conversation of the conference call itself is being written into a receive ring buffer in memory **210**. The receive cell buffer makes use of hardware in an ATM packet framer/deframer circuit which identifies cells from raw incoming data but does not utilize the higher level deframing hardware which identifies, packets of cells.

IsoBuffer integrated circuit **209** also includes a constant bit rate (CBR) buffer manager block **410** which manages raw unframed or nondeframed streams of data. The CBR buffer manager **410** keeps track of where a stream of raw data is being written into memory **210** by tracking frames (frames usually are transmitted at a 8 kHz rate) rather than by tracking the beginning and ending of packets. Given the number of bytes in a frame, and the starting location in memory **210**, CBR buffer manager **410** can determine from the number of frames received the location at which raw nondeframed information is being written into memory **210**. Nondeframed data in memory **210** may be deframed later in software by a CPU coupled to ISA bus **201**. This constant bit rate buffer feature may be used to support a high level protocol which is not supported in hardware on integrated circuit **209** by a dedicated packet framer/deframer circuit.

Arbiter **409** determines which of the ISA bus **201**, the buffer managers in block **408**, or the CBR buffer manager **410** will have access to the buffer RAM **210**. Any number of arbiter circuits can be used for this purpose. In one embodiment, each of the blocks **408**, **410** and an ISA bus interface **411** provides a request signal on its own dedicated request line to the arbiter **409**.

The microfiche appendix contains RTL code and schematics describing a specific embodiment of an integrated circuit which is described in block diagram form by FIGS. **3–5**. The RTL code specifies blocks **403–408** of FIG. **5** whereas the schematics specify blocks **409–411**. It is to be understood that the block diagram of FIG. **5** is illustrative of the functions of the various blocks and does not necessary indicate physical connections between the hardware circuits. In some embodiments, multiplexer/demultiplexer **406** is not disposed in the data path between the isochronous network port of the integrated circuit and the packet framer/deframer circuits of the integrated circuit but rather the packet framer/deframer circuits are all coupled substantially directly to the isochronous network port and appropriate ones of the packet framer/deframer circuits are enabled one at a time by multiplexer/demultiplexer **406**. Similarly, the buffer managers in block **408** and the CBR buffer manager in block **410** are not actually physically disposed in the illustrated data paths to buffer memory port **401** but rather are associated with information transfers through these paths. In some embodiments, arbiter **409** includes a bidirectional multiplexer/demultiplexer for coupling a selected data path to buffer memory port **401**. The selected data path may extend from ISA bus **201**, from isochronous network port **400**, or from one of the packet framer/deframer circuits **403–405**. In some embodiments a multiplexer in block **406** selectively couples the respective outputs of the framers in blocks **403–405** to an output part of port **400** whereas a demultiplexer in block **406** simultaneously selectively couples an input part of port **400** to the deframers in blocks **403–405**.

Although the invention is described in connection with certain illustrative embodiments for instructional purposes, the invention is not limited thereto. In some embodiments, the buffer memory is disposed on the same integrated circuit as the packet framer/deframer circuits and the circuit switch multiplexer/demultiplexer. Buses other than the ISA bus can be supported including the PCI bus and the Apple NuBUS. Accordingly, modifications, adaptations, and combinations of various aspects of the specific embodiments can be practiced without departing from the scope of the invention as set forth in the following claims.

What is claimed is:

1. An integrated circuit, comprising:

an isochronous network port;

a first protocol packet framer/deframer circuit;

a second protocol packet framer/deframer circuit; and

a circuit switch multiplexer/demultiplexer coupled to said isochronous network port, said first protocol packet framer/deframer circuit, and said second protocol packet framer/deframer circuit, wherein said circuit switch multiplexer/demultiplexer comprises a multiplexer/demultiplexer, and a storage device, said multiplexer/demultiplexer being at least in part controlled based on a value output from said storage device.

2. The integrated circuit of claim 1, wherein a plurality of isochronous frames are received on said isochronous network port, each of said isochronous frames comprising a plurality of slots, a first of said slots of a frame being supplied to and deframed by said first protocol packet framer/deframer circuit, a second of said slots of said frame being supplied to and deframed by said second protocol packet framer/deframer circuit.

3. The integrated circuit of claim 1, wherein said first protocol packet framer/deframer circuit deframes ATM formatted slots, and wherein said second protocol packet framer/deframer circuit deframes HDLC formatted slots.

4. The integrated circuit of claim 3, wherein said first protocol packet framer/deframer circuit deframes ATM cells.

5. The integrated circuit of claim 3, wherein said first protocol packet framer/deframer circuit deframes both ATM cells and ATM packets.

6. The integrated circuit of claim 1, wherein said storage device comprises a plurality of memory locations, and wherein said circuit switch multiplexer/demultiplexer further comprises:

a receive counter, said receive counter being incremented after a receipt of a slot of information received on said isochronous network port, a count value output from said receive counter pointing to a corresponding memory location of said plurality of memory locations of said storage device.

7. The integrated circuit of claim 1, further comprising:

a parallel bus port, said storage device being accessible from said parallel bus port.

8. The integrated circuit of claim 1, further comprising:

a parallel bus port;

parallel bus interface circuitry coupled to said parallel bus port;

a memory; and

an arbiter circuit coupled to said parallel bus interface circuitry and to said memory, said arbiter arbitrating access to said memory.

9. The integrated circuit of claim 8, further comprising:

a buffer manager circuit coupled to said first protocol packet framer/deframer circuit, said second protocol packet framer/deframer circuit and to said arbiter circuit, said buffer manager circuit comprising:

first and second receive pointer registers for pointing to a receive buffer in said memory; and

first and second transmit pointer registers for pointing to a transmit buffer in said memory.

10. The integrated circuit of claim 8, further comprising:

means, coupled to said circuit switch multiplexer/demultiplexer, for managing buffering of substantially nondeframed isochronous network data in said memory.

11. A method, comprising:

deframing information of a slot of a frame of network information using a first protocol packet deframer circuit;

deframing information of another slot of said frame of network information using a second protocol packet deframer circuit, said first and second protocol packet deframer circuits both being disposed on the same integrated circuit;

incrementing a counter of said integrated circuit so that a count value output from said counter corresponds with a slot number of the slot being received into said integrated circuit; and

using said count value to address a slot mapping memory of said integrated circuit.

12. The method of claim 11, wherein said integrated circuit has a parallel bus port, said method further comprising:

programming said slot mapping memory of said integrated circuit via said parallel bus port.

13. The method of claim 11, further comprising:

storing information deframed by said first protocol packet deframer circuit in a first ring buffer; and

storing information deframed by said second protocol packet deframer circuit in a second ring buffer.

14. An integrated circuit, comprising:

a first packet deframer circuit which deframes information in accordance with a first network protocol;

a second packet deframer circuit which deframes information in accordance with a second network protocol; and

means for causing said first packet deframer circuit to deframe information in a first isochronous network slot of a frame in accordance with said first network protocol and for causing said second packet deframer circuit to deframe information in a second isochronous network slot of said frame in accordance with said second network protocol, wherein said means comprises means for storing slot mapping information.

15. The integrated circuit of claim 14, wherein said first network protocol is an ATM protocol and wherein said second network protocol is an HDLC protocol.

16. An integrated circuit comprising:

a first packet deframer circuit which deframes information in accordance with a first network protocol;

a second packet deframer circuit which deframes information in accordance with a second network protocol;

means for causing said first packet deframer circuit to deframe information in a first isochronous network slot of a frame in accordance with said first network protocol and for causing said second packet deframer circuit to deframe information in a second isochronous network slot of said frame in accordance with said second network protocol;

means for managing a receive ring buffer;

a parallel bus port; and

parallel bus interface circuitry coupled to said parallel bus port.

17. The integrated circuit of claim 14, further comprising:

a first packet framer circuit which frames information in accordance with a network protocol; and

a second packet framer circuit which frames information in accordance with a network protocol,

wherein said means for causing comprises:

a multiplexer having a first input lead, a second input lead, and an output lead, said first input lead being coupled to an output lead of said first packet framer circuit, said second input lead being coupled to an output lead of said second packet framer circuit, and an output lead being coupled to an output part of an isochronous network port of said integrated circuit; and

a demultiplexer having an input lead, a first output lead, and a second output lead, said input lead being coupled to an input part of said isochronous network port, said first output lead being coupled to an input lead of said first packet deframer circuit, and said

second output lead being coupled to an input lead of said second packet deframer circuit.

18. An integrated circuit, comprising:

an isochronous network port, wherein the isochronous network port receives frame of information, said frame having a plurality of non-isochronous and isochronous slots, and each of said isochronous slots having information of one of at least a first protocol or a second protocol;

a first protocol packet framer/deframer circuit;

a second protocol packet framer/deframer circuit; and

a circuit switch multiplexer/demultiplexer coupled to said isochronous network port, said first protocol packet framer/deframer circuit, and said second protocol packet framer/deframer circuit, wherein the circuit switch multiplexer/demultiplexer couples said isochronous first protocol slots to the first protocol packet framer/deframer circuit and couples said isochronous second protocol slots to the second protocol packet framer/deframer circuit.

19. The integrated circuit of claim **18** further comprising:

a first demultiplexer coupled to said isochronous network port, wherein the first demultiplexer separates the non-isochronous slots from the isochronous slots, and the circuit switch multiplexer/demultiplexer is coupled to the first demultiplexer.

20. The integrated circuit of claim **18**, wherein said circuit switch multiplexer/demultiplexer comprises:

a multiplexer/demultiplexer; and

a storage device, said multiplexer/demultiplexer being at least in part controlled based on a value output from said storage device.

21. The integrated circuit of claim **18**, wherein a plurality of isochronous slots are received on said isochronous network port, a first of said isochronous slots of a frame being provided to and deframed by said first protocol packet framer/deframer circuit, and a second of said isochronous slots of said frame being provided to and deframed by said second protocol packet framer/deframer circuit.

22. The integrated circuit of claim **18**, wherein said first protocol packet framer/deframer circuit deframes ATM formatted slots, and wherein said second protocol packet framer/deframer circuit deframes HDLC formatted slots.

23. The integrated circuit of claim **22**, wherein said first protocol packet framer/deframer circuit deframes ATM cells.

24. The integrated circuit of claim **22**, wherein said first protocol packet framer/deframer circuit deframes both ATM cells and ATM packets.

25. The integrated circuit of claim **20**, wherein said storage device comprises a plurality of memory locations, and wherein said circuit switch multiplexer/demultiplexer further comprises:

a receive counter, said receive counter being incremented after a receipt of a slot of information received on said isochronous network port, a count value output from said receive counter pointing to a corresponding memory location of said plurality of memory locations of said storage device.

26. The integrated circuit of claim **20**, further comprising:

a parallel bus port, said storage device being accessible from said parallel bus port.

27. The integrated circuit of claim **20**, further comprising:

a parallel bus port;

parallel bus interface circuitry coupled to said parallel bus port;

a memory; and

an arbiter circuit coupled to said parallel bus interface circuitry and to said memory, said arbiter arbitrating access to said memory.

28. The integrated circuit of claim **27**, further comprising:

a buffer manager circuit coupled to said first protocol packet framer/deframer circuit, said second protocol packet framer/deframer circuit and to said arbiter circuit, said buffer manager circuit comprising:

first and second receive pointer registers for pointing to a receive buffer in said memory; and

first and second transmit pointer registers for pointing to a transmit buffer in said memory.

29. The integrated circuit of claim **27**, further comprising:

means, coupled to said circuit switch multiplexer/demultiplexer, for managing buffering of substantially nondeframed isochronous network data in said memory.

30. A method, comprising:

framing network information, wherein network information frames include non-isochronous and isochronous slots;

deframing information of an isochronous slot of using a first protocol packet deframer circuit; and

deframing information of another isochronous slot using a second protocol packet deframer circuit, said first and second protocol packet deframer circuits both being disposed on the same integrated circuit.

31. The integrated circuit of claim **30**, wherein said first protocol packet framer/deframer circuit deframes ATM formatted slots, and wherein said second protocol packet framer/deframer circuit deframes HDLC formatted slots.

32. The method of claim **30** wherein each isochronous slot is formatted with at least one of a first protocol or a second protocol, the method further comprising the steps of:

separating the non-isochronous slots from the isochronous slots into a non-isochronous data stream and an isochronous data stream;

coupling the isochronous slots formatted with the first protocol to the first protocol packet deframer circuit; and

coupling the isochronous slots formatted with the second protocol to the second protocol packet deframer circuit.

33. The method of claim **32** further comprising the step of:

demultiplexing the isochronous slots; and

wherein the separating step includes the step of demultiplexing with a first demultiplexer each network information frame.

34. The method of claim **30** further comprising the steps of:

flaming information having a first protocol using a first protocol packet framer circuit;

framing information having a second protocol using a second protocol packet framer circuit;

combining the first protocol framed information and the second protocol framed information into isochronous slots; and

combining isochronous slots with non-isochronous slots into a frame.

35. The method of claim **30**, further comprising:

incrementing a counter of said integrated circuit so that a count value output from said counter corresponds with a slot number of the slot being received into said integrated circuit; and using said count value to address a slot mapping memory of said integrated circuit.

36. The method of claim **35**, wherein said integrated circuit has a parallel bus port, said method further comprising:

programming said slot mapping memory of said integrated circuit via said parallel bus port.

37. The method of claim **35**, further comprising:

storing information deframed by said first protocol packet deframer circuit in a first ring buffer; and

storing information deframed by said second protocol packet deframer circuit in a second ring buffer.

38. An integrated circuit, comprising:

means for framing information, each information frame having isochronous and non-isochronous slots and each of said isochronous slots having information formatted by one of at least a first network protocol or a second network protocol;

means for receiving the framed information;

means for separating the isochronous slots and the non-isochronous slots;

a first means for combining information formatted by a first protocol into a first packet;

a second means for combining information formatted by a second protocol into a second packet; and

means for coupling first protocol formatted information in an isochronous slot to the first means for combining and for coupling second protocol formatted information in another isochronous slot to the second means for combining.

39. The integrated circuit of claim **38** further comprising:

a first means for separating a packet of information formatted by a first protocol into first segments of information;

a second means for disassembling a packet of information formatted by a second protocol into second segments of information; and

means for combining the first information segments and the second information segments into an isochronous data stream; means for combining the isochronous data stream with a non-isochronous data stream.

40. The integrated circuit as in claim **39** wherein the means for combining includes the step of inserting the first segments and the second segments into isochronous slots of a frame and non-isochronous data stream segments into non-isochronous slots of the frame.

41. The integrated circuit of claim **38**, wherein said first network protocol is an ATM protocol and wherein said second network protocol is an HDLC protocol.

42. The integrated circuit of claim **38**, wherein said means for coupling comprises means for storing slot mapping information.

43. The integrated circuit of claim **38**, further comprising:

means for managing a receive ring buffer;

a parallel bus port; and

parallel bus interface circuitry coupled to said parallel bus port.

44. The integrated circuit of claim **38**, further comprising:

a first packet framer circuit which frames information in accordance with a network protocol; and

a second packet framer circuit which frames information in accordance with a network protocol,

wherein said means for coupling comprises: a multiplexer having a first input lead, a second input lead, and an output lead, said first input lead being coupled to an output lead of said first packet framer circuit, said second input lead being coupled to an output lead of said second packet framer circuit, and an output lead being coupled to an output part of an isochronous network port of said integrated circuit; and

a demultiplexer having an input lead, a first output lead, and a second output lead, said input lead being coupled to an input part of said isochronous network port, said first output lead being coupled to an input lead of said first packet deframer circuit, and said second output lead being coupled to an input lead of said second packet deframer circuit.

45. An apparatus, comprising:

an isochronous port;

one or more first protocol packet framer/deframer circuits;

one or more second protocol packet framer/deframer circuits; and

a circuit switch multiplexer/demultiplexer coupled to the isochronous port, at least one of the first protocol packet framer/deframer circuits, and at least one of the second protocol packet framer/deframer circuits, wherein the circuit switch multiplexer/demultiplexer comprises a multiplexer/demultiplexer and a storage device, the multiplexer/demultiplexer being at least in part controlled based on an output from the storage device.

46. The apparatus of claim 45, wherein the isochronous port comprises a time division multiplexed port.

47. An apparatus, comprising:

an isochronous port;

a first protocol circuit;

a second protocol circuit; and

a circuit switch multiplexer/demultiplexer coupled to the isochronous port, the first protocol circuit, and the second protocol circuit, wherein the circuit switch multiplexer/demultiplexer comprises a multiplexer/demultiplexer and a storage device, the multiplexer/demultiplexer being at least in part controlled based on an output from the storage device.

48. The apparatus of claim 47, wherein the first protocol circuit manages raw data.

49. The apparatus of claim 47, wherein the first protocol circuit manages unframed data.

50. The apparatus of claim 47, wherein the first protocol circuit manages nondeframed data.

51. The apparatus of claim 47, wherein the first protocol circuit comprises a constant bit rate buffer circuit.

52. The apparatus of claim 47, wherein the second protocol circuit comprises a packet framer/deframer circuit.

53. The apparatus of claim 47, wherein the second protocol circuit comprises an HDLC framer/deframer circuit.

54. The apparatus of claim 47, wherein the second protocol circuit comprises multiple packet framer/deframer circuits.

55. The apparatus of claim 47, wherein the second protocol circuit comprises multiple HDLC framer/deframer circuits.

56. The apparatus of claim 47, wherein the second protocol circuit comprises an asynchronous transfer mode framer/deframer circuit.

57. The apparatus of claim 47, wherein the isochronous port comprises a time division multiplexed port.

58. An apparatus, comprising:

an isochronous port;

one or more first protocol circuits;

one or more second protocol circuits;

a circuit switch multiplexer/demultiplexer coupled to the isochronous port, at least one of the first protocol circuits, and at least one of the second protocol circuits, wherein the circuit switch multiplexer/demultiplexer comprises a multiplexer/demultiplexer and a storage device, the multiplexer/demultiplexer being at least in part controlled based on an output from the storage device; and

a buffer memory, wherein a signal path is provided from the isochronous port to at least one of the first protocol circuits, and from the at least one first protocol circuit to the buffer memory, and from the buffer memory to at least one of the second protocol circuits, and from the second protocol circuit to the isochronous port.

59. The apparatus of claim 58, wherein at least one of the first protocol circuit manages raw data.

60. The apparatus of claim 58, wherein at least one of the first protocol circuit manages unframed data.

61. The apparatus of claim 58, wherein the first protocol circuit manages nondeframed data.

62. The apparatus of claim 58, wherein the first protocol circuit comprises a constant bit rate buffer circuit.

63. The apparatus of claim 58, wherein the second protocol circuit comprises a packet framer/deframer circuit.

64. The apparatus of claim 58, wherein the second protocol circuit comprises an HDLC framer/deframer circuit.

65. The apparatus of claim 58, wherein the second protocol circuit comprises multiple packet framer/deframer circuits.

66. The apparatus of claim 58, wherein the second protocol circuit comprises multiple HDLC framer/deframer circuits.

67. The apparatus of claim 58, wherein the second protocol circuit comprises an asynchronous transfer mode framer/deframer circuit.

68. The apparatus of claim 58, wherein the isochronous port comprises a time division multiplexed port.

69. A method, comprising:

deframing information of a received slot of information using a first protocol packet deframer circuit;

deframing information of another received slot of information using a second protocol packet deframer circuit;

generating an output that corresponds with the slot being received; and

using the output to address a slot mapping memory.

70. An apparatus, comprising:

a first packet deframer circuit which deframes information in accordance with a first protocol;

a second packet deframer circuit which deframes information in accordance with a second protocol; and

means for causing the first packet deframer circuit to deframe information in a first isochronous slot of a frame in accordance with the first protocol and for causing the second packet deframer circuit to deframe information in a second isochronous slot of the frame in accordance with the second protocol, wherein the means comprises means for storing slot mapping information.

71. An apparatus comprising:

a first packet deframer circuit which deframes information in accordance with a first protocol;

a second packet deframer circuit which deframes information in accordance with a second protocol;

means for causing the first packet deframer circuit to deframe information in a first isochronous slot of a frame in accordance with the first protocol and for causing the second packet deframer circuit to deframe information in a second isochronous slot of the frame in accordance with the second protocol;

means for managing a receive buffer;

a port; and

interface circuitry coupled to the port.

72. An apparatus comprising:

a first packet deframer circuit which deframes information in accordance with a first protocol;

a second packet deframer circuit which deframes information in accordance with a second protocol;

means for causing the first packet deframer circuit to deframe information in a first isochronous slot of a frame in accordance with the first network protocol and for causing the second packet deframer circuit to deframe information in a second isochronous slot of the frame in accordance with the second protocol;

means for managing a receive buffer;

a bus port for coupling to a bus; and

interface circuitry coupled to the bus port, wherein the bus supports multiple transfer types, such as direct memory access, shared memory access or standard I/O access.

73. An apparatus, comprising:

an isochronous port, wherein the isochronous port receives a frame of information, the frame having a plurality of non-isochronous and isochronous slots, and each of the isochronous slots having information of one of at least a first protocol or a second protocol;

a first protocol packet framer/deframer circuit;

a second protocol packet framer/deframer circuit; and

a circuit switch multiplexer/demultiplexer coupled to the isochronous port, the first protocol packet framer/deframer circuit, and the second protocol packet framer/deframer circuit, wherein the circuit switch multiplexer/demultiplexer couples the isochronous first protocol slots to the first protocol packet framer/deframer circuit and couples the isochronous second protocol slots to the second protocol packet framer/deframer circuit.

74. A method, comprising:

framing information, wherein information frames include non-isochronous and isochronous slots;

deframing information of an isochronous slot of using a first protocol packet deframer circuit; and

deframing information of another isochronous slot using a second protocol packet deframer circuit, said first and second protocol packet deframer circuits being coupled to a common buffer memory.

75. An apparatus, comprising:

means for framing information, each information frame having isochronous and non-isochronous slots and each of the isochronous slots having information formatted by one of at least a first protocol or a second protocol;

means for receiving the framed information;

means for separating the isochronous slots and the non-isochronous slots;

a first means for combining information formatted by a first protocol into a first packet;

a second means for combining information formatted by a second protocol into a second packet; and

means for coupling first protocol formatted information in an isochronous slot to the first means for combining and for coupling second protocol formatted information in another isochronous slot to the second means for combining.

76. An apparatus comprising:

a network port;

a multiplexer/demultiplexer circuit coupled to the network port;

a first protocol circuit and a second protocol circuit each coupled to the multiplexer/demultiplexer circuit; and

a buffer coupled to the first and second protocol circuit;

wherein a signal path is provided from the network port to the first protocol circuit, and from the first protocol circuit to the buffer, and from the buffer to the second protocol circuit, and from the second protocol circuit to the network port.

77. The apparatus of claim 76, wherein the first protocol circuit manages raw data.

78. The apparatus of claim 76, wherein the first protocol circuit manages unframed data.

79. The apparatus of claim 76, wherein the first protocol circuit manages nondeframed data.

80. The apparatus of claim 76, wherein the first protocol circuit comprises a constant bit rate buffer circuit.

81. The apparatus of claim 76, wherein the second protocol circuit comprises a packet framer/deframer circuit.

82. The apparatus of claim 76, wherein the second protocol circuit comprises an HDLC framer/deframer circuit.

83. The apparatus of claim 76, wherein the second protocol circuit comprises multiple packet framer/deframer circuits.

84. The apparatus of claim 76, wherein the second protocol circuit comprises multiple HDLC framer/deframer circuits.

85. The apparatus of claim 76, wherein the second protocol circuit comprises an asynchronous transfer mode framer/deframer circuit.

86. The apparatus of claim 76, wherein the network port comprises a time division multiplexed port.

87. A method comprising:

coupling information from a network to an isochronous port, the information including non-isochronous and isochronous slots;

coupling the information from the isochronous port to a multiplexer/demultiplexer;

selectively coupling the information from the multiplexer/demultiplexer to a first protocol circuit and a second protocol circuit; and

selectively coupling the information from/to the first and second protocol circuit to a buffer;

wherein a signal path is provided from the isochronous port to the first protocol circuit, and from the first protocol circuit to the buffer, and from the buffer to the second protocol circuit, and from the second protocol circuit to the isochronous port.

88. The method of claim 87, wherein the first protocol circuit manages raw data.

89. The method of claim 87, wherein the first protocol circuit manages unframed data.

90. The method of claim 87, wherein the first protocol circuit manages nondeframed data.

91. The method of claim 87, wherein the first protocol circuit comprises a constant bit rate buffer circuit.

92. The method of claim 87, wherein the second protocol circuit comprises a packet framer/deframer circuit.

93. The method of claim 87, wherein the second protocol circuit comprises an HDLC framer/deframer circuit.

94. The method of claim 87, wherein the second protocol circuit comprises multiple packet framer/deframer circuits.

95. The method of claim 87, wherein the second protocol circuit comprises multiple HDLC framer/deframer circuits.

96. The method of claim 87, wherein the second protocol circuit comprises an asynchronous transfer mode framer/deframer circuit.

97. The method of claim 87, wherein the network port comprises a time division multiplexed port.

* * * * *