US00RE38482E

(19) **United States**

(12) **Reissued Patent**

Leung et al.

(10) **Patent Number: US RE38,482 E**

(45) **Date of Reissued Patent: *Mar. 30, 2004**

(54) **DELAY STAGE CIRCUITRY FOR A RING OSCILLATOR**

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(73) Assignee: **Rambus Inc.**, Los Altos, CA (US)

(*) Notice: This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/631,028**

(22) Filed: **Aug. 2, 2000**

Related U.S. Patent Documents

Reissue of:

(64) Patent No.: **5,799,051**
Issued: **Aug. 25, 1998**
Appl. No.: **08/711,908**
Filed: **Sep. 12, 1996**

U.S. Applications:

(60) Continuation of application No. 08/347,844, filed on Dec. 1, 1994, now Pat. No. 5,596,610, which is a continuation of application No. 08/161,769, filed on Dec. 2, 1993, now abandoned, which is a division of application No. 07/890,034, filed on May 28, 1992, now abandoned.

(51) **Int. Cl.**[7] **H03D 3/24**

(52) **U.S. Cl.** **375/357**; 375/376; 375/377; 330/253; 330/261; 330/277; 327/154; 327/156; 327/163; 327/287; 327/288

(58) **Field of Search** 375/219, 220, 375/222, 354, 357, 371, 373, 376, 377; 713/400, 401, 500; 327/291, 295, 297, 298, 287, 288; 330/253, 261, 277

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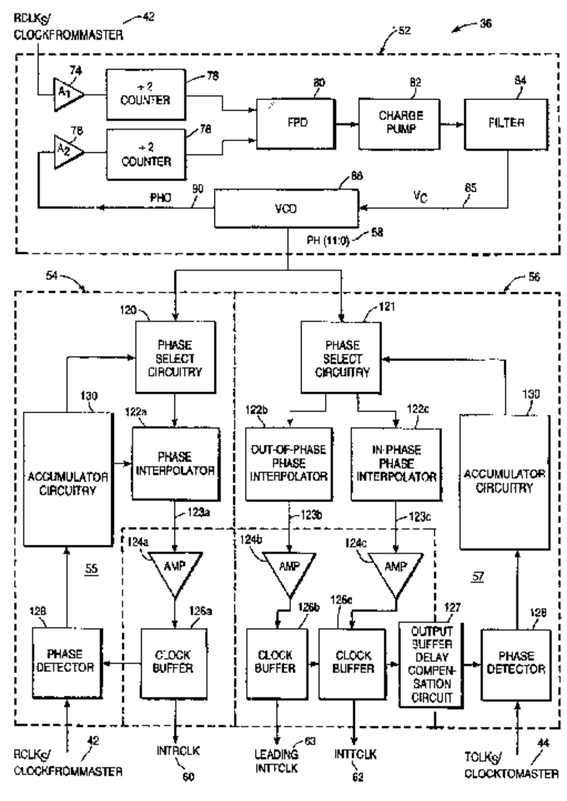
Primary Examiner—Amanda T. Le

(57) **ABSTRACT**

A ring oscillator includes an even-numbered plurality of ring coupled delay stages. Each delay stage includes a differential amplifier, a voltage clamping circuit, and a current source. The differential amplifier receives first and second input signals from a preceding delay stage. The differential amplifier provides a first output signal and a complementary second output signal at first and second nodes, respectively. The voltage clamping circuit is coupled between the first and second nodes to limit a peak-to-peak voltage swing of each of the first and second output signals. The current source is coupled to the differential amplifier and varies a bias current in accordance with a delay bias voltage.

103 Claims, 14 Drawing Sheets



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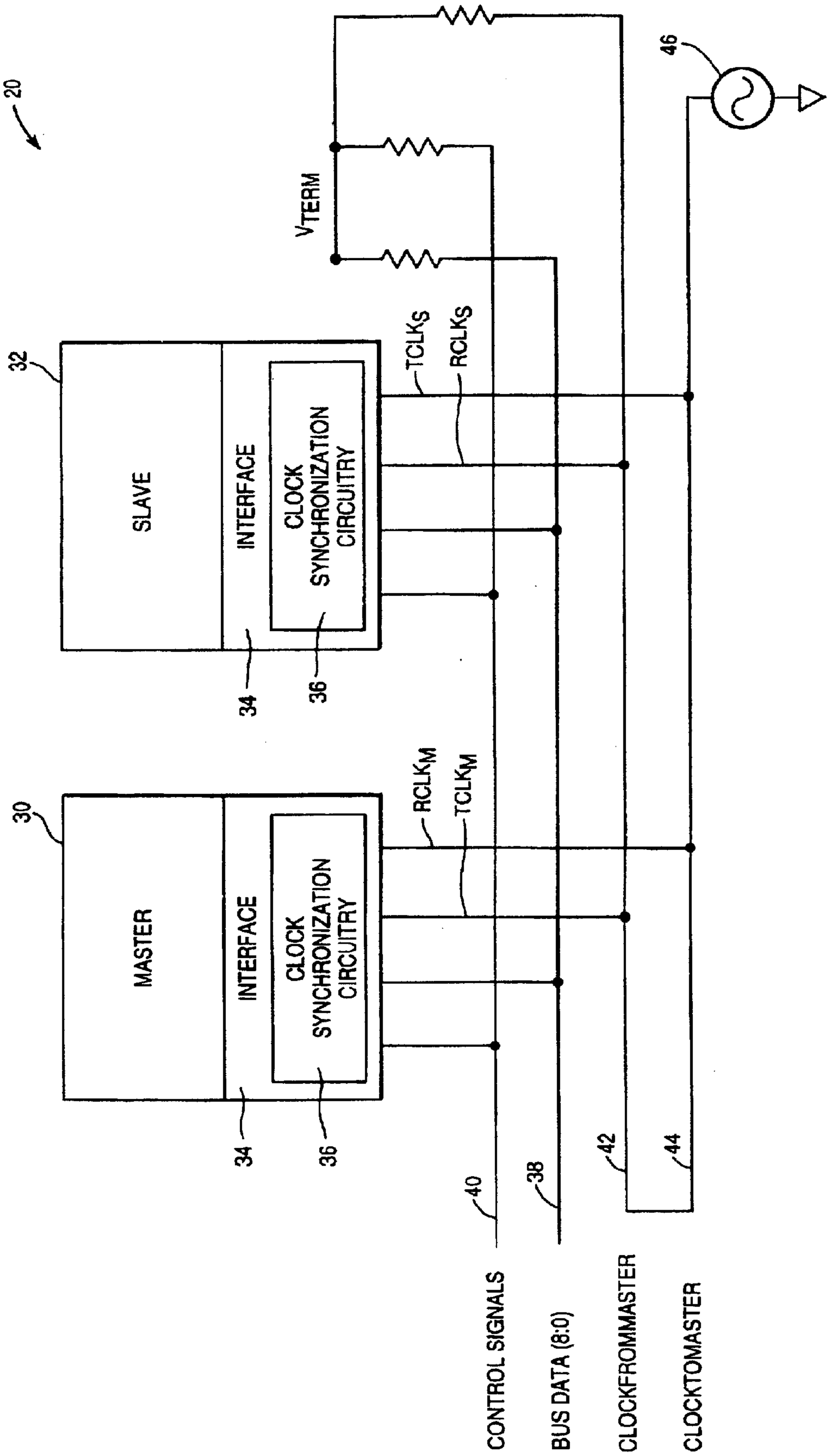
20
46
VTERM
TCLKS
RCLKS
32
SLAVE
INTERFACE
CLOCK SYNCHRONIZATION CIRCUITRY
34
36
RCLKM
TCLKM
30
MASTER
INTERFACE
CLOCK SYNCHRONIZATION CIRCUITRY
34
36
40
38
42
44
CONTROL SIGNALS
BUS DATA (8:0)
CLOCKFROMMASTER
CLOCKTOMASTER

FIG_1

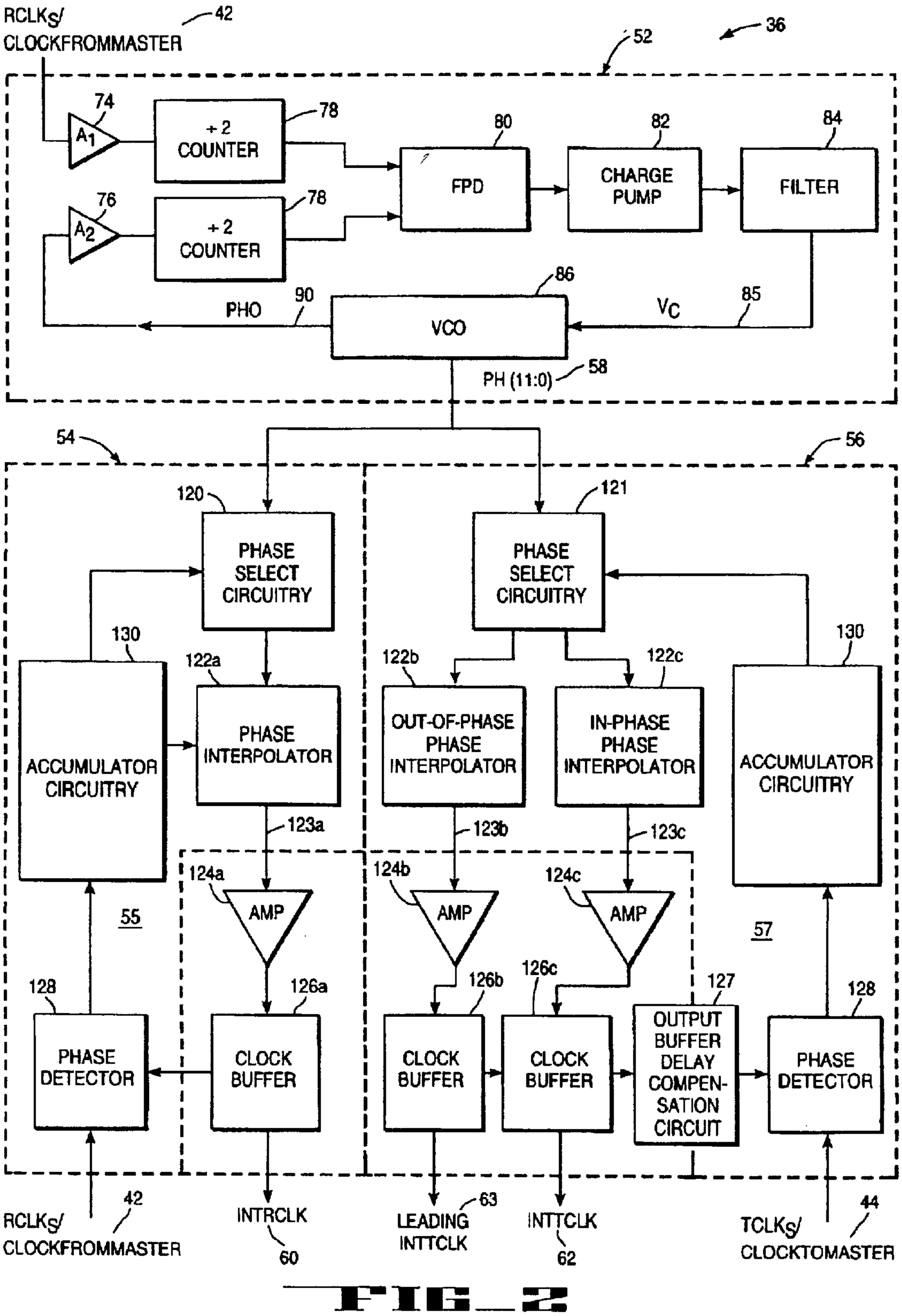
RCLKs/
CLOCKFROMMASTER
42
36
52
74
A1
+2
COUNTER
78
80
FPD
82
CHARGE
PUMP
84
FILTER
76
A2
+2
COUNTER
78
86
PHO
90
VCO
Vc
85
PH (11:0)
58
54
56
120
PHASE
SELECT
CIRCUITRY
121
PHASE
SELECT
CIRCUITRY
130
122a
122b
122c
130
ACCUMULATOR
CIRCUITRY
PHASE
INTERPOLATOR
OUT-OF-PHASE
PHASE
INTERPOLATOR
IN-PHASE
PHASE
INTERPOLATOR
ACCUMULATOR
CIRCUITRY
123a
123b
123c
124a
124b
124c
AMP
AMP
AMP
55
57
128
126a
126b
126c
127
128
PHASE
DETECTOR
CLOCK
BUFFER
CLOCK
BUFFER
CLOCK
BUFFER
OUTPUT
BUFFER
DELAY
COMPEN-
SATION
CIRCUIT
PHASE
DETECTOR
42
63
44
RCLKs/
CLOCKFROMMASTER
INTRCLK
60
LEADING
INTTCLK
INTTCLK
62
TCLKs/
CLOCKTOMASTER

FIG_2

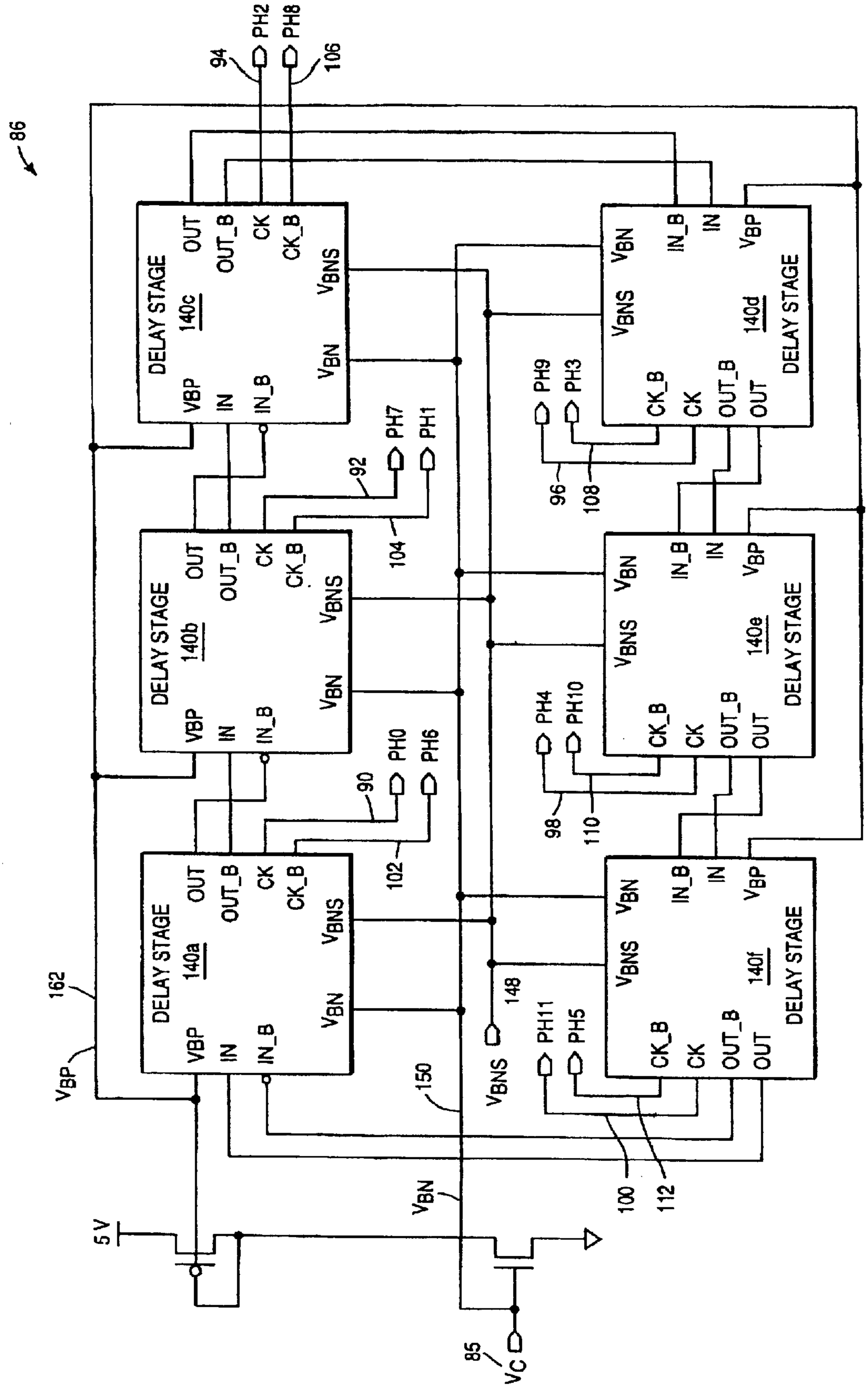
86
94
PH2
PH8
106
DELAY STAGE
140c
VBP
IN
IN_B
OUT
OUT_B
CK
CK_B
VBNS
VBN
92
PH7
PH1
104
140b
90
PH0
PH6
102
140a
162
VBP
150
VBNS
148
PH9
PH3
96
108
140d
PH4
PH10
98
110
140e
PH11
PH5
140f
VBN
5V
85
VC
100
112

FIG. 3

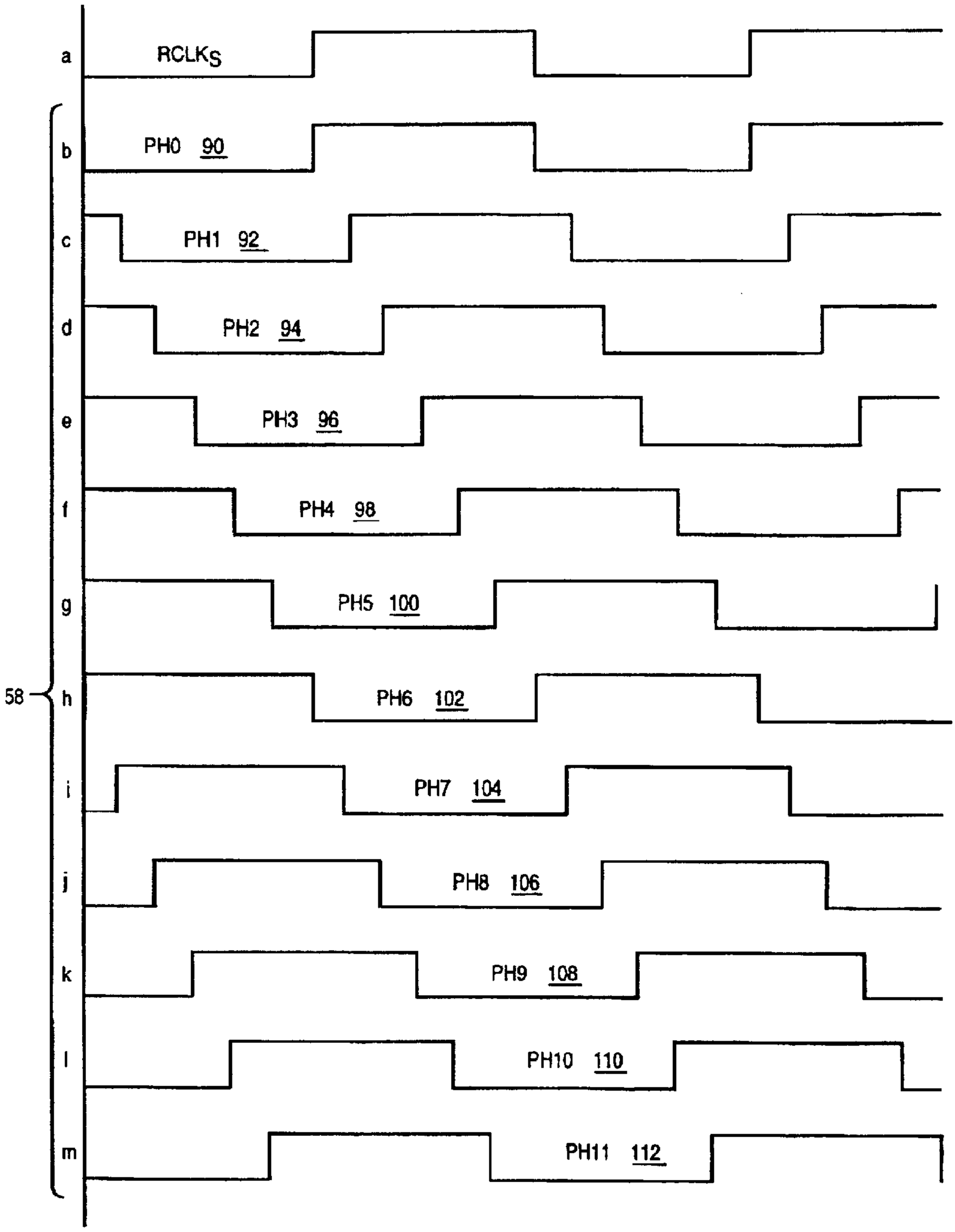
a
RCLKS
58
b
PH0 90
c
PH1 92
d
PH2 94
e
PH3 96
f
PH4 98
g
PH5 100
h
PH6 102
i
PH7 104
j
PH8 106
k
PH9 108
l
PH10 110
m
PH11 112

FIG_4

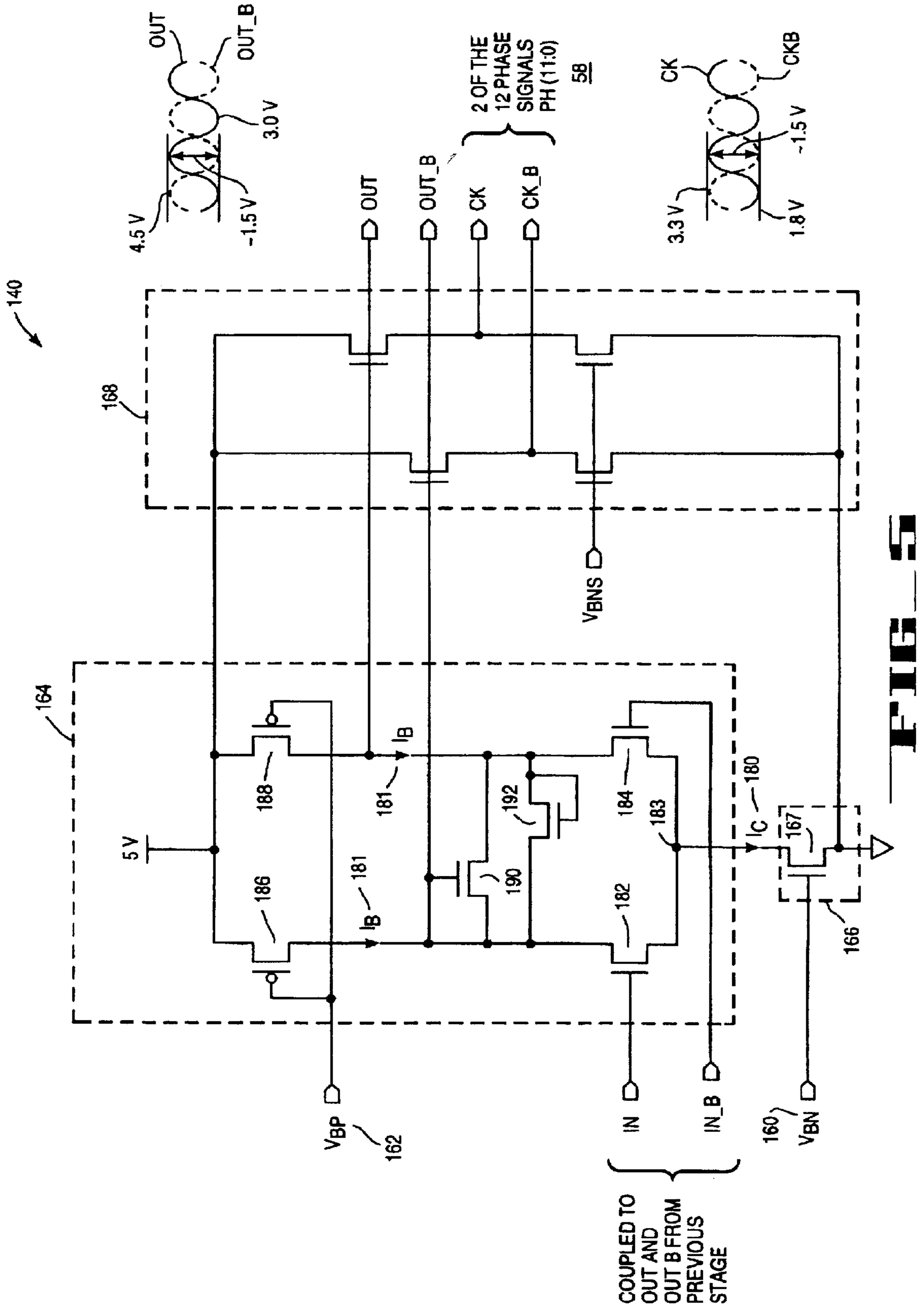
140
168
OUT
OUT_B
4.5 V
-1.5 V
3.0 V
OUT
OUT_B
CK
CK_B
2 OF THE 12 PHASE SIGNALS PH(11:0)
58
CK
CKB
3.3 V
1.8 V
-1.5 V
VBNS
164
188
186
181
IB
5 V
190
192
184
183
182
IC
180
167
166
VBP
162
160
VBN
IN
IN_B
COUPLED TO OUT AND OUT B FROM PREVIOUS STAGE

FIG. 5

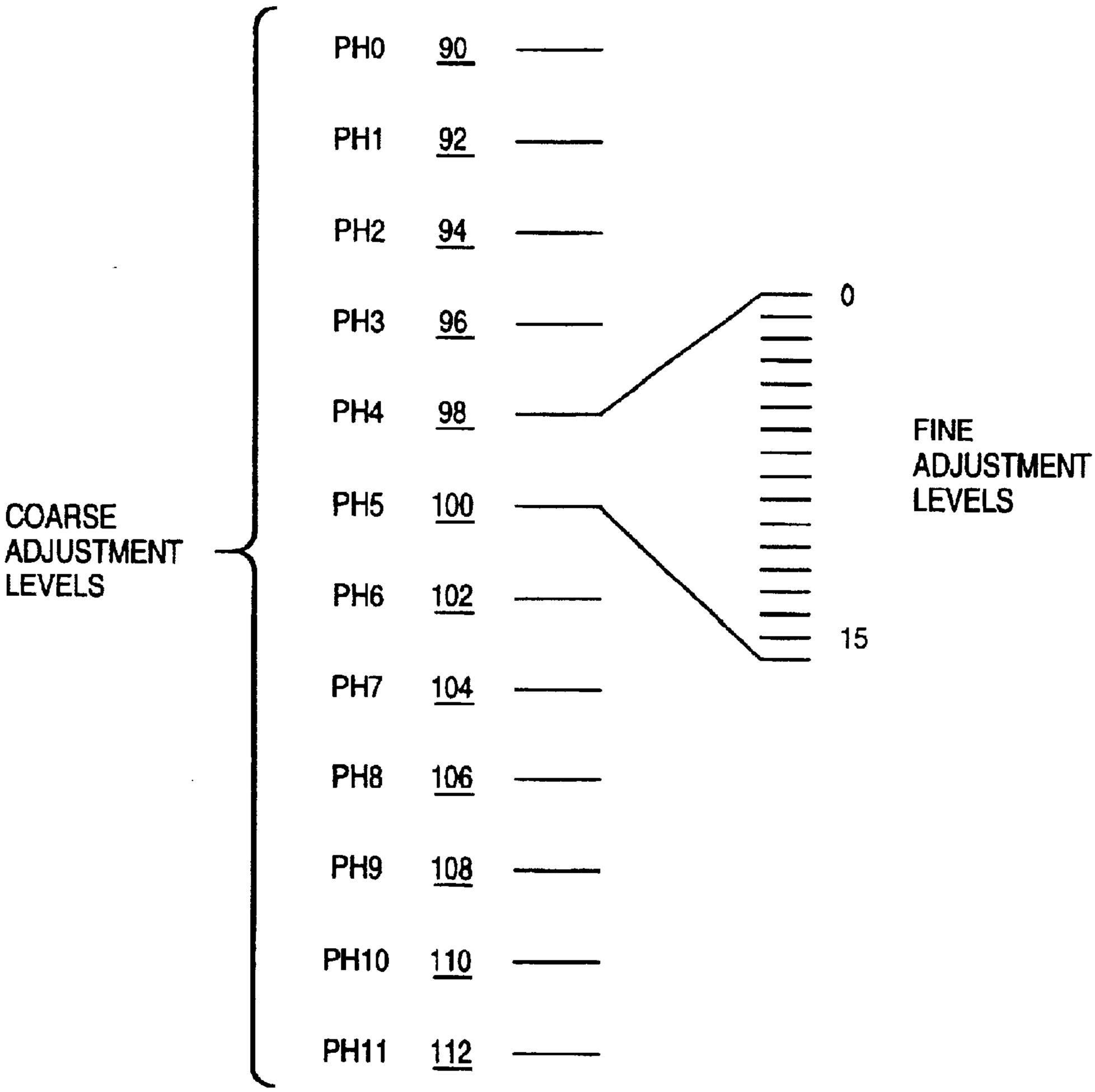
PH0 90
PH1 92
PH2 94
PH3 96
PH4 98
PH5 100
PH6 102
PH7 104
PH8 106
PH9 108
PH10 110
PH11 112
COARSE ADJUSTMENT LEVELS
0
15
FINE ADJUSTMENT LEVELS

FIG_6

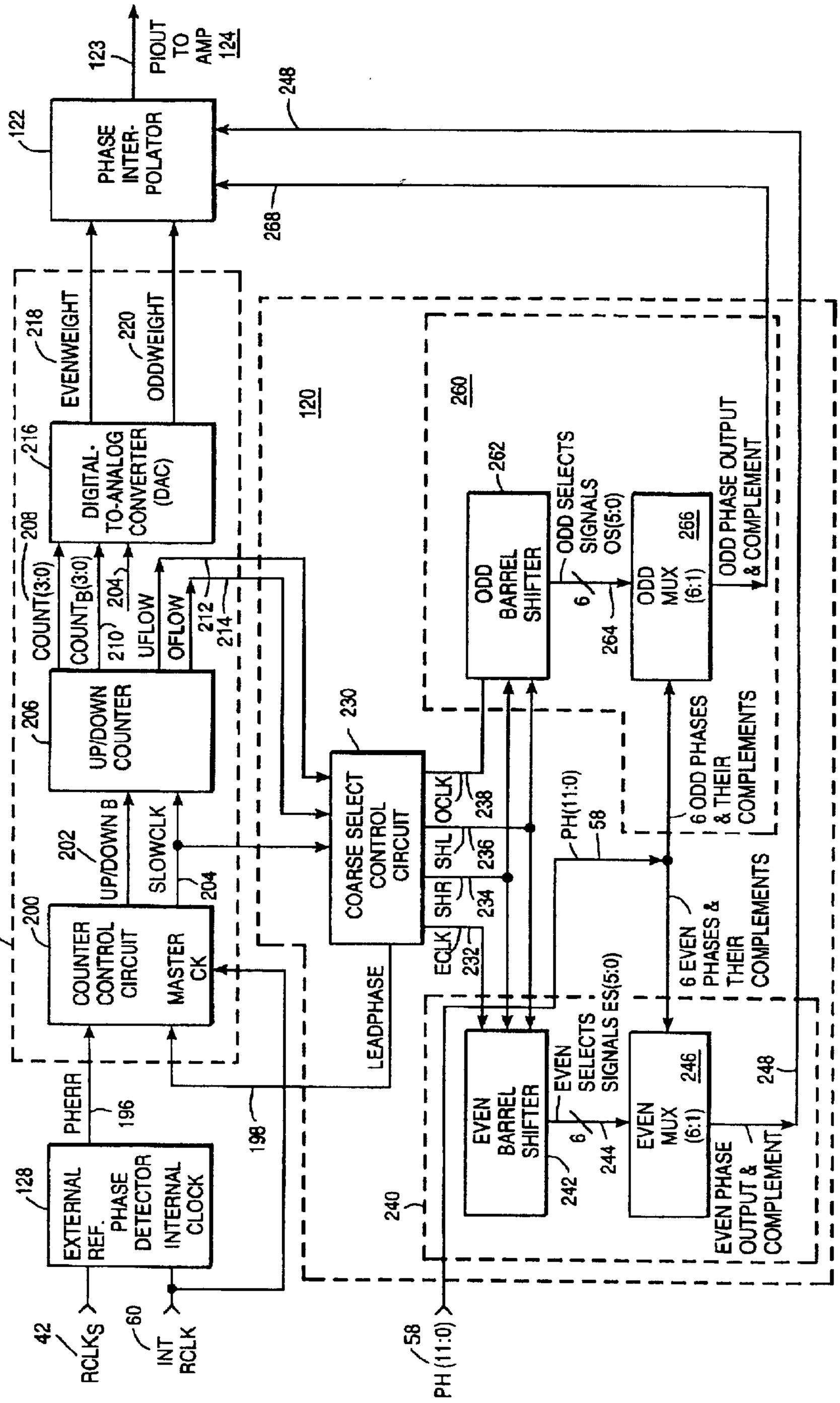
55
130
120
260
PHASE INTER-POLATOR
122
123
PIOUT TO AMP 124
248
268
DIGITAL-TO-ANALOG CONVERTER (DAC)
216
208
COUNT(3:0)
COUNTB(3:0)
210
204
UFLOW
OFLOW
212
214
EVENWEIGHT
218
ODDWEIGHT
220
UP/DOWN COUNTER
206
UP/DOWN B
202
SLOWCLK
204
COUNTER CONTROL CIRCUIT
200
MASTER CK
COARSE SELECT CONTROL CIRCUIT
230
LEADPHASE
198
OCLK
238
SHL
236
SHR
234
ECLK
232
ODD BARREL SHIFTER
262
ODD SELECTS SIGNALS OS(5:0)
6
264
ODD MUX (6:1) 266
ODD PHASE OUTPUT & COMPLEMENT
PH(11:0)
58
6 ODD PHASES & THEIR COMPLEMENTS
6 EVEN PHASES & THEIR COMPLEMENTS
EVEN BARREL SHIFTER
242
EVEN SELECTS SIGNALS ES(5:0)
6
244
EVEN MUX (6:1) 246
248
EVEN PHASE OUTPUT & COMPLEMENT
240
PHERR
196
EXTERNAL REF. PHASE DETECTOR
128
INTERNAL CLOCK
42
RCLKS
60
INT RCLK
58
PH(11:0)

FIG. 7

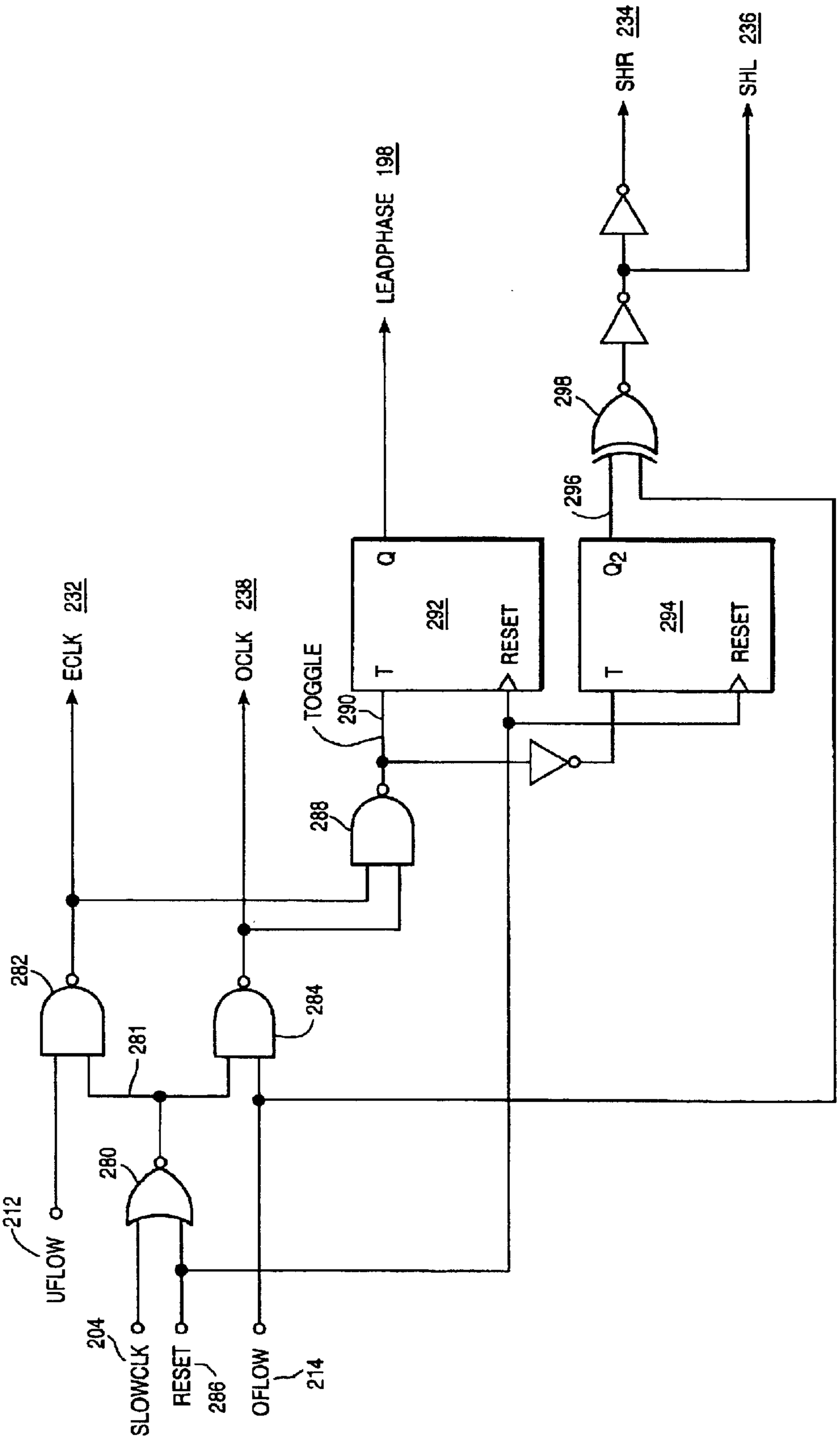
230
ECLK 232
OCLK 238
TOGGLE 290
LEADPHASE 198
SHR 234
SHL 236
Q
292
T
RESET
Q_2
294
298
296
288
282
281
284
280
212
UFLOW
204
SLOWCLK
RESET
286
OFLOW
214

FIG. 8

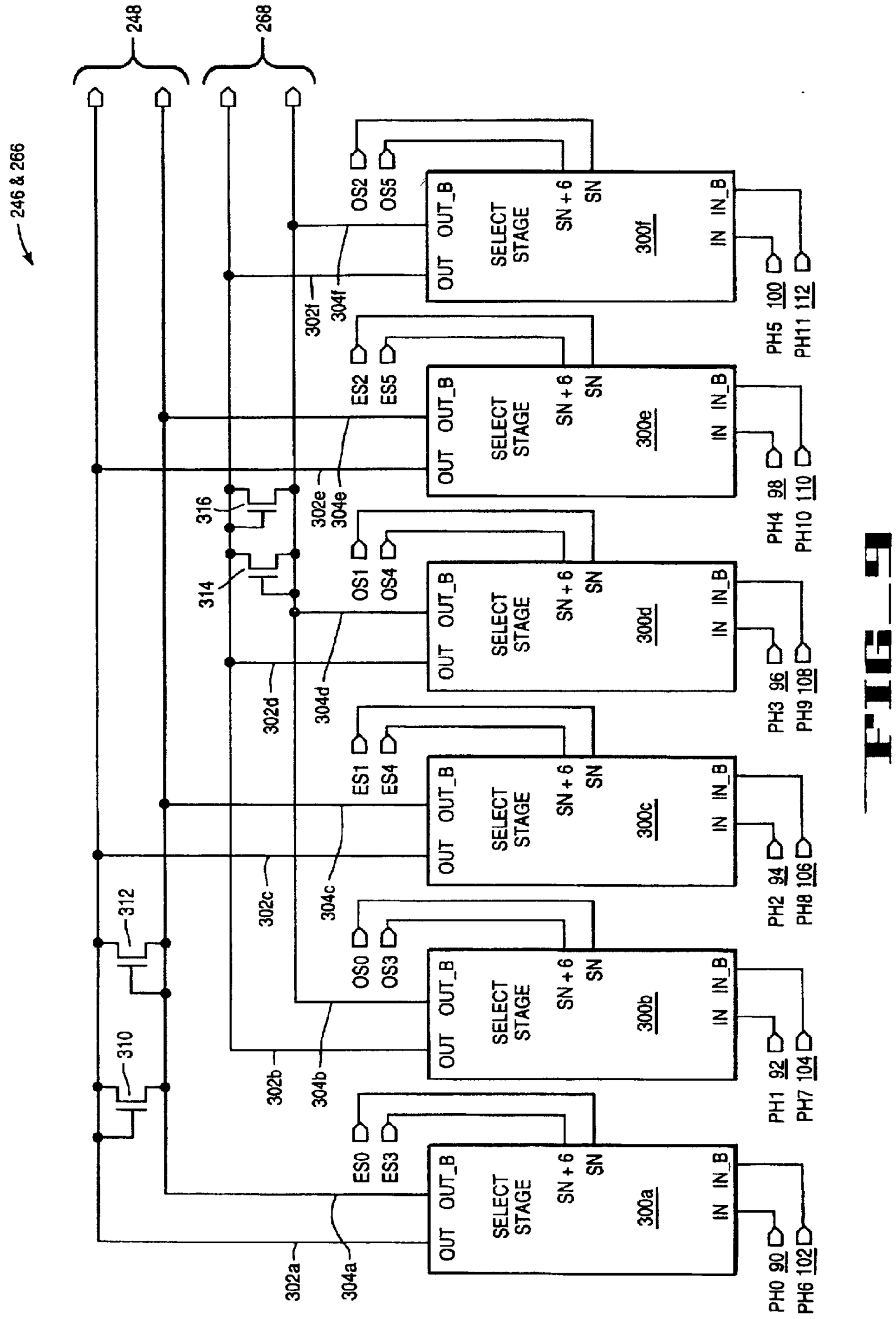
248
268
246 & 266
OS2
OS5
SELECT STAGE
SN + 6
SN
OUT OUT_B
IN IN_B
300f
302f
304f
PH5 100
PH11 112
ES2
ES5
300e
302e
304e
PH4 98
PH10 110
316
314
OS1
OS4
300d
302d
304d
PH3 96
PH9 108
ES1
ES4
300c
302c
304c
PH2 94
PH8 106
312
310
OS0
OS3
300b
302b
304b
PH1 92
PH7 104
ES0
ES3
300a
302a
304a
PH0 90
PH6 102

FIG. 5

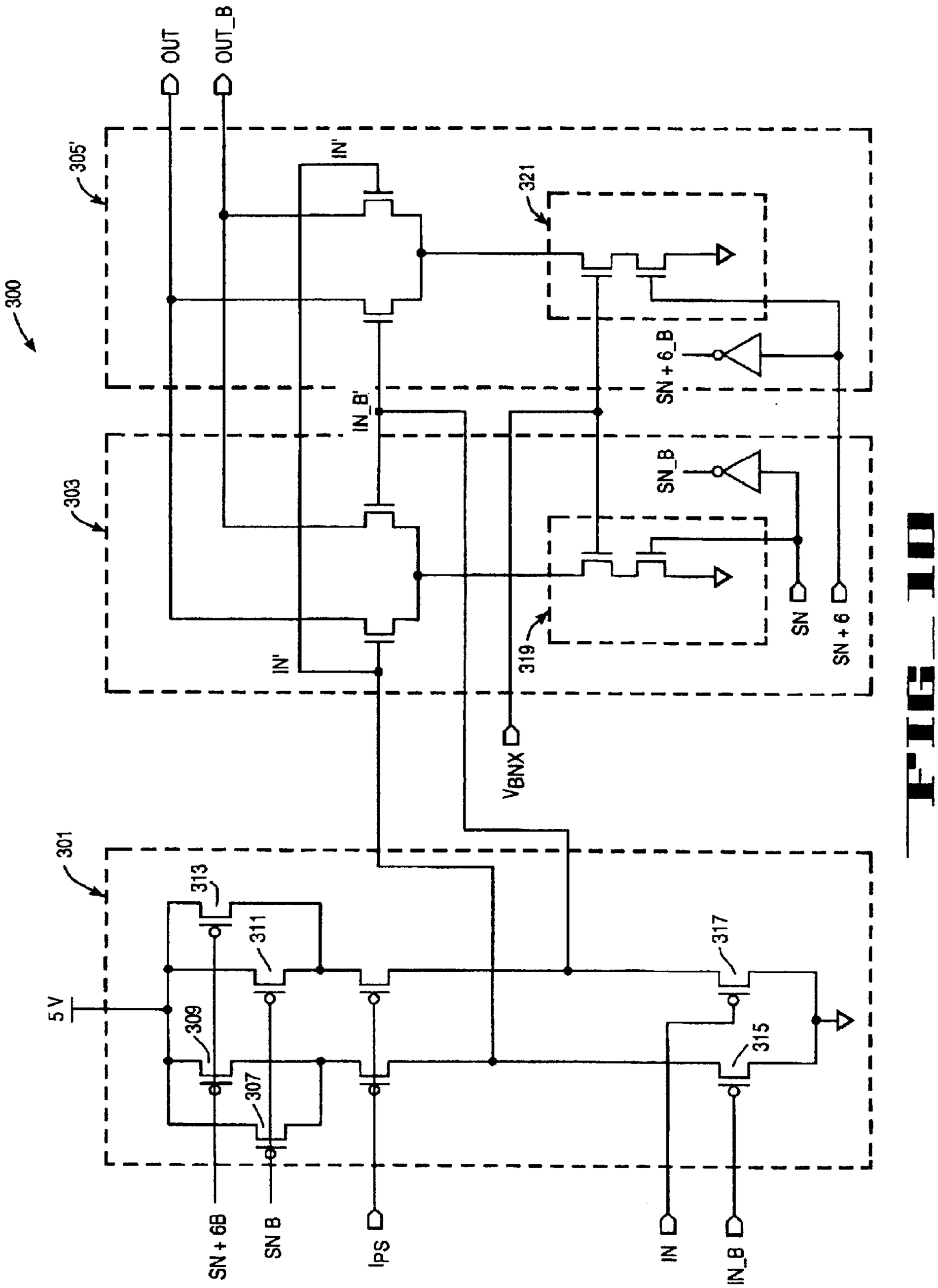
300
301
303
305'
319
321
OUT
OUT_B
IN'
IN_B'
IN'
SN + 6_B
SN_B
SN
SN + 6
V_{BNX}
5 V
313
311
309
307
317
315
SN + 6B
SN B
I_{PS}
IN
IN_B

FIG. 10

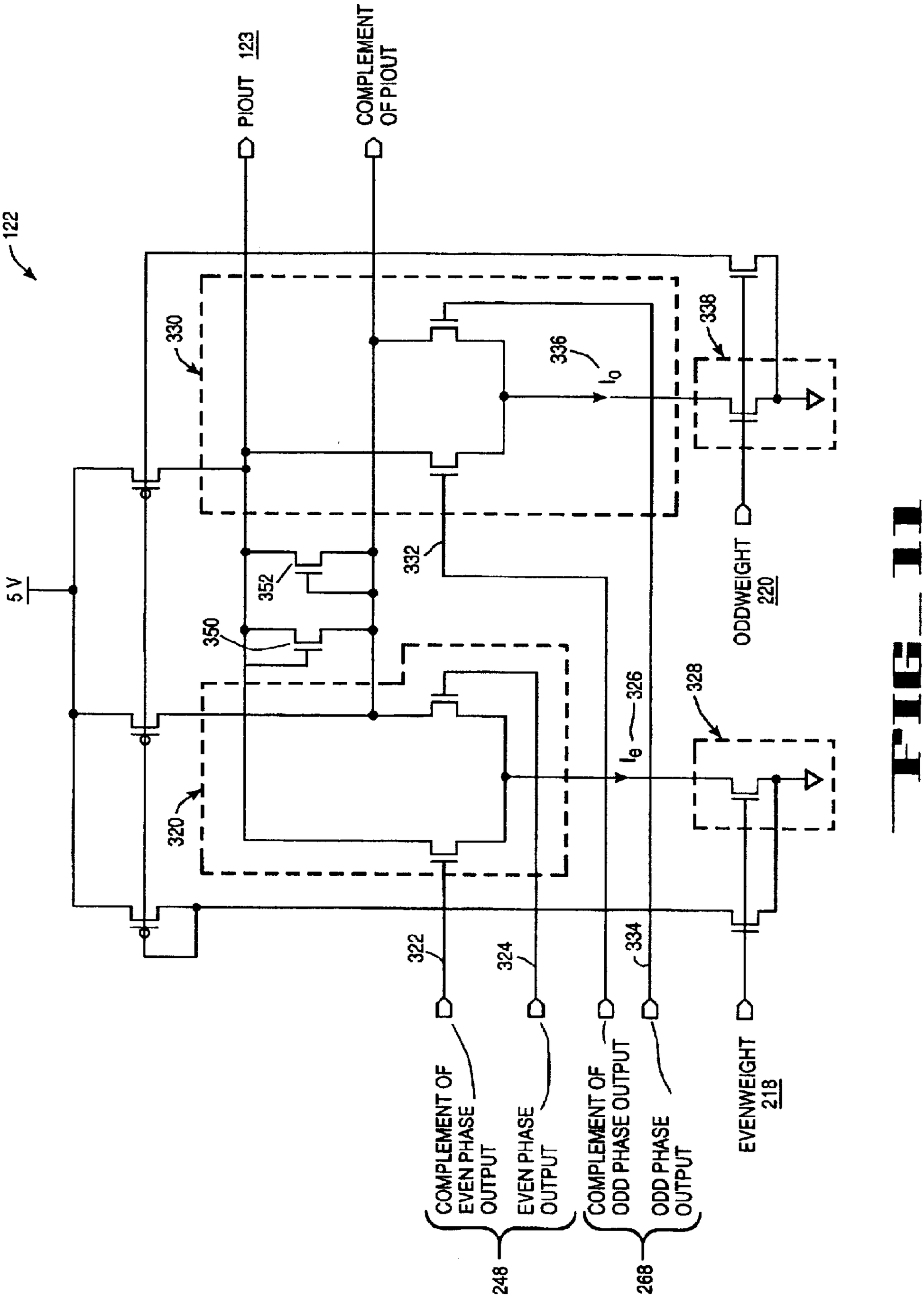
122
330
336
I_O
338
332
352
350
320
326
I_e
328
322
324
334
5 V
COMPLEMENT OF EVEN PHASE OUTPUT
EVEN PHASE OUTPUT
COMPLEMENT OF ODD PHASE OUTPUT
ODD PHASE OUTPUT
248
268
EVENWEIGHT 218
ODDWEIGHT 220
PIOUT 123
COMPLEMENT OF PIOUT

FIG. 11

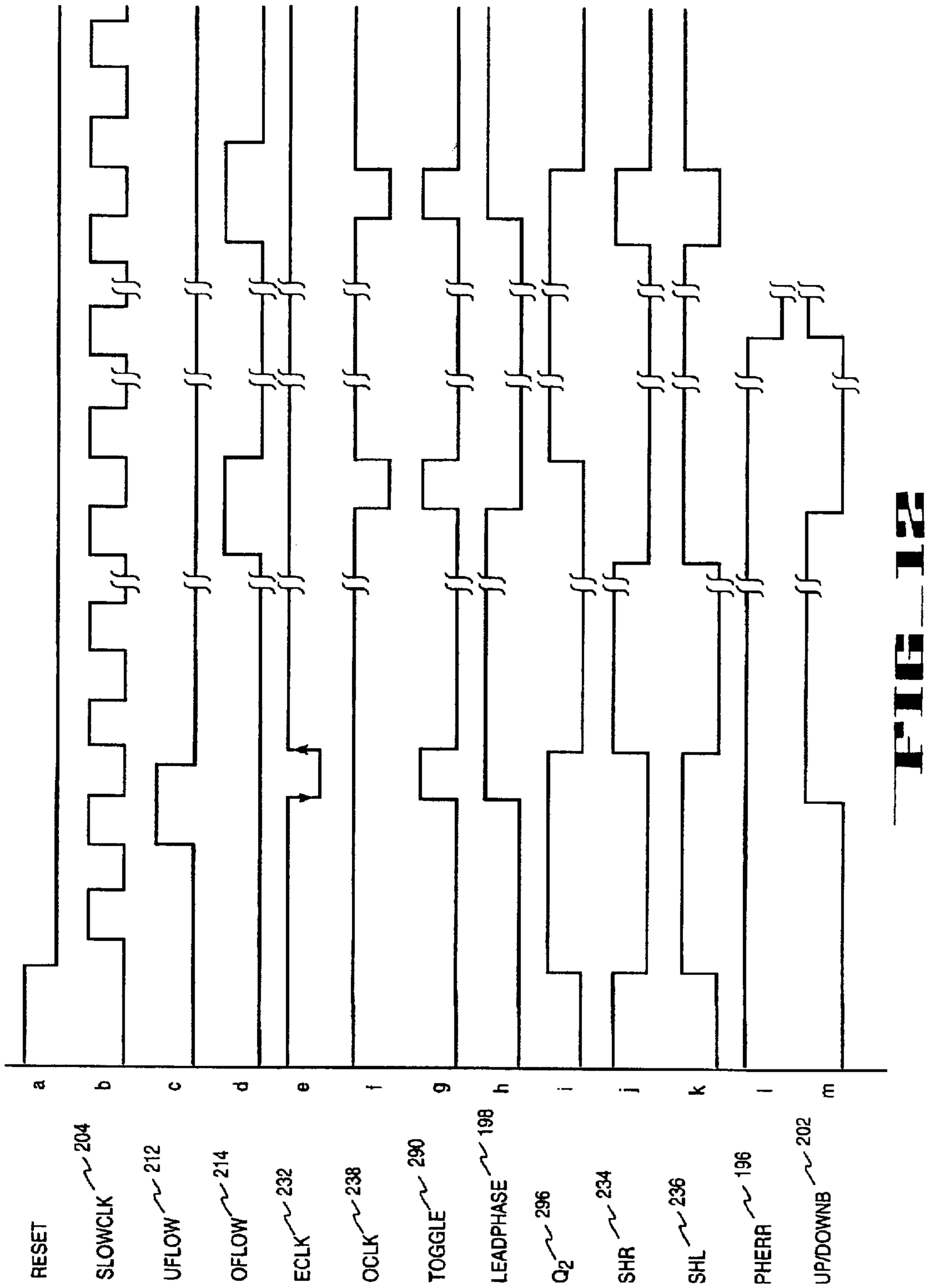
RESET
SLOWCLK 204
UFLOW 212
OFLOW 214
ECLK 232
OCLK 238
TOGGLE 290
LEADPHASE 198
Q_2 296
SHR 234
SHL 236
PHERR 196
UP/DOWNB 202
a
b
c
d
e
f
g
h
i
j
k
l
m

FIG. 12

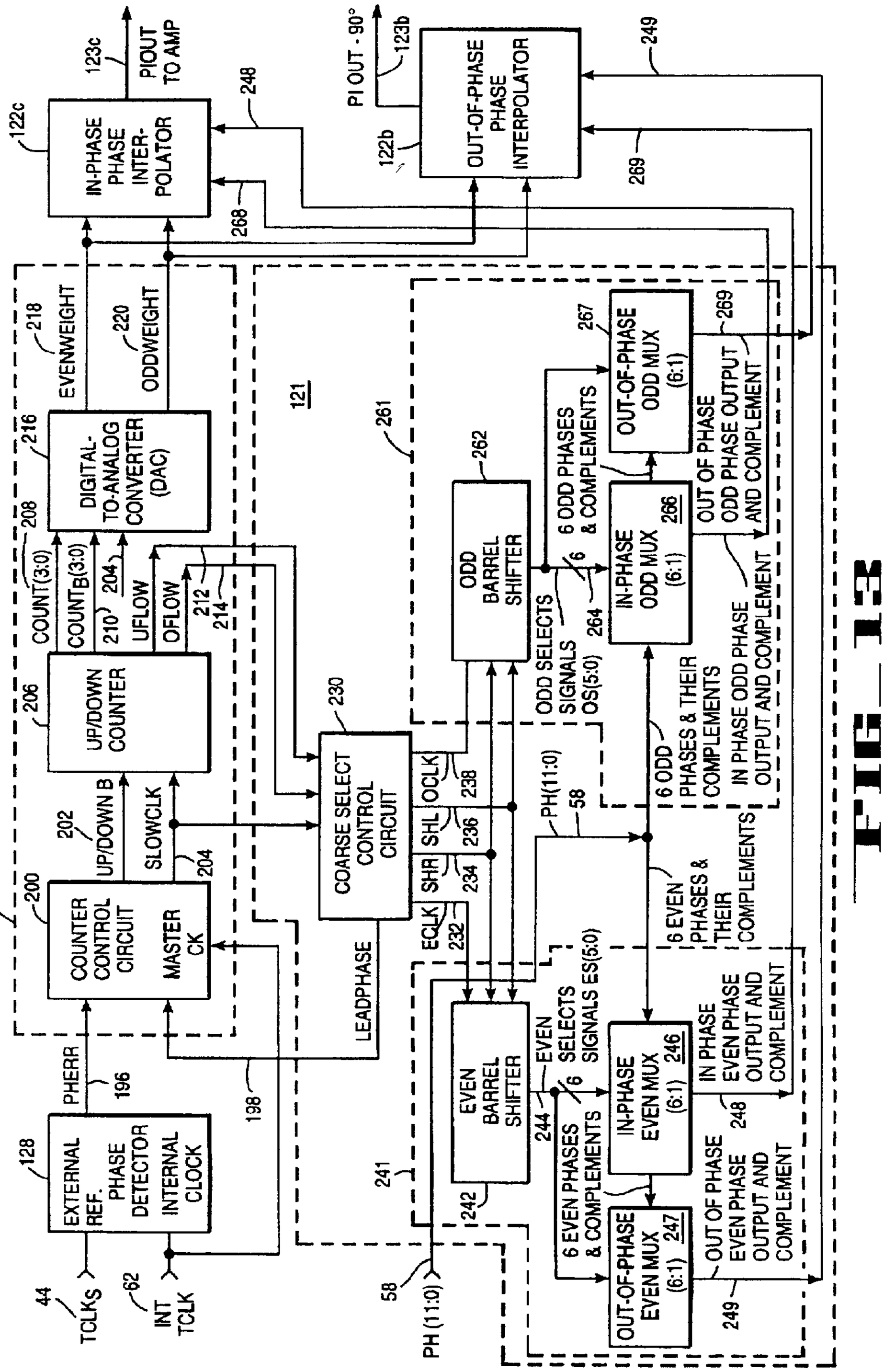
57
130
121
261
PIOUT TO AMP
123c
122c
IN-PHASE PHASE INTER-POLATOR
248
PI OUT - 90°
123b
122b
OUT-OF-PHASE PHASE INTERPOLATOR
249
269
268
EVENWEIGHT
218
ODDWEIGHT
220
DIGITAL-TO-ANALOG CONVERTER (DAC)
216
208
COUNT(3:0)
COUNT_B(3:0)
210
204
UFLOW
OFLOW
212
214
UP/DOWN COUNTER
206
UP/DOWN B
202
SLOWCLK
204
COUNTER CONTROL CIRCUIT
MASTER CK
200
PHERR
196
198
LEADPHASE
COARSE SELECT CONTROL CIRCUIT
230
EXTERNAL REF. PHASE DETECTOR
INTERNAL CLOCK
128
44
TCLKS
62
INT TCLK
ODD BARREL SHIFTER
262
6 ODD PHASES & COMPLEMENTS
OUT-OF-PHASE ODD MUX (6:1)
267
IN-PHASE ODD MUX (6:1)
266
OUT OF PHASE ODD PHASE OUTPUT AND COMPLEMENT
269
ODD SELECTS
SIGNALS
OS(5:0)
264
6
PH(11:0)
58
6 ODD PHASES & THEIR COMPLEMENTS
IN PHASE ODD PHASE OUTPUT AND COMPLEMENT
6 EVEN PHASES & THEIR COMPLEMENTS
EVEN BARREL SHIFTER
EVEN SELECTS
SIGNALS ES(5:0)
244
IN-PHASE EVEN MUX (6:1)
246
IN PHASE EVEN PHASE OUTPUT AND COMPLEMENT
248
6 EVEN PHASES & COMPLEMENTS
OUT-OF-PHASE EVEN MUX (6:1)
247
OUT OF PHASE EVEN PHASE OUTPUT AND COMPLEMENT
249
241
242
ECLK
232
SHR
234
SHL
236
OCLK
238

FIG. 13

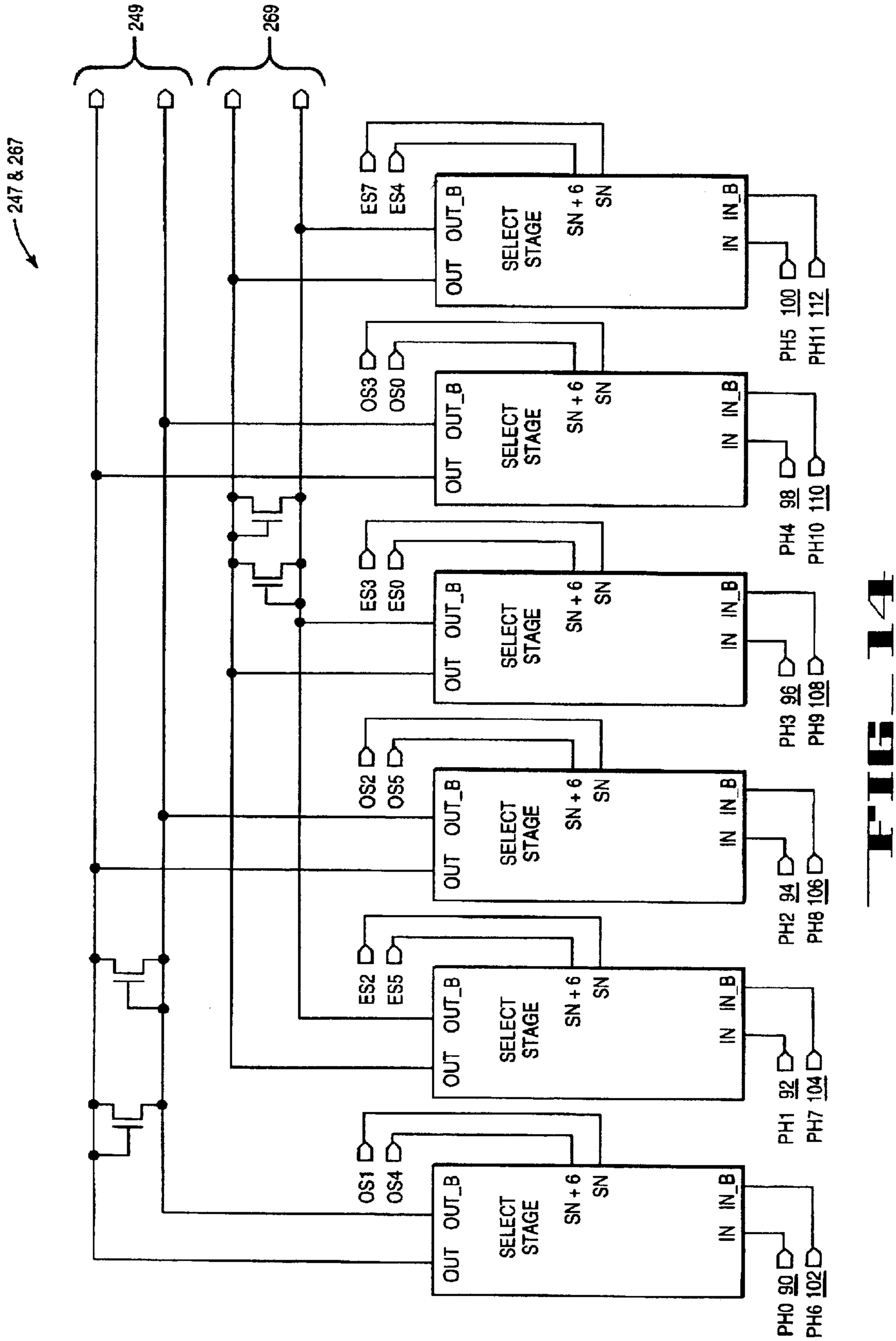
249
269
247 & 267
ES7
ES4
OS3
OS0
ES3
ES0
OS2
OS5
ES2
ES5
OS1
OS4
OUT OUT_B
SELECT STAGE
SN + 6
SN
IN IN_B
PH5 100
PH11 112
PH4 98
PH10 110
PH3 96
PH9 108
PH2 94
PH8 106
PH1 92
PH7 104
PH0 90
PH6 102

FIG. 14

DELAY STAGE CIRCUITRY FOR A RING OSCILLATOR

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of application Ser. No. 08/347,844, filed Dec. 1, 1994 (now U.S. Pat. No. 5,596,610), which is a continuation of application Ser. No. 08/161,769, filed Dec. 2, 1993 (now abandoned), which is a divisional of application Ser. No. 07/890,034, filed May 28, 1992 (now abandoned).

FIELD OF INVENTION

The present invention relates to clock synchronization circuitry including a cascaded phase locked loop. In particular the present invention relates to a delay stage for a ring oscillator and a fine phase tuning circuitry, both used in the cascaded phase locked loop.

BACKGROUND OF THE INVENTION

Clock synchronization in integrated circuits is typically performed by a phase locked loop (PLL).

Some prior PLLs use a ring oscillator as a voltage controlled oscillator. A ring oscillator is a chain of inversion elements coupled together in a negative feedback fashion, with each element contributing a delay amount which adds up to half an oscillation period. Some prior phase locked loop implementations using ring oscillators suffer phase offset and deadband problems, which are difficult to minimize without compromising one or the other.

One disadvantage of prior ring oscillators is that the number of phase signals that can be generated are limited by the number of inversion elements contained in the ring oscillator. The number of inversion elements is, in turn, limited by the length of time delay contributed by each inversion element. The greater the time delay of the inversion element, the fewer the number of inversion elements that can be included in the ring oscillator.

Another disadvantage of some prior oscillators is that they must include an odd number of inversion elements to develop a phase shift of greater than 180°.

Other prior PLLs use voltage controlled delay line to generate the phase shift necessary for oscillation. Such prior PLLs have a limited delay range, typically a clock period or less. Hence, the frequency of operation of such prior PLLs is very limited. Prior PLLs including delay lines also tend to be susceptible to supply noise because of their use of CMOS inverters, which couple supply noise directly into output signals.

SUMMARY AND OBJECTS OF THE INVENTION

One object of the present invention is to provide a method and circuitry for synchronizing internal device functions to an external clock.

Another object of the present invention is to provide a method and circuitry for clock synchronization that allows phase deadband characteristics to be easily optimized.

Another object of the present invention is to provide a method and circuitry for clock synchronization that allows easy optimization of stability characteristics.

Another object of the present invention is to provide a method and circuitry for clock synchronization that minimizes the affect of the delay of clock buffers.

Another object of the present invention is to provide a method and circuitry for clock synchronization that minimizes the affect of a cock distribution network on loop stability.

A still further object of the present invention is to provide a method and circuitry for clock synchronization that allows easy optimization of loop bandwidth.

A further object of the present invention is to provide a method and circuitry for clock synchronization that provides high rejection of power supply noise.

Another object of the present invention is to provide a method and circuitry for fine phase adjustment with small static phase error and high loop stability.

Another object of the present invention is to provide a method and circuitry for phase adjustment in which there are no boundary conditions or start up conditions to be concerned with.

Another object of the present invention is to provide a method and circuitry for clock synchronization that provides smooth phase adjustment.

Another object of the present invention is to provide a method and circuitry for clock synchronization that is suitable for a wide range of frequencies.

Another object of the present invention is to provide a method and circuitry for clock synchronization that minimizes restart response time after power down.

Another object of the present invention is to provide a method and circuitry for clock synchronization that compensates for the delays associated with data input circuitry and data output circuitry.

A still further object of the present invention is to provide a method and circuitry for clock synchronization that generates an output signal with an controlled phase offset with respect to the input reference signal.

A method of performing phase adjustment in a phase locked loop is described. First, two phase signals are selected from a multiplicity of phase signals. The two selected phase signals are selected by a select signal. Next, an output signal is generated by interpolating between the two selected phase signals. The contribution of each of the two selected phase signals to the output signal is determined by a weighting signal.

Also described is phase tuning circuitry, which includes a phase selector and a phase interpolator. The phase selector selects two phase signals from a multiplicity of phase signals in response to a select signal. The two selected phase signals are coupled to the phase interpolator. The phase interpolator generates an output signal by interpolating between the two selected phase signals. The relative contribution of each of the two selected phase signals to the output signal is determined by a weighting signal.

Also described is a delay stage for a ring oscillator. The ring oscillator includes an even number of cascaded delay stages. Each delay stage includes a differential amplifier, which generates two complementary output signals. Coupled between the complementary output signals, two voltage clamping means limit the peak-to-peak voltage swing of the output signal. Limiting the peak-to-peak voltage swing of the output signal speeds-up the delay stage and allows the ring oscillator to includes a greater number of delay stages.

Other objects, features, and advantages of the present invention will be apparent from the accompanying drawings and the detailed description that follows.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings in which like references indicate similar elements and in which:

FIG. **1** is a block diagram of a high speed computer bus.

FIG. **2** is a block diagram of a phase locked loop.

FIG. **3** is a block diagram of the VCO.

FIG. **4** is a diagram of the relationship between the external reference signal and the phase signals output by the VCO.

FIG. **5** is a schematic diagram of a delay stage of the VCO.

FIG. **6** is an illustration of the phase adjustment levels of the phase selection circuitry and the phase interpolator.

FIG. **7** is a detailed block diagram of the receive subloop within the phase locked loop.

FIG. **8** is a schematic diagram of the coarse select control circuit.

FIG. **9** is a block diagram of the even multiplexer and the odd multiplexer.

FIG. **10** is a schematic diagram of a multiplexer select stage.

FIG. **11** is a schematic diagram of the phase interpolator.

FIG. **12** is a timing diagram for a subloop of the phase locked loop.

FIG. **13** is a detailed block diagram of the transmit subloop within the phase locked loop.

FIG. **14** is a block diagram of the out-of-phase even multiplexer and the out-of-phase odd multiplexer.

DETAILED DESCRIPTION

FIG. **1** is a block diagram of a high speed digital computer bus system **20**. Devices **30** and **32** use clock synchronization circuitry **36** to synchronize the transfer of data between data bus **38**. Clock synchronization circuitry **36** is a cascaded phase locked loop (PLL) **36**. The main loop of PLL **36** utilizes a ring voltage controlled oscillator (VCO), which includes an even number of cascaded delay stages of the present invention. Two subloops coupled to the main loop perform fine phase tuning according to the method and circuitry of the present invention to generate two internal clock signals.

As will be described in more detail below, each delay stage of the present invention generates two complementary output signals using a differential amplifier. Coupled between the two complementary output signals, two clamping devices limit the peak-to-peak voltage swing of the complementary output signals. When the delay stages are cascaded together, they provide twelve different phase signals that are used by the subloops.

The method and circuitry for fine phase adjustment used in the subloops also will be described in detail below. Briefly described, the phase tuning circuitry of the present invention includes a phase selector and a phase interpolator. The phase selector selects an even phase signal and an odd phase signal from the twelve phase signals output by the VCO of the main loop. The even and odd phase signals are selected by an even select signal and an odd select signal, respectively. The phase interpolator interpolates between the even phase signal and the odd phase signal to generate an output signal. The effect of the even phase signal and the odd phase signal on the output signal is determined by an even weighting signal and an odd weighting signal, respectively. The weighting signals allow even phase signals and odd phase signals to switch without introducing jitter onto the output signal.

The high speed digital computer bus system **20** of FIG. **1** includes master device **30**, slave devices **32**, only one of which is shown, and data bus **38**. Data bus **38** transfers data between devices **30** and **32** at data rates up to 500 MBytes per second, in the preferred embodiment.

Master device **30** is an intelligent device, such as a microprocessor, an application specific integrated circuit (ASIC), a memory controller, or a graphics engine. Master **30** differs from slave device **32** in that master device **30** initiates data requests, such as requests to read or write slave devices **32**.

Slave devices **32** do not include as much intelligence as master device **30** and can only respond to data requests. Slave devices **32** may be dynamic random access memories (DRAMs), static random access memories (SRAMs), read only memories (ROMs), electrically programmable read only memories (EPROMs), or flash memories.

Master device **30** and slave devices **32** transfer data synchronously. That is, data transfers are referenced to the clock edges of clock signals CLOCKFROMMASTER **42** and CLOCKTOMASTER **44**. Both clock signals **42** and **44** are generated by clock source **46**. Both clock signals **42** and **44** are carried by a single clockline, which turns around near master device **30**. From there, the clockline extends back toward clock source **46**, where it is terminated. As a result, both CLOCKFROMMASTER **42** and CLOCKTOMASTER **44** run at the same frequency. The phase shift between clock signals **42** and **44** varies depending upon the location of devices **30** and **32** relative to the turnaround in the clockline. The phase difference between clock signals **42** and **44** is approximately 0° near the turnaround and increases as distance from the turnaround increases.

Slave devices **32** transmit data with the edges of CLOCKTOMASTER **44** and receive data with CLOCKFROMMASTER **42**. Analogously, master device **30** transmits data with the edges of CLOCKFROMMASTER **42** and receives data with CLOCKTOMASTER **44**. Clock and data signals remain synchronized as they propagate toward their destination because clock lines **42** and **44** and data bus **38** are matched for delay.

Devices **30** and **32** interface with data bus **38** and clock signals **42** and **44** using interface **34**. Interface **34** performs a number of tasks. Among those tasks, interface **34** converts the low voltage levels of data bus **38** to ordinary CMOS levels. Interface **34** also generates internal clocks for receiving and transmitting data. Interface **34** uses clock synchronization circuitry **36** to perform voltage level conversion and clock synchronization.

FIG. **2** illustrates in block diagram form clock synchronization circuitry **36** that is the heart of interface **34**. Phase locked loop **36** synchronizes the reception of data to the device's external receive clock, CLOCKTOMASTER **44** or CLOCKFROMMASTER **42**, as the case may be. Similarly, phase locked loop **36** synchronizes the transmission of data with the device's external transmit clock, CLOCKTOMASTER **44** or CLOCKFROMMASTER **42**, as the case may be.

Phase locked loop **36** performs both synchronization tasks using a cascaded design, which includes main loop **52** and two subloops, a receive subloop **54** and a transmit subloop **56**. Main loop **52** acquires and tracks frequency, outputting **12** phase signals, PH(11:0) **58**, all with the same frequency, to subloops **54** and **56**. Subloops **54** and **56** perform fine

phase tracking of clock signals **42** and **44** by selecting two phase signals from PH(11:0) **58**. The two selected phase signals are interpolated to generate internal receive and transmit clock signals, INTRCLK **60**, INTTCLK **62**, and LEADING INTTCLK **63**. INTRCLK **60** is in-phase with external receive clock **42**. INTTCLK **62** is also in phase with its external reference clock signal, $TCLK_S$ **44**. In contrast, LEADING INTTCLK **63** leads $TCLK_S$ **44** by 90° in a preferred embodiment.

Main loop **52** uses a conventional second order architecture to track and acquire signal frequencies ranging from 50 MHz to 250 MHz. Main loop **52** has a short pull in time of less than 10 usec. The amount of static phase error generated by main loop **52** has no affect upon the phase tracking accuracy of PLL **36** because subloops **54** and **56** perform phase acquisition. Thus, static phase error in main loop **52** may be, and is, traded for reduced deadband and improved stability characteristics. In contrast, the jitter of phase signals PH(11:0) **58** is minimized because it directly affects the jitter within subloops **54** and **56**.

Optimization of the stability of phase signals PH(11:0) **58** is further aided by the cascaded design of PLL **36**. Clock distribution and buffering is performed by subloops **54** and **56**, rather than main loop **52**. Thus, main loop stability is unaffected by buffer and clock distribution delay. Consequently, main loop bandwidth may be easily optimized and the size of filter **[82]** *84* reduced. This is particularly important in embodiments in which filter **84** and all of PLL **36** is fabricated on a single die.

Main loop **52** includes amplifiers **74** and **76**, counters **78**, frequency-phase detector (FPD) **80**, charge pump **82**, filter **84**, and voltage controlled oscillator (VCO) **86**.

Amplifier **74** amplifies $RCLK_S$ to a voltage swing of 0 volts to 5 volts, as required by FPD **80**. Amplifier **76** similarly amplifies PH**0** **90** to a voltage swing of 0 volts to 5 volts. The gain of amplifiers **74** and **76** necessarily differ because the voltage swings of $RCLK_S$ and PH**0** **90** differ. This difference in amplification prior to frequency and phase detection by FPD **80** introduces static phase error into main loop **52**. The static phase error so introduced is tolerable because it does not affect the phase tuning of subloops **54** and **56**.

Prefered implementations of phase locked loop **36** include counters **78** to increase the frequency range of PLL **36**. Counters **78** divide the frequency of their inputs by two, prior to coupling their outputs to FPD **80**. Counters **78** thus enhance the frequency response of FPD **80** by expanding the range of frequencies that FPD **80** can accommodate.

FPD **80** is a sequential frequency detector, selected for its large tracking range and short pull-in time.

Charge pump **82** converts the output of FPD **80** into current pulses. Charge pump **82** eliminates deadband with its high input sensitivity. Charge pump **82** introduces static phase error because its mechanisms for switching from a high-to-low output and from a low-to-high output are not symmetrical. This static phase error is tolerable because main loop **52** does not perform phase tuning. Thus, charge pump **82** may, and does, differ from prior charge pumps because within main loop **52** dead band characteristics may be reduced without concern for static phase error.

Filter **84** converts the current pulses into the analog control voltage **85** coupled to VCO **86** using a standard one-pole, one zero, passive filter.

VCO **86** is a six delay stage ring oscillator. Each delay stage generates two of the twelve phase signals. PH(11:0) **58**. The differential design of the VCO stage provides high power-supply rejection (PSR), as well as complementary outputs.

FIG. **3** illustrates in block diagram form ring voltage controlled oscillator **86**. VCO **86** varies from previous ring oscillators in two respects. First, VCO **86** includes an even number of delay stages **140**. VCO **86** is able to generate 180° phase shift with an even number of delay stages **140** because each delay stage **140** generates two complementary outputs that are appropriately coupled to the next delay stage. Second, VCO **86** includes a greater number of delay stages than normal. VCO **86** is able to include more delay stages because each delay stage **140** contributes less delay then prior delay stages.

Each delay stage **140**a–**140**f of VCO **86** generates two pairs of complementary output signals, OUT and OUTB, and CK and CKB. CK and CKB are buffered, level shifted versions of OUT and OUTB. Thus, CK and CKB have the same voltage swings and frequencies as OUT and OUTB. The buffering of CK and CKB prevents their loading from affecting the stability of VCO **86**.

Delay stages **140**a–**140**f are coupled together via OUT and OUTB so that the entire phase shift from the input of delay stage **140**a to the output of delay stage **140**f is greater than or equal to 180° at the oscillation frequency. Outputs OUT of delay stages **140**a–**140**e are coupled together to the INB inputs of the next delay stage **140**b–**140**f. Outputs OUTB of delay stages **140**a–**140**e are coupled to inputs IN of delay stages **140**b–**140**f. Only the coupling between delay stages **140**f and **140**a varies from this pattern.

Outputs CK and CKB of each stage stage **140**a–**140**f are coupled to subloops **54** and **56** as two of the twelve phases **58** output by VCO **86**.

Control voltage, V_c **85**, controls the frequency at which each delay stage **140**a–**140**f switches via bias voltage, V_{BN} **160**, V_c **85** can vary between 3.5 volts to 0 volts, giving VCO **86** a wide locking range, V_c **85** also ensures that phase signals PH(11:0) **58** have a symmetrical voltage swing via bias voltage, V_{BP} **162**.

FIG. **4** illustrates the relationship between the twelve phase signals **58** generated by VCO **86**. When PLL **36** is in lock PH**0** **90** should be in-phase with reference signal, $RCLK_S$, except for the static phase error contributed by amplifiers **74** and **76**, and charge pump **82**. The remaining phases, PH(11:1) **58**, are evenly spaced across the clock period of $RCLK_S$.

The first stage of VCO **86**, delay stage **140**a, output PH**0** **90** and PH**6** **102**. These signals may be referred to as PH**0** and its complement or PH**6** and its complement.

The second delay stage **140**b generates PH**1** **92** and PH**7** **104**. These signals are also referred to as PH**1** and it complement or PH**7** and its complement.

PH**2** **94** and PH**8** **106** are the outputs of the delay stage **140**c. These signals are also referred to as PH**2** and its complement or PH**8** and its complement.

Complementary phase signals PH**3** **96** and PH**9** **108** are generated by delay stage **140***d*.

The fifth delay stage **140**e generates the complementary phase signals PH**4** **98** and PH**10** **110**.

Delay stage **140**f generates PH**5** **100** and PH**11** **112**. These signals are also referred to as PH**5** and its complement or PH**11** and its complement.

FIG. **5** is a schematic diagram of a delay stage **140** within VCO **86**. Delay stage **140** includes differential amplifier **164**, current source **166**, and source follower buffer **168**.

The delay time of delay stage **140** is controlled by bias current I_B **181**. Varying I_B **181** varies the delay time of delay stage **140**. Bias current I_B **181** is, in turn, controlled by bias

voltage, V_{BN} **160**. The delay time of delay stage **140** is smallest when V_{BN} is at its maximum level of 3.5 volts.

Another factor contributes to the relatively small delay time of delay stage **140**. Unlike prior delay stages, the voltage swing of OUT and OUTB and CK and CKB is limited. This increases the frequency range of delay stage **140**, allowing it to operate at higher frequencies.

Limiting the voltage swing of OUT and OUTB and CK and CKB also increases power supply rejection (PSR) by preventing transistors **186**, **188** and **167** from entering deeply into their linear region of operation and keeping their output resistance relatively high.

The biasing of transistors **186** and **188** is controlled by V_{BP} **162**. The bias generator for V_{BP} **162** (not shown) uses a simple current mirror design. More complex bias generators, which include common-mode feedback, could be used to set V_{BP} **162** such that the desired voltage level is maintained at OUT and OUTB.

The voltage swing between OUT and OUTB is limited to approximately 1.5 volts peak-to-peak by transistors **190** and **192**. Transistors **190** and **192** are coupled in diode fashion between OUT and OUTB, thus clamping the peak-to-peak voltage swing.

The range of possible voltage levels for OUT and OUTB is 4.5 volts to 3.0 volts. This is illustrated by the two waveforms in the upper right corner of FIG. **5**. The range of voltage levels for CK and CKB is 3.3 volts to 1.8 volts. This is illustrated by the two waveforms in the lower right corner of FIG. **5**.

The symmetrical shape of CK, CKB, OUT and OUTB results because I_C **180** is approximately equal to $2\times I_B$ **181**. Setting the common mode voltage level of OUT and OUTB near 3.75 V prevents node **183** from going to ground. As a result, the output impedance of current source **166** remains high, keeping the VCO common mode rejection of power supply noise high.

Referring once again to FIG. **2**, consider now subloops **54** and **56**. Subloop **54** is a single first order loop. Subloop **56**, in contrast to subloop **54**, includes two first order loops. One loop is closed and is used to generate the in phase internal transmit clock, INTTCLK **62**. This closed loop is essentially identical to subloop **54**, varying only in its input signal and output signal. The second loop within subloop **56** operates open loop, generating the leading internal transmit clock LEADING INTTCLK **63**. The amount of phase by which LEADING INTTCLK **63** leads INTTCLK **62** is fixed, but selectable, as will be described in detail below.

For simplicity's sake, subloop **54** will be described in detail first. Aided by that discussion, subloop **56** will then be described.

Subloop **54** performs phase tuning using the 12 phase signals generated by VCO **86**, PH(11:0) **58**. The heart of subloop **54** is phase select circuitry **120** and phase interpolator **122***a*. Phase select circuitry **120** performs coarse phase adjustment by selecting as outputs an even phase signal and an odd phase signal from PH(11:0) **58**. Even phase signals are PH**0 90**, PH**2 94**, PH**4 98**, PH**6 102**, PH**8 106**, and PH**10 110**. Odd phase signals are PH**1 92**, PH**3 96**, PH**5 100**, PH**7 104**, PH**9 108**, and PH**11 112**. Normally, the selected odd phase signal and the selected even phase signal will be adjacent to each other. For example, PH**3 96** is adjacent to even phases PH**2 94** and PH**4 98**. Phase interpolator **122***a* generates a signal that lies between the selected odd phase signal and the selected even phase signal. Phase interpolator **122***a* can generate 16 discrete values between the two selected phase signals using an even weighting signal and an odd weighting signal.

FIG. **6** illustrates the phase adjustment levels of phase selection circuitry **120** and phase interpolator **122**. The inputs to phase select circuitry **120**, PH(11:0) **58**, are represented by 12 horizontal lines, which are vertically evenly spaced apart. These lines represent twelve coarse adjustment levels across the period of the external reference clock; e.g., $RCLK_S$. These twelve levels are further subdivided by phase interpolator **122**, which generates 16 fine adjustment levels between each coarse adjustment level. Thus, the clock period is divided into 12×16, or 192, phase divisions.

Referring once again to FIG. **2**, amplifier **124***a* amplifies the output of phase interpolator **122***a* and passes it on to clock buffer **126***a*. Clock buffer **126***a* then distributes INTRCLK **60** throughout the device, **30** or **32**.

Phase detector **128** compares the internal clock signal, INTTCLK **60** to the external reference, $RCLK_S$ **42**, and indicates the polarity of the phase error to accumulator circuitry **130**.

In one embodiment phase detector **128** is a latch. Phase detector **128** is preferably the same type of latch used by the data input circuitry of interface **34**, which allows subloop **54** to compensate for the delay caused by data input circuitry. Preferably, internal receive clock, INTRCLK **60**, is fedback to the latch's clock input and the reference signal, $RCLK_S$ **42**, is coupled to the latch's data input. Thus, INTRCLK **60** determines the time at which $RCLK_S$ **42** is sampled. When subloop **54** is in lock, phase detector **128** outputs a stuttering string of logical 1s and 0s. Phase detector **128** outputs a logic 1 when the low-to-high transition of INTRCLK **60** occurs before the low-to-high transition of $RCLK_S$ **42**. Conversely, phase detector **125** outputs a logic 0 when the low-to-high transition of INTRCLK **60** occurs after the low-to-high transition of $RCLK_S$ **42**.

Accumulator circuitry **130** uses the output of phase detector **128** to control both phase select circuitry **120** and phase interpolator **122**. In other words, accumulator circuitry **130** controls both coarse and fine phase adjustment.

The cooperation between accumulator circuitry **130**, phase select circuitry **120**, and phase interpolator **122** can be understood in greater detail with reference to FIG. **7**. FIG. **7** illustrates portion **55** of subloop **54**.

Accumulator circuitry **130** responds to two input signals, PHERR **196** and LEADPHASE **198**. PHERR **196** is the output of phase detector **128** and as such indicates the polarity of the phase error between the internal clock and the external clock. PHERR **196** indicates that the internal clock lags the external clock with a logic 1. With a logic 0 PHERR **196** indicates the internal clock leads the external clock. LEADPHASE **198** indicates whether the leading phase signal selected by phase select circuitry **122** is even or odd. LEADPHASE **198** is a logic 0 when the leading phase is even and a logic 1 when the leading phase is odd. For example, when phase select circuitry **122** selects PH**3** and PH**4** as its outputs LEADPHASE is a logic 1. LEADPHASE **198** is likewise a logic 1 when phase select circuitry **122** selects PH**11** and PH**0**. Conversely, LEADPHASE **198** is a logic 0 when PH**6** and PH**7** are selected.

Counter control circuit **200** exclusively NORes PHERR **196** and LEADPHASE **198** together to generate UP/DOWNB signal **202**. UP/DOWNB **202** controls up/down counter **206**. When UP/DOWNB **202** is a logic 1 up/down counter **206** counts up. Up/down counter **206** counts down when UP/DOWNB **202** is a logic 0.

Counter control circuit **200** also generates an internal clock signal **204** to synchronize the operation of subloop **54**. Counter control circuit **200** divides down the clock gener-

ated by subloop **54**, INTRCLK **60**, to generate SLOWCLK **204**. In the preferred embodiment, counter control circuit **200** divides INTRCLK **60** by 16.

Up/down counter **206** generates a number of signals, **208**, **210**, **212**, and **214**, in response to UP/DOWNB **202**. These signals, **208**, **210**, **212**, and **214**, control phase select circuitry **120** and phase interpolator **122**. Up/down counter **206** represents the value of its count via COUNT(3:0) **208**. The sixteen levels of fine phase adjustment of phase interpolator **122** result from the resolution of COUNT(3:0) **208** and its complement, COUNTB (3:0) **210**. Up/down counter **206** outputs two other signals, OFLOW **214** and UFLOW **212**. Overflow signal, OFLOW **214**, goes active high when up/down counter **206** is requested to increment COUNT (3:0) **208** above it maximum value; i.e., 15. Analogously, underflow signal, UFLOW **212**, goes active high when up/down counter **206** is requested to decrement COUNT (3:0) **208** below it minimum value; i.e., 0. UFLOW **212** and OFLOW **214** control phase select circuitry **120**.

Digital-to-analog converter (DAC) **216** converts COUNT (3:0) **208** into an analog signal to generate EVENWEIGHT **218**. Similarly, COUNTB(3:0) **210** is converted into an analog signal to generate ODDWEIGHT **220**. Phase interpolator **122** determines the weighting of odd and phase select signals in response to EVENWEIGHT **218** and ODDWEIGHT **220**.

Phase select circuitry **120** includes coarse select control circuit **230**, which controls even phase select circuit **240** and odd phase select circuit **260**. Coarse select control circuit **230** clocks even phase select circuit **240** using even clock signal, ECLK **232**. The operation of even phase select circuit **240** is controlled by shift right and shift left signals, SHR **234** and SHL **236**, SHR **234** and SHL **236** also control odd phase select circuit **260**. Coarse select control circuit **230** generates a unique clock signal, OCLK **238**, to clock odd phase select circuit **260**.

While tuning up or down through phase PH(b **11**:**0**) **58**, coarse select control circuit **230** alternately brings active OCLK **238** and ECLK **232**. This alternating action derives from the alternating action of UFLOW **212** and OFLOW **214**.

The relationship between UFLOW **212**, OFLOW **214**, OCLK **238**, and ECLK **232** can be understood in greater detail with reference with FIG. **8**. FIG. **8** illustrates coarse select control circuit **230**.

Shift clocks OCLK **238** and ECLK **232** are generated using NOR gate **280**, and NAND gates **282** and **284**. RESET **286** and SLOWCLK **204** are NORed together by gate **280**. The output of NOR gate **280**, signal **281**, is generally an inverted version of SLOWCLK **204**, except when RESET **286** is active high. Signal **281** is coupled to gates **282**. NAND gate **282** combines signal **281** and UFLOW **212** to generate ECLK **232**. Similarly, NAND gate **284** combines signal **281** and OFLOW **214** to generate OCLK **238**.

LEADPHASE **198**, SHR **234**, and SHL **236** are generated using NAND gate **288** and toggle flip-flops **[290]** *292* and **[292]** *294*. NAND gate **288** combines OCLK **238** and ECLK **232** to generate TOGGLE **290**. TOGGLE **290** is coupled to the T input of toggle flip-flop **292**, which outputs LEADPHASE **198**. Toggle flip-flop **292** resets LEADPHASE **198** to a logic zero when RESET **286** is active high.

TOGGLE **[292]** *290* is inverted and then coupled to toggle flip-flop **294**. Toggle flip-flop **294** couples its output **296** to EX-NOR gate **298**, which exclusively NORes output **296** with OFLOW **214**. SHL **236** is an inverted version of the output of EX-NOR gate **298** and SHR **234**.

Referring again to FIG. **7**, consider the influence of coarse select control circuit **230** upon circuits **240** and **260**. Even phase select circuit **240** includes a barrel shifter **242** and an analog 6-to-1 multiplexer **246**. Even barrel shifter **242** generates six even select signals, ES(5:0) **244**, for even multiplexer **246**. Even select signals **244** are digital signals. Barrel shifter **242** brings only one of the six even select signals **244** active high at a time. This is because barrel shifter **242** is initially loaded with a value of 1. Which of the six even select signals is active depends upon the previous state of barrel shifter **246** and the states of SHR **234** and SHL **236**.

From its inputs **58**, even multiplexer **246** selects one of the six even phase signals using even select signals, ES(5:0) **244**. Even multiplexer **246** associates one even select signal with one even phase signal. As a result, even multiplexer **246** selects as even phase output signal **248** the single even phase signal associated with an active even select signal.

Like even phase select circuit **240**, odd phase select circuit **260** includes a barrel shifter **262** and an analog 6:1 multiplexer **266**. Odd select circuit **260** differs from even phase select circuit **240** only in its input and output signals. In other words, odd phase select circuit **260** functions like even phase select circuit **240**.

FIG. **9** is a block diagram of a preferred embodiment of even multiplexer **246** and odd multiplexer **266**. For simplicity's sake, the pull-up circuitry associated with multiplexer **246** and odd multiplexer **266** has been omitted. Each multiplexer **246** and **266** uses three identical multiplexer select stages **300**.

Even phase multiplexer **246** includes three select stages **300**a, **300**c, and **300**e. Each even select stage **300**a, **300**c and **300**e receives two complementary even phase signals, and two even select signals. Using these input signals, each even select stage **300**a, **300**c, and **300**e generate two complementary outputs, OUT **302**a, **302**c, and **302**e and OUTB **304**a, **304**c, and **304**e. All three OUT signals **302**a, **302**c, and **302**e are tied together and coupled to phase interpolator **122** as the even phase output signal. Similarly, all three OUTB signals **304**a, **304**c, and **304**e are tied together and coupled to phase interpolator **122** as the complement of the even phase output signal. To minimize propagation delay and maximize power supply rejection, the voltage swing of the even phase output signal and its complement **248** are clamped by transistors **310** and **312**, which are coupled in diode fashion between the outputs of delay stages **300**a, **300**c, and **300***e*.

Odd multiplexer **266** mirrors the design of even multiplexer **246**. Odd multiplexer includes three select stages **300**b, **300**d, and **300**f. Each odd select stage **300**b, **300**d, and **300**f receives two complementary odd phase signals, and two odd select signals. Using these input signals, each odd select stage generates two complementary outputs, OUT **302**b, **302**d, and **302**f and OUTB **304**b, **304**d, and **304**f. All three OUT signals **302**b, **302**d, and **302**f are tied together and coupled to phase interpolator **122** as the odd phase output signal. Similarly, all three OUTB signals **304**b, **304**d, and **304**f are tied together and coupled to phase interpolator **122** as the complement of the odd phase output signal. The peak-to-peak voltage swing of odd phase output signal and its complement **268** is clamped by transistors **314** and **316**, which are coupled between the two signal lines in diode fashion.

The operation of multiplexers **246** and **266** can be understood in greater detail with reference to FIG. **10**. FIG. **10** illustrates schematically a single multiplexer select stage **300**.

Multiplexer select stage **300** performs its function using buffering stage **301** and differential amplifiers **303** and **305**. Buffering stage **301** buffers and shifts the voltage levels of input signals IN and INB. The outputs of buffering stage **301**, IN' and INB', are then coupled to differential amplifiers **303** and **305**. The selected differential amplifier, **303** or **305**, then couples the appropriate input signals to OUT and OUTB.

The operation of multiplexer select stage **300** is controlled by the select signals coupled to SN and SN+6. The active signal of the pair of select signals, SN or SN+6, performs two functions. First, the active select signal enables buffering stage **301**. Second, the active select signal turns on one of the two differential amplifiers **303** and **305**.

The enabling of buffering stage **301** is achieved via four transistors **307**, **309**, **311**, and **313** near the top of buffering stage **301**. Two transistors, **307** and **309**, are coupled to amplifier **315**. Similarly, transistors **311** and **313** are coupled to amplifier **317**. Transistors **307** and **311** are turned on and off by an inverted version of SN, SN_B. An inverted version of SN+6, SN+6_B, turns transistors **309** and **315** on and off.

Consider the operation of buffering stage **301** when one of the select inputs, SN or SN+6, is active. For example assume SN is active high. SN_B places a low voltage on the gates of transistors **307** and **311**, causing them to conduct. Amplifiers **315** and **317** responds by coupling level shift versions of IN and IN_B, IN' and IN_B' to the inputs of differential amplifiers **303** and **305**. Buffering stage **301** responds nearly identically to an active select signal on SN+6. In this case, transistors **309** and **313** conduct, rather than transistors **307** and **311**.

Each differential amplifier **303** and **305** is controlled by a single select signal SN and SN+6. Thus, only one differential amplifier at a time drives OUT and OUT_B.

Both differential amplifiers are enabled via their current sources **319** and **321**. For example, when active high, SN turns current source **319** on. Differential amplifier **303** responds by coupling IN' and OUT and IN_B' and OUTB. Similarly, active SN+6 turns on current source **321**. In response, differential amplifier **305** couples IN_B' to OUT and IN' to OUT_B.

Referring yet again to FIG. **7**, consider now the influence of phase selector **120** upon phase interpolator **122**. Phase interpolator **122** performs fine phase tuning by interpolating between its inputs, even phase output signals **248** and odd output signals **268**. The relative contribution of these input signals **248** and **268** to signal PIOUT **123** is determined by weighting signals, EVENWEIGHT **218** and ODDWEIGHT **220**.

The manner in which phase interpolator **122** generates PIOUT **123** can be understood in greater detail with reference to the schematic diagram of FIG. **11**. Even phase output signal and its complement **248** are weighted by differential amplifier **320**. Even phase output signal is coupled to one of the inputs **322** of differential amplifier **320**, while the complement of the even phase output signal is coupled to the other input **324** of differential amplifier **320**. The amplification of signals **248** is determined by I_E **326**, the current generated by current source **328**. EVENWEIGHT **218** controls the magnitude of I_E **326**, thus controlling the contribution of signals **248** to PIOUT **123**. As EVENWEIGHT **218** decreases in voltage level, the contribution of even phase output signals **248** to PIOUT **123** also decreases, and vice-versa.

Similarly, differential amplifier **330** weights odd phase output signals **268**. One signal is coupled to input **332** and the other is coupled to input **334**. The current generated by current source **338**, I_O **336**, determines the amplification of odd phase output signals **268**. ODDWEIGHT **220**, the input to current source **338**, controls the magnitude of I_O **336** and thus the amplification of odd phase output signals **268**. The amplification of odd phase output signals **268** decreases and increases directly with the voltage level of ODDWEIGHT **220**.

The outputs of differential amplifiers **320** and **330** are summed together by coupling their outputs together. The peak-to-peak voltage swing of the outputs of differential amplifiers **320** and **330** are clamped by transistors **350** and **352** to minimize propagation delay and maximize power supply rejection. The voltage swings of PIOUT **123** and its complement could also be clamped by other means, such as diodes.

Armed with an understanding of the architecture of subloop **54**, consider its operation while locking on $RCLK_S$ **42**. Assume that the phase of $RCLK_S$ **42** is initially some value between PH**2** **94** and PH**3** **96**. FIG. **12** illustrates the response of subloop **54** under these circumstances.

Active RESET **286** forces even barrel shifter **242** to output a value of 000001 (binary) as even select signals, ES(5:0) **244**. Even multiplexer **246** responds to ES(5:0) **244** by coupling PH**0** **90** and its complement, PH**6** **102**, to phase interpolator **122**. Active RESET **286** also forces odd select signals, OS(5:0) **264**, to 000001 (binary). Odd multiplexer **266** responds by selecting PH**1** **92** and its complement, PH**7** **104**, as its outputs **268**.

Active RESET **286** may also be used to force the outputs **208**, **210**, **212**, and **214** of up/down counter **206** to known states, though this is not necessary. If RESET **286** does not control these signals they may begin in any state upon power up. In either case, for purposes of illustration, assume that COUNT(3:0) **208** begins at 0000 (binary) and COUNTB (3:0) **210** begins at 1111 (binary). Also assume that both UFLOW **212** and OFLOW **214** start up their inactive state. Thus, EVENWEIGHT **218** is at its minimum value and ODDWEIGHT **220** is at its maximum value.

Phase interpolator **122** responds to its input signals **218**, **220**, **248**, and **268**by bringing PIOUT **123** in-phase with PH**1** **92**. Thus, the output of subloop **54**, INTRCLK **60**, is also in-phase with PH**1** **92**.

Phase detector **128** responds to INTRCLK **60** lagging $RCLK_S$ **42** by forcing PHERR **196** to a logic 0.

Counter control circuit **200** exclusively NORes PHERR **96** with LEADPHASE **198**, which has had no opportunity to change from its reset value. Active RESET **286** forces LEADPHASE **198** to a logic low. Thus, counter control circuit **200** forces UP/DOWNB **202** to a logic low.

Up/down counter **206** responds to the command to count down from UP/DOWNB **202** by underflowing; i.e., bringing underflow signal UFLOW **212** active high. The values of COUNT(3:0) **208** and COUNTB(3:0) **210** remain unchanged.

Coarse select control circuit **230** pulses active even shift clock, ECLK **232**. On the active edge of ECLK **232**, SHL **236** goes active high. Even barrel shifter **242** shifts left in response, forcing even select signals ES(5:0) **244** to change to 000010 (binary). Even multiplexer **246** is forced to switch its selection from PH**0** **90** to PH**2** **94** by the new value of even select signals **244**.

Phase interpolator **122** is not immediately affected by the switching of even phase output signals **248**. EVENWEIGHT **218** remains at its minimum value after even multiplexer

246 changes its selection, preventing even phase output signals 248 from contributing to PIOUT 123. Thus, phase interpolator 122 glitchlessly switches from an output generated by one pair of phase signals, PH0 90 and PH1 92, to an output generated by another pair of phase signals, PH1 92 and PH2 94.

It is not long the case that the even phase output signals 248 do not contribute to PIOUT 123. LEADPHASE 198 changes state with ECLK 232. LEADPHASE 198 now indicates that odd phase output signal is the lower of the two selected phase signals coupled to phase interpolator 122. Counter control circuit 200 responds to this change in LEADPHASE 198. PHERR 196 remains high, thus counter control circuit 200 forces UP/DOWNB 202 high. Up/down counter 206 begins counting up, increasing the value of COUNT(3:0) 208 and decreasing the value of COUNTB (3:0) 210. As up/down counter 206 counts up, phase interpolator 122 gradually tunes PIOUT 123 from phase alignment with PH1 92 to phase alignment with PH2 94. That occurs when COUNT(3:0) 208 reaches its maximum value of COUNTB(3:0) 210 reaches its minimum value.

INTRCLK 60, in phase with PH2 94, continues to lag $RCLK_S$ 42, which has a phase somewhere between PH2 94 and PH3 96. Phase detector 128 therefore maintains PHERR 196 at a logic 1. Consequently, counter control circuit 202 continues to request that up/down counter 206 increase COUNT(3:0) 208 until up/down counter 206 overflows, bringing OFLOW 214 active high.

Active OFLOW 214 pulses active odd shift clock, OCLK 238. On the active edge of OCLK 238, SHL 236 goes active high, forcing odd barrel shifter 262 to shift left. Odd select signals, OS(5:0) 264, select PH3 96 with a value of 000010 (binary).

The switching by odd phase output signal 268 does not affect PIOUT 123 because COUNTB(3:0) is 0000 (binary) during overflow conditions. Thus, ODDWEIGHT 220 prevents odd phase output signal 268 from contributing to PIOUT 123. Once again, phase interpolator 122 glitchlessly switches from an output generated from one pair of phase signals, PH1 92 and PH2 94, to an output generated by another pair of phase signals, PH2 94 and PH3 96.

Soon after odd multiplexer 268 changes its selection, ODDWEIGHT 220 begins to increase in value and to affect PIOUT 123. This gradual change begins when LEADPHASE 198 changes state with OCLK 238. Afterward, LEADPHASE 198 indicates that the low phase signal is even phase output signal 248. PHERR 196 remains high, thus counter control circuit 200 responds to LEADPHASE 198 by forcing UP/DOWNB 202 low. Up/down counter 206 begins counting down, decreasing the value of COUNT(3:0) 208 and increasing the value of COUNTB(3:0) 210. As up/down counter 206 counts down, phase interpolator 122 gradually tunes PIOUT 123 into near phase alignment with $RCLK_S$ 42. When that occurs, PHERR 96 stutters between a logic 1 and a logic 0. Up/down counter 206 responds by see-sawing COUNT(3:0) 208 between two consecutive binary values, and may underflow or overflow, allowing even select signals 248 and odd select signals 268 to change without causing glitches on PIOUT 123.

Subloop 54 is not only capable of turning up through PH(11:0) 58 to lock on $RCLK_S$ 42. Subloop 54 tunes down when necessary. For example, consider the situation when $RCLK_S$ 42 changes phase after subloop 54 has locked. Assume that the phase of $RCLK_S$ 42 changes from a value in between PH3 96 and PH2 94 to a value in between PH2 94 and PH1 92. FIG. 12 also illustrates the response of subloop 54 to this situation.

PHERR 198 initially indicates that INTRCLK 60 leads $RCLK_S$ 42. In other words, PHERR 198 becomes and remains a logic 0 for a relatively long period of time. Counter control logic 200 responds by directing up/down counter 206 to count up. Up/down counter 206 does so until it overflows, bringing OFLOW 214 active high while COUNT(3:0) 208 remains at 1111 (binary) and COUNTB (3:0) 210 remains at 0000 (binary).

Active OFLOW 214 pulses odd shift clock, OCLK 238, low. Active OFLOW 214 also brings SHR 234 active high and forces SHL 236 inactive low. Thus, on the active edge of OCLK 238 odd barrel shifter 262 shifts right. This changes OS(5:0) 264 from 000010 (binary) to 000001 (binary). Odd multiplexer 266 responds by deselecting PH3 96 and selecting PH1 92 as odd output signal. Again, phase interpolator 122 prevents the switching of odd output signals 268 from affecting PIOUT 123 because ODDWEIGHT 220 is at it minimum value. Subloop 54 tunes between PH2 94 and PH1 92 as necessary to lock on $RCLK_S$ 44.

Given this description of subloop 54, consider now the operation of subloop 56. Referring again to FIG. 2, the closed loop within subloop 56 closely resembles subloop 54, including phase detector 128, accumulator circuitry 130, phase select circuitry 121, in-phase phase interpolator 122c, amplifier 124*c*, clock buffer 126*c*, and output buffer delay compensation circuit 127. As its name implies, output buffer delay compensation circuit 127 allows subloop 56 to compensate for the delay contributed to INTTCLK 62 by the output buffers of interface 34. The open loop includes phase select circuitry 121, out-of-phase interpolator 122b, amplifier 124*b*, and clock buffer 126*b*.

The heart of subloop 56 is phase select circuitry 121, in-phase phase interpolator 122c, and out-of-phase interpolator 122b. Phase select circuitry 121 performs coarse phase tuning for both the open loop and the closed loop within subloop 56. Each phase interpolator 122b and 122c generates a fine-tuned signal that lies between the two pairs of phase signals coupled to it by phase selector 121. Like subloop 54, both loops with subloop 56 generate 16 fine levels of adjustment between each coarse adjustment level.

Phase select circuitry 121 gives rise to a major difference between subloop 54 and subloop 56. Unlike phase select circuitry 120, phase select circuitry 121 selects two pairs of even phase output signals and two pairs of odd phase output signals. One set of pairs of even and odd phase output signals 248 and 268 is in-phase with $TCLK_S$ 44 and are coupled to in-phase phase interpolator 122c. The other set of pairs of even and odd phase output signals 249 and 269 are out-of-phase with $TCLK_S$ 44 and are coupled to out-of-phase phase interpolator 122*b*.

The cooperation of phase select circuitry 121 and phase interpolators 122b and 122c can be understood in greater detail with reference to FIG. 13. As can be seen, portion 57 closely resembles portion 55. For this reason, the following description of portion 57 focuses on its differences as compared to portion 55. Unless otherwise stated, portion 57 functions like portion 55, as described with reference to FIGS. 7–12.

The primary difference between phase select circuitry 120 and phase select circuitry 121 arises from even select circuit 241 and odd select circuit 261. Where even select circuit 240 included only one even multiplexer, even select circuit 241 includes two, in-phase even multiplexer 246 and out-of-phase even multiplexer 247. Multiplexers 246 and 247 are identical and receive identical input signals, even select signals 244 and phase signals 58. Even select signals 244 are

coupled to multiplexers **246** and **247** in different fashions, however. As a result, in-phase even multiplexer **246** outputs signals **248** that are substantially in-phase with $TCLK_S$ **44**, while out-of-phase multiplexer **247** outputs signals **249** that are out-of-phase with $TCLK_S$ **44**.

Similar to even select circuit **241**, odd select circuit **261** includes two odd multiplexers **266** and **267**. In-phase odd multiplexer **266** and out-of-phase odd multiplexer **267** are identical and receive identical input signals, odd select signals **264** and phase signals **58**. These input signals **264** and **58** are coupled to multiplexers **266** and **267** in differing fashions such that in-phase odd multiplexer **266** outputs signals **268** in substantially in-phase with $TCLK_S$ **44** and out-of-phase odd multiplexer **267** outputs signals out-of-phase with $TCLK_S$ **44**.

In-phase even multiplexer **246** and in-phase odd multiplexer **266** are coupled to even select signals **244**, odd select signals **264**, and phase signals **58** as shown in FIG. **9**. The coupling of even select signals **244**, odd select signals **266**, and phase signals **58** is shown in FIG. **14**. For simplicity's sake, the pull-up circuitry associated with multiplexer **247** and odd multiplexer **267** has been omitted. In the embodiment shown, out-of-phase even phase output signals **249** and out-of-phase odd phase output signals **269** lead their in-phase counterparts **248** and **268** by substantially 90°. This phase shift in the out-of-phase multiplexer is achieved by associating each select signal with a phase signal **58** that leads by 90° the phase signal associated with that same select signal in the corresponding in-phase multiplexer. For example, in in-phase even multiplexer **246** even select signal ES**0** selects phase signal PH**0 90**. In contrast, out-of-phase even multiplexer **247** selects PH**9 108** using ES**0**. Analogously, while OS**3** is used to select PH**7** in in-phase odd multiplexer **266**, OS**3** is used to select PH**4 98** in out-of-phase odd multiplexer **267**.

The degree of phase shift between signals **248** and **249**, and **268** and **269**, may be arbitrarily selected in other embodiments simply by altering which select signal selects which phase signal in out-of-phase multiplexers **247** and **267**.

Out-of-phase phase interpolator **122**b uses the output of out-of-phase multiplexers **247** and **267** to generate PIOUT-90° **123**b. Out-of-phase interpolator **122**b also responds to EVENWEIGHT **218** and ODDWEIGHT **220**, as discussed with respect to FIGS. **7–12**.

Thus, circuitry for performing fine phase adjustment within a phase locked loop has been described. The phase selector selects an even phase signal and an odd phase signal from the twelve phase signals output by the VCO. The even and odd phase signals are selected by an even select signal and an odd select signal, respectively. The phase interpolator interpolates between the even phase signal and the odd phase signal to generate an output signal. The affect of each phase input signal on the output signal is determined by an even weighting signal and an odd weighting signal, respectively. Together, the weighting signals and the switching mechanisms of the phase select circuitry prevent glitches from appearing on the output signal when either the even phase signal or the odd phase signal is switching.

A method of performing fine phase adjustment in a phase locked loop has also been described. First, two phase signals are selected from a multiplicity of phase signals. The two phase signals are selected by a select signal. Next, an output signal is generated by interpolating between the two phase signals. The contribution of each of the two phase signals to the output signal is determined by a weighting signal. The weighting signals prevent glitches from appearing on the output signal when either the even phase signal or the odd phase signal is switching.

Finally, a delay stage for a ring oscillator has also been described. Each delay stage includes a differential amplifier, which generates two complementary output signals. Coupled between the complementary output signals, two voltage clamping means limit the peak-to-peak voltage swing of the output signal. Limiting the peak-to-peak voltage swing of the output signal speeds-up the delay stage and allows the ring oscillator to include a greater number of delay stages, and increases the power supply rejection of the oscillator.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

What is claimed is:

1. A ring oscillator comprising:

a plurality of ring coupled delay stages, each delay stage comprising:

(A) a differential amplifier for generating a differential output signal comprising a first output signal at a first node and a second output signal at a second node, wherein the differential amplifier further comprises:

(i) a first transistor coupled to the first node;

(ii) a second transistor coupled to the second node and the first transistor, wherein the first and second transistors are biased by an output level biasing voltage;

(iii) a third transistor coupled to the first node, wherein the third transistor receives a first input signal from a preceding delay stage;

(iv) a fourth transistor coupled to the second node and the third transistor, wherein the fourth transistor receives a second input signal from the preceding delay stage;

(B) a self-biased voltage clamping circuit coupled to the first and second nodes to limit a peak-to-peak voltage swing of the differential output signal; and

(C) a current source coupled to the differential amplifier, the current source varying a bias current through the current source in accordance with a delay bias voltage.

2. The ring oscillator of claim **1**, wherein the voltage clamping circuit further comprises:

(i) a first diode-coupled transistor; and

(ii) a second diode-coupled transistor, wherein the first and second diode-coupled transistors are cross-coupled between the first and second nodes.

3. The ring oscillator of claim **2**, wherein the first and second diode-coupled transistor are metal-oxide semiconductor transistors.

4. The ring oscillator of claim **2**, wherein the first and second diode-coupled transistors are N-type transistors.

5. The ring oscillator of claim **1**, wherein the current source further comprises a fifth transistor.

6. The ring oscillator of claim **1** wherein the first and second transistors are of a first type, wherein the third and fourth transistors are of a second type.

7. The ring oscillator of claim **6** wherein the first and second transistors are P-type and the third and fourth transistors are N-type.

8. The ring oscillator of claim 6 wherein the first and second transistors are N-type and the third and fourth transistors are P-type.

9. The ring oscillator of claim 6 wherein the first and second types are complementary.

10. The ring oscillator of claim 1 wherein each delay stage further comprises a source follower buffer.

11. A ring oscillator comprising:

a plurality of ring coupled delay stages, each delay stage comprising:

(A) a differential amplifier for generating a first output signal at a first node and a second output signal at a second node, wherein the differential amplifier further comprises:

(i) a first transistor coupled between the first node and a first potential;

(ii) a second transistor coupled between the second node and the first potential, wherein the first and second transistors are biased by an output level biasing voltage;

(iii) a third transistor coupled between the first node and a third node, wherein the third transistor receives a first input signal from a preceding delay stage;

(iv) a fourth transistor coupled between the second node and the third node, wherein the fourth transistor receives a second input signal from the preceding delay stage;

(B) a current source coupled between the third node and a second potential, the current source varying a bias current through the current source in accordance with a delay bias voltage; and

(C) a voltage clamping circuit coupled to the first and second nodes to limit a relative peak-to-peak voltage swing of the first and second output signals without independently clamping each of the first and second nodes.

12. The ring oscillator of claim 11, wherein the voltage clamping circuit further comprises:

(i) a first diode-coupled transistor; and

(ii) a second diode-coupled transistor, wherein the first and second diode-coupled transistors are cross-coupled between the first and second nodes.

13. The ring oscillator of claim 12, wherein the first and second diode-coupled transistors are metal-oxide semiconductor transistors.

14. The ring oscillator of claim 12, wherein the first and second diode-coupled transistors are N-type transistors.

15. The ring oscillator of claim 11, wherein the current source further comprises a fifth transistor.

16. The ring oscillator of claim 11 wherein the first and second transistors are of a first type, wherein the third and fourth transistors are of a second type.

17. The ring oscillator of claim 16 wherein the first and second transistors are P-type and the third and fourth transistors are N-type.

18. The ring oscillator of claim 16 wherein the first and second transistors are N-type and the third and fourth transistors are P-type.

19. The ring oscillator of claim 16 wherein the first and second types are complementary.

20. The ring oscillator of claim 11 wherein each delay stage further comprises a source follower buffer.

21. A ring oscillator comprising:

a plurality of ring coupled delay stages, each delay stage comprising:

a differential amplifier providing a differential output signal;

a self-biased voltage clamping circuit coupled to limit a peak-to-peak voltage swing of the differential output signal; and

a current source coupled to the differential amplifier, the current source varying a bias current through the current source in accordance with a delay bias voltage.

22. The ring oscillator of claim 21, wherein the differential amplifier provides a first output signal at a first node and a second output signal at a second node, the first and second output signal forming the differential output signal, wherein the voltage clamping circuit further comprises:

(i) a first diode-coupled transistor; and

(ii) a second diode-coupled transistor, wherein the first and second diode-coupled transistors are cross-coupled between the first and second nodes.

23. A ring oscillator comprising:

a plurality of ring coupled delay stages, each delay stage comprising:

a differential amplifier providing a differential output signal comprising a first output signal at a first node and a second output signal at a second node;

a voltage clamping circuit coupled to the first and second nodes to limit a peak-to-peak voltage swing of the differential output signal without independently clamping each of the first and second nodes; and

a current source coupled to the differential amplifier, the current source varying a bias current through the current source in accordance with a delay bias voltage.

24. The ring oscillator of claim 23, wherein the voltage clamping circuit further comprises:

(i) a first diode-coupled transistor; and

(ii) a second diode-coupled transistor, wherein the first and second diode-coupled transistors are cross-coupled between the first and second nodes.

25. A synchronous memory device comprising:

an array of memory cells to store data;

a clock synchronization loop to generate a plurality of clock signals, each clock signal having a timing relationship with respect to a reference clock signal;

first interpolator circuitry to generate a first internal clock signal from a first and a second clock signal of the plurality of clock signals, wherein a phase of the first internal clock signal is interpolated from respective phases of the first and second clock signals according to phase information indicative of whether the first internal clock signal leads or lags a first external clock signal; and

interface circuitry to synchronize a transmission of data with the first internal clock signal.

26. The memory device of claim 25 wherein the clock synchronization loop is a phase locked loop circuit.

27. The memory device of claim 25 wherein the timing relationship of each one of the plurality of clock signals is a respective phase offset from a phase of the reference clock signal.

28. The memory device of claim 25 wherein the clock synchronization loop comprises a plurality of delay elements coupled in series, each delay element outputting at least one of the plurality of clock signals.

29. The memory device of claim 28 wherein the plurality of delay elements in an even number of delay elements.

30. The memory device of claim 25 further comprising selection circuitry, coupled to the clock synchronization loop, to select the first and second clock signals from the plurality of clock signals.

31. The memory device of claim 30 further comprising:

a detector circuit to detect a phase polarity between the first internal clock signal and the first external clock signal;

a shift register, coupled in parallel with the selection circuitry, to output selection signals that control selection of the first and second clock signals; and

a control circuit to provide shift information to the shift register based on the phase polarity such that the selection signals output by the shift register select clock signals of the plurality of clock signals that have phases neighboring, on respective either sides, the phase of the first external clock signal.

32. The memory device of claim 25, further comprising:

a detector circuit, coupled to the first interpolator circuitry, to detect the phase information; and

a control circuit to generate a control voltage that is responsive to the phase information, wherein the first interpolator circuitry steers the phase of the first internal clock signal between the phase of the first and second clock signals in response to the control voltage.

33. The memory device of claim 32 wherein after detection the phase information is represented by a binary value.

34. The memory device of claim 32 wherein the control circuit comprises:

a digital counter to generate a digital count value in response to the phase information; and

a digital to analog converter to generate the control voltage from the digital count value.

35. The memory device of claim 25 further comprising a buffer circuit to receive a second external clock signal and generate the reference clock signal using the second external clock signal.

36. The memory device of claim 35 wherein a reception of data is synchronized with the second external clock signal.

37. The memory device of claim 35 wherein the plurality of clock signals comprises a clock signal that is in phase with the second external clock signal.

38. The memory device of claim 25 further comprising second interpolator circuitry to generate a second internal clock signal from a pair of clock signals of the plurality of clock signals, wherein a phase of the second internal clock signal is interpolated from respective phases of the pair of clock signals according to phase information indicative of whether the second internal clock signal leads or lags a second external clock signal.

39. The memory device of claim 25 wherein the data is transmitted during a plurality of clock edge transitions of the first external clock signal.

40. An integrated circuit device comprising:

interface circuitry to receive first and second external clock signals; and

clock synchronization circuitry to synchronize a transmission of data with the first external clock signal and to synchronize a reception of data with the second external clock signal, the clock synchronization circuitry including:

a reference loop to receive a reference clock signal and generate a plurality of clock signals, each clock signal of the plurality of clock signals having a predetermined timing relationship with the reference clock signal;

a first subloop circuit, coupled to the reference loop, to synchronize the transmission of data with the first external clock signal using the plurality of clock signals; and

a second subloop circuit, coupled to the reference loop, to synchronize the reception of data with the second external clock signal using the plurality of clock signals.

41. The integrated circuit device of claim 40 wherein the first subloop circuit generates an internal transmit clock signal having a phase relationship with respect to the first external clock signal.

42. The integrated circuit device of claim 41 wherein the phase relationship is a quadrature relationship.

43. The integrated circuit device of claim 41 wherein the internal transmit clock is in phase with the first external clock signal.

44. The integrated circuit device of claim 40 wherein the first subloop circuit further comprises:

selection circuitry to select first and second clock signals of the plurality of clock signals;

interpolator circuitry to interpolate between the first and second clock signals, and to generate an internal transmit clock signal in response to a control signal, wherein the control signal steers the phase of the internal transmit clock signal between respective phases of the first and second clock signals; and

detector circuitry to detect phase information indicative of whether the internal transmit clock signal leads or lags the first external clock signal, and to generate the control signal using the phase information.

45. The integrated circuit device of claim 40 wherein the second subloop circuit generates an internal receive clock signal having a phase relationship with respect to the second external clock signal.

46. The integrated circuit device of claim 45 wherein the internal receive clock signal is in phase with the second external clock signal.

47. The integrated circuit device of claim 40 wherein the second subloop circuit further comprises:

selection circuitry to select first and second clock signals of the plurality of clock signals;

interpolator circuitry to interpolate between the first and second clock signals, and to generate an internal receive clock signal in response to a control signal, wherein the control signal steers the phase of the internal receive clock signal between respective phases of the first and second clock signals; and

detector circuitry to detect phase information indicative of whether the internal receive clock signal leads or lags the second external clock signal, and to generate the control signal using the phase information.

48. The integrated circuit device of claim 40 wherein a first clock signal of the plurality of clock signals is in phase with the second external clock signal, and the other clock signals of the plurality of clock signals have respective phases that are evenly spaced across a clock period of the second external clock signal.

49. The integrated circuit device of claim 40 wherein the reference loop is a phase locked loop circuit.

50. The integrated circuit device of claim 40 wherein the data is transmitted during a plurality of clock edge transitions of the first external clock signal.

51. The integrated circuit device of claim 40 further comprising a buffer circuit to receive the second external clock signal and to generate the reference clock signal from the second external clock signal.

52. A clock synchronization circuit comprising:

a plurality of delay stages coupled in series to output a plurality of clock signals, each delay stage having a delay time with respect to a reference clock signal;

interpolator circuitry to generate a first clock signal using a pair of clock signals of the plurality of clock signals, wherein a phase of the first clock signal is interpolated between respective phases of each clock signal of the pair of clock signals in accordance with information indicative of whether a phase of the first clock signal leads or lags a phase of an input clock signal; and

a detector circuit to compare the phase of the first clock signal with the phase of the input clock signal, to generate the information indicative of whether the phase of the first clock signal leads or lags the phase of the input clock signal.

53. The clock synchronization circuit of claim 52 wherein the plurality of delay stages is an even number of delay stages.

54. The clock synchronization circuit of claim 52 further comprising a buffer to output the reference clock signal, wherein the buffer receives the input clock signal.

55. The clock synchronization circuit of claim 52 wherein each delay stage of the plurality of delay stages comprises:

a first output terminal;

a second output terminal;

a first transistor having a source, a drain, and a gate, the source and gate being coupled to the first output terminal, and the drain being coupled to the second output terminal; and

a second transistor having a source, a drain, and a gate, the source and gate being coupled to the second output terminal, and the drain being coupled to the first output terminal.

56. The clock synchronization circuit of claim 52 wherein the plurality of delay stages is included in a phase locked loop circuit.

57. The clock synchronization circuit of claim 52 further comprising selection circuitry to select the pair of clock signals from the plurality of clock signals.

58. The clock synchronization circuit of claim 52 wherein the detector circuit comprises a phase detector to compare the phase of the first clock signal with the phase of the input clock signal, the phase detector to generate a binary signal that indicates whether the first clock signal leads or lags the input clock signal.

59. The clock synchronization circuit of claim 52 wherein the detector circuit comprises:

a counter circuit to change a count value in a first direction when the phase of the input clock signal lags the phase of the first clock signal, and change the count value in a second direction when the phase of the input clock signal leads the phase of the first clock signal; and

a digital to analog converter circuit to generate an analog control signal from the count value, wherein the analog control signal steers the phase of the first clock signal between the respective phases of each clock signal of the pair of clock signals.

60. A synchronous memory device comprising:

an array of memory cells to store data;

clock synchronization circuitry including:

a plurality of delay stages coupled in series;

a first multiplexer circuit, coupled to the plurality of delay stages, to perform selection of a delay time for a first internal clock signal, the selection being controlled by a first plurality of control signals;

a first shift register circuit to generate the first plurality of control signals in accordance with information indicative of whether a phase of an external clock signal leads or lags a phase of an internal transmit clock signal; and

a detector circuit to compare the phase of the external clock signal with the phase of the internal transmit clock signal and generate the information; and

interface circuitry to output data from the memory device, the data being output in synchronism with the internal transmit clock signal, the internal transmit clock signal being generated using the first internal clock signal.

61. The memory device of claim 60 further comprising:

a second multiplexer circuit, coupled to the plurality of delay stages, to perform selection of a delay time for a second internal clock signal, the selection being controlled by a second plurality of control signals; and

a second shift register circuit to generate the second plurality of control signals in accordance with the information indicative of whether the phase of the external clock signal leads or lags the phase of the internal transmit clock signal.

62. The memory device of claim 61 further comprising:

interpolator circuitry to generate the internal transmit clock signal by interpolating between phases of the first and a second internal clock signals in accordance with a control voltage; and

a control circuit to generate the control voltage according to the information indicative of whether the phase of the external clock signal leads or lags the phase of the internal transmit clock signal.

63. The memory device of claim 62 wherein the control circuit comprises:

a counter circuit to generate a digital count value based on the information; and

a digital to analog converter to generate the control voltage based on the digital count value.

64. The memory device of claim 60, wherein the first internal clock signal is generated by an output of a delay stage of the plurality of delay stages.

65. The memory device of claim 60 wherein the plurality of delay stages is included in a phase locked loop circuit.

66. A synchronous memory device comprising:

an array of memory cells to store data;

a plurality of delay elements coupled in series, each delay element generating a respective output signal having a different phase;

a detector circuit to compare a phase of an external clock signal with a phase of an internal transmit clock signal, the detector circuit to generate information indicative of whether the phase of the external clock signal leads or lags the phase of the internal transmit clock signal;

a multiplexer circuit, coupled to the plurality of delay elements, to select a first output signal generated by the plurality of delay elements in response to the information; and

an interface circuit to output data from the memory device, the data being output in synchronism with the internal transmit clock signal, the internal transmit clock signal being generated using at least the first output signal selected by the multiplexer circuit.

67. The memory device of claim 66 further comprising a shift register coupled to the multiplexer circuit to control selection of the first output signal.

68. The memory device of claim 66 further comprising:

a control circuit to generate a control voltage that is responsive to the information; and

interpolator circuitry to generate the internal transmit clock signal using the first output signal and a second

output signal generated by the plurality of delay elements, the phase of the internal transmit clock signal being interpolated between the phases of the first and second output signals in response to the control voltage.

69. The memory device of claim 68 wherein the control circuit comprises:

a digital converter to generate a digital count value in response to the information; and

a digital to analog converter to generate the control voltage using the digital count value.

70. The memory device of claim 66 wherein the plurality of delay elements is included in a phase locked loop circuit.

71. A clock synchronization circuit comprising:

a plurality of delay stages coupled in series to output a plurality of clock signals, each delay stage having a respective delay time with respect to a reference clock signal; and

interpolator circuitry coupled to the plurality of delay stages, the interpolator circuitry to generate a first clock signal using a pair of clock signals of the plurality of clock signals, wherein a phase of the first clock signal is interpolated between respective phases of each clock signal of the pair of clock signals in accordance with information indicative of whether the phase of the first clock signal leads or lags a target phase, wherein the target phase is based on transitions in an input signal.

72. The clock synchronization circuit of claim 71 further comprising detector circuitry coupled to the interpolator circuitry, the detector circuitry to compare the phase of the first clock signal with the target phase, the detector circuitry to generate the information indicative of whether the phase of the first clock signal leads or lags the target phase.

73. The clock synchronization circuit of claim 72 wherein the detector circuitry comprises a counter circuit to change a count value in a first direction when the target phase lags the phase of the first clock signal, and change the count value in a second direction when the target phase leads the phase of the first clock signal, wherein the information indicative of whether the phase of the first clock signal leads or lags the target phase is based on the count value.

74. The clock synchronization circuit of claim 73 wherein the information indicative of whether the phase of the first clock signal leads or lags the target phase is provided as an analog control signal, and wherein the detector circuitry further comprises a digital to analog converter circuit coupled to the counter circuit, the digital to analog converter circuit to generate the analog control signal from the count value, wherein the analog control signal controls interpolation between the respective phases of the clock signals of the pair of clock signals to produce the phase of the first clock signal.

75. The clock synchronization circuit of claim 71 wherein the target phase is detected based on sampling of the input signal.

76. The clock synchronization circuit of claim 75 wherein the input signal is sampled using the first clock signal.

77. The clock synchronization circuit of claim 76 wherein the input signal is a clock signal.

78. The clock synchronization circuit of claim 71 wherein the input signal includes clock information.

79. The clock synchronization circuit of claim 78 wherein the input signal is a clock signal.

80. The clock synchronization circuit of claim 79 wherein the input signal and the reference clock signal are both derived from an external clock signal.

81. The clock synchronization circuit of claim 80 wherein the input signal is the reference clock signal.

82. The clock synchronization circuit of claim 71 wherein the plurality of delay stages is an even number of delay stages.

83. The clock synchronization circuit of claim 71 wherein the plurality of delay stages and the interpolator circuitry are formed on a single integrated circuit device.

84. The clock synchronization circuit of claim 83 further comprising a buffer coupled to the interpolator circuitry, the buffer to receive the input signal from external to the integrated circuit device.

85. The clock synchronization circuit of claim 83 further comprising a buffer coupled to the plurality of delay stages, the buffer to receive the reference clock signal from external to the integrated circuit device.

86. The clock synchronization circuit of claim 71 wherein each delay stage of the plurality of delay stages comprises:

a first output terminal;

a second output terminal;

a first transistor having a source, a drain, and a gate, the source and gate being coupled to the first output terminal, and the drain being coupled to the second output terminal; and

a second transistor having a source, a drain, and a gate, the source and gate being coupled to the second output terminal, and the drain being coupled to the first output terminal.

87. The clock synchronization circuit of claim 71 wherein the plurality of delay stages is included in a phase locked loop circuit.

88. The clock synchronization circuit of claim 71 further comprising selection circuitry coupled to the interpolator circuitry, the selection circuitry to select the pair of clock signals from the plurality of clock signals.

89. The clock synchronization circuit of claim 71 further comprising a phase detector to compare the phase of the first clock signal with the target phase, and to generate the information indicative of whether the phase of the first clock signal leads or lags the target phase, wherein the information is represented by a binary signal.

90. The clock synchronization circuit of claim 71 wherein each delay stage of the plurality of delay stages generates complementary outputs, wherein each output of the complementary outputs is one of the plurality of clock signals.

91. A method for clock synchronization, comprising:

generating a plurality of clock signals from a reference clock signal, wherein each clock signal of the plurality of clock signals is delayed from the reference clock signal by a corresponding delay time such that a plurality of different delays with respect to the reference clock signal are represented in the plurality of clock signals;

detecting phase of an input signal, wherein the phase of the input signal represents a target phase; and

generating a first clock signal based on a pair of clock signals of the plurality of clock signals, wherein generating the first clock signal includes interpolation between the pair of clock signals using information indicative of whether the phase of the first clock signal leads or lags the target phase.

92. The method of claim 91 wherein detecting phase of the input signal further comprises sampling the input signal.

93. The method of claim 92 wherein sampling the input signal further comprises sampling the input signal based on the first clock signal.

94. The method of claim 93 wherein the input signal is a clock signal.

95. The method of claim 94 wherein the input signal and the reference clock signal are generated from an external clock signal.

96. The method of claim 92 further comprises selecting the pair of clock signals from the plurality of clock signals based on the sampling of the input signal.

97. The method of claim 91 wherein generating the plurality of clock signals further comprises generating the plurality of clock signals using a plurality of delay stages coupled in series, wherein each delay stage of the plurality of delay stages generates complementary outputs, wherein each output of the complementary outputs is one of the plurality of clock signals.

98. The method of claim 91 wherein the input signal includes clock information.

99. The method of claim 98 wherein the input signal is a clock signal.

100. An integrated circuit comprising:

a plurality of delay stages coupled in series to output a plurality of clock signals, each delay stage of the plurality of delay stages having a delay time with respect to a reference clock signal;

a phase detector to determine the phase of an input signal by sampling the input signal, wherein the phase of the input signal is based on at least one transition in the input signal, the phase detector to generate information indicative of whether a phase of a first clock signal leads or lags the phase of the input signal; and

interpolator circuitry coupled to the plurality of delay stages and the phase detector, the interpolator circuitry to generate the first clock signal using a pair of clock signals of the plurality of clock signals, wherein the phase of the first clock signal is interpolated between respective phases of the pair of clock signals in accordance with the information indicative of whether the phase of the first clock signal leads or lags the phase of the input signal.

101. The integrated circuit of claim 100 wherein the phase detector samples the input signal using the first clock signal.

102. The integrated circuit of claim 100 wherein the input signal includes clock information.

103. The integrated circuit of claim 102 wherein the input signal is a clock signal.

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