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Sutardja et al.

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(54) CONTROLLABLE INTEGRATOR

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(BM)

(*) Notice: This patent is subject to a terminal dis-

claimer.

- (21) Appl. No.: 09/950,086
- (22) Filed: Sep. 12, 2001

Related U.S. Patent Documents

Reissue of:

(64) Patent No.: 5,805,006
Issued: Sep. 8, 1998
Appl. No.: 08/848,549
Filed: Apr. 28, 1997

U.S. Applications:

- (63) Continuation of application No. 08/848,549, filed on Apr. 28, 1997, now Pat. No. 5,805,006.

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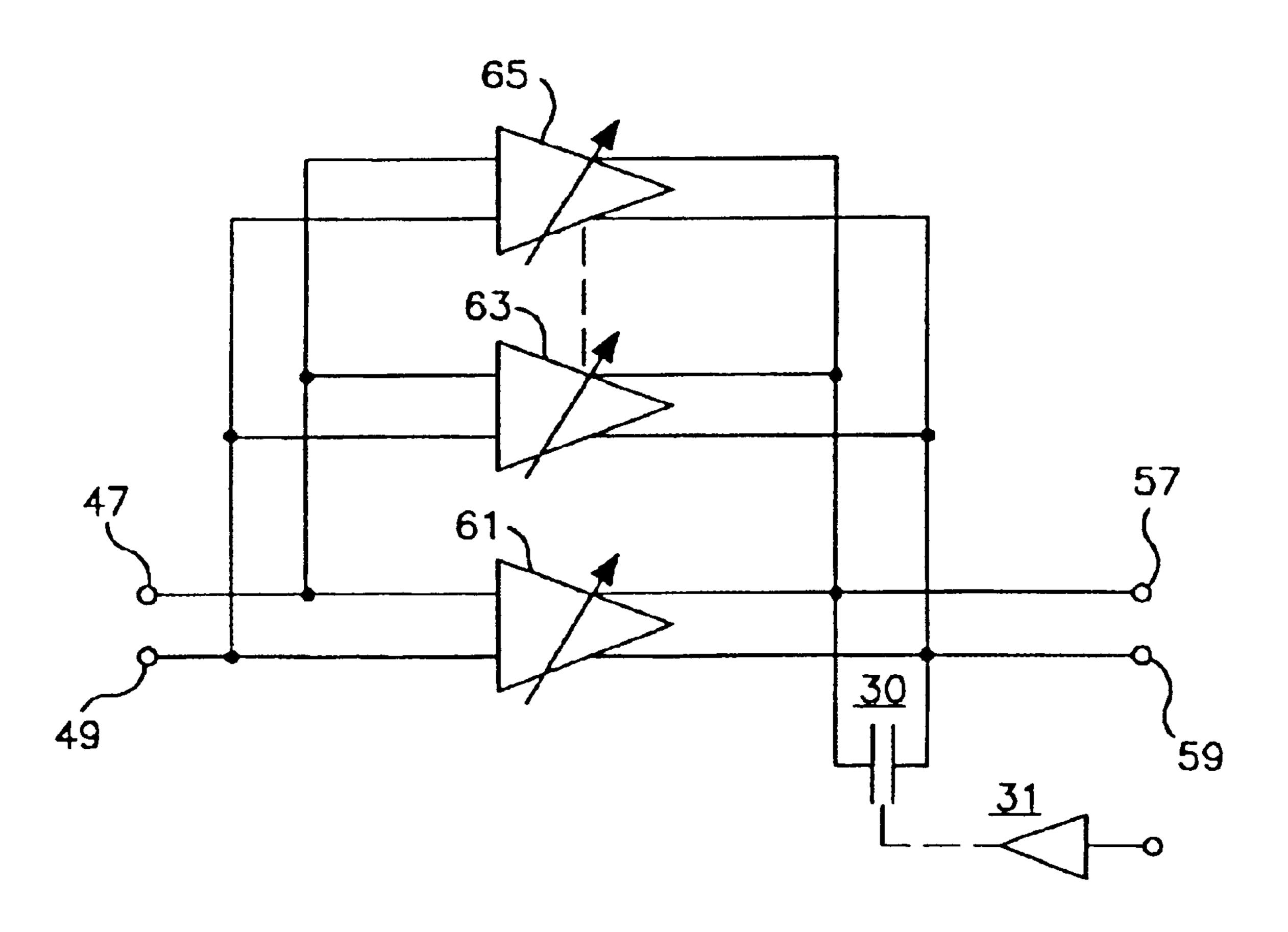
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Primary Examiner—Toan Tran

(57) ABSTRACT

Integrated circuitry for selectively introducing capacitance and for controlling the transconductance transfer function of one or more amplifiers includes concatenated differential amplifiers with one or more pairs of switchable capacitive components differentially connected across outputs of the differential amplifiers to facilitate operation over a wide range of operating frequencies under control of external signals.

21 Claims, 2 Drawing Sheets



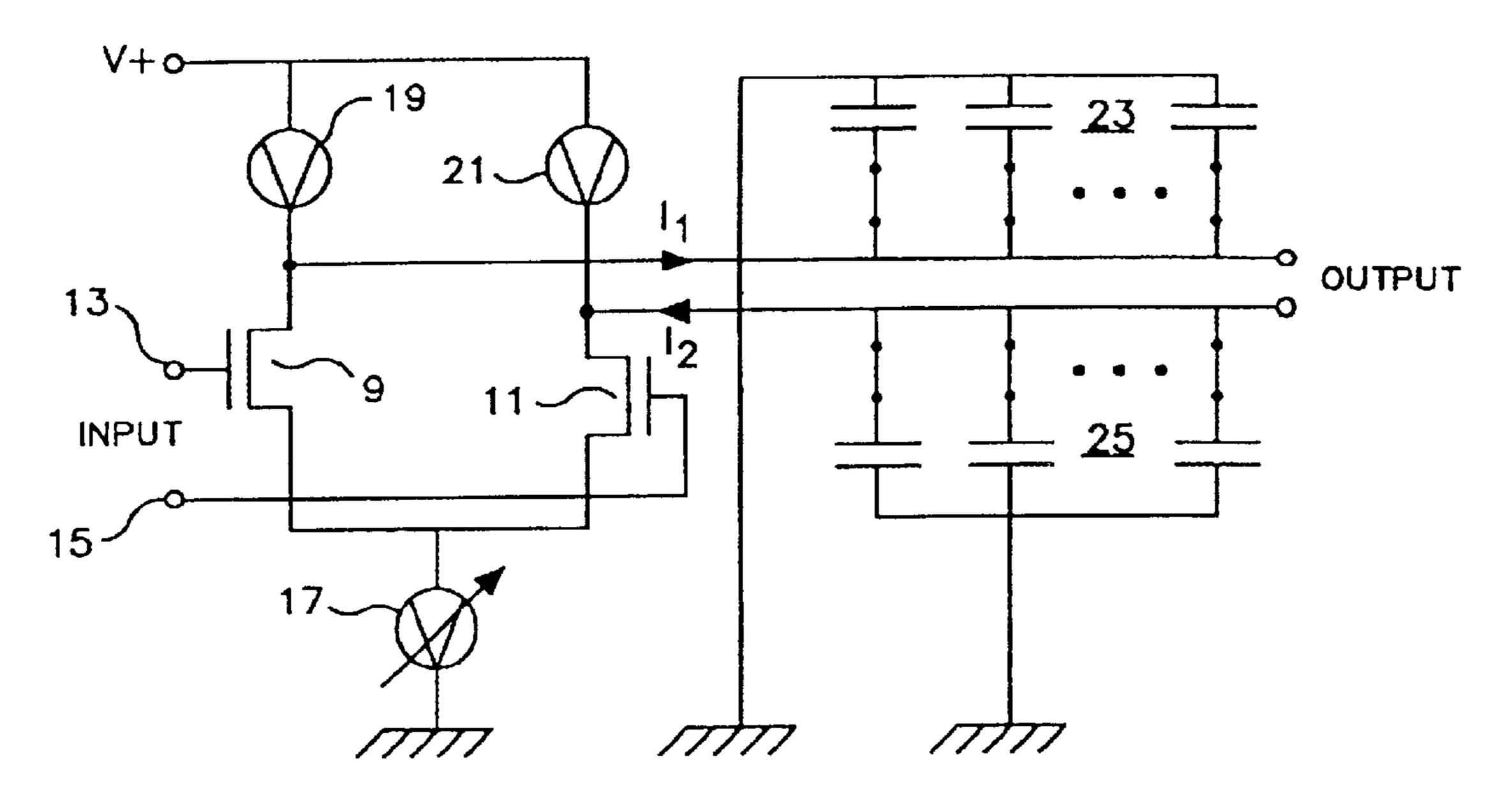


FIGURE 1
(PRIOR ART)

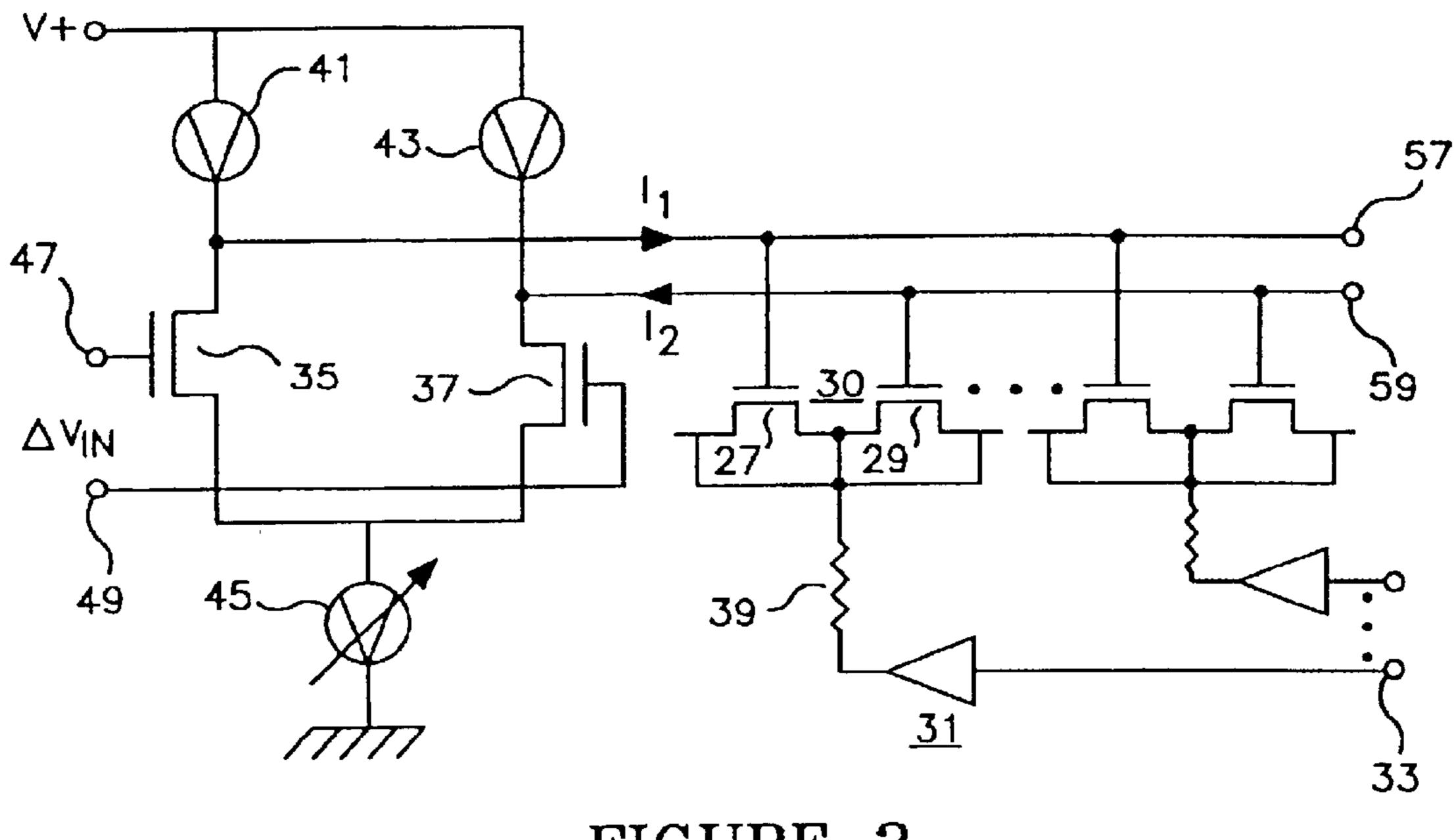


FIGURE 2

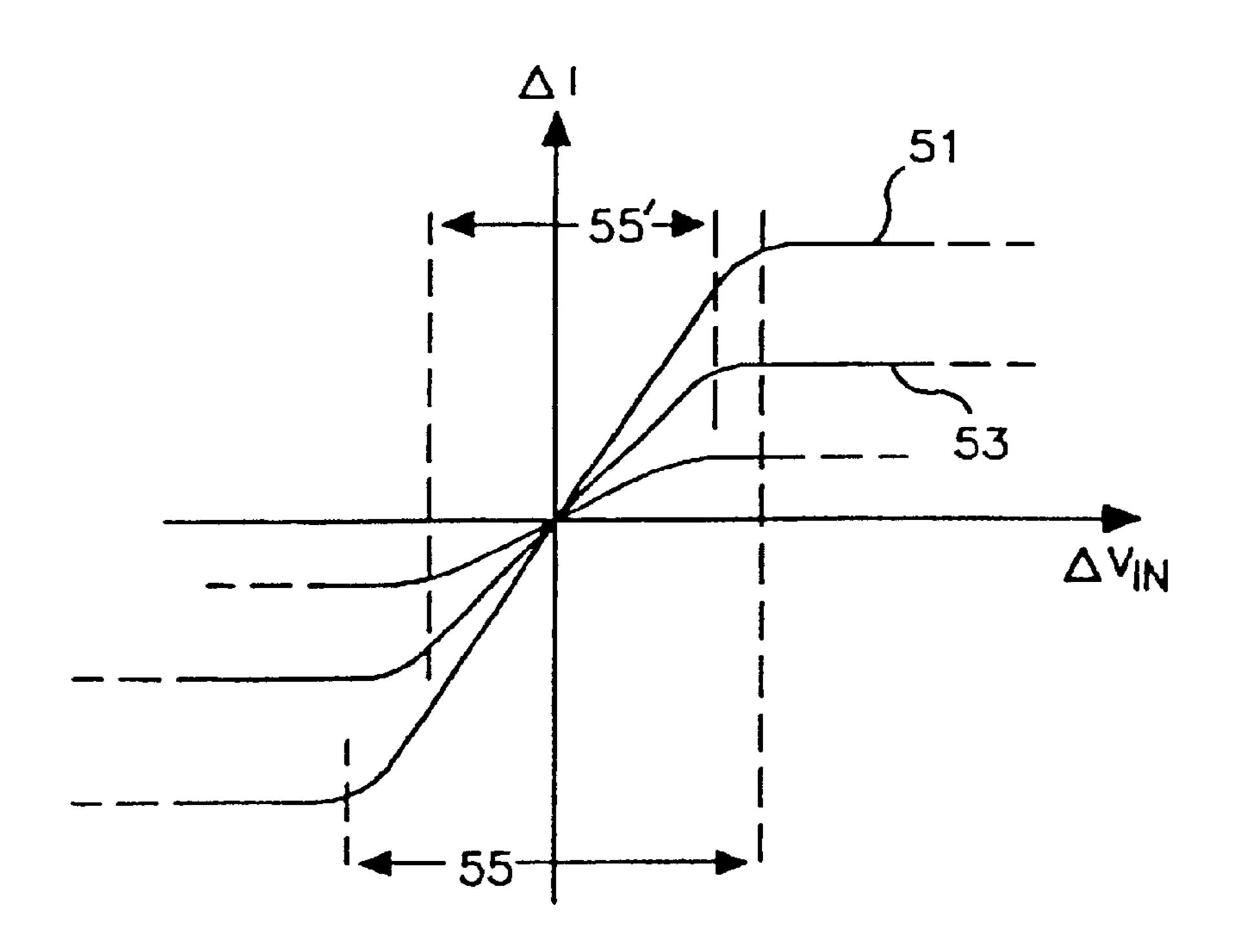


FIGURE 3

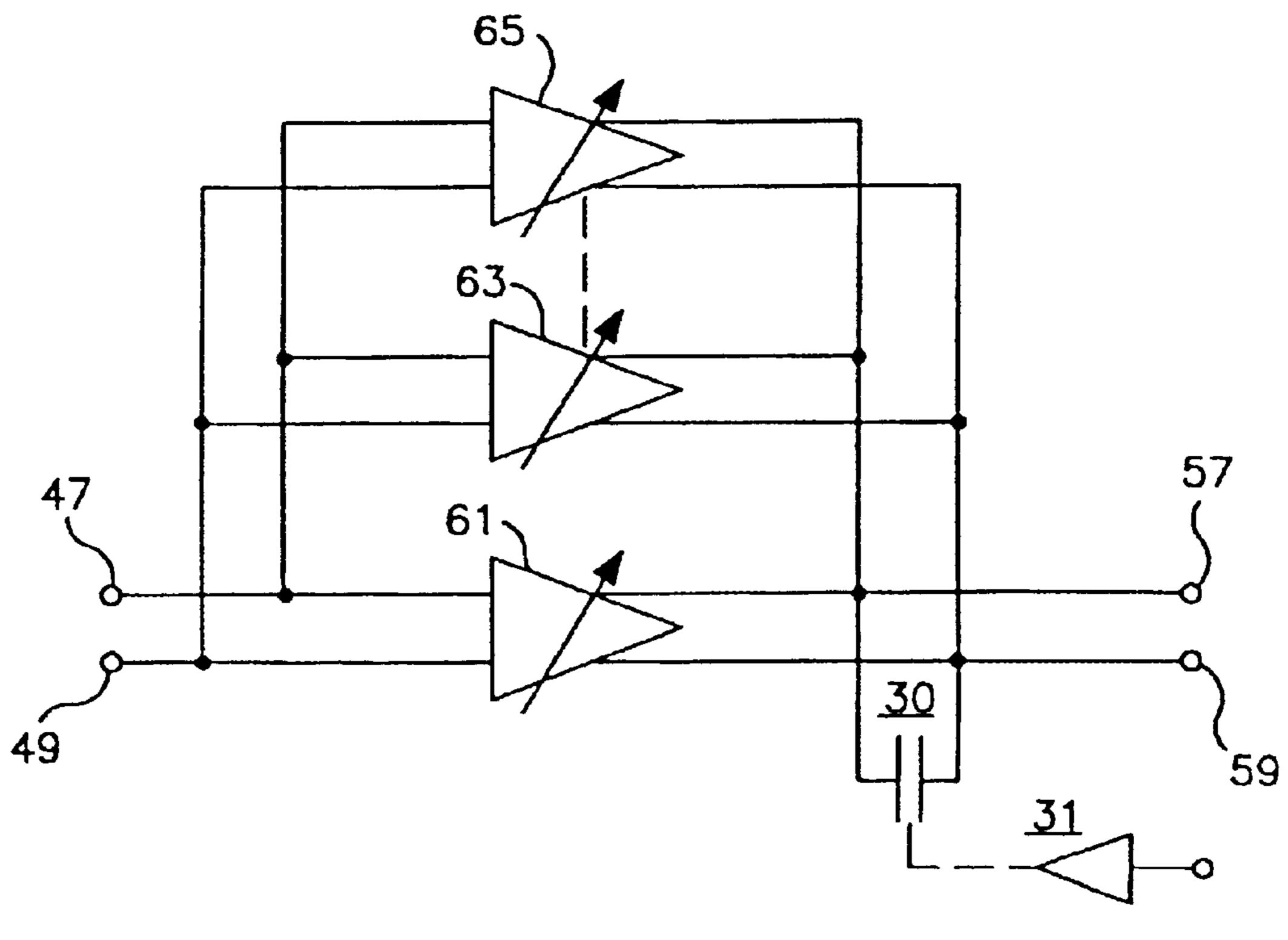


FIGURE 4

CONTROLLABLE INTEGRATOR

Matter enclosed in heavy brackets [] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions 5 made by reissue.

Notice: More than one reissue application has been filed for the reissue of U.S. Pat. No. 5,805,006. The reissue applications are application Ser. Nos. 09/609,007 (now U.S. Reissue Pat. No. RE37,739) and 09/950,086 (the present 10 application), which is a continuation reissue application of U.S. Pat. No. 5,805,006.

FIELD OF THE INVENTION

This invention relates to integrators and more particularly to circuitry in an integrated circuit that controls frequency response characteristics over a wide range of frequencies with adjustable capacitance and controllable transconductance.

BACKGROUND OF THE INVENTION

Circuit components formed in integrated circuits commonly exhibit wide variations in operating characteristics attributable to variations in the semiconductor processes that form the integrated circuit of such components. By traditional design practices, additional or redundant components may be formed in an integrated circuit during the processing phase, and such additional components may thereafter be connected in or out of a circuit using a laser beam to selectively sever connecting links as required to adjust the operating characteristics of the circuit. Alternatively, signal controllable switches may be incorporated into the design of the integrated circuit to selectively connect additional components in response to externally applied control signals. However, such switches are not ideal in that they incorporate appreciable resistance into a circuit in the conductive state which can be detrimental to high frequency operating characteristics of the integrated circuit.

SUMMARY OF THE INVENTION

In accordance with one embodiment of the present invention, additional capacitive components may be selectively switched into circuit configuration in response to external control signals without introducing significant resistance with the capacitive components. In addition, controllable gain elements may be selectively controlled to amplify the effectiveness of capacitive components in the circuit for a wide range of operating frequency characteristics of the circuit as selectively configured.

DESCRIPTION OF THE DRAWINGS

- FIG. 1 is a circuit diagram of a conventional transconductance integrator;
- FIG. 2 is a circuit diagram of one embodiment of the present invention;
- FIG. 3 is a graph illustrating the operating characteristics of a transconductance amplifier; and
- FIG. 4 is a circuit diagram of another embodiment of the present invention for providing wide dynamic control of 60 operating frequency characteristics of the composite circuitry.

DETAILED DESCRIPTION OF THE INVENTION

Referring now to FIG. 1, there is shown a conventional integrator including a differential pair of gain stages 9, 11

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such as field-effect transistors having control electrodes, or gates, coupled to receive control signals applied to inputs 13, 15. The source electrodes, or sources, of the gain stages are coupled together and to a controllable current source 17, and each of the drain electrodes, or drains, is coupled to a controllable current sources 19, 21 and to one or more capacitive elements 23, 25. The sum of the current sources 19, 21 is usually set equal to the current from source 17. Selected ones of the capacitive elements may be coupled to ground, for example, via links that may be removed via laser-beam machining to alter the operating frequency characteristics of the circuit. Alternatively, semiconductor switches may be substituted (not shown) for the links to facilitate control of capacitance in the circuit in response to externally applied signals. However, such semiconductor switches commonly introduce significant resistance along with capacitance thus switched into the circuit, and this adversely affects high frequency operating characteristics of the circuit thus configured.

In accordance with one embodiment of the present invention, one or more differential pairs of capacitive elements are formed for selective connection into the circuit in response to an applied control signal. Specifically, as shown in FIG. 2, each capacitive element is formed as a pair of gain elements 27, 29 such as insulated-gate field-effect transistors with source and drain connected in common as one capacitive electrode and with the gate forming another capacitive electrode. The source-drain connections are connected in common to a control switch 31 that may also include a gain element responsive to an applied control signal for switching in or out the differential pair of capacitive components 27, 29. Specifically, at low-level applied control signal appearing on control input 33 (representative of the ON condition for NMOS type transistors 27, 29) the source-drain connec-35 tions form conductive channels in the region of the respective gates in known manner to form capacitive components differentially connected across the outputs of the gain stages 35, 37. Thus, for each capacitive component of capacitance C, the differential connection of such components yields C/2 40 capacitance, without the equivalent resistance 39 of a control switch (in the biasing circuit) affecting the capacitance in the circuit thus configured. At high-level applied control signal appearing on control input 33 (representative of the OFF) condition for NMOS type transistors 27, 29), wide depletion 45 regions form adjacent the sources-drains, or essentially no channels form in the vicinities of the gates to contribute only a small fraction of the original capacitance introduced into the circuit. One or more banks of differentially connected capacitive components, each controlled by such bias-50 adjusting switching circuitry, may be provided to facilitate adjustment or control of the frequency response characteristics of the circuit thus configured.

Referring now to FIG. 3, there is shown a graph of the transfer function of the differential amplifier of FIG. 2 that includes gain elements 35, 37 and current sources 41, 43, 45 connected as shown. Specifically, as the differential of the control voltages 47, 49 applied to the control electrodes increases, the differential of drain currents I₁, I₂ (ΔI=I₁-I₂) increases, as shown by the curve 51. In the semiconductor amplifier circuit of FIG. 2, the sum of the drain currents 41, 43 substantially equals the combined current 45, and reducing these current levels typically alters the transfer function of the semiconductor amplifier, as shown by curve 53. The range of control voltages 55 over which the transfer function remains substantially linear diminishes with reduced current levels, as illustrated with reference to curve 53. Thus, at low levels of the combined source currents through current

source 45, the substantially linear range of the transfer function on applied control voltages is narrow, and widens 55 with increased current levels. However, for a given level of the combined currents through source 45, significant increases in applied signal voltages appearing at inputs 47, 49 introduces significant non-linearity in the transfer function for operation at applied signal levels beyond the substantially linear range 55.

In accordance with another embodiment of the present invention, a plurality of amplifiers similar to the amplifier of $_{10}$ FIG. 2 are assembled in parallel, as illustrated in FIG. 4, between the differential inputs 47, 49 and the differential outputs 57, 59. Each of the amplifiers may be selectively controlled, for example, via a controllable current source 45 that conducts the currents from the commonly connected sources in each amplifier. In this way, each of the amplifiers 61, 63, 65 may be selectively disabled or enabled to selectively expand the linear range 55, 55' of the combined transfer function. In addition, with one or more pairs of differentially connected capacitive components 27, 29 connected across the outputs 57, 59, the range of frequencies over which the integrated circuit may be operated can be greatly increased, for example, to over 6:1 for operations at about 40 MHz to about 270 MHz. Additionally, for selected values of capacitance C switched into the circuit in the 25 manner previously described, control of one or more of the current sources in the amplifiers 61, 63, 65 may thus be externally controlled to maintain the transconductance (g_m) to capacitance (C) ratio (g_m/C) substantially constant over a population of integrated circuits thus configured, and for 30 operation of a particular integrated circuit with selected frequency response characteristics. Of course, various known semiconductor technologies such as bi-polar or NMOS or CMOS processes may be used to form integrated circuits including amplifiers and capacitive components, as 35 described above.

Therefore, one design of integrated circuit according to the present invention facilitates formation of g_m/C integrators operable over a wide range of frequencies, with dynamic responses conveniently controllable by signals that $_{40}$ may be internal or external to the integrated circuit.

What is claimed is:

[1. Integrator apparatus comprising:

an amplifier including a pair of outputs and being responsive to differential input signals for producing differ- 45 ential output signals on the pair of outputs; and

- a pair of capacitive components connected to the pair of outputs and to a common source of first control signal, the capacitive components including insulated-gate, field-effect transistors having gates connected to 50 respective ones of the pair of outputs and having sources and drains connected in common to receive said first control signal for altering the capacitance of each pair of capacitive component in response to the first control signal applied to the sources and drains 55 thereof.]
- [2. Integrator apparatus according to claim 1 comprising a plurality of pairs of capacitive components, each including insulated-gate, field-effect transistors having gates connected to respective ones on the pair of outputs and having sources and drains connected in common to receive the first control signal therefor for altering the capacitance of the capacitive components in response to the first control signal applied to the sources and drains of each of the plurality of pairs of capacitive components.]

[3. Integrator apparatus according to claim 2 wherein the amplifier includes a plurality of differential amplifiers, each

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having a pair of outputs coupled in common to the plurality of pairs of capacitive components, and each having a pair of inputs connected in common to receive applied differential signals, at least one of the plurality of differential amplifiers also having a transfer function from inputs thereof to outputs thereof that is controllable in response to a second control signal applied thereto for altering the combined transfer function of the plurality of differential amplifiers from the inputs thereof connected in common to the differential outputs thereof coupled in common in response to applied second control signal.

- [4. Integrator apparatus according to claim 1 wherein said amplifier includes a pair of field-effect transistors, each having a drain electrode connected to respective ones of said pair of outputs, and having source electrodes connected in common, with the source and drain electrodes of each transistor forming a conduction channel thereof, and transistors having gate electrodes connected to receive the differential input signals applied thereto to alter the conduction channel thereof; and
 - a current source connected to the drain electrode of each transistor, and another current source connected to the common connection of the source electrodes for conducting the sum of currents in the conduction channels of the pair of transistors.
- [5. Integrator apparatus according to claim 4 wherein said another current source is adjustable to alter the transfer function of the amplifier from the gate electrodes to the pair of outputs thereof.]
- [6. Integrator apparatus according to claim 3 wherein the second control signal is adjusted to maintain substantially constant the ratio of the transconductance of the amplifier to the capacitance provided by the capacitive components in response to first control signal applied thereto.]
 - 7. Integrator apparatus comprising:
 - a plurality of differential amplifiers connected in parallel, said plurality of differential amplifiers having differential inputs connected in common to receive an applied differential signal,
 - said plurality of differential amplifiers having differential outputs connected in common to output a differential amplified signal, and
 - each of said plurality of differential amplifiers having a transfer function from input thereof to output thereof, wherein each of said plurality of differential amplifiers is individually controllable in response to a respective control signal applied thereto, for altering the transfer function of a corresponding one of said plurality of differential amplifiers from the input thereof to the output thereof.
 - 8. Integrator apparatus, comprising:
 - a plurality of differential amplifiers connected in parallel, said plurality of differential amplifiers having differential inputs connected in common to receive an applied differential signal,
 - said plurality of differential amplifiers having differential outputs connected in common to output a differential amplified signal,
 - each of said plurality of differential amplifiers having a transfer function from input thereof to output thereof, wherein each of said plurality of differential amplifiers is individually controllable in response to a respective control signal applied thereto, for altering the transfer function of a corresponding one of said plurality of differential amplifiers from the input thereof to the output thereof, and

wherein each of said plurality of differential amplifiers is selectively enabled or disabled.

9. Integrator apparatus, comprising:

a plurality of differential amplifiers connected in parallel, said plurality of differential amplifiers having differential 5 inputs connected in common to receive an applied differential signal,

said plurality of differential amplifiers having differential outputs connected in common to output a differential amplified signal,

each of said plurality of differential amplifiers having a transfer function from input thereof to output thereof, wherein each of said plurality of differential amplifiers is individually controllable in response to a respective control signal applied thereto, for altering the transfer function of a corresponding one of said plurality of differential amplifiers from the input thereof to the output thereof, and

wherein each of said plurality of differential amplifiers is selectively controllable to expand the linear range of a combined transfer function of the integrator apparatus.

10. Integrator apparatus according to claim 7, further comprising a plurality of constant current sources each providing a respective control signal to a corresponding one of the plurality of differential amplifiers.

11. An amplifier comprising:

a plurality of differential amplifiers, each having:

a pair of gain elements having (i) a pair of differential input terminals, (ii) a pair of differential output terminals, and (iii) a pair of common terminals; and a controllable current source in combination with said 30 pair of common terminals,

wherein said plurality of differential amplifiers are connected in parallel,

wherein each of said pair of differential input terminals is connected in common with the differential input termi- 35 nals of other ones of said plurality of differential amplifiers,

wherein each of said pair of differential output terminals is connected in common with the differential output terminals of other ones of said plurality of differential 40 amplifiers,

wherein each of said plurality of differential amplifiers has a response characteristic defined by a corresponding transfer function from said pair of input terminals to said pair of output terminals, and

wherein each of said controllable current source individually controls the corresponding transfer function of a respective one of said plurality of differential amplifiers.

12. An amplifier, comprising:

a plurality of differential amplifiers, each having: a pair of gain elements having:

(i) a pair of differential input terminals,

(ii) a pair of differential output terminals, and

(iii) a pair of common terminals; and

a controllable current source in combination with said pair of common terminals,

wherein said plurality of differential amplifiers are connected in parallel,

wherein each of said pair of differential input terminals is 60 connected in common with the differential input terminals of other ones of said plurality of differential amplifiers,

wherein each of said pair of differential output terminals is connected in common with the differential output 65 terminals of other ones of said plurality of differential amplifiers,

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wherein each of said plurality of differential amplifiers has a response characteristic defined by a corresponding transfer function from said pair of input terminals to said pair of output terminals,

wherein each of said controllable current source individually controls the corresponding transfer function of a respective one of said plurality of differential amplifiers, and

wherein each of said plurality of differential amplifiers is selectively enabled or disabled.

13. An amplifier, comprising:

a plurality of differential amplifiers, each having: a pair of gain elements having:

(i) a pair of differential input terminals,

(ii) a pair of differential output terminals, and

(iii) a pair of common terminals; and

a controllable current source in communication with said pair of common terminals,

wherein said plurality of differential amplifiers are connected in parallel,

wherein each of said pair of differential input terminals is connected in common with the differential input terminals of other ones of said plurality of differential amplifiers,

wherein each of said pair of differential output terminals is connected in common with the differential output terminals of other ones of said plurality of differential amplifiers,

wherein each of said plurality of differential amplifiers has a response characteristic defined by a corresponding transfer function from said pair of input terminals to said pair of output terminals,

wherein each of said controllable current source individually controls the corresponding transfer function of a respective one of said plurality of differential amplifiers, and

wherein each of said plurality of differential amplifiers is selectively controllable to expand the linear range of a combined transfer function of the amplifier.

14. An amplifier comprising:

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a plurality of differential amplifiers connected in parallel, each having:

a pair of differential input terminals;

a pair of differential output terminals; and a controllable current source,

wherein each of said pair of differential input terminals is connected in common with the differential input terminals of other ones of said plurality of differential amplifiers,

wherein each of said pair of differential output terminals is connected in common with the differential output terminals of other ones of said plurality of differential amplifiers,

wherein each of said plurality of differential amplifiers has a response characteristic defined by a corresponding transfer function from said pair of input terminals to said pair of output terminals, and

wherein each of said controllable current source individually controls the corresponding transfer function of a respective one of said plurality of differential amplifiers.

15. An amplifier, comprising:

a plurality of differential amplifiers connected in parallel, each having:

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a pair of differential input terminals; a pair of differential output terminals; and a controllable current source,

- wherein each of said pair of differential input terminals is connected in common with the differential input terminals of other ones of said plurality of differential amplifiers,
- wherein each of said pair of differential output terminals is connected in common with the differential output 10 terminals of other ones of said plurality of differential amplifiers,
- wherein each of said plurality of differential amplifiers has a response characteristic defined by a corresponding transfer function from said pair of input terminals 15 to said pair of output terminals,
- wherein each of said controllable current source individually controls the corresponding transfer function of a respective one of said plurality of differential 20 amplifiers, and
- wherein each of said plurality of differential amplifiers is selectively enabled or disabled.
- 16. An amplifier, comprising:
- a plurality of differential amplifiers connected in parallel, 25 each having:
 - a pair of differential input terminals,;
 - a pair of differential output terminals; and
 - a controllable current source,
- wherein each of said pair of differential input terminals is connected in common with the differential input terminals of other ones of said plurality of differential amplifiers,
- wherein each of said pair of differential output terminals is connected in common with the differential output terminals of other ones of said plurality of differential amplifiers,
- wherein each of said plurality of differential amplifiers has a response characteristic defined by a correspond- 40 ing transfer function from said pair of input terminals to said pair of output terminals,
- wherein each of said controllable current source individually controls the corresponding transfer function of a respective one of said plurality of differential 45 amplifiers, and
- wherein each of said plurality of differential amplifiers is selectively controllable to expand the linear range of a combined transfer function of the amplifier.
- 17. Integrator apparatus comprising:
- a plurality of differential amplifier means for amplifying a differential signal connected in parallel,
- said plurality of differential amplifier means having differential inputs connected in common to receive an 55 applied differential signal,
- said plurality of differential amplifier means having differential outputs connected in common to output a differential amplified signal, and
- each of said plurality of differential amplifier means 60 having a transfer function from input thereof to output thereof, wherein each of said plurality of differential amplifier means is individually controllable in response to a respective control signal applied thereto, for altering the transfer function of a corresponding one of said 65 plurality of differential amplifier means from the input thereof to the output thereof.

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- 18. Integrator apparatus, comprising:
- a plurality of differential amplifier means for amplifying a differential signal connected in parallel,
- said plurality of differential amplifier means having differential inputs connected in common to receive an applied differential signal,
- said plurality of differential amplifier means having differential outputs connected in common to output a differential amplified signal,
- each of said plurality of differential amplifier means having a transfer function from input thereof to output thereof, wherein each of said plurality of differential amplifier means is individually controllable in response to a respective control signal applied thereto, for altering the transfer function of a corresponding one of said plurality of differential amplifier means from the input thereof to the output thereof, and
- wherein each of said plurality of differential amplifier means is selectively enabled or disabled.
- 19. Integrator apparatus, comprising:
- a plurality of differential amplifier means for amplifying a differential signal connected in parallel,
- said plurality of differential amplifier means having differential inputs connected in common to receive an applied differential signal,
- said plurality of differential amplifier means having differential outputs connected in common to output a differential amplified signal,
- each of said plurality of differential amplifier means having a transfer function from input thereof to output thereof, wherein each of said plurality of differential amplifier means is individually controllable in response to a respective control signal applied thereto, for altering the transfer function of a corresponding one of said plurality of differential amplifier means from the input thereof to the output thereof, and
- wherein each of said plurality of differential amplifier means is selectively controllable to expand the linear range of a combined transfer function of the integrator apparatus.
- 20. An amplifier comprising:
- a plurality of differential amplifier means for amplifying a differential signal, each having:
 - a pair of gain means having (i) a pair of differential input means for inputting a differential signal, (ii) a pair of differential output means for outputting a differential signal, and (iii) a pair of common means; and
 - a controllable current source means for providing a current in communication with said pair of common *means*;
- wherein said plurality of differential amplifier means are connected in parallel;
- wherein each of said pair of differential input means is connected in common with the differential input means of other ones of said plurality of differential amplifier *means*;
- wherein each of said pair of differential output means is connected in common with the differential output means of other ones of said plurality of differential amplifier means;
- wherein each of said plurality of differential amplifier means has a response characteristic defined by a corresponding transfer function from said pair of input means to said pair of output means; and

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- wherein each of said controllable current source means individually controls the corresponding transfer function of a respective one of said plurality of differential amplifier means.
- 21. An amplifier, comprising:
- a plurality of differential amplifier means for amplifying a differential signal, each having:
 - a pair of gain means having:
 - (i) a pair of differential input means for inputting a differential signal,
 - (ii) a pair of differential output means for outputting a differential signal, and
 - (iii) a pair of common means; and
 - a controllable current source means for providing a current in communication with said pair of common 15 means;
- wherein said plurality of differential amplifier means are connected in parallel;
- wherein each of said pair of differential input means is connected in common with the differential input means 20 of other ones of said plurality of differential amplifier means;
- wherein each of said pair of differential output means is connected in common with the differential output means of other ones of said plurality of differential ²⁵ amplifier means;
- wherein each of said plurality of differential amplifier means has a response characteristic defined by a corresponding transfer function from said pair of input means to said pair of output means,
- wherein each of said controllable current source means individually controls the corresponding transfer function of a respective one of said plurality of differential amplifier means, and
- wherein each of said plurality of differential amplifier ³⁵ means is selectively enabled or disabled.
- 22. An amplifier, comprising:
- a plurality of differential amplifier means for amplifying a differential signal, each having:
 - a pair of gain means having:
 - (i) a pair of differential input means for inputting a differential signal,
 - (ii) a pair of differential output means for outputting a differential signal, and
 - (iii) a pair of common means; and
 - a controllable current source means for providing a current in communication with said pair of common means,
- wherein said plurality of differential amplifier means are connected in parallel,
- wherein each of said pair of differential input means is connected in common with the differential input means of other ones of said plurality of differential amplifier means,
- wherein each of said pair of differential output means is connected in common with the differential output means of other ones of said plurality of differential amplifier means,
- wherein each of said plurality of differential amplifier 60 means has a response characteristic defined by a corresponding transfer function from said pair of input means to said pair of output means,
- wherein each of said controllable current source means individually controls the corresponding transfer func- 65 tion of a respective one of said plurality of differential amplifier means, and

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- wherein each of said plurality of differential amplifier means is selectively controllable to expand the linear range of a combined transfer function of the amplifier. 23. An amplifier comprising:
- a plurality of differential amplifier means connected in parallel, each having:
 - a pair of differential input means for inputting a differential signal,
 - a pair of differential output means for outputting a differential signal, and
 - a controllable current source means for supplying a current;
- wherein each of said pair of differential input means is connected in common with the differential input means of other ones of said plurality of differential amplifier means;
- wherein each of said pair of differential output means is connected in common with the differential output means of other ones of said plurality of differential amplifier means;
- wherein each of said plurality of differential amplifier means has a response characteristic defined by a corresponding transfer function from said pair of input means to said pair of output means; and
- wherein each of said controllable current source means individually controls the corresponding transfer function of a respective one of said plurality of differential amplifier means.
- 24. An amplifier, comprising:
- a plurality of differential amplifier means connected in parallel, each having:
 - a pair of differential input means for inputting a differential signal,
 - a pair of differential output means for outputting a differential signal, and
 - a controllable current source means for supplying a current;
- wherein each of said pair of differential input means is connected in common with the differential input means of other ones of said plurality of differential amplifier means,
- wherein each of said pair of differential output means is connected in common with the differential output means of other ones of said plurality of differential amplifier means,
- wherein each of said plurality of differential amplifier means has a response characteristic defined by a corresponding transfer function from said pair of input means to said pair of output means,
- wherein each of said controllable current source means individually controls the corresponding transfer function of a respective one of said plurality of differential amplifier means, and
- wherein each of said plurality of differential amplifier means is selectively enabled or disabled.
- 25. An amplifier, comprising:
- a plurality of differential amplifier means connected in parallel, each having:
 - a pair of differential input means for inputting a differential signal,
 - a pair of differential output means for outputting a differential signal, and
 - a controllable current source means for supplying a current;
- wherein each of said pair of differential input means is connected in common with the differential input means of other ones of said plurality of differential amplifier means,

wherein each of said pair of differential output means is connected in common with the differential output means of other ones of said plurality of differential amplifier means,

wherein each of said plurality of differential amplifier ⁵ means has a response characteristic defined by a corresponding transfer function from said pair of input means to said pair of output means,

wherein each of said controllable current source means individually controls the corresponding transfer function of a respective one of said plurality of differential amplifier means, and

wherein each of said plurality of differential amplifier means is selectively controllable to expand the linear range of a combined transfer function of the amplifier. 26. A method of integrating an applied differential signal comprising the steps of:

providing a plurality of differential amplifiers connected in parallel,

arranging differential inputs of the plurality of differential in common to receive the applied differential signal,

arranging differential outputs of the plurality of differential amplifiers in common to output a differential amplified signal,

wherein each of the plurality of differential amplifiers has a transfer function from input thereof to output thereof, and

individually controlling each of said plurality of differential amplifiers in response to a respective control signal applied thereto, for altering the transfer function 12

of a corresponding one of said plurality of differential amplifiers from the input thereof to the output thereof. 27. A method of amplifier an applied signal comprising the steps of:

providing a plurality of differential amplifiers, each having:

a pair of gain elements having (i) a pair of differential input terminals, (ii) a pair of differential output terminals, and (iii) a pair of common terminals;

applying a current to the pair of common terminals; arranging the plurality of differential amplifiers in parallel;

arranging each of the pair of differential input terminals nals in common with the differential input terminals of other ones of the plurality of differential amplifiers;

arranging each of the pair of differential output terminals nals in common with the differential output terminals of other ones of the plurality of differential amplifiers;

wherein each of the plurality of differential amplifiers has a response characteristic defined by a corresponding transfer function from the pair of input terminals to the pair of output terminals; and

individually controlling the current applied to a respective one of the plurality of differential amplifiers to individually control the corresponding transfer function thereof.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : RE38,455 E

APPLICATION NO. : 09/950086

DATED : March 9, 2004

INVENTOR(S) : Sehat Sutardja et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification

Column 1, Line 9 Insert -- 10/614,084,-- after "Ser. Nos."

Signed and Sealed this
Twentieth Day of May, 2014

Michelle K. Lee

Michelle K. Lee

Deputy Director of the United States Patent and Trademark Office