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(54) **DYNAMIC RANDOM ACCESS MEMORY USING IMPERFECT ISOLATING TRANSISTORS**

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**Related U.S. Patent Documents**

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- (52) **U.S. Cl.** ..... **365/203; 365/149; 365/208**
- (58) **Field of Search** ..... **365/203, 149, 365/208, 189.01, 222, 204, 205, 207**

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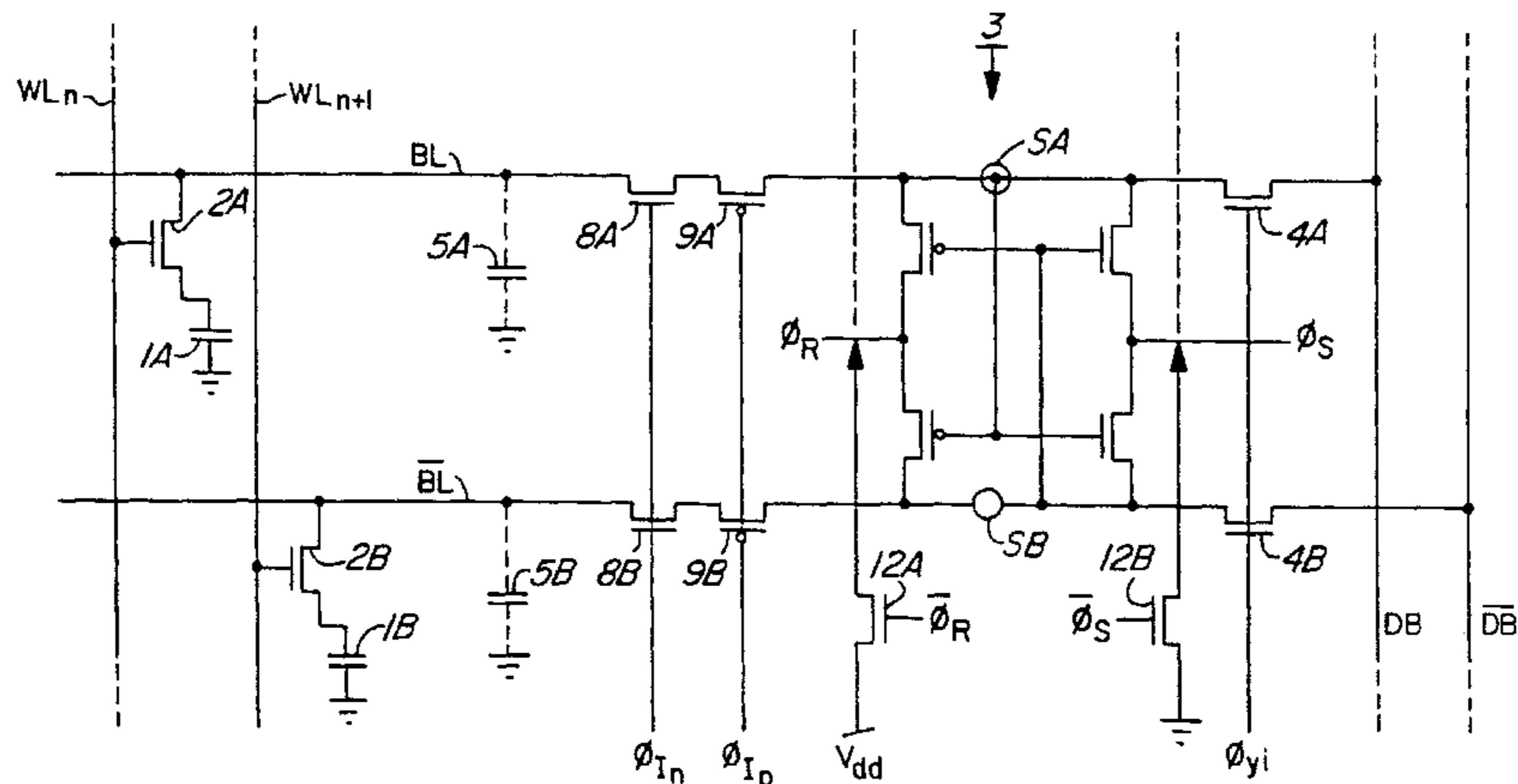
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(57) **ABSTRACT**

Apparatus and methods for controlling the sensing of bit lines which facilitates the distribution of bit line charging current to be distributed any time, and facilitates the fast raising of the sense modes to full logic levels. An embodiment is comprised of a plurality of bit storage capacitors, a folded bit line for receiving charge stored on one of the capacitors, having bit line capacitance, a sense amplifier having a pair of sense nodes for sensing a voltage differential across the sense nodes, apparatus connected to the bit line and the sense nodes for imperfectly isolating the sense nodes from the bit line whereby current can leak therethrough, apparatus for enabling the sense amplifier and for disabling the isolating apparatus and thereby removing the isolation between the sense amplifier and the bit line, whereby current passing through the sense amplifier to the sense nodes is enabled to charge the bit line capacitance through the isolating apparatus to predetermined logic voltage level.

**36 Claims, 3 Drawing Sheets**



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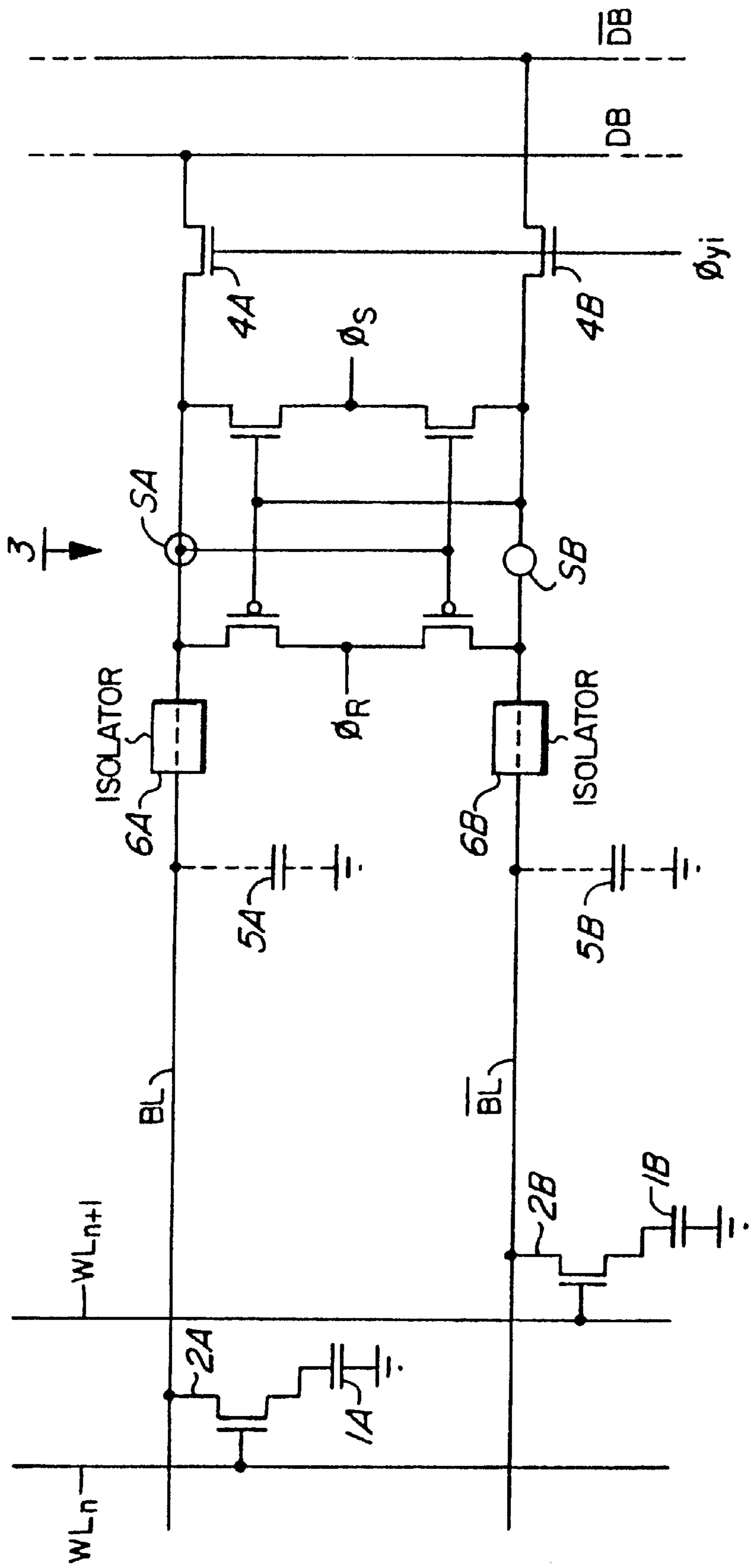


FIG. 1 PRIOR ART

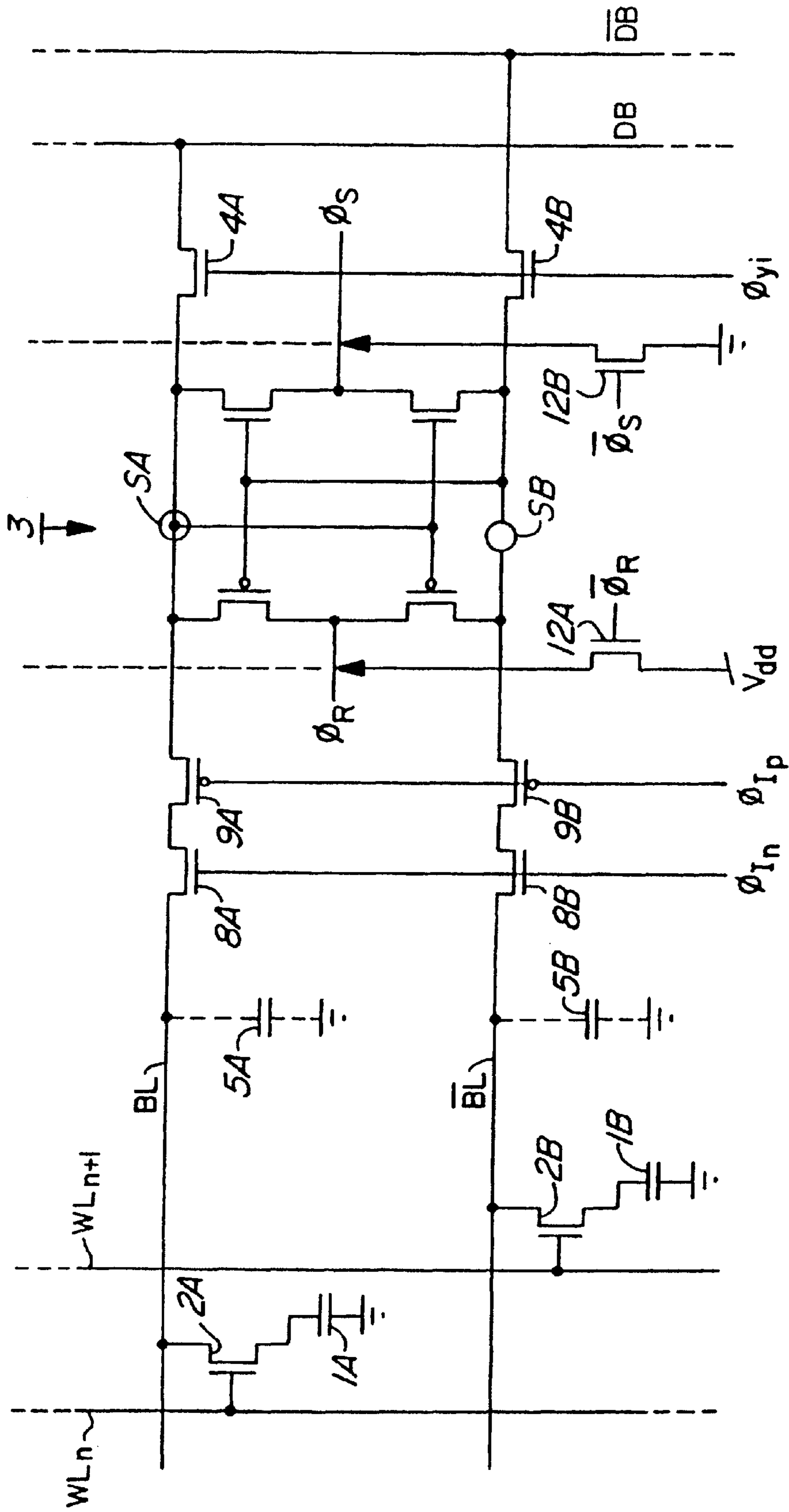


FIG. 2

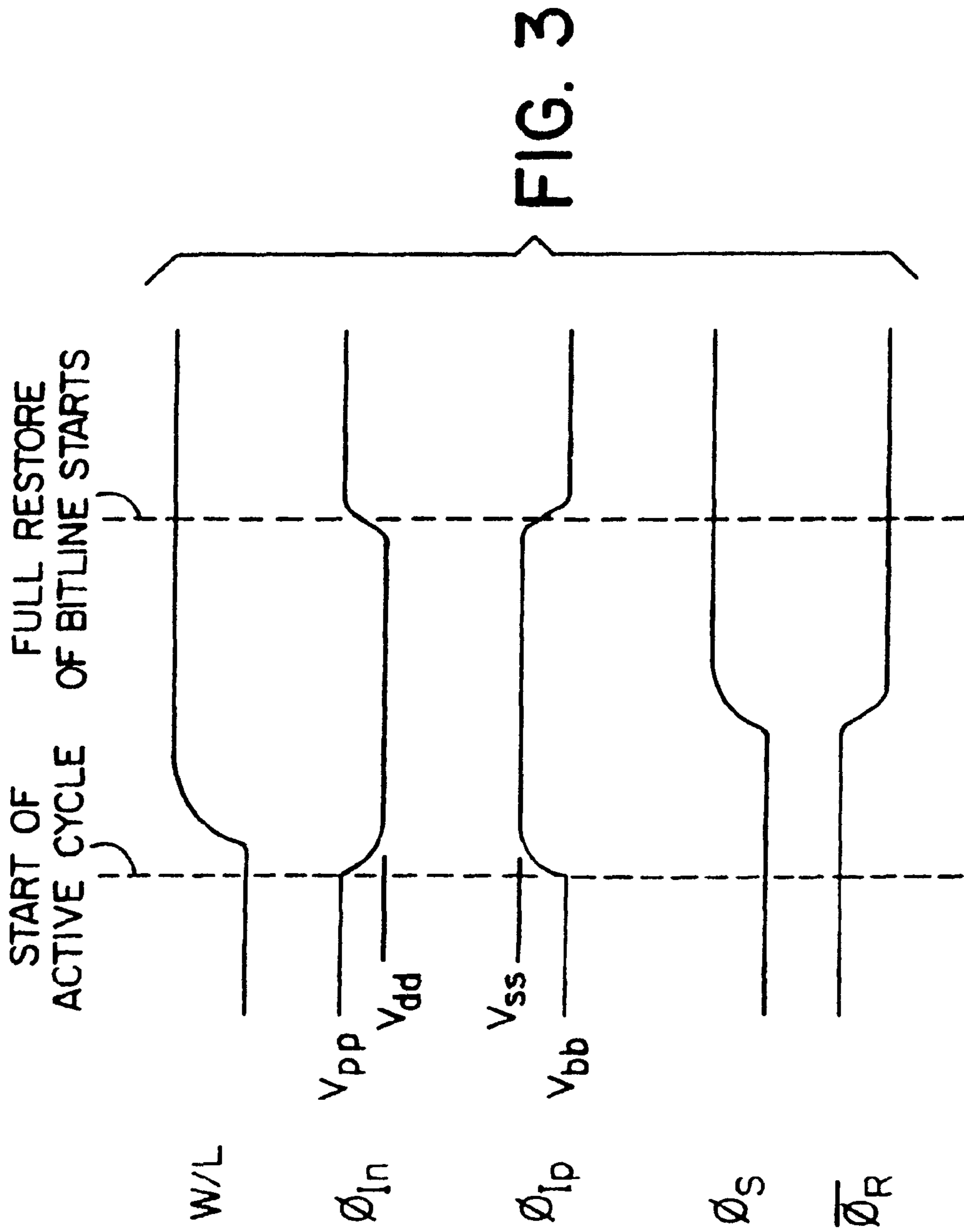


FIG. 3

**DYNAMIC RANDOM ACCESS MEMORY  
USING IMPERFECT ISOLATING  
TRANSISTORS**

**Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.**

This application is a continuation application of Ser. No. 07/680,747, filed Apr. 5, 1991, now abandoned.

**FIELD OF THE INVENTION**

This invention relates to semiconductor dynamic random access memories (DRAMs) and in particular to apparatus and methods for controlling the sensing of bit lines.

**BACKGROUND TO THE INVENTION**

A DRAM is generally formed of an array of bit storage capacitors which are accessed via word lines and bit lines, the word lines being located in rows and the bit lines being located in columns. The capacitors are coupled via access transistors to the bit lines upon being enabled by the word lines; each capacitor is thus associated with the intersection of a bit line and word line.

In high speed DRAMs, the bit lines are usually provided as a folded bit line (pairs of complementary bit lines), with a sense amplifier connected to both bit lines of a folded bit line. During a read operation the charge stored on a capacitor is dumped on one of the lines of the folded bit lines, and the sense amplifier senses the resulting differential in potential between the two lines of a folded bit line, applying full logic voltage levels to the bit lines which both restore the charge on the storage capacitors and apply full logic levels to data buses to which the bit lines are coupled.

Bit lines typically have a capacitance of around 0.2–0.5 pF. During sensing, current being passed through the sense amplifier to provide full logic voltage levels on the bit lines is consumed in charging the capacitance of the bit lines. The bit line voltage differential must exceed a certain noise margin before the levels on the bit lines can be read to the databases. Clearly the voltage differential on the lines of the bit lines must be above that certain level, which requires a substantial capacitor charging time, which in turn results in a slowed sensing interval.

A technique for attempting to deal with bit line capacitance is to insert an isolation device to isolate the sense nodes associated with the sense amplifier from the bit lines during the initial sensing period. In other words, a memory capacitor associated with one of the lines of the bit line is enabled to dump its charge on one bit line, following which both bit lines are completely isolated from the sense amplifier. Since the small amount of capacitance associated with the sense node retains some charge differential, subsequent enabling of the sense amplifier causes it to sense this differential, and to apply the full logic level to the sense nodes for application to the database. Since the sense nodes are now completely isolated from the bit lines, the bit lines need not be charged up by the power supply associated with the sense amplifier, and the time for charging the bit line capacitances thus is substantially eliminated.

However since the capacitance associated with the sense nodes isolated from the bit lines is so small, only a fraction of the total charge differential is available for sensing. This is dangerous, in the sense that the differential can be marginal, and an erroneous bit sensed. In addition, operation of the isolators introduces an additional step in a memory access sequence, sacrificing memory speed.

It has also been found that the conductive tracks which carry the sense amplifier clock signals must supply considerable current in order to provide, for all sense amplifiers on the chip, full logic levels. That current must not only charge the bit lines and sense nodes, but also the databases. The conductive tracks across the semiconductor integrated circuit contains resistance, and the heavy clock current passing down the tracks creates a voltage difference. This creates a significant differential in the speed of operation of sense amplifiers close to the sense amplifier clock drivers from those at the far ends of the tracks. Access of data from the memory must be slowed to accommodate the slowest sense amplifier.

**SUMMARY OF THE INVENTION**

One embodiment of the present invention uses an isolation device as in the prior art described above, but utilizes an imperfect isolation device which can be enabled over an interval and in addition provide a voltage drop. Preferably the isolation device is a field effect transistor (FET) which has its source drain circuit in series between a sense node and an associated bit line. The gate of each FET is held at a voltage which maintains it imperfectly open, and changes to a level which allows each FET to conduct when the sense amplifier operates (e.g. its gate-source voltage is similar to the logic level supplied by the sense amplifier). The imperfect isolation referred to herein means that the source-drain of the FET is in a high resistance state, but allows some charge leakage through it.

Thus when the memory capacitor dumps its charge on the associated bit line, the charge leaks through the imperfect isolation device to the associated sense node of the sense amplifier. During a first part of the sense cycle the voltage on the gate of each isolation field effect transistor is changed to the logic level which is to be applied to the sense amplifier. Due to the leakage through the imperfect isolating device, charge from the memory capacitor leaks to the sense node.

During a subsequent portion of the sense interval, the sense amplifier is enabled. Due to the charge differential between its sense nodes, the sense amplifier applies full logic voltage level to the sense nodes, which is applied to the databases. However due to the voltage drop across the isolating FET, there is significantly less current consumed in charging the bit line capacitance. As a result the sense nodes reach full logic levels considerably faster than in the prior art.

Some time after sensing is started, the gate source bias of the isolating FET is increased to allow bit lines to be charged to full logic levels (overcoming the threshold voltage drop in the FET). This allows bit line charging current to be distributed over time.

According to an embodiment of the present invention, a dynamic random access memory (DRAM) is comprised of a plurality of bit storage capacitors, a folded bit line for receiving charge stored on one of the capacitors, having bit line capacitance, a sense amplifier having a pair of sense nodes for sensing a voltage differential across the sense nodes, apparatus connected to the bit line and the sense nodes for imperfectly isolating the sense nodes from the bit line whereby current can leak therethrough, apparatus for enabling the sense amplifier and for disabling the isolating apparatus and thereby removing the isolation between the sense amplifier and the bit line, whereby current passing through the sense amplifier to the sense nodes is enabled to charge the bit line capacitance through the isolating apparatus to predetermined logic voltage level.

In accordance with another embodiment of the invention a dynamic random access memory (DRAM) is comprised of a plurality of bit lines and associated sense amplifiers, the bit lines being arrayed across an integrated circuit chip and the sense amplifiers being disposed in a row, a pair of low resistance power supply conductors extending in parallel with the row for carrying logic high level and logic low level voltages, sense amplifier enabling signal conductors extending across the chip accessible to the sense amplifiers, apparatus for coupling sense inputs of the sense amplifiers to the power supply conductors, and apparatus coupling the sense amplifier enabling signal conductors to the apparatus for coupling sense inputs, for enabling passage of current resulting from the logic high level and low level voltages to the sense amplifiers.

In accordance with another embodiment of the present invention a dynamic random access memory (DRAM) is comprised of a plurality of bit storage capacitors, a folded bit line for receiving charge stored on one of the capacitors having bit line capacitance, a sense amplifier having a pair of sense nodes for sensing a voltage differential across the sense nodes, the sense amplifier having respective sense enable and restore enable inputs for providing full high and full low logic levels respectively to the sense nodes, power supply apparatus for providing full high and full low logic level voltages, a pair of field effect transistors, one having its source-drain circuit connected between the restore enable input and the high logic level power supply voltage and the other having its source-drain circuit connected between the sense enable input and the power supply low-logic level power supply voltage, and apparatus for providing restore and sense signals to gates of the one and other field effect transistors respectively, whereby restore and sense current is supplied to the sense amplifier from the power supply apparatus rather than from the apparatus for providing restore and sense signals.

In accordance with a further embodiment of the invention, a method of sensing in a folded bit line type of dynamic random access memory (DRAM) having a bit storage capacitor for coupling to the bit line and a sensing amplifier having sense nodes, is comprised of the steps of imperfectly isolating the sense nodes of the sensing amplifier from the bit line using an imperfectly isolating apparatus, coupling the capacitor to the bit line thereby dumping its charge thereon, leaking the charge through the imperfect isolating apparatus to one of the sense nodes thereby causing a voltage differential across the sense nodes, sensing the differential by the sense amplifier, and applying full high and low logic levels respectively to the sense nodes, and, inhibiting isolation of the sense nodes from the bit lines, whereby full logic levels are applied to the complementary bit lines.

In accordance with another embodiment of the present invention, in order to make substantially more equal the enabling time of the sense amplifiers closest to their clock driver and those farthest away, the enabling inputs to the sense amplifiers are connected through local pull down field effect transistors to local power supply tracks which have little resistance from one end to the other of the integrated circuit memory. The gates of these pull down transistors are connected to the sense amplifier clock conductive tracks since very little current is required by the gates of those transistors, and very little voltage drop thus occurs between the near and far ends of the integrated circuit. Accordingly enabling of the sense amplifiers is substantially speeded at locations remote from the near end sense amplifiers, and there is substantially reduced differential in enabling speed between the near and far end of the sense amplifiers.

In order to reduce the number of transistors required, groups of sense amplifiers may be coupled to the same pull down transistors.

#### BRIEF DESCRIPTION TO THE DRAWINGS

A better understanding of the invention will now be obtained by reference to the detailed description below, in conjunction with the following drawings, in which:

FIG. 1 is a schematic diagram of a portion of a bit line circuit and sense amplifier in accordance with the prior art,

FIG. 2 is a schematic diagram of a portion of a bit line circuit and sense amplifier in accordance with the present invention, and

FIG. 3 is a waveform diagram used to describe the function of the present invention.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS OF THE INVENTION

Turning first to FIG. 1, a portion of a prior art bit line and sense amplifier circuit is shown. Bit storage capacitors 1A and 1B are coupled through field effect transistors (FETs) 2A and 2B to complementary bit lines BL and /BL of a folded bit line. The gates of transistors 2A and 2B are connected to word lines  $WL_n$  and  $WL_{n+1}$  in a well known manner.

A sense amplifier 3 is connected to the bit lines also in a well known manner. The bit lines are coupled to databuses DB and /DB via FETs 4A and 4B.

The sense amplifier 3 is formed of a pair of N-channel transistors having their series connected source-drain circuits connected across the bit lines of the folded bit line, their junction being connected to an active low logic level source  $\phi_s$ , and a pair of P-channel FETs having their series connected source-drain circuits connected across bit lines BL and /BL, their junction being connected to an active high level source  $\phi_R$ . The gates of the N and P-channel transistors connected to a first bit line are connected together and to the other bit line, and the gates of the transistors connected to the other transistor are connected together and to the first bit line.

In operation a transistor e.g. 2B is enabled from a word line, and the charge, representing a bit, stored on a capacitor e.g. 1B is dumped to the associated bit line /BL. This creates a voltage differential between bit lines BL and /BL which appears across sense nodes SA and SB. When the logic levels  $\phi_s$  and  $\phi_R$  are applied to the sense amplifier 3, the voltage differential causes the circuit to latch, applying the full logic levels of  $\phi_s$  and  $\phi_R$  to the bit lines. This restores the charge on the capacitor 1B to full logic level. Upon enabling of the transistors 4A and 4B by the signal  $\phi_{yi}$ , the resulting full logic level on the bit lines is applied to the databuses DB and /DB.

Associated with each bit line is an inherent capacitance 5A and 5B, which results from the length and breadth of the bit line track on the semiconductor and the substrate. Those capacitances 5A and 5B must be charged by the current from the power supply supplying the full logic levels  $\phi_s$  and  $\phi_R$ . This takes a considerable period of time and current requirement.

Therefore isolates 6A and 6B have been used to isolate the bit line from the sensing nodes SA and SB associated with the sense amplifier. The isolators are devices which completely isolate the bit lines from the sense nodes.

As noted earlier, while the aforementioned device was successful in isolating the bit lines from the sense nodes, thus

eliminating the requirement to charge the bit line capacitances 5A and 5B during the initial part of the sensing interval, the differential between sense nodes was sometimes uncertain and sometimes small, and was affected by noise, or even being below the noise level. Accordingly an incorrect bit value could be sensed.

In addition, since the isolator must be turned on and off, additional steps in the memory access sequence must be performed. Further, the isolator must be inhibited in order to restore the logic level to the memory capacitor and indeed, if an incorrect bit were read, the restored bit value would also be incorrect. Clearly both speed and reliability of the memory were sacrificed.

FIG. 2 illustrates an embodiment of the present invention. An imperfect isolation device 8A and 8B, driven from a source  $\phi_{In}$  is connected in series between each bit line and each sense node. In the embodiment shown in FIG. 2 the imperfect isolation devices are N-channel enhancement mode FETs 8A and 8B. However alternatively, or in addition, P-channel enhancement mode FETs are connected in series between each bit line and each sense node. The gates of the transistors 9A and 9B are connected together to a logic source  $\phi_{IP}$ .

With reference to FIGS. 2 and 3, operation of the device is as follows. At the beginning of an active cycle the voltage  $\phi_{IN}$  is brought from a boosted level, e.g.  $V_{pp}$  to a lower level that still allows cell charge to flow to the sense amplifier as noted, e.g.  $V_{dd}$ . Then, as described earlier, either transistor 2A or 2B is enabled, causing the charge on either bit storage capacitor 1A or 1B to be dumped on an associated bit line. Charge on the bit line leaks through the high resistance source-drain circuit transistor 8A or 8B (assuming transistors 9A and 9B are not present) to the sense nodes SA or SB, charging the small capacitance associated therewith.

Subsequently the sense amplifier 3 is enabled by applying high logic level  $\phi_s$  and low logic level  $\phi_R$ , as described earlier. The sense amplifier is caused to apply the full logic levels  $\phi_s$  and  $\phi_R$  to the sense nodes SA and SB, latching due to the differential thereacross. However due to the voltage drop between the sources and drains of transistors 8A and 8B, bit line capacitances 5A and 5B will only be charged up to a reduced voltage less than full logic level applied to the sense nodes. Since capacitances 5A and 5B are charged a reduced amount, the sensing interval is considerably reduced from the prior art; the sensing is faster because the sense node voltage differential develops faster for the same sense current budget. Data can be read out over the data bus by enabling column access transistors 4A and 4B, as soon as a sufficient potential exists across the sense nodes. Hence memory access time is improved by the isolation devices. While the restore charge on capacitors 1A and 1B is less than full logic level, they can be fully restored after column access.

After the peak current has occurred in the first stage of sensing the  $\phi_{IN}$  level is brought back up to the boosted level  $V_{pp}$  to allow full restore of the bit lines. This causes a second peak in sensing current. Compared to prior art sensing current peaks are lower and are distributed over time.

It was noted earlier that P-channel transistors 9A and 9B could be used in place of transistors 8A and 8B, or in series therewith as shown in the figure. If P-channel transistors are used, their gates should initially be at a  $\phi_{IP}$  level  $V_{bb}$ , and are raised to a level  $V_{ss}$  during the initial part of sensing when a high impedance isolation device is required.

It had been noted earlier that resistive voltage drops in the conductive tracks in the semiconductor memory from the

sense amplifier driver circuits to the far end of the array cause quick sensing at the near end of the array (close to the sense amplifier driver circuits) and slow (retarded) sensing at the far end of the array. Thus memory access must be delayed to accommodate the sensing of the slowest column.

According to another embodiment of the invention, rather than driving the logic  $\phi_s$  and  $\phi_R$  input leads of the sense amplifiers directly from the sense amplifier drivers, local pull down FETs or pull up FETs are used. Indeed, these FETs may be shared among several sense amplifiers in adjacent columns.

As shown in FIG. 2, rather than the sense amplifier being connected to  $\phi_s$  and  $\phi_R$  logic sources, they are connected through the source-drain circuits of FETs 12A and 12B to voltage sources  $V_{dd}$  and ground ( $V_{ss}$ ) respectively. The gates of transistors 12A and 12B are driven from the  $\phi_R$  and  $\phi_s$  logic sources respectively.

The ground and  $V_{dd}$  power tracks on an integrated circuit memory normally are of low resistance. Therefore the provision of those sources to the sense amplifiers is through short and low resistance conductors.

However since the  $\phi_R$  and  $\phi_s$  logic signals driving the gates of transistors 12A and 12B require only a small amount of current, there will be a considerably reduced voltage drop in their conductive tracks from one end of the memory to the other. Thus the difference in operation time of the sense amplifiers between the near and far ends is considerably reduced, and can be considerably increased in speed over prior art DRAMs.

The result of the last-described embodiment is increased reliability, since leaky bit lines which have been deprogrammed will not affect sense line current in other bit lines, if local sense clock drivers are shared only among bit lines with the same redundancy address. No additional power supplies are required other than those normally on the chip.

The result of the above embodiments is increase in sensing speed and more uniformity of sensing speed across a large DRAM.

It should be noted that either or the embodiments can be used separately or in conjunction. For example, N-channel bit line isolation devices could be used in conjunction with local sensing amplifier enabling pull downs as described, to control peak  $V_{dd}$  current and  $V_{ss}$  current respectively.

A person understanding this invention may now conceive of alternative structures and embodiments or variations of the above. All of those which fall within the scope of the claims appended hereto are considered to be part of the present invention.

We claim:

1. A dynamic random access memory (DRAM) comprising:

- (a) a plurality of bit storage capacitors,
- (b) a folded bit line comprised of a complementary bit line pair for receiving charge stored on one of said capacitors, having bit line capacitance,
- (c) a sense amplifier having a pair of sense nodes for sensing a voltage differential across said sense nodes,
- (d) high resistance controllable current leakage imperfect isolating means connecting said bit line to said sense nodes for receiving an enabling voltage *from a first voltage supply* for causing current leakage therethrough between said sense nodes and the bit line while maintaining high resistance,
- (e) means for applying said enabling voltage for causing effective current to leak through the imperfect isolating means,



(f) means for enabling said sense amplifier and establishing full predetermined logic levels across said sense nodes,

(g) means *applying a voltage from a second voltage supply to the imperfect isolating means* for disabling said imperfect isolating means and thereby removing isolation between said sense nodes and the bit line,

whereby current passing through the sense amplifier to said sense nodes is enabled to charge said bit line capacitance through said imperfect isolating means to a predetermined logic voltage level.

2. A DRAM as defined in claim 1 in which said imperfect isolating means is a pair of N-channel enhancement mode field effect transistors each having a source-drain circuit in series with a bit line of the bit line pair.

3. A DRAM as defined in claim 2 including a voltage source applied to gates of each field effect transistor having an initial voltage level which is higher than said logic voltage [level] levels and a following enabling voltage level which is equal to *one of* said logic [level] levels, and at a later time a disabling voltage equal to the initial voltage level.

4. A DRAM as defined in claim 1 in which said isolating means is a pair of P-channel enhancement mode field effect transistors each having a source-drain circuit in series with a bit line of the bit line pair.

5. A DRAM as defined in claim 4 including a voltage source applied to gates of each field effect transistor having an initial voltage level which is lower than said logic voltage [level] levels and a following enabling voltage level which is equal to *one of* said logic [level] levels, and at a later time a disabling voltage equal to said initial voltage level.

6. A dynamic random access memory (DRAM) as defined in claim 1, further comprising:

(a) the sense amplifier having respective sense enable and restore enable inputs for providing full high and full low logic levels respectively to said sense nodes,

(b) power supply means for providing full high and full low logic level voltages,

(c) a pair of field effect transistors, one being a P-channel enhancement mode type having its source-drain circuit connected between said restore enable input and the high logic level power supply voltage and the other being an N-channel enhancement mode type having its source-drain circuit connected between the sense enable input and the low logic level power supply voltage, and

(d) means for providing restore and sense signals to gates of said one and other field effect transistors respectively,

whereby restore and sense current is supplied to said sense amplifier from said power supply means rather than from said means for providing restore and sense signals.

7. A dynamic random access memory (DRAM) as defined in claim 1 comprising a plurality of bit lines and associated sense amplifiers, the bit lines being arrayed across an integrated circuit chip and the sense amplifiers being disposed in a row, a pair of low-resistance power supply conductors extending in parallel with said row for carrying logic high level and logic low level voltages, sense amplifier enabling signal conductors extending across said chip accessible to said sense amplifiers, means for coupling sense inputs of said sense amplifiers to said power supply conductors, and means coupling said sense amplifier enabling signal conductors to enabling inputs of said means for coupling sense inputs, for enabling passage of current

resulting from said logic high level and low level voltages to said sense amplifiers.

8. A DRAM as defined in claim 7 in which said means for coupling sense inputs of said sense amplifiers is comprised of field effect transistors having their gates connected to said sense amplifier enabling signal conductors, said gates forming said enabling inputs.

9. A DRAM as defined in claim 8 in which the sense inputs of groups of said sense amplifiers are connected together to the same field effect transistor drain terminal.

10. A DRAM as defined in claim 1, further comprising:

(a) the sense amplifier having sense enable and restore enable inputs for providing full high and full low logic levels respectively to said sense nodes,

(b) power supply means for providing full high and full low logic level voltages,

(c) a pair of field effect transistors, one having its source-drain circuit connected between said restore enable input and the high logic level power supply voltage and the other having its source-drain circuit connected between the sense enable input and the low logic level power supply voltage, and

(d) means for providing restore and sense signals to gates of said one and other field effect transistors respectively,

whereby restore and sense current is supplied to said sense amplifier from said power supply means rather than from said means for providing restore and sense signals.

11. A DRAM as defined in claim 1, further comprising a plurality of bit lines and associated sense amplifiers, the bit lines being arrayed across an integrated circuit chip and the sense amplifiers being disposed in a row, a pair of low-resistance power supply conductors extending in parallel with said row for carrying logic high level and logic low level voltages, sense amplifier enabling signal conductors extending across said chip accessible to said sense amplifiers, means for coupling sense inputs of said sense amplifiers to said power supply conductors, and means coupling said sense amplifier enabling signal conductors to enabling inputs of said means for coupling sense inputs, for enabling passage of current resulting from said logic high level and low level voltages to said sense amplifiers.

12. A DRAM as defined in claim 3, further comprising a plurality of bit lines and associated sense amplifiers, the bit lines being arrayed across an integrated circuit chip and the sense amplifiers being disposed in a row, a pair of low-resistance power supply conductors extending in parallel with said row for carrying logic high level and logic low level voltages, sense amplifier enabling signal conductors extending across said chip accessible to said sense amplifiers, means for coupling sense inputs of said sense amplifiers to said power supply conductors, and means coupling said sense amplifier enabling signal conductors to enabling inputs of said means for coupling sense inputs, for enabling passage of current resulting from said logic high level and low level voltages to said sense amplifiers.

13. A DRAM as defined in claim 5, further comprising a plurality of bit lines and associated sense amplifiers, the bit lines being arrayed across an integrated circuit chip and the sense amplifiers being disposed in a row, a pair of low-resistance power supply conductors extending in parallel with said row for carrying logic high level and logic low level voltages, sense amplifiers enabling signal conductors extending across said chip accessible to said sense amplifiers, means for coupling sense inputs of said sense

amplifiers to said power supply conductors, and means coupling said sense amplifier enabling signal conductors to enabling inputs of said means for coupling sense inputs, for enabling passage of current resulting from said logic high level and low level voltages to said sense amplifiers.

14. A DRAM as defined in claim 11 in which said means for coupling sense inputs of said sense amplifiers is comprised of field effect transistors having their gates connected to said sense amplifier enabling signal conductors, said gates forming said enabling inputs.

15. A DRAM as defined in claim 14 in which the sense inputs of groups of said sense amplifiers are connected together to the same field effect transistor drain terminal.

16. A method of sensing in a folded bit line type of dynamic random access memory (DRAM) having a bit storage capacitor for coupling to the bit line and a sensing amplifier having sense nodes, comprising:

- (a) imperfectly isolating the sense nodes of the sensing amplifier from the bit line using an imperfect isolating means *enabled from a first voltage supply*,
- (b) coupling the capacitor to the bit line, thereby dumping its charge thereon,
- (c) leaking said charge through the imperfect isolating means to one of the sense nodes, thereby causing a voltage differential across said sense nodes,
- (d) sensing said differential by said sense amplifier and applying full high and low logic voltage levels respectively to said sense nodes,
- (e) inhibiting isolation of said sense nodes from said bit line, *by disabling the imperfect isolating means from a second voltage supply*, whereby full logic levels are applied to complementary bit lines of said folded bit line.

17. A method as defined in claim 16, in which the isolating means is comprised of the source-drain circuits of a pair of enhancement mode field effect transistors respectively connected between the sense nodes and the complementary bit lines of the folded bit line, [and] said *inhibiting* isolating step is comprised of applying an inhibiting voltage to gates of said field effect transistors, and the [inhibiting] isolating step is comprised of changing the inhibiting voltage to the same voltage as one of said full logic voltage levels, whereby upon application of said full logic levels to said sense nodes during the sensing step, a field effect transistor having a gate voltage closest to a logic level applied to a sense node to which it is connected is caused to inhibit current flow into the bit line.

18. A method as defined in claim 16 wherein the voltage differential across said sense nodes is sensed without complete isolation during a memory cycle.

19. A DRAM as defined in claim 1 wherein the voltage differential across said sense nodes is sensed without complete isolation during a memory cycle.

20. A semiconductor memory device comprising:
- a plurality of bit storage capacitors;
  - a bit line comprised of a complementary bit line pair for receiving charge stored on one of said capacitors;
  - a sense amplifier having a pair of sense nodes for sensing a voltage differential across said sense nodes and establishing full logic levels across said sense nodes; and
  - an isolator coupled between said complementary bit line pair and said sense nodes for operatively coupling a selected complementary bit line pair to said sense nodes in response to a controlling signal, the controlling signal being provided from a voltage supply having

a voltage level beyond the full logic levels to restore full logic levels to the selected complementary bit line pair during a restoring portion of an active memory cycle.

21. A semiconductor memory device as claimed in claim 20 wherein the isolator comprises n-channel transistors and the voltage supply supplies a voltage  $V_{pp}$  which is greater than the full logic levels.

22. A semiconductor memory as claimed in claim 21 wherein said controlling signal is a  $V_{pp}$  voltage during a pre-initial portion of said active memory cycle, a  $V_{dd}$  logic level voltage during an initial portion of said active memory cycle, and said  $V_{pp}$  voltage level again during said restoring portion of said active memory cycle.

23. A semiconductor memory device as claimed in claim 20 wherein the isolator comprises p-channel transistors and the voltage supply supplies a voltage  $V_{bb}$  below the full logic levels.

24. A semiconductor memory device as claimed in claim 23 wherein said controlling signal is said  $V_{bb}$  voltage during a pre-initial portion of said active memory cycle, a  $V_{ss}$  logic level voltage during an initial portion of said active memory cycle, and said  $V_{bb}$  voltage level again during said restoring portion of said active memory cycle.

25. A semiconductor memory device as claimed in claim 20 wherein said controlling signal attains a voltage for imperfect isolation of a selected complementary bit line pair during an initial portion of an active memory cycle.

26. A semiconductor memory device comprising:
- a plurality of bit storage capacitors;
  - a bit line comprised of a complementary bit line pair for receiving charge stored on one of said capacitors;
  - a sense amplifier having a pair of sense nodes for sensing a voltage differential across said sense nodes and establishing full logic levels across said sense nodes; and
  - n-channel transistors coupled between said complementary bit line pair and said sense nodes for operatively coupling a selected complementary bit line pair to said sense nodes, a  $V_{pp}$  voltage greater than the full logic levels being applied to gates of said n-channel transistors during a restoring portion of an active memory cycle.

27. A semiconductor memory device comprising:
- plurality of bit storage capacitors;
  - a bit line comprised of a complementary bit line pair for receiving charge stored on one of said capacitors;
  - a sense amplifier having a pair of sense nodes for sensing a voltage differential across said sense nodes and establishing full logic levels across said sense nodes; and
  - p-channel transistors coupled between said complementary bit line pair and said sense nodes for operatively coupling a selected complementary bit line pair to said sense nodes, a  $V_{bb}$  voltage less than the full logic levels being applied to gates of said p-channel transistors during a restoring portion of an active memory cycle.

28. A method of sensing in a dynamic random access memory (DRAM) having a bit line, a bit storage capacitor for coupling to the bit line, a sense amplifier having sense nodes and isolation transistors between said bit lines and sense amplifier, comprising:

- coupling the capacitor to the bit line, thereby dumping its charge thereon;
- sensing a voltage differential across said sense nodes by said sense amplifier and applying full high and low logic voltage levels respectively to said sense nodes; and

restoring to the bit storage capacitor the full high and low logic voltage levels by applying to said isolation transistors a controlling signal from a voltage supply having a voltage level beyond the full high and low logic voltage levels.

29. A method as claimed in claim 28 wherein the isolating transistor is an n-channel transistor and the voltage supply supplies a voltage  $V_{pp}$  which is greater than the logic level.

30. A method as claimed in claim 29 wherein said controlling signal is a  $V_{pp}$  voltage during a pre-initial portion of said active memory cycle, a  $V_{aa}$  logic level voltage during an initial portion of said active memory cycle, and said  $V_{pp}$  voltage level again during said restoring portion of said active memory cycle.

31. A method as claimed in claim 28 wherein the isolation transistors comprise a p-channel transistor and the voltage supply supplies a voltage  $V_{bb}$  below the full logic levels.

32. A method as claimed in claim 31 wherein said controlling signal is said  $V_{bb}$  voltage during a pre-initial portion of said active memory cycle, a  $V_{ss}$  logic level voltage during an initial portion of said active memory cycle, and said  $V_{bb}$  voltage level again during said restoring portion of said active memory cycle.

33. A method as claimed in claim 28 wherein said controlling signal attains a voltage for imperfect isolation of a selected complementary bit line pair during an initial portion of an active memory cycle.

34. A method of sensing in a dynamic random access memory (DRAM) having a bit line, a bit storage capacitor for coupling to the bit line, a sense amplifier having sense nodes and n-channel isolation transistors between said bit lines and sense amplifier, comprising:

coupling the capacitor to the bit line, thereby dumping its charge thereon;

sensing a voltage differential across said sense nodes by said sense amplifier and applying full high and low logic voltage levels respectively to said sense nodes; and

restoring to the bit storage capacitor the full high and low logic by applying to said n-channel isolation transistors a  $V_{pp}$  voltage greater than the full high logic level.

35. A method of sensing in a dynamic random access memory (DRAM) having a bit line, a bit storage capacitor for coupling to the bit line, a sense amplifier having sense nodes and p-channel isolation transistors between said bit lines and sense amplifier, comprising:

coupling the capacitor to the bit line, thereby dumping its charge thereon;

sensing a voltage differential across said sense nodes by said sense amplifier and applying full high and low logic voltage levels respectively to said sense nodes; and

restoring to the bit storage capacitor the full high and low logic voltage levels by applying to said p-channel isolation transistors a  $V_{bb}$  voltage less than the full low logic voltage level.

36. A semiconductor memory device comprising:

a plurality of bit storage capacitors;

a bit line comprised of a complementary bit line pair for receiving charge stored on one of said capacitors;

a sense amplifier having a pair of sense nodes for sensing a voltage differential across said sense nodes and establishing full logic levels across said sense nodes; and

isolation means coupled between said complementary bit line pair and said sense nodes for operatively coupling a selected complementary bit line pair to said sense nodes in response to a controlling signal, the controlling signal being provided from a voltage supplying having a voltage level beyond the full logic levels to restore full logic levels to the selected complementary bit line pair during a restoring portion of an active memory cycle.

\* \* \* \* \*

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : RE 37,641 E Page 1 of 1  
DATED : April 9, 2002  
INVENTOR(S) : Richard C. Foss, Peter B. Gillingham, Robert Harland, Masami Mitsuhashi and  
Atsushi Wada

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1,

Delete lines 9 & 10 and replace with the following paragraph:

-- More than one reissue application has been filed for the reissue of Patent No. 5,414,662. The reissue applications are application numbers 08/853,507 (the present reissue patent, which is a continuation application of Ser. No. 07/680,747, filed Apr. 5, 1991, now abandoned) and 10/032,431, which is a continuation of the present reissue patent. --

Column 12,

Line 31, delete "supplying" and insert -- supply --.

Signed and Sealed this

Twenty-fourth Day of September, 2002

*Attest:*



*Attesting Officer*

JAMES E. ROGAN  
*Director of the United States Patent and Trademark Office*

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : RE 37,641 E  
DATED : April 9, 2002  
INVENTOR(S) : Richard C. Foss et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page,

Item [30], add:

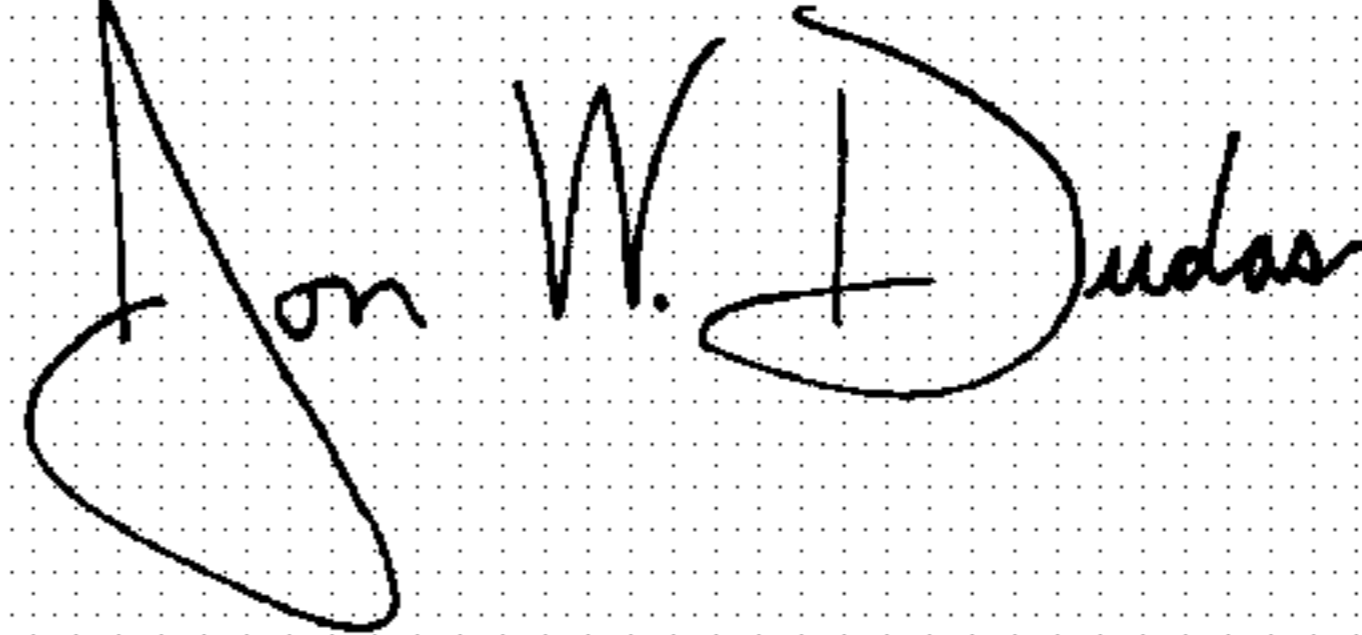
-- **Foreign Application Priority Data**

April 6, 1990 [GB] United Kingdom 9007789

April 5, 1991 [GB] United Kingdom 9107164 --

Signed and Sealed this

Twenty-fifth Day of May, 2004

A handwritten signature in black ink on a dotted background. The signature reads "Jon W. Dudas" in a cursive style.

JON W. DUDAS

*Acting Director of the United States Patent and Trademark Office*