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Doan et al.

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(54) **PLANARIZATION OF A GATE ELECTRODE FOR IMPROVED GATE PATTERNING OVER NON-PLANAR ACTIVE AREA ISOLATION**

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(51) **Int. Cl.**[7] **H01L 21/306**; B44C 1/22; C23F 1/00; C03C 15/00

(52) **U.S. Cl.** **438/585**; 438/592; 438/636; 438/645; 438/699

(58) **Field of Search** ..... 438/690, 691, 438/692, 693, 697, 699, 745, 747, 636, 645, 626, 629; 216/38, 52, 88, 89, 90, 91; 156/345 LP

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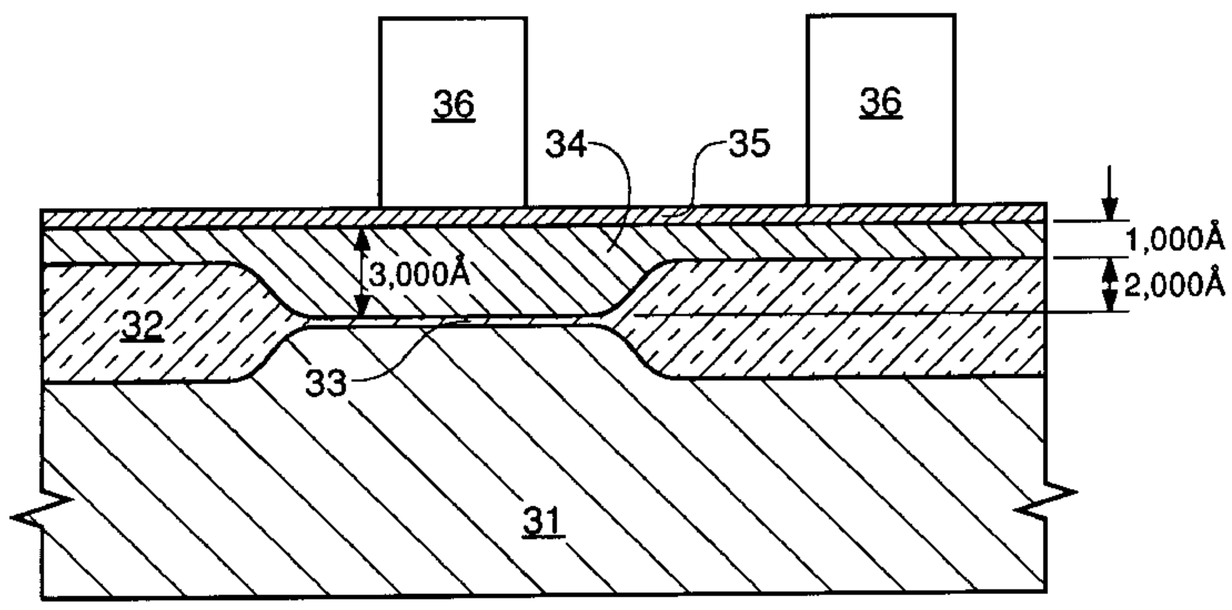
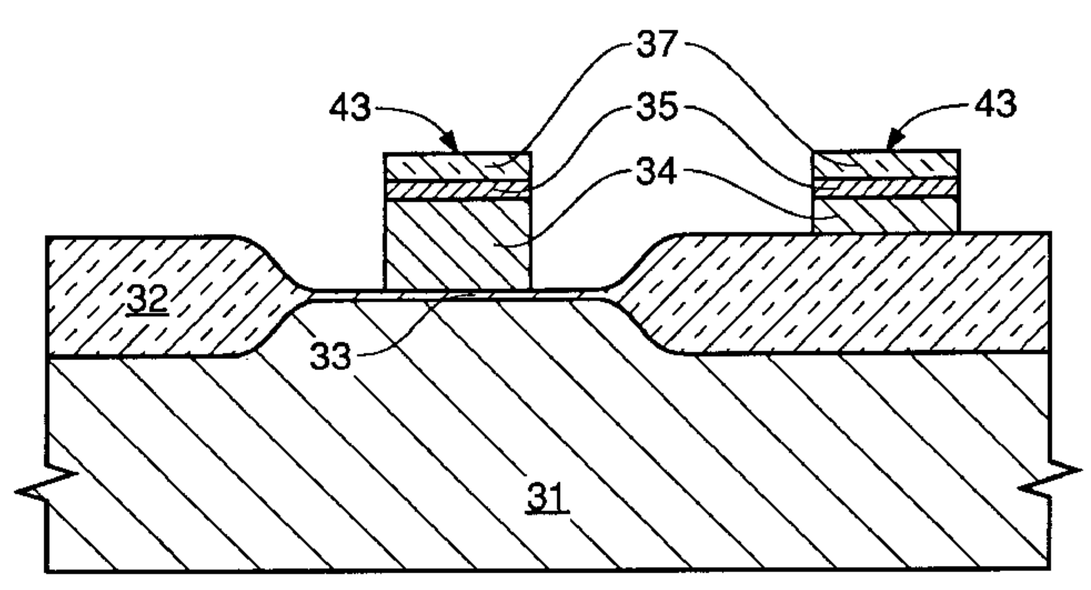
(57) **ABSTRACT**

The present invention is a process for providing a planarized transistor gate on a non-planar starting substrate, by depositing a layer of planarized conductive polysilicon material overlying neighboring field oxide isolation regions such that the height of the conductive polysilicon material extends above the [topology] *topography* of the field oxide isolation regions; depositing a layer of conductive silicide material superjacent and coextensive the conductive polysilicon material; and then patterning the planarized conductive polysilicon material and the conductive silicide material thereby forming the planarized transistor gate.

61 Claims, 5 Drawing Sheets





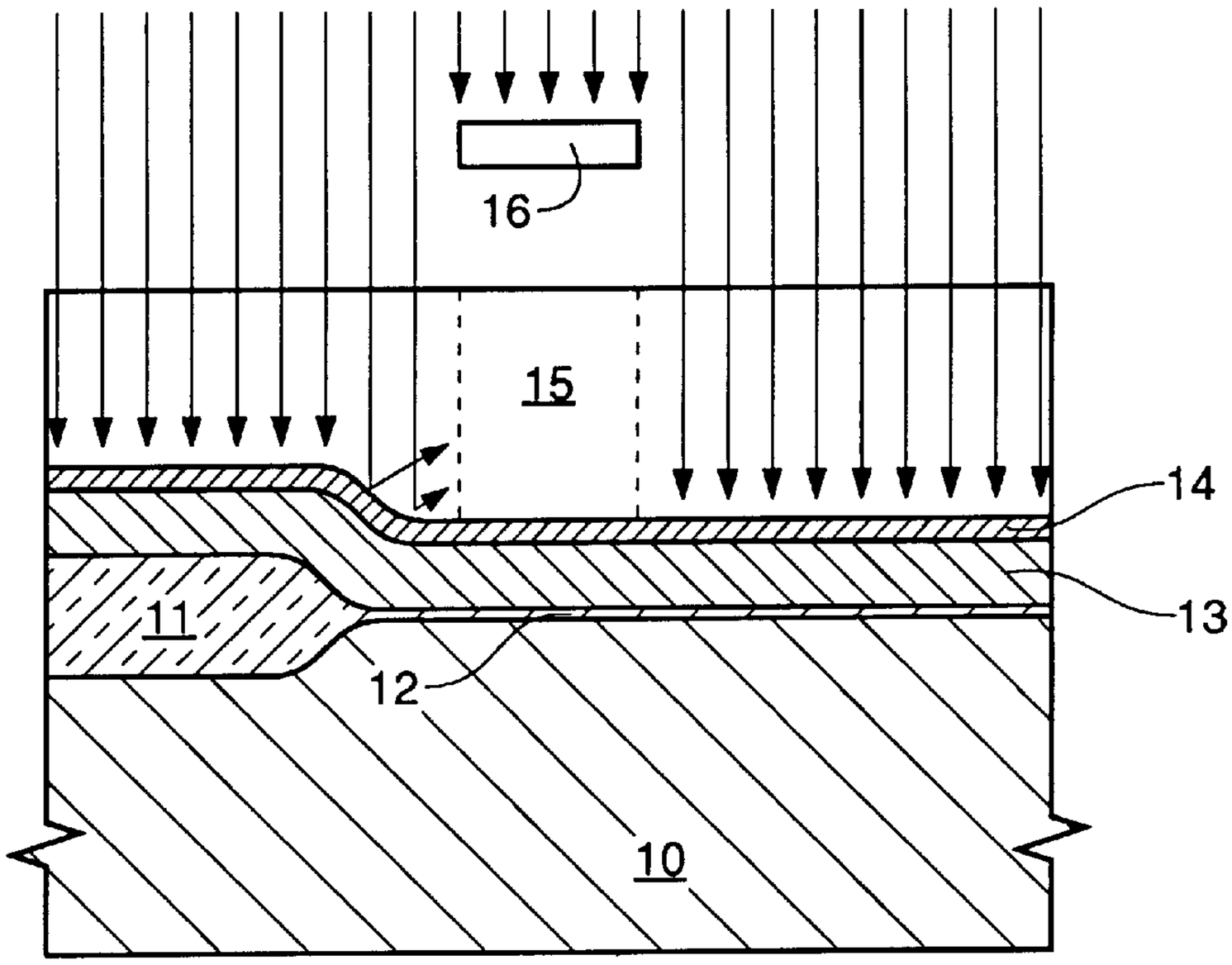


FIG. 1
(RELATED ART)

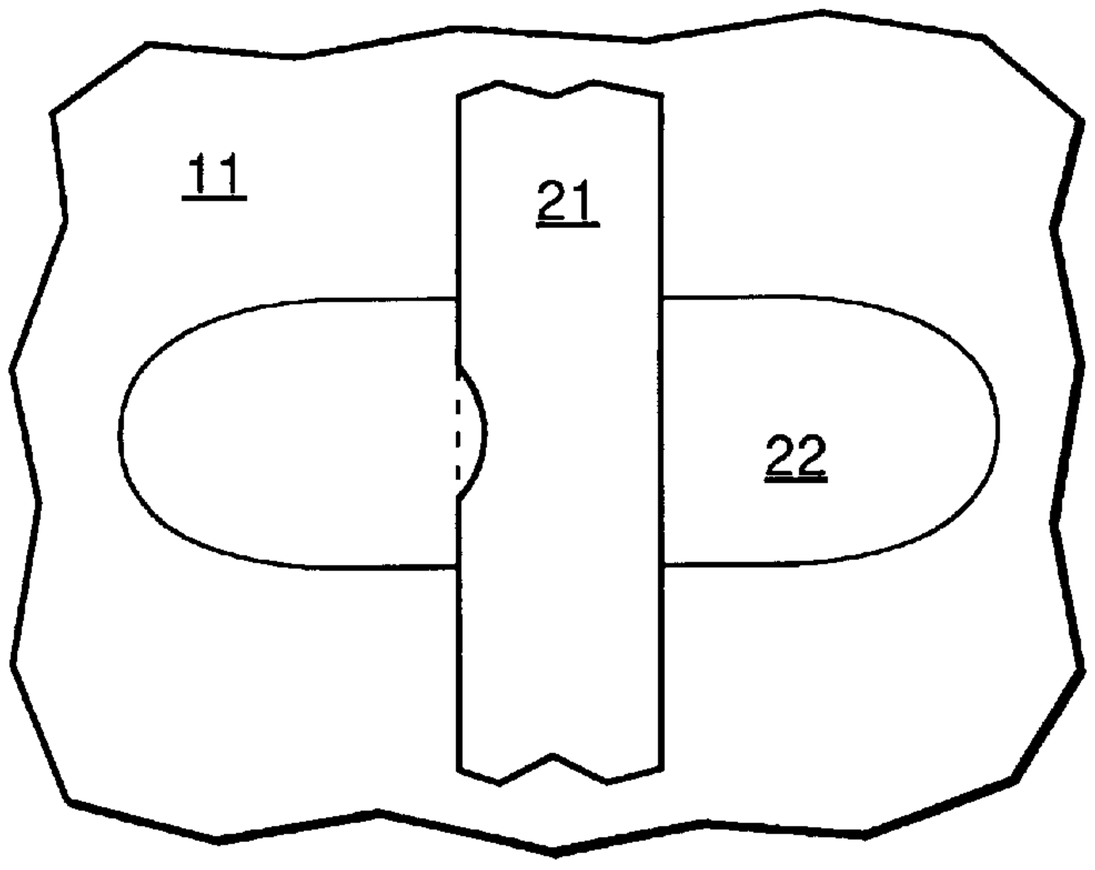


FIG. 2
(RELATED ART)

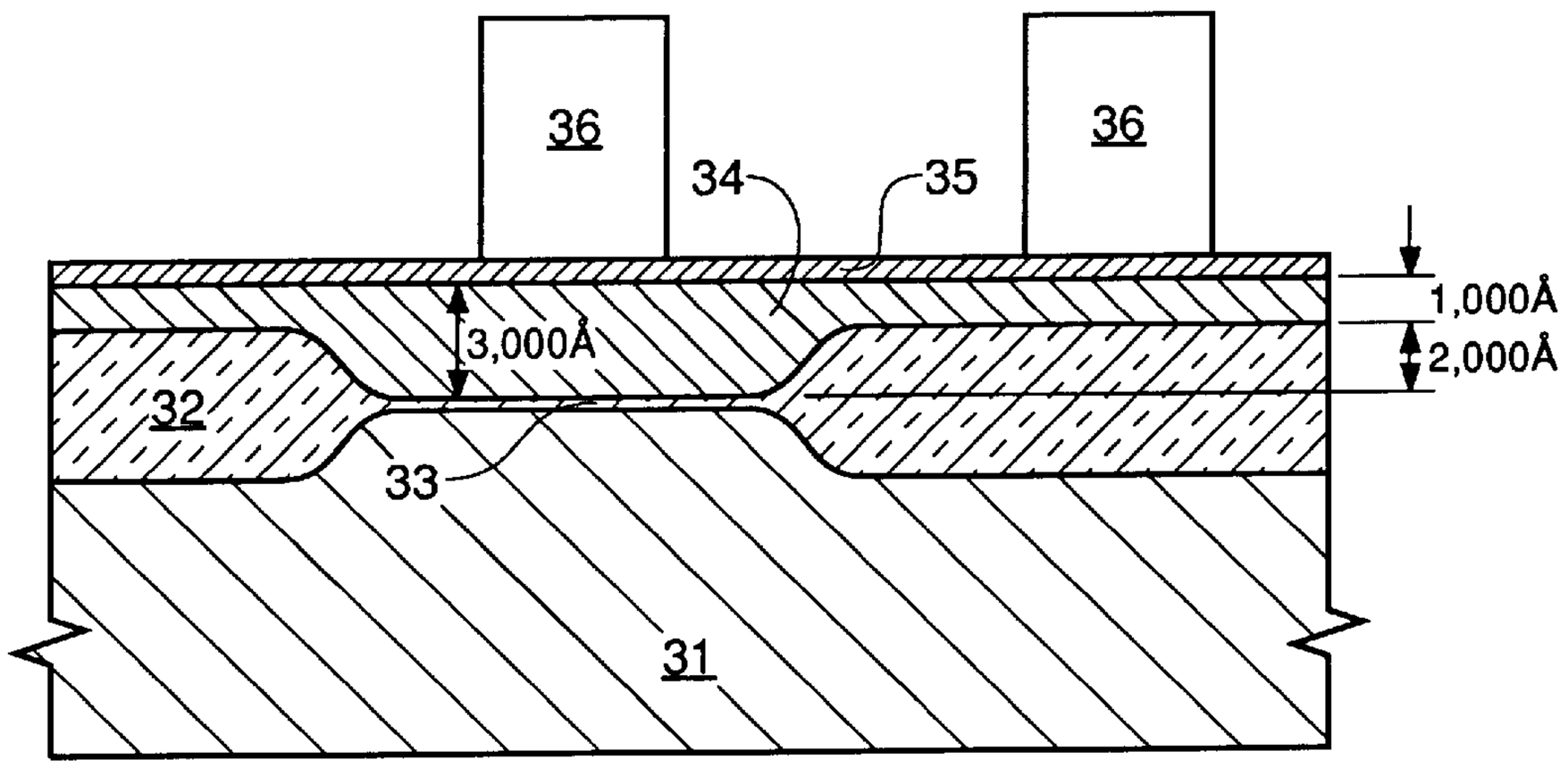


FIG. 3

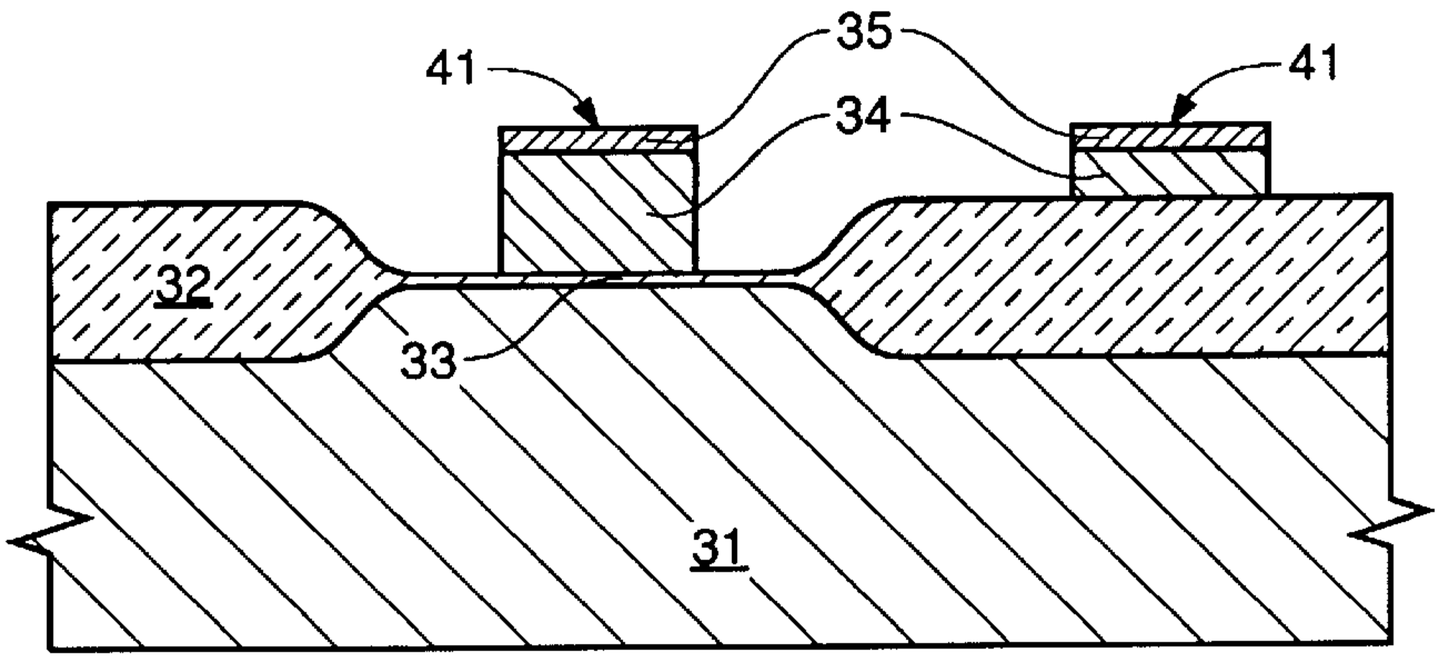


FIG. 4A

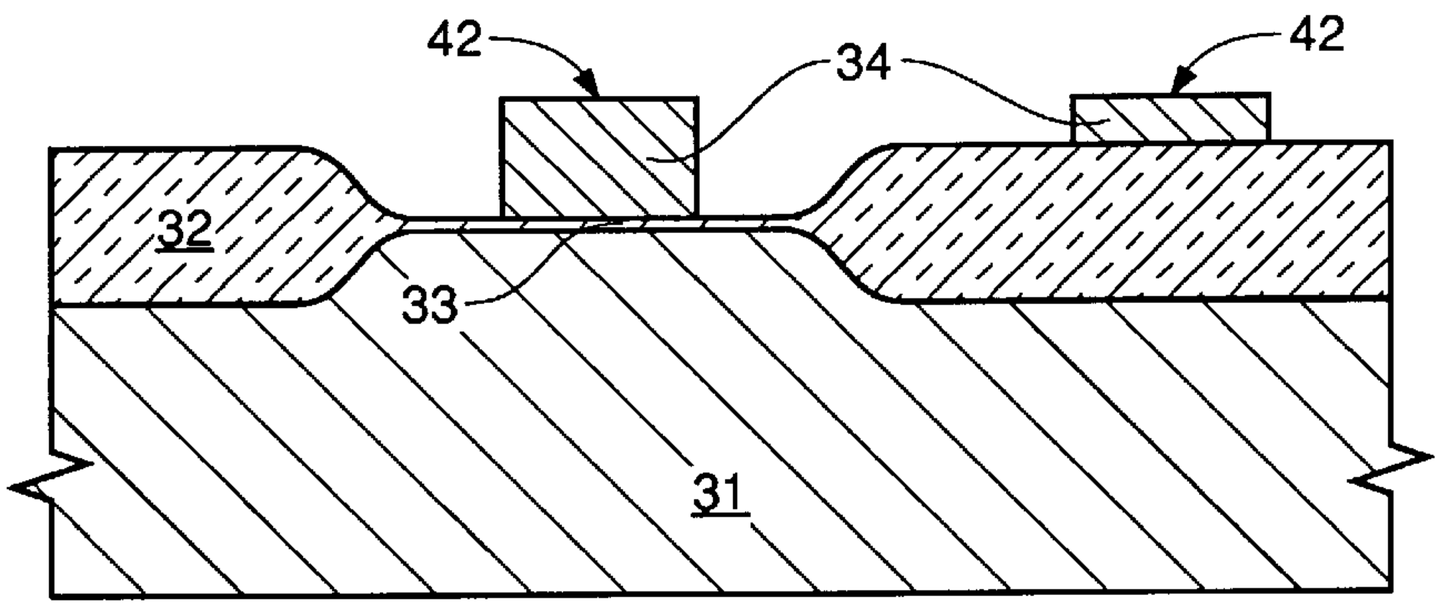


FIG. 4B

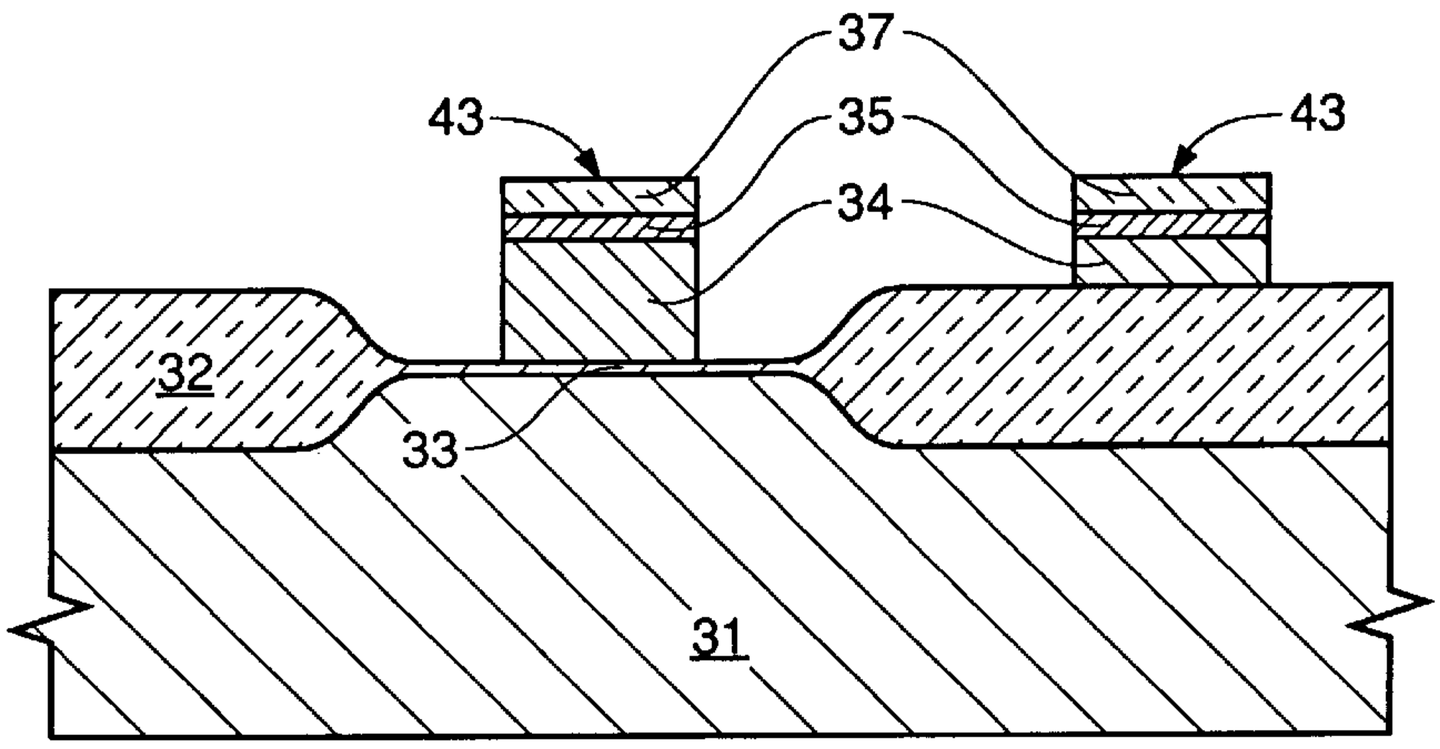


FIG. 4C

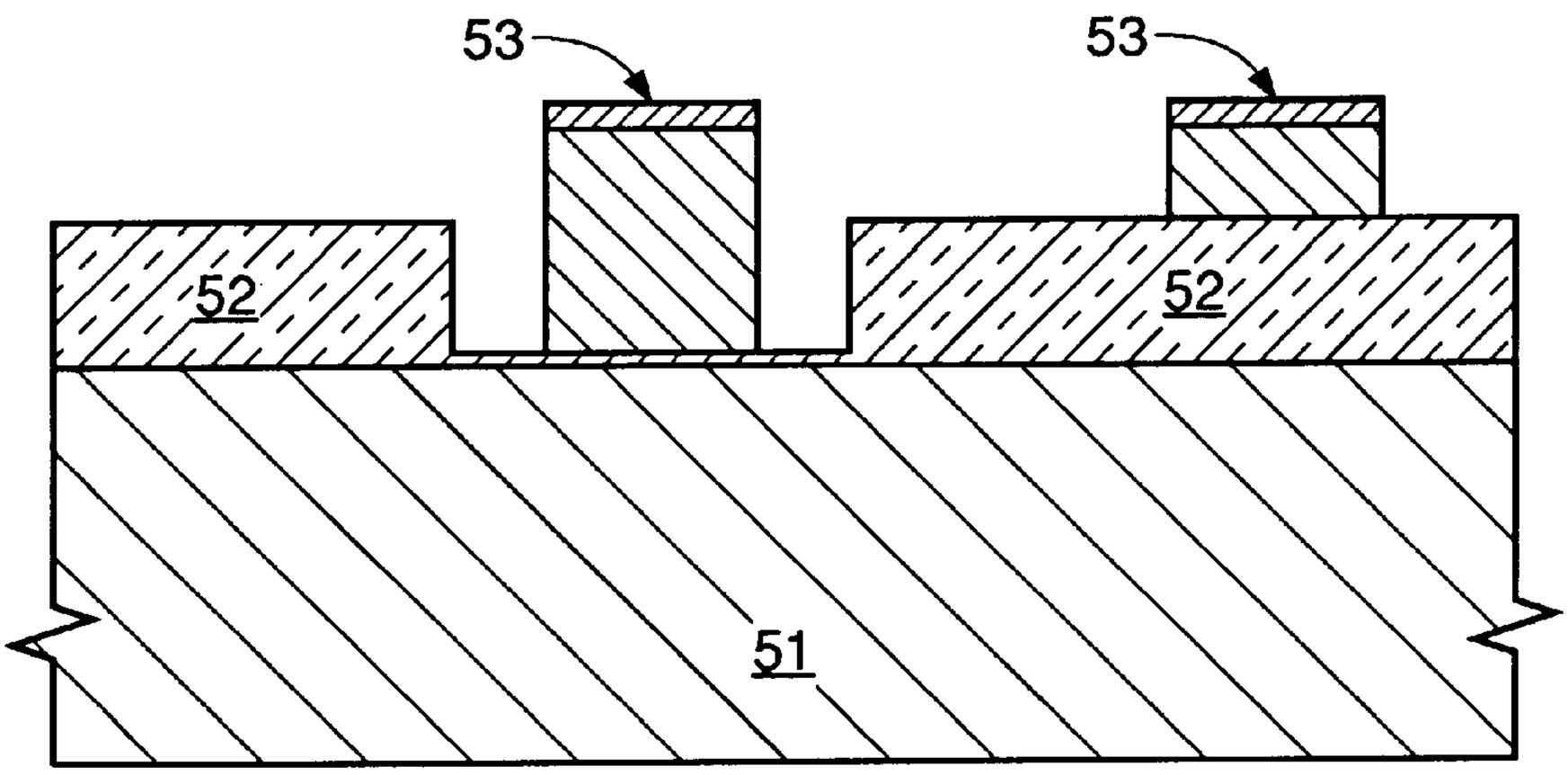


FIG. 5

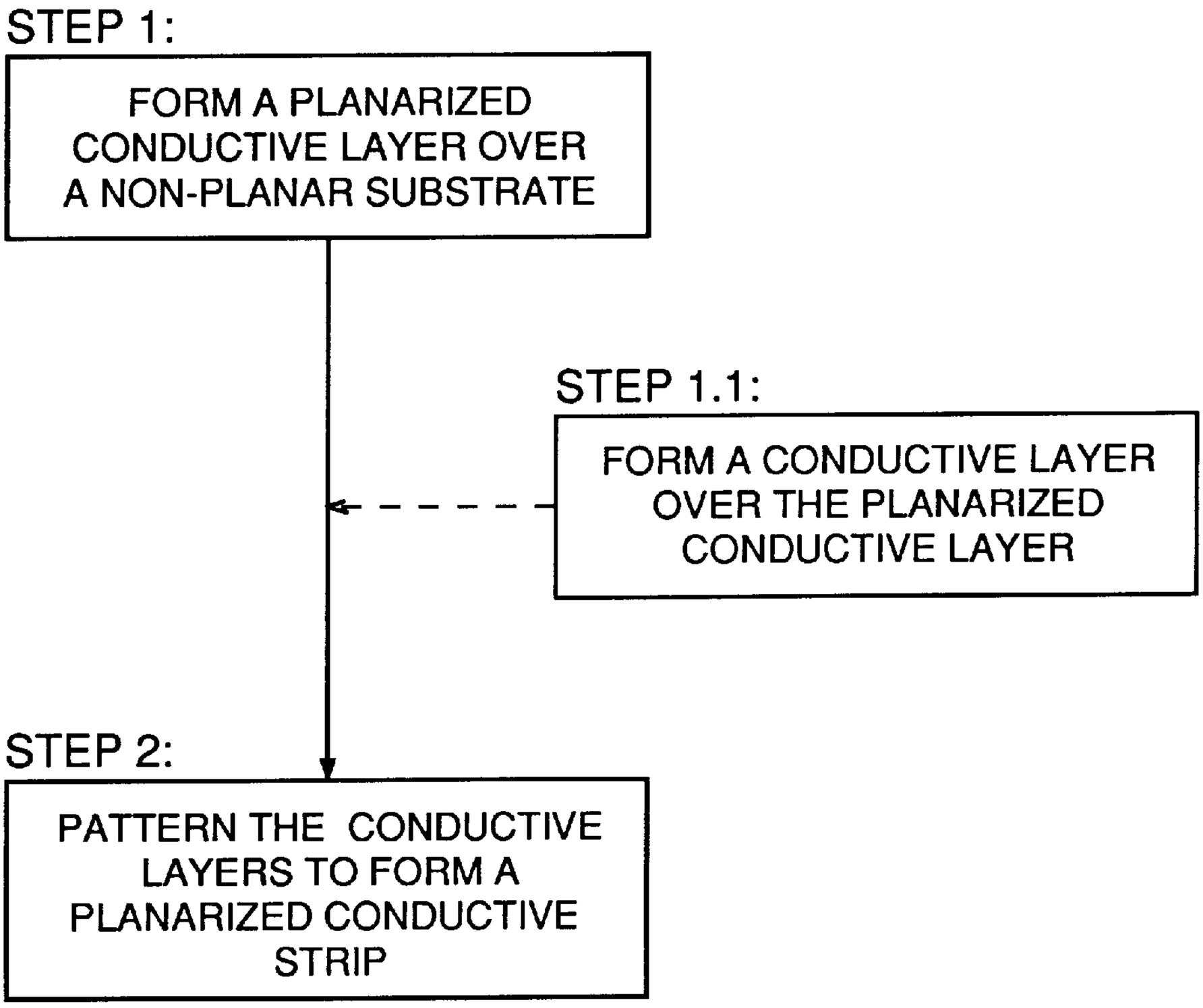

STEP 1:
FORM A PLANARIZED CONDUCTIVE LAYER OVER A NON-PLANAR SUBSTRATE
STEP 1.1:
FORM A CONDUCTIVE LAYER OVER THE PLANARIZED CONDUCTIVE LAYER
STEP 2:
PATTERN THE CONDUCTIVE LAYERS TO FORM A PLANARIZED CONDUCTIVE STRIP

FIG. 6

PLANARIZATION OF A GATE ELECTRODE FOR IMPROVED GATE PATTERNING OVER NON-PLANAR ACTIVE AREA ISOLATION

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

FIELD OF THE INVENTION

This invention relates to *a* semiconductor fabrication process and more particularly to a process for gate patterning over an active area isolation.

BACKGROUND OF THE INVENTION

During semiconductor fabrication, a conventional process starts with a wafer substrate **10**, as depicted in FIG. **1**, that has patterned thin oxide layers **12** separating isolation regions of thick (or field) oxide **11**. In the process depicted in FIG. **1**, during exposure and patterning of photoresist **15** via reticle **16**, light can reflect off of the uneven **[**topology**]** *topography* of silicide **14** and cause what is know as reflective notching. The reflective notching in the photoresist pattern is then transferred into the underlying conductive layer following a subsequent etch.

As seen from the top view of FIG. **2**, a conductive strip **21** shows the results of reflective notching during the exposure of the photoresist that has caused some of the conductive strip to be removed during the etching of the strip. In this case, the conductive strip **21** has been patterned over active area **22** to serve as a control gate to an MOS device. It becomes obvious that this reflective notch is undesirable as it would reduce the reliability of the MOS device.

The present invention addresses the reflective notching problem by forming a planarized conductor on a wafer's surface that has **[**a**]** *an* uneven **[**topology**]** *topography* that results from the formation of **[**spaced apart**]** *spaced-apart*, patterned oxide isolation regions including oxide regions formed by LOCOS trench isolation and other advanced isolation technologies.

SUMMARY OF THE INVENTION

The present invention is realized in a process for providing a planarized conductor on a non-planar starting substrate**[**,**]** by:

a) forming a first layer of planarized conductive material overlying neighboring isolation regions such that the height of the conductive material extends above the **[**topology**]** *topography* of the isolation regions; and

b) patterning the first and second conductive material thereby forming the planarized conductor.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a composite cross-sectional view of an in-process wafer portion depicting a conventional method used to pattern a gate electrode between field oxide isolation regions;

FIG. **2** is an overhead view of the results of the process steps of FIG. **1** wherein reflective notching is demonstrated;

FIG. **3** is a composite cross-sectional view of an in-process wafer portion depicting a silicide layer overlying a planarized polysilicon which in turn overlies a starting substrate;

FIG. **4A** is a composite cross-sectional view of the in-process wafer portion of FIG. **3** depicting the results of an etch;

FIG. **4**B is a composite cross-sectional view of an in-process wafer portion depicting a planarized conductive control **[**gates**]** *gate* made of a single planarized polysilicon layer overlying a starting substrate;

FIG. **4**C is a composite **[**cross sectional**]** *cross-sectional* view of an in-process wafer portion depicting a planarized conductive control gate made of planarized polysilicon, silicide and partially reflective insulator layers overlaying a **[**staring**]** *starting* substrate;

FIG. **5** is a composite cross-sectional view of the in-process wafer portion utilizing the process steps of the present invention in a second embodiment; and

FIG. **6** is a flow diagram depicting the process steps of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In a preferred embodiment and referring now to FIG. **3**, a silicon substrate **31**, has patterned thick oxide isolation regions **32** (formed by a LOCOS isolation), spaced apart by a thin oxide film **33** (i.e. grown gate oxide). Next, a thick layer of conductively doped polysilicon **34** (*e.g., a conductive material*) is formed overlying thick oxide regions **32** and thin oxide film **33**. In this example, thick oxide **[**region extends**]** *regions 32 extend* approximately **[**2000Å**]** *2000 ANG* above the substrate's surface. Therefore, polysilicon **34** must be thick enough whereby its thickness extends substantially above the **[**2000Å**]** *2000 ANG* height of the thick oxide *regions* **32**. In this case, after planarization of polysilicon **34**, **[**1000Å**]** *1000 ANG* of polysilicon **34** **[**remains**]** *remain* to overlie thick oxide *regions* **32**. *Thus, the overall thickness of the polysilicon 34* (*e.g., a conductive material layer*) *after planarization is about 3000 Å.* Next a layer of reflective material **35**, such as silicide (i.e. tungsten silicide, titanium silicide, etc.) or metal is formed over planarized polysilicon **34**. The higher the capability *that the reflective* material **35** has to reflect the photolithographic light during subsequent patterning of planarized conductive strips, the less susceptible are the patterned conductive strips to reflective notching. *The planarization of the conductively doped polysilicon 34* (*e.g., a conductive material*) *can be achieved by abrasion, such as chemical mechanical polishing.*

Referring now to FIG. **[4]** *4A*, planarized polysilicon **34** and silicide **35** are patterned to form planarized conductive strips **41** that will serve as (planarized) control gates to a MOS transistor.

As an alternative to FIGS. **3** and **[4***a,* FIG. **4***b* show**]** *4A, FIG. 4B shows* planarized conductive strips **42** that **[**is**]** *are* formed out of polysilicon only.

As another alternative to FIGS. **3** and **[4***a,* FIG. **4***c* show**]** *4A, FIG. 4C shows* planarized conductive strips **43** that are formed out of polysilicon **34**, silicide **35** and a partially reflective insulator **37** (such as nitride).

FIG. **5** shows a second embodiment depicting the use of the process steps of the present invention wherein a thick oxide is patterned and etched to form thick blocks of isolation oxide **52** that **[**is**]** *are* spaced apart by a thin gate oxide **51** that results from the etching of thick oxide **52**. To form gate oxide **51**, the thick oxide is etched to bare silicon and then a thin gate oxide is thermally grown on silicon **31**. The process steps **[**than**]** *then* follow those discussed in FIGS. **3** and **4** **[**and**]** to form resultant planarized conductive strips **53** that will serve as (planarized) control gates to a MOS transistor.

FIG. **6** is a flow diagram depicting the general process steps of the present invention described above wherein**[**;

Step A]: *Step 1* comprises forming a planarized conductive layer over [an] *a* non-planar substrate; Alternate [Step B] *Step 1.1* comprises forming a second conductive layer on the planarized conductive layer of [Step A] *Step 1*; and [Step C] *Step 3* comprises [patterned] *patterning* the conductive layers of [Steps A and C] *Steps 1 and 3* to form a planarized conductor.

From the process steps described in the two embodiments above, one skilled in the art could utilize these steps to form planarized conductive strips on [an] *a* non-planarized surface wherein the conductive strips comprise various conductive materials including multiple doped polysilicon layers, metal layers and any combination thereof.

Therefore, it is to be understood that although the present invention has been described with reference to several embodiments, various modifications, known to those skilled in the art, may be made to the structure and process steps presented herein without departing from the invention as recited in the several claims appended hereto.

What is claimed is:

1. A process for providing a planarized conductor on a non-planar starting substrate, said process comprising the steps of:

forming a layer of planarized conductive material overlying neighboring isolation regions such that the height of said *planarized* conductive material *layer* extends above the [topology] *topography* of said *neighboring* isolation regions;

forming a layer of reflective material superjacent and coextensive said planarized conductive material *layer*; and

patterning said *planarized* conductive material *layer* thereby forming said planarized conductor.

2. The process of claim **1**, wherein said *layer of* reflective material comprises a layer of reflective conductive material.

3. The process of claim **1**, wherein said *layer of* reflective material comprises a layer of partially reflective insulative material.

4. The process of claim **1**, wherein said layer of planarized conductive material is planarized by chemical mechanical polishing.

5. The process of claim **1**, wherein said layer of planarized conductive material comprises conductively doped polysilicon.

6. The process of claim **2**, wherein said layer of reflective conductive material comprises a material selected from [the] *a* group of metal silicides and metals.

7. The process of claim **6**, wherein said metal silicides comprise [the] *a* group of tungsten silicide and titanium silicide.

8. The process of claim **3**, wherein said *layer of* partially reflective insulating material comprises nitride.

9. A process for providing a planarized transistor gate on a non-planar starting substrate, said process comprising the steps of:

forming a layer of planarized conductive material overlying neighboring isolation regions such that the height of said *planarized* conductive material *layer* extends above the [topology] *topography* of said *neighboring* isolation regions;

forming a layer of reflective material superjacent and coextensive said planarized conductive material *layer*; and

patterning said *planarized* conductive material *layer* thereby forming said [thereby forming said] planarized transistor gate.

10. The process of claim **9**, wherein said layer of reflective material comprises reflective conductive material.

11. The process of claim **9**, wherein said reflective material comprises a layer of partially reflective insulative material.

12. The process of claim **9**, wherein said layer of planarized conductive material is planarized by chemical mechanical polishing.

13. The process of claim **9**, wherein said layer of planarized conductive material comprises conductively doped polysilicon.

14. The process of claim **10**, wherein said layer of reflective conductive material comprises a material selected from [the] *a* group of metal silicides and metals.

15. The process of claim **14**, wherein said metal silicides comprise [the] *a* group of tungsten silicide and titanium silicide.

16. The process of claim **11**, wherein said partially reflective insulating material comprises nitride.

17. The process of claim **9**, wherein said layer of planarized conductive material comprises in-situ conductively doped polysilicon.

18. The process of claim **9**, wherein said layer of planarized conductive [polysilicon] material is approximately 3000 Å thick.

19. The process of claim **9**, wherein said layer of planarized conductive [polysilicon] material has a thickness of approximately 1000 Å overlying said field oxide.

20. A process for providing a conductor on a non-planar substrate comprising:

forming a layer of conductive material on said non-planar substrate such that the height of said layer of conductive material extends above the topography of said non-planar substrate;

planarizing said conductive material layer;

forming a layer of at least partially reflective material over said planarized conductive material layer; and

patterning said planarized conductive material layer.

21. The process of claim 20, wherein forming said layer of at least partially reflective material comprises forming a layer of at least partially reflective conductive material.

22. The process of claim 20, wherein forming said layer of at least partially reflective material comprises forming a layer of at least partially reflective insulating material.

23. The process of claim 22, wherein forming said layer of at least partially reflective insulative material comprises forming a layer of material having nitride.

24. The process of claim 20, wherein planarizing said conductive material layer includes abrading said conductive material layer.

25. The process of claim 24, wherein planarizing said conductive material layer includes chemical mechanical polishing of said conductive material layer.

26. The process of claim 20, wherein said forming said conductive material layer includes forming a layer of material having conductively doped polysilicon.

27. The process of claim 20, wherein forming said conductive material layer comprises forming a single layer of said conductive material layer.

28. The process of claim 21, wherein forming said layer of at least partially reflective conductive material comprises forming a layer of material selected from a group of metal silicides and metals.

29. The process of claim 28, wherein forming a layer of said metal silicides comprises forming a layer of material selected from a group of tungsten silicide and titanium silicide.

30. A process for providing a transistor gate on a non-planar substrate, said process comprising the steps of:

forming a layer of conductive material on said non-planar substrate such that the height of said layer of conductive material extends above the topography of said non-planar substrate;

planarizing said conductive material layer;

forming a layer of at least partially reflective material over said planarized conductive material layer; and

patterning said planarized conductive material layer.

31. The process of claim 30, wherein forming said layer of at least partially reflective material comprises forming a layer of at least partially reflective conductive material.

32. The process of claim 30, wherein forming said layer of at least partially reflective material comprises forming a layer of at least partially reflective insulative material.

33. The process of claim 32, wherein forming said layer of at least partially reflective insulative material comprises forming a layer of material having nitride.

34. The process of claim 30, wherein planarizing said conductive material layer includes abrading said conductive material layer.

35. The process of claim 34, wherein planarizing said conductive material layer includes chemical mechanical polishing of said conductive material layer.

36. The process of claim 30, wherein forming said conductive material layer includes forming a layer of material having conductively doped polysilicon.

37. The process of claim 30, wherein forming said conductive material layer comprises forming a single layer of said conductive material layer.

38. The process of claim 31, wherein forming said layer of at least partially reflective conductive material comprises forming a layer of material selected from a group of metal silicides and metals.

39. The process of claim 38, wherein forming said layer of metal silicides comprises forming a layer of material selected from a group of tungsten silicide and titanium silicide.

40. The process of claim 30, wherein forming said conductive material layer comprises forming a layer of in-situ conductively doped polysilicon.

41. The process of claim 30, wherein forming said conductive material layer comprises forming a layer of conductive material having a thickness of approximately 3000 Å.

42. The process of claim 30, wherein forming said conductive material layer comprises forming a layer of conductive material having a thickness of approximately 1000 Å above the topography of said non-planar substrate.

43. A process for providing a conductor on a non-planar substrate comprising:

forming a substantially planar layer of conductive material on said non-planar substrate such that the height of said substantially planar layer of conductive material extends above the topography of said non-planar substrate;

forming a layer of at least partially reflective material over said substantially planar conductive material layer; and

patterning said substantially planar conductive material layer.

44. The process of claim 43, wherein forming said layer of at least partially reflective material comprises forming a layer of at least partially reflective, conductive material.

45. The process of claim 43, wherein forming said layer of at least partially reflective material comprises forming a layer of at least partially reflective, insulative material.

46. The process of claim 45, wherein forming said layer of at least partially reflective insulative material comprises forming a layer of material having nitride.

47. The process of claim 43, wherein forming said substantially planar conductive material layer comprises forming a layer of material having conductively doped polysilicon.

48. The process of claim 43, wherein forming said substantially planar conductive material layer comprises forming a single layer of said substantially planar conductive material layer.

49. The process of claim 44, wherein forming said layer of at least partially reflective conductive material comprises forming a layer of material selected from a group of metal silicides and metals.

50. The process of claim 49, wherein forming a layer of said metal silicides comprises forming a layer of material selected form a group of tungsten silicide and titanium silicide.

51. A process for providing a transistor gate on a non-planar substrate, said process comprising the steps of:

forming a substantially planar layer of conductive material on said non-planar substrate such that the height of said substantially planar layer of conductive material extends above the topography of said non-planar substrate;

forming a layer of at least partially reflective material over said substantially planar conductive material layer; and

patterning said substantially planar conductive material layer.

52. The process of claim 51, wherein forming said layer of at least partially reflective material comprises forming a layer of at least partially reflective conductive material.

53. The process of claim 51, wherein forming said layer of at least partially reflective material comprises forming a layer of at least partially reflective insulative material.

54. The process of claim 53, wherein forming said layer of at least partially reflective insulative material comprises forming a layer of material having nitride.

55. The process of claim 51, wherein said substantially planar conductive material layer comprises forming a layer of material having conductively doped polysilicon.

56. The process of claim 51, wherein forming said substantially planar conductive material comprises forming a single layer of said substantially planar conductive material layer.

57. The process of claim 52, wherein forming said at least partially reflective conductive material layer comprises forming a layer of material selected from a group of metal silicides and metals.

58. The process of claim 57, wherein forming said metal silicides comprises forming a layer of material selected from a group of tungsten silicide and titanium silicide.

59. The process of claim 51, wherein forming said substantially planar conductive material layer comprises forming a layer of in-situ conductively doped polysilicon.

60. The process of claim 51, wherein forming said substantially planar conductive material layer comprises forming a layer of conductive material having a thickness of approximately 3000 Å.

61. The process of claim 51, wherein forming said substantially planar conductive material layer comprises forming a layer of conductive material having a thickness of approximately 1000 Å above the topography of said non-planar substrate.

* * * * *