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(54) **HIGH DEFINITION TELEVISION RECEIVER**

OTHER PUBLICATIONS

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“VSB Transmission System”, Zenith Electronics Corporation, Dec. 17, 1993, pp 8–16, FIGS. 9, 12, 14.\*

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(57) **ABSTRACT**

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A HDTV receiver which is improved in its overall performance and is simplified in its configuration, by improving a symbol timing restoring circuit, includes a tuner for selecting a necessary channel from input signals via an antenna, an IF processing & carrier restoring portion for performing an IF process & carrier restoration from the output of the tuner, an analog-to-digital converter (ADC) for converting the output of the IF processing & carrier restoring portion into a digital signal, a timing restoring portion for restoring a timing from the output of the ADC, a 2:1 down-sampler for 2:1 down-sampling the output of the ADC, a sync detector for detecting a sync from the output of the 2:1 down-sampler, a channel equalizer for performing a channel equalization from the output of the 2:1 down-sampler, a phase controller for correcting the phase error from the output of the channel equalizer, an optimal viterbi decoder for performing a viterbi decoding operation from the output of the phase controller, a deinterleaver for dissipating the output of the optimal viterbi decoder in order to enhance the correction capability due to burst errors, an error controller for performing a Reed-Solomon decoding operation with respect to the output of the deinterleaver, and a derandomizer for releasing the output of the error controller and restoring a signal randomly formed at a transmission port reversely.

**Related U.S. Patent Documents**

Reissue of:

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(52) **U.S. Cl.** ..... **348/426; 348/726; 348/538; 375/355; 375/371**

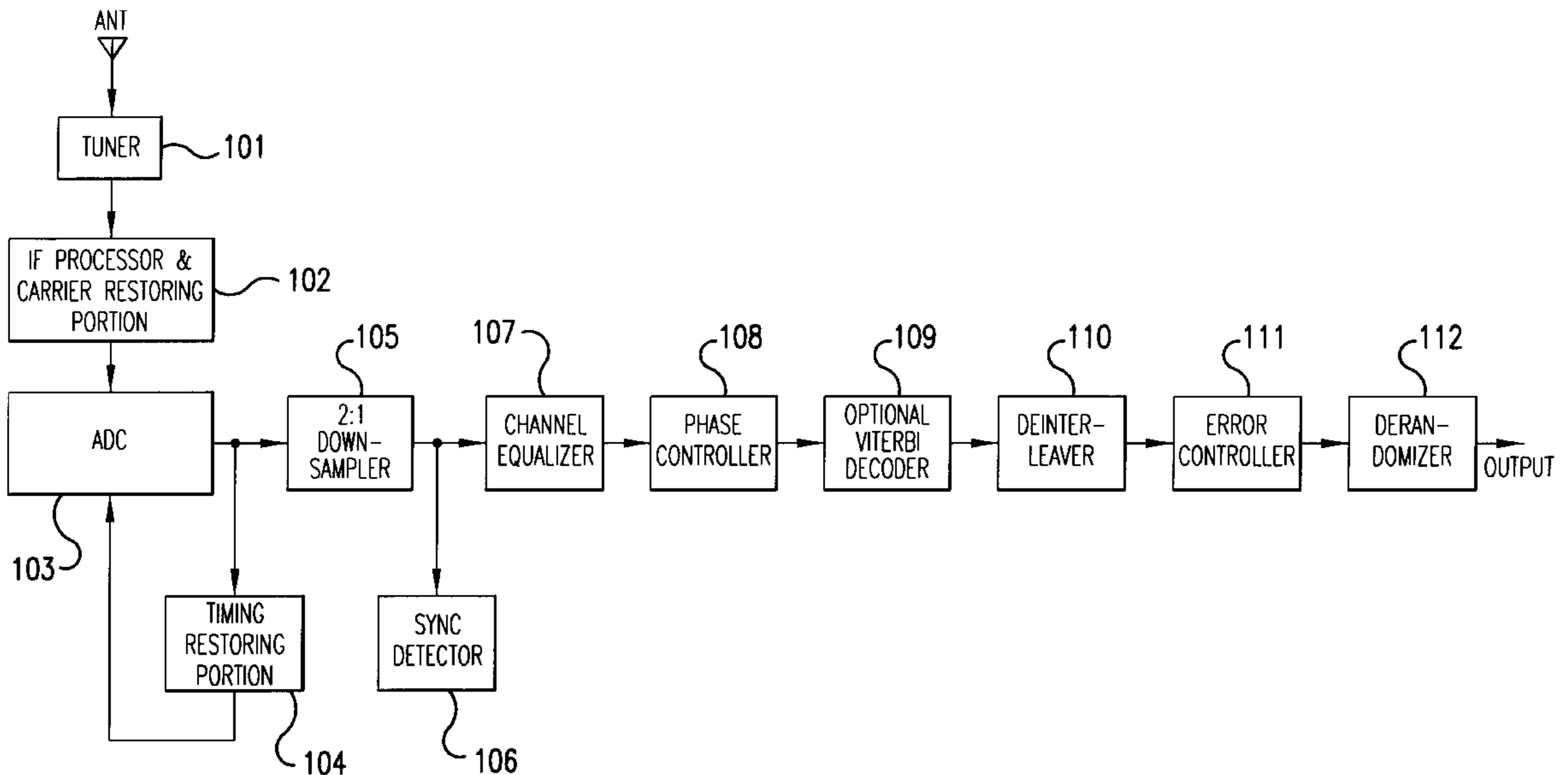
(58) **Field of Search** ..... 348/426, 726, 348/731, 735, 536, 537, 538, 392, 424; 375/316, 341, 355, 359, 371, 376; H04N 7/015

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**30 Claims, 4 Drawing Sheets**



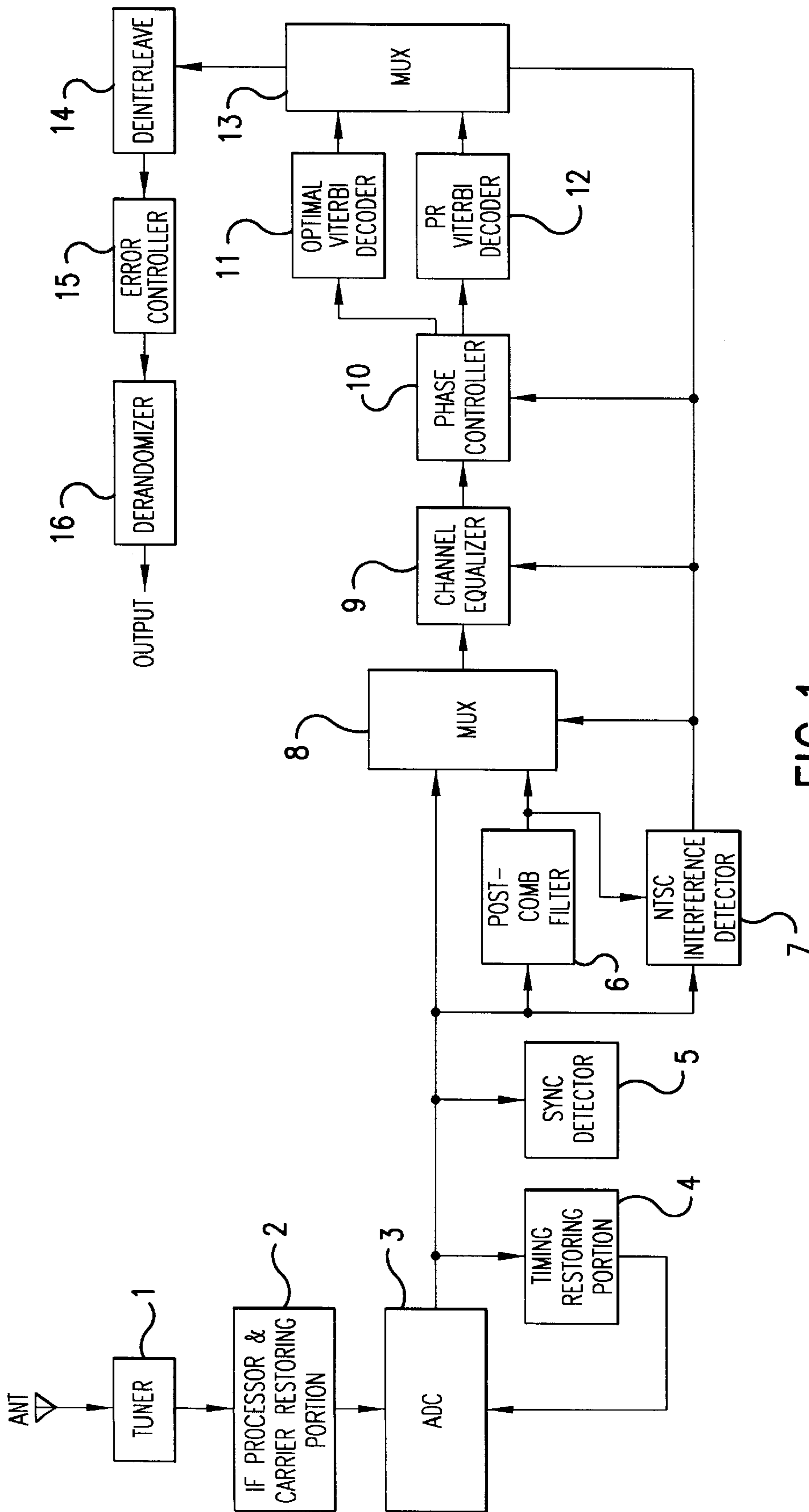


FIG. 1  
PRIOR ART

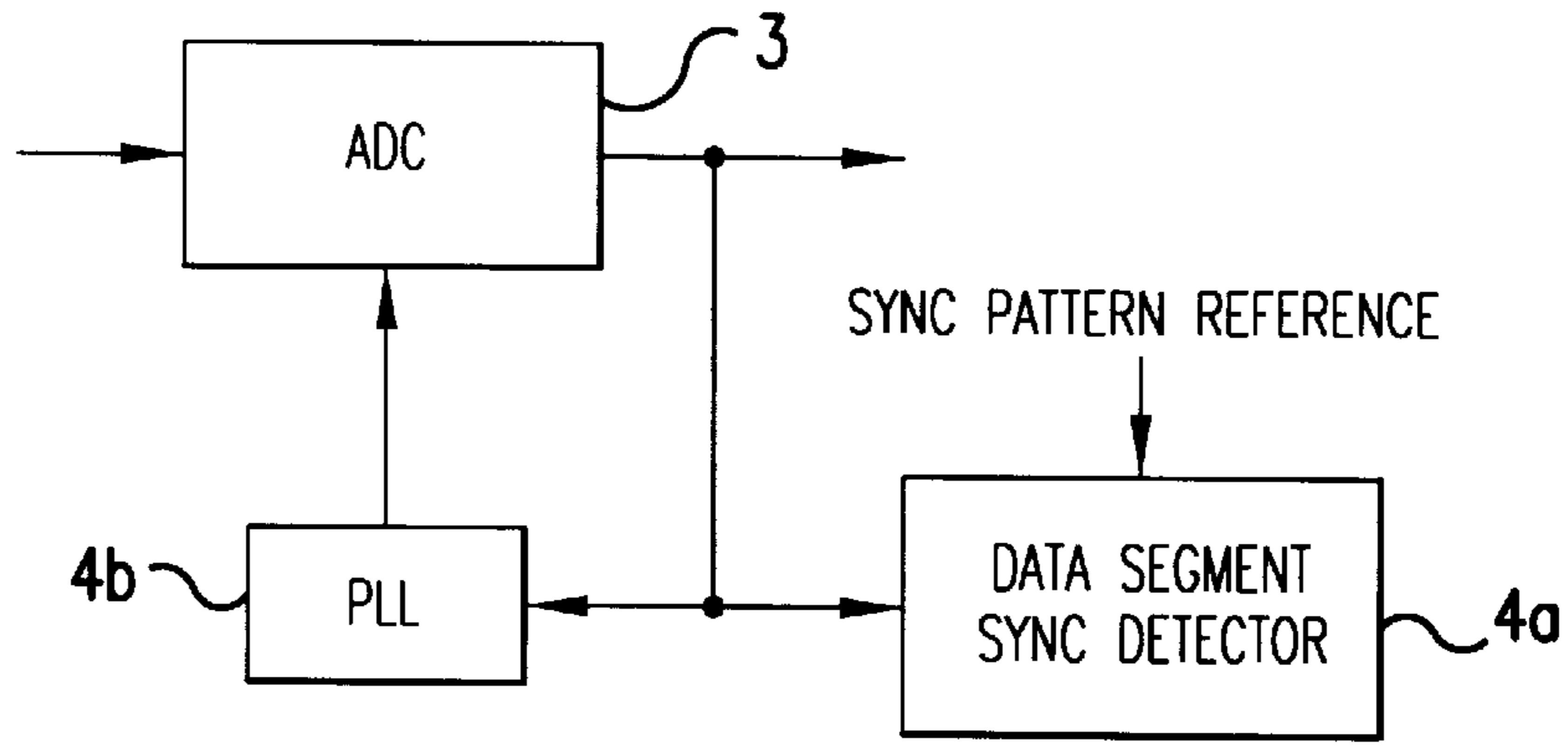
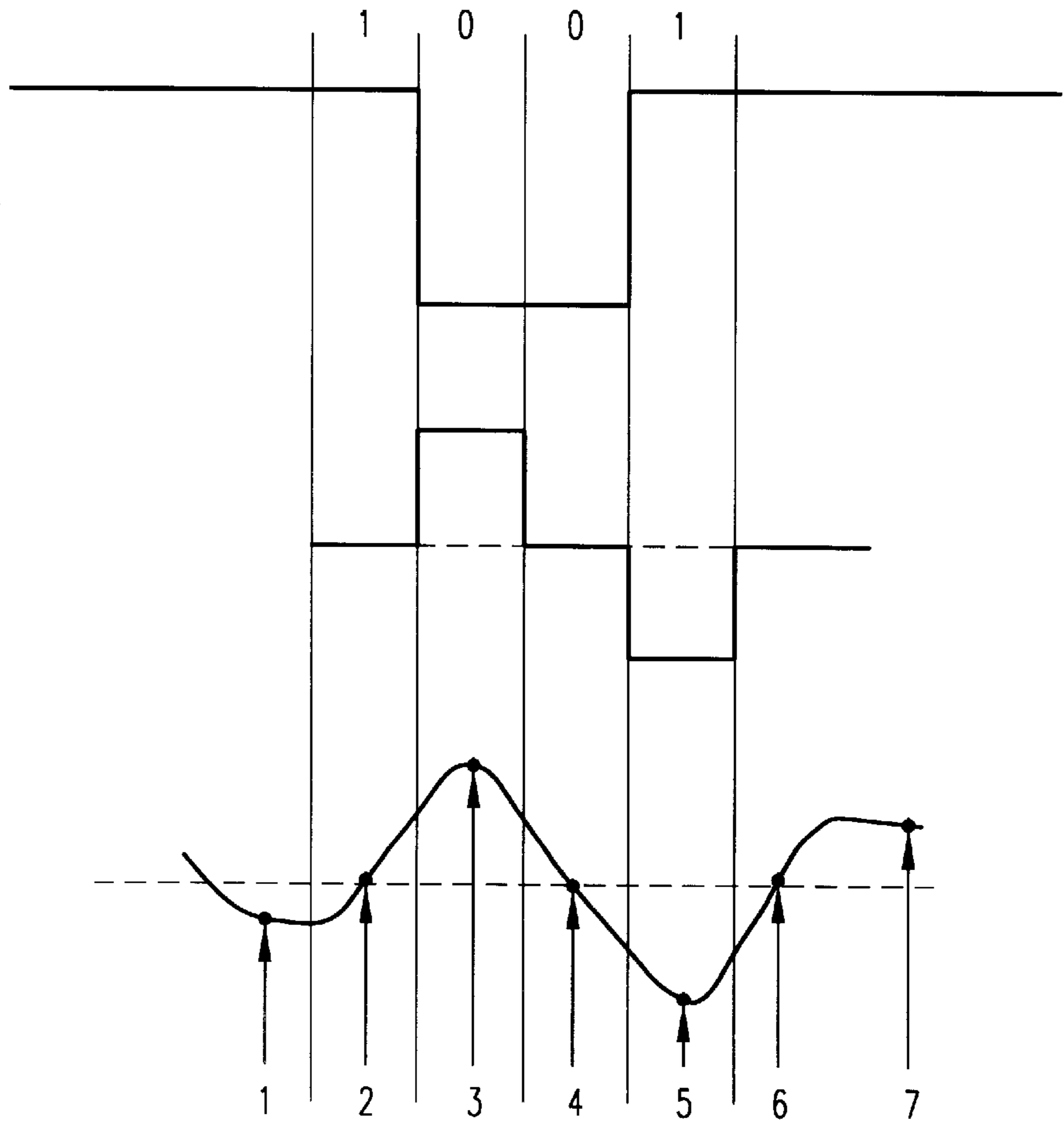


FIG. 2  
PRIOR ART

FIG. 3A  
PRIOR ART

FIG. 3B  
PRIOR ART

FIG. 3C  
PRIOR ART



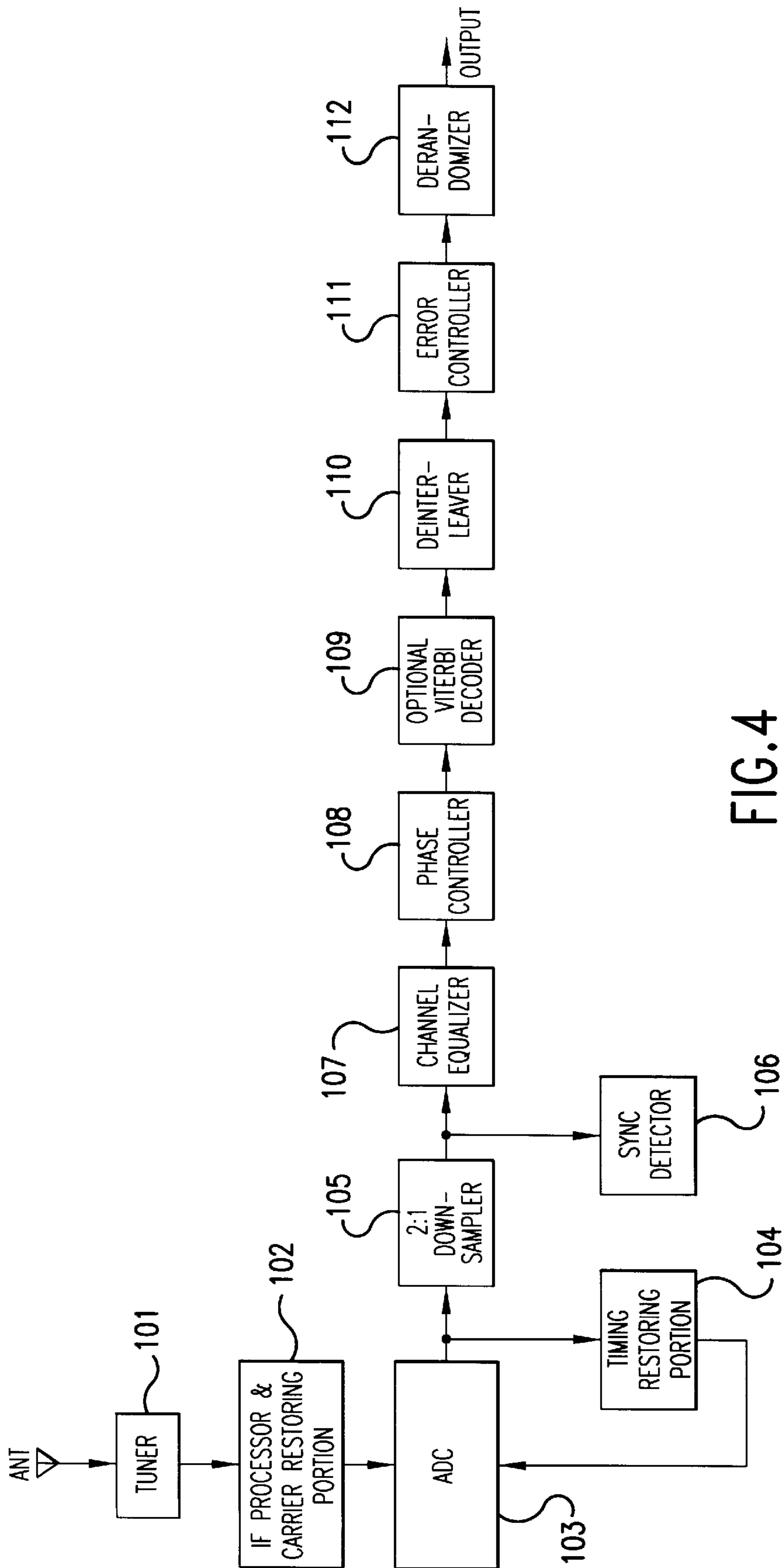


FIG. 4

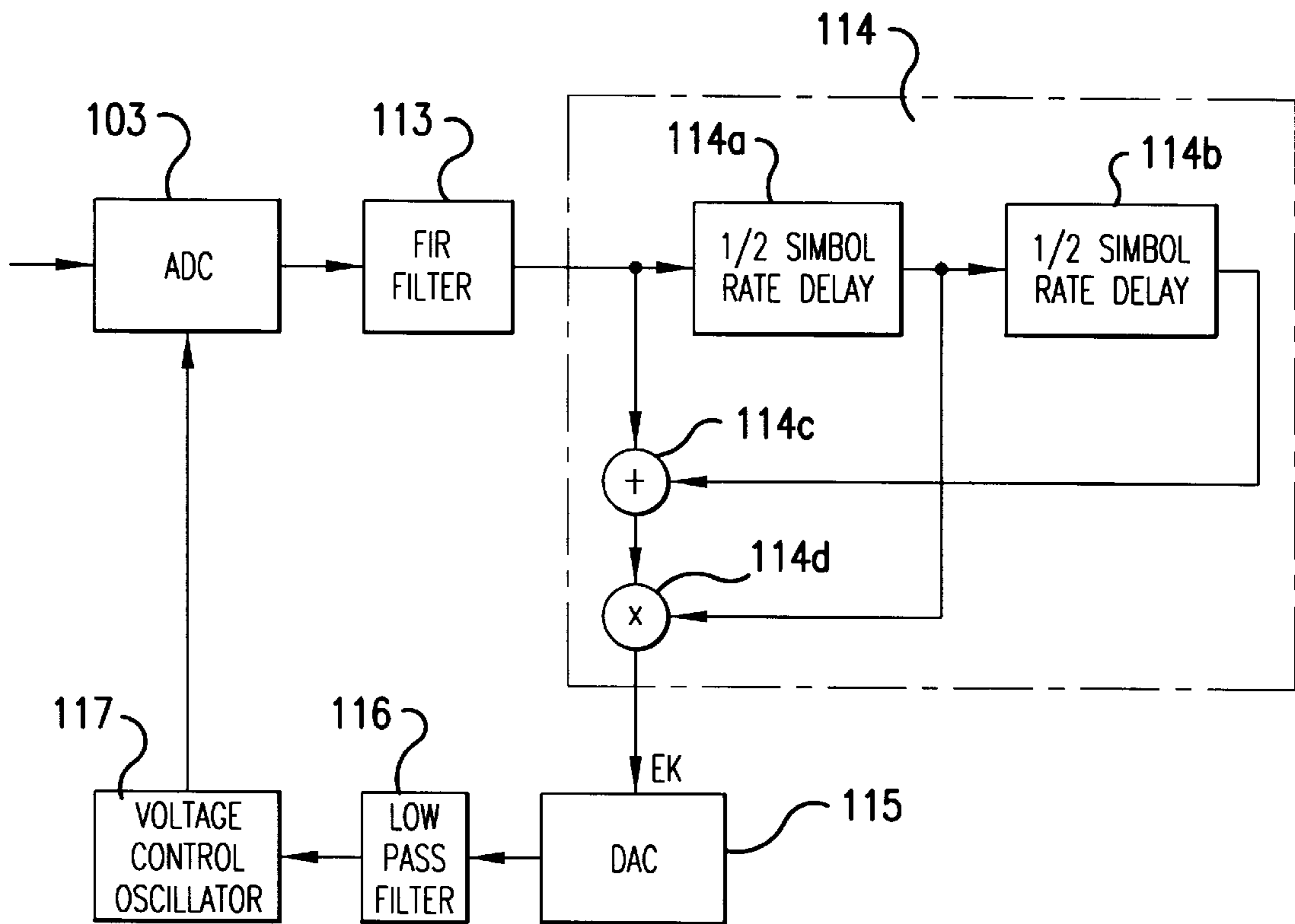


FIG.5

## HIGH DEFINITION TELEVISION RECEIVER

**Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.**

## BACKGROUND OF THE INVENTION

The present invention relates to a high definition television (HDTV) receiver, and more particularly, to a HDTV receiver which is improved in its overall performance and is simplified in its configuration, by improving a symbol timing restoring circuit.

FIG. 1 is a block diagram of a conventional 8-vestigial sideband (VSB) receiver, in which a high-frequency signal input from an antenna (ANT) is demodulated and is carrier-restored when a channel is selected in a tuner 1 and a signal having a central frequency of 44 MHz is automatic-gain controlled and IF-bandpass filtered in an IF processor & carrier restoring portion 2.

This signal is digitally sampled in an analog-to-digital converter (ADC) 3 and precise symbol timing is detected by a timing restoring portion 4, thereby controlling the timing of ADC 3.

The output of ADC 3 is also input to a sync detector 5 to detect a data segment sync from a data segment sync pattern (FIG. 3A) and to detect a field sync from a field sync pattern being in the first line of a transmission format.

At this time, the data segment sync and field sync detected in sync detector 5 are used as the control signals of subsequent blocks 7 through 16.

NTSC (National Television System Committee) interference detector 7 receives a signal passing through a post-comb filter 6 and a signal not passing therethrough and determines whether there is an identical channel interference with that of NTSC or not, to then transmit a comb control signal SC1.

If there is no NTSC identical channel interference, the signal not passing through post-comb filter 6 is selected by a multiplexer 8. A channel equalizer 9 equalizes the incoming signal which is set to 8 levels to remove the intersymbol interference due to a ghost generated at the channel.

Also, a phase corrector 10 corrects the phase error remaining after signal-processing, setting the incoming signal to 8 levels. An optimal viterbi decoder 11 performs a 4-state viterbi decoding operation and the decoded output is output through multiplexer 13.

If there is NTSC identical channel interference, the output of post-comb filter 6 is selected as the output of multiplexer 8. At this time, post-comb filter 6 subtracts data delayed for 12 symbol period from the current data.

Therefore, the original 8 level data becomes 15 level data. The NTSC identical channel interference is removed. At this time, channel equalizer 9 and phase controller 10 operate assuming that the incoming signal is 15 level data, and multiplexer 13 selects and outputs the output of a partial response (PR) viterbi decoder 12.

PR viterbi decoder 12, an 8-state decoder, has much more complex structure than that of optimal viterbi decoder 11.

The output of multiplexer 13 is dissipated in order to enhance the correction capability for burst errors in a deinterleaver 14. An error controller 15 performs a Reed-Solomon decoding operation.

Also, a derandomizer 16 releases a signal randomly formed in a transmission port reversely. Timing restoring

portion 4 is constituted by a data segment sync detector 4a and a phase locked loop (PLL) 4b, as shown in FIG. 2. The digitally converted signal is concurrently output to data segment sync detector 4a and PLL 4b.

At this time, data segment sync detector 4a detects a data segment sync, based on the data pattern "1001" for 4 symbol period of 2 levels shown in FIG. 3A.

PLL 4b detects the phase error for the timing from a data segment sync pattern. The output of a phase detector is as shown as FIG. 3B, digitally, and as FIG. 3C, analogically.

The position of a sampling point 4 shown in FIG. 3C is a zero-crossing point, and a symbol timing is detected using the zero-crossing point.

However, the aforementioned conventional art adopting a post-comb filter for reducing the NTSC identical channel interference has a very complex configuration.

## SUMMARY OF THE INVENTION

To solve these problems, it is an object of the present invention to provide a HDTV receiver, which allows a better symbol timing restoration even if there is an NTSC identical channel interference, by improving a symbol timing restoring circuit, and which is simplified in its configuration, by eliminating a post-comb filter.

To accomplish the above object, there is provided a HDTV receiver comprising: a tuner for selecting a necessary channel from input signals via an antenna; an IF processing & carrier restoring portion for performing an IF process & carrier restoration from the output of the tuner; an analog-to-digital converter (ADC) for converting the output of the IF processing & carrier restoring portion into a digital signal; a timing restoring portion for restoring a timing from the output of the ADC; a 2:1 down-sampler for 2:1 down-sampling the output of the ADC; a sync detector for detecting a sync from the output of the 2:1 down-sampler; a channel equalizer for performing a channel equalization from the output of the 2:1 down-sampler; a phase controller for correcting the phase error from the output of the channel equalizer; an optimal viterbi decoder for performing a viterbi decoding operation from the output of the phase controller; a deinterleaver for dissipating the output of the optimal viterbi decoder in order to enhance the correction capability due to burst errors; an error controller for performing a Reed-Solomon decoding operation with respect to the output of the deinterleaver; and a derandomizer for releasing the output of the error controller and restoring a signal randomly formed at a transmission port reversely.

## BRIEF DESCRIPTION OF THE DRAWINGS

The above objects and advantages of the present invention will become more apparent by describing in detail a preferred embodiment thereof with reference to the attached drawings in which:

FIG. 1 is a block diagram of a conventional HDTV receiver;

FIG. 2 is a detailed block diagram of a timing restoring portion shown in FIG. 1;

FIGS. 3A through 3C are timing charts shown in FIG. 2;

FIG. 4 is a block diagram of a HDTV receiver according to the present invention; and

FIG. 5 is a detailed block diagram of a timing restoring portion shown in FIG. 4.

## DETAILED DESCRIPTION OF THE INVENTION

As shown in FIG. 4, the HDTV receiver according to the present invention has a simpler configuration than the con-

ventional system in that post-comb filter 6, NTSC interference detector 7, multiplexer 8, PR viterbi decoder 12 and multiplexer 13 are eliminated from the conventional one. Channel equalizer 9 and phase corrector 10 of the conventional system correspond to channel equalizer 107 and phase controller 108 of the present invention, respectively. Timing restoring portion 4 of the conventional system corresponds to a new timing restoring portion 104 of the present invention, so that a symbol timing restoration is performed well even in the case of the NTSC identical channel interference.

As shown in FIG. 5, timing restoring portion 104 includes an FIR filter 113 for filtering only the signal of a necessary symbol rate among the signals passing through ADC 103, a phase error detector 114 for detecting a phase error (ek) from the output of FIR filter 113, a digital-to-analog converter (DAC) 115 for converting again the output of phase error detector 114 into an analog signal, a lowpass filter 116 for lowpass-filtering the output of DAC 115, and a voltage controlled oscillator 117 for varying an oscillated frequency according to the output of lowpass filter 116 to supply a signal required in ADC 103.

At this time, phase error detector 114 is constituted by  $\frac{1}{2}$  symbol rate delays 114a and 114b for delaying the output of FIR filter 113 by  $\frac{1}{2}$  symbol rate, an adder 114c for adding the output of FIR filter 113 with the output of  $\frac{1}{2}$  symbol rate delay 114b, and a multiplier 114d for multiplying the output of adder 114c with the output of  $\frac{1}{2}$  symbol rate delay 114a to output a phase error (ek).

In the present invention having the aforementioned configuration, the operation of a tuner 101 and an IF processing & carrier restoring portion is the same as that of the conventional art. ADC 103 uses a clock of 21.52 MHz for over-sampling twice the symbol rate with a sampling clock, which is because the data twice over-sampled is required in timing restoring portion 104.

The signal restored from timing restoring portion 104 is directly supplied to 2:1 down-sampler 105, and 2:1 down-sampler 105 samples only the data of a desired symbol rate. A sync detector 106 detects a data segment sync and a data field sync.

A channel equalizer 107 to which only 8 level data is applied equalizes in accordance therewith. Also, phase controller 108 and optimal viterbi decoder 109 to which only 8 level data are applied, operate irrespective of 15 level data.

The operations of deinterleaver 110, error controller 111 and derandomizer 112 will be omitted here, since the respective elements operate in the same manner as that of the corresponding elements of the conventional system.

The signal passing through ADC 103 undergoes a bandpass filtering operation of central 5.38 MHz ( $=\frac{1}{2}T$ , here,  $1/T$  is symbol rate) in FIR filter 113 of timing restoring portion 104.

The output of FIR filter 113 is delayed in  $\frac{1}{2}$  symbol rate delays 114a and 114b by  $\frac{1}{2}$  symbol rate. The output of  $\frac{1}{2}$  symbol rate delay 114b and the output of FIR filter 113 is added in an adder 114c. The added output and the output of  $\frac{1}{2}$  symbol rate delay 114a is multiplied in a multiplier 114d to then output a phase error (ek).

A phase error (ek) is converted into an analog signal in DAC 115 and is lowpass-filtered in a low-pass in lowpass filter 116. Then, voltage-controlled oscillator (VC) 117 supplies a clock required for DAC 103.

In other words, the signal passing through timing restoring portion 104 becomes a symmetric IF bandpass filtered signal of central 5.38 MHz. A zero crossing always occurs at a position of odd number times of  $T/2$ .

As described above, according to the the present invention, a symbol timing restoration is done well even if there is an NTSC identical channel interference, by improving a symbol timing restoring circuit. Also, based on the improved symbol timing restoring circuit, a post-comb filter can be eliminated, which considerably simplifies the overall circuit configuration.

What is claimed is:

1. [A] An HDTV receiver comprising:

a tuner for selecting a necessary channel from input signals via an antenna;

an IF processing & carrier restoring portion for performing an IF process & carrier restoration from [the] an output of said tuner;

an analog-to-digital converter (ADC) for converting [the] an output of said IF processing & carrier restoring portion into a digital signal;

a timing restoring portion for restoring [said] timing from the output of said ADC;

a 2:1 down-sampler for 2:1 down-sampling [the] an output of said ADC;

a sync detector for detecting a sync from [the] an output of the 2:1 down-sampler;

a channel equalizer for performing a channel equalization from [the] an output of the 2:1 down-sampler;

a phase controller for correcting [the] a phase error from [the] an output of the channel equalizer;

an optimal viterbi decoder for performing a viterbi decoding operation from [the] an output of said phase controller;

a deinterleaver for dissipating [the] an output of said optimal viterbi decoder in order to enhance [the correction] a capability [due] to correct burst errors;

an error controller for performing a Reed-Solomon decoding operation with respect to [the] an output of said deinterleaver; and

a derandomizer for releasing [the] an output of said error controller and restoring a signal randomly formed at a transmission port reversely.

2. [A] An HDTV receiver as claim 1, where said timing restoring portion comprises:

an FIR filter for filtering only the signal of a necessary symbol rate among [the] a plurality of signals passing through said ADC;

a phase error detector for detecting [an] a phase error (ek) from the output of said FIR filter;

a digital-to-analog converter (DAC) for converting again the output of said phase error detector into an analog signal;

a lowpass filter for lowpass-filtering the output of said DAC; and

a voltage controlled oscillator for varying an oscillated frequency according to the output of said lowpass filter to supply a signal required in said ADC.

3. [A] An HDTV receiver as claim [1] 2, where said phase error detector comprises:

first and second  $\frac{1}{2}$  symbol rate delays for delaying the output of said FIR filter by  $\frac{1}{2}$  symbol rate;

an adder for adding the outputs of said second  $\frac{1}{2}$  symbol rate delay; and

a multiplier for multiplying the output of said adder with the output of said first  $\frac{1}{2}$  symbol rate delay to output a phase error (ek).

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4. A digital television receiver comprising:  
 a tuner for selecting a channel from input signals;  
 an IF processing portion for performing an IF process from an output signal of the tuner;  
 an analog-to-digital converter coupled to the IF processing portion and converting an output signal from the IF processing portion into a digital signal;  
 a timing restoring portion coupled to the analog-to-digital converter and restoring a timing from an output signal of the analog-to-digital converter;  
 an N:M sampler coupled to the analog-to-digital converter and N:M sampling the output signal of the analog-to-digital converter, where N and M are integers and N is greater than M;  
 a sync detector coupled to the N:M sampler and detecting a sync from an output signal of the N:M sampler;  
 a channel equalizer coupled to the N:M sampler and performing a channel equalization from the output signal of the N:M sampler;  
 a phase controller coupled to the channel equalizer and correcting a phase error from an output of the channel equalizer;  
 a deinterleaver coupled to the phase controller and enhancing an error correction capability;  
 an error controller coupled to the deinterleaver and performing a decoding operation with respect to an output signal of the deinterleaver; and  
 a derandomizer coupled to the error controller and releasing an output signal of the error controller and restoring a randomly formed signal.
5. The digital television receiver according to claim 4, wherein the tuner includes the IF processing portion.
6. The digital television receiver according to claim 4, further comprising a carrier restoration portion performing carrier restoration from the output signal of the tuner.
7. The digital television receiver according to claim 4, wherein the N:M sampler includes a 2:1 down sampler.
8. The digital television receiver according to claim 4, further comprising an optimal viterbi decoder coupled to the phase controller and performing a decoding operation from the output signal of the phase controller.
9. The digital television receiver according to claim 8, wherein the deinterleaver dissipates an output signal of the optimal viterbi decoder.
10. The digital television receiver according to claim 4, wherein the timing restoring portion comprises:  
 an FIR filter for filtering a signal of a selected symbol rate among a plurality of signals input to the timing restoring portion;  
 a phase error detector for detecting a phase error from an output signal of said FIR filter;  
 a digital-to-analog converter for converting output signal of the phase error detector into an analog signal;  
 a low pass filter for low-pass filtering an output signal of the digital-to-analog converter; and  
 a voltage controlled oscillator for varying an oscillating frequency according to an output signal of the low pass filter to supply a signal required in the analog-to-digital converter.
11. The digital television receiver according to claim 10, wherein the phase error detector comprises:  
 first and second  $\frac{1}{2}$  symbol rate delays for delaying the output signal of the FIR filter by  $\frac{1}{2}$  symbol rate;  
 an adder for adding the output signal of the FIR filter and an output signal of the second  $\frac{1}{2}$  symbol rate delay; and

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- a multiplier for multiplying an output signal of the adder with an output signal of the first  $\frac{1}{2}$  symbol rate delay to output the phase error.
12. The digital television receiver of claim 4, wherein the timing restoring portion restores symbol timing to the output signal of the analog-digital converter.
13. A digital television receiver comprising:  
 an input unit receiving a television signal and generating a digital signal through at least a 2:1 upsampling;  
 a timing restoring portion restoring a timing from the upsampled digital signal;  
 a down-sampler for at least 2:1 down sampling the upsampled digital signal and outputting a down-sampled signal;  
 a sync detector detecting a sync from the down-sampled signal of the down-sampler;  
 a channel equalizer performing a channel equalization from the down-sampled signal of the down-sampler and outputting a channel equalized signal;  
 a phase controller correcting a phase error from the channel equalized signal of the channel equalizer and outputting a phase controlled signal;  
 a deinterleaver coupled to the phase controller and enhancing an error correction capability and outputting a deinterleaved signal;  
 an error controller performing a decoding operation with respect to the deinterleaved signal of the deinterleaver and outputting a decoded signal; and  
 a derandomizer releasing the decoded signal of the error controller and restoring a randomly formed signal.
14. The digital television receiver according to claim 13, wherein the input unit comprises:  
 a tuner selecting a channel from input signal via an antenna;  
 an IF processing portion for performing an IF process from an output signal of the tuner;  
 a carrier restoring portion for performing a carrier restoration from the output signal of the tuner; and  
 an analog-to-digital converter converting an output signal of the IF processing portion into the digital signal.
15. The digital television receiver according to claim 14, wherein the timing restoring portion comprises:  
 an FIR filter for filtering a signal of a selected symbol rate among a plurality of signals input to the timing restoring portion;  
 a phase error detector for detecting a phase error from an output signal of said FIR filter;  
 a digital-to-analog converter for converting output signal of the phase error detector into an analog signal;  
 a low pass filter for low-pass filtering an output signal of the digital-to-analog converter; and  
 a voltage controlled oscillator for varying an oscillating frequency according to an output signal of the low pass filter to supply a signal required in the analog-to-digital converter.
16. The digital television receiver according to claim 15, wherein the phase error detector comprises:  
 first and second  $\frac{1}{2}$  symbol rate delays for delaying the output signal of the FIR filter by  $\frac{1}{2}$  symbol rate;  
 an adder for adding the output signal of the FIR filter and an output signal of the second  $\frac{1}{2}$  symbol rate delay; and  
 a multiplier for multiplying an output signal of the adder with an output signal of the first  $\frac{1}{2}$  symbol rate delay to output the phase error.



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17. The digital television receiver of claim 14, wherein the timing restoring portion restores symbol timing to the upsampled digital signal.

18. The digital television receiver of claim 17, wherein the timing restoring portion comprises:

- a filter for filtering a signal of a selected symbol rate among a plurality of signals input to the filter;
- a phase error detector for detecting a phase error in an output signal of said filter;
- a low pass filter for low-pass filtering an output signal of the phase error detector; and
- a voltage controlled oscillator for varying an oscillating frequency supplied to the low pass filter to supply a signal required in the analog-to-digital converter.

19. The digital television receiver according to claim 13, wherein the input unit comprises:

- a tuner selecting a channel from an input signal via an antenna; and
- an IF processing portion for performing an IF process from an output signal of the tuner.

20. The digital television receiver according to claim 13, wherein the input unit comprises:

- a tuner selecting a channel from input signal via an antenna;
- an IF processing portion for performing an IF process from an output signal of the tuner; and
- carrier restoring portion for performing a carrier restoration from the output signal of the tuner.

21. The digital television receiver according to claim 13, further comprising an optimal viterbi decoder coupled to the phase controller and performing a decoding operation from the output signal of the phase controller.

22. The digital television receiver according to claim 21, wherein the deinterleaver dissipates an output signal of the optimal viterbi decoder.

23. The digital television receiver of claim 13, wherein the timing restoring portion restores symbol timing to the upsampled digital signal.

24. The digital television receiver of claim 13, wherein the television signal is an 8-VSB digital television signal.

25. The digital television receiver of claim 24, wherein the input unit also receives an NTSC television signal on a same channel as the 8-VSB digital television signal, and further wherein the timing restoring portion restores symbol timing to the upsampled digital signal.

26. A digital television receiver, comprising:

- a tuner for selecting one channel of a plurality of channels;

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an IF processor coupled to an output of said tuner for IF processing an output signal of the tuner;

an analog-to-digital converter coupled to an output of the IF processor for converting an output signal of the IF processor to a digital signal;

a timing restoring portion for controlling timing of the analog-to-digital converter;

an N:M downsampler coupled to the output of the analog-to-digital converter for sampling the digital signal, wherein N and M are integers and N is greater than M;

a channel equalizer coupled to an output of the N:M downsampler for channel equalizing the digital signal;

a phase controller coupled to an output of the channel equalizer for correcting a phase error in the digital signal;

a deinterleaver coupled to an output of the phase controller for enhancing a capability to correct burst errors in the digital signal;

an error controller coupled to an output of the deinterleaver for decoding the digital signal; and

a derandomizer coupled to an output of said error controller for derandomizing the digital signal.

27. The digital television receiver of claim 26, wherein the tuner receives an 8-VSB digital television signal in the selected channel.

28. The digital television receiver of claim 27, wherein the tuner also receives an NTSC television signal on a same channel as the 8-VSB digital television signal.

29. The digital television receiver of claim 26, wherein the timing restoration portion restores symbol timing to the digital signal.

30. The digital television receiver of claim 26, wherein the timing restoration portion comprises:

- a filter coupled to the output of the analog-to-digital converter for filtering a signal of a selected symbol rate among a plurality of signals input to the filter;

- a phase error detector for detecting a phase error in an output signal of said filter;

- a low pass filter for low-pass filtering an output signal of the phase error detector; and

- a voltage controlled oscillator coupled to an output of the low pass filter and providing a signal for controlling timing of the analog-to-digital converter.

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