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Harlin et al.

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[54] DYNAMIC VIDEO RAM INCORPORATING ON CHIP VECTOR/IMAGE MODE LINE MODIFICATION

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Related U.S. Patent Documents

Reissue of:

[64] Patent No.: 5,148,524
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Appl. No.: 277,687
Filed: Nov. 29, 1988

U.S. Applications:

[63] Continuation of Ser. No. 306,180, Sep. 14, 1994, abandoned.

[51] Int. Cl.⁶ G06F 12/02; G06F 13/38

[52] U.S. Cl. 395/517

[58] Field of Search 365/189, 230;
398/164-166, 550; 395/432, 494, 421.07,
421.08

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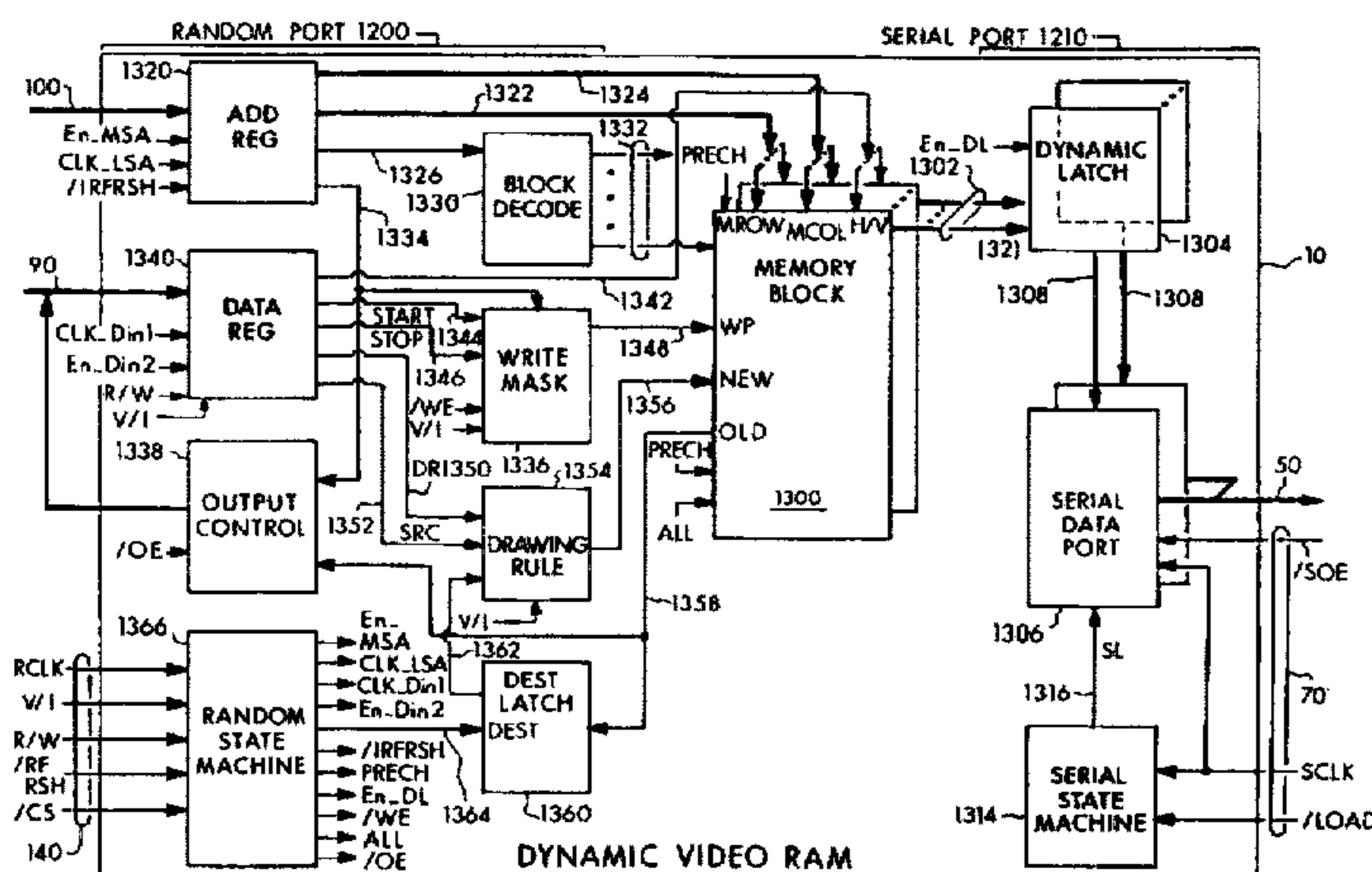
Primary Examiner—Thomas M. Heckler

Attorney, Agent, or Firm—Renner, Otto, Boisselle, Sklar

[57] ABSTRACT

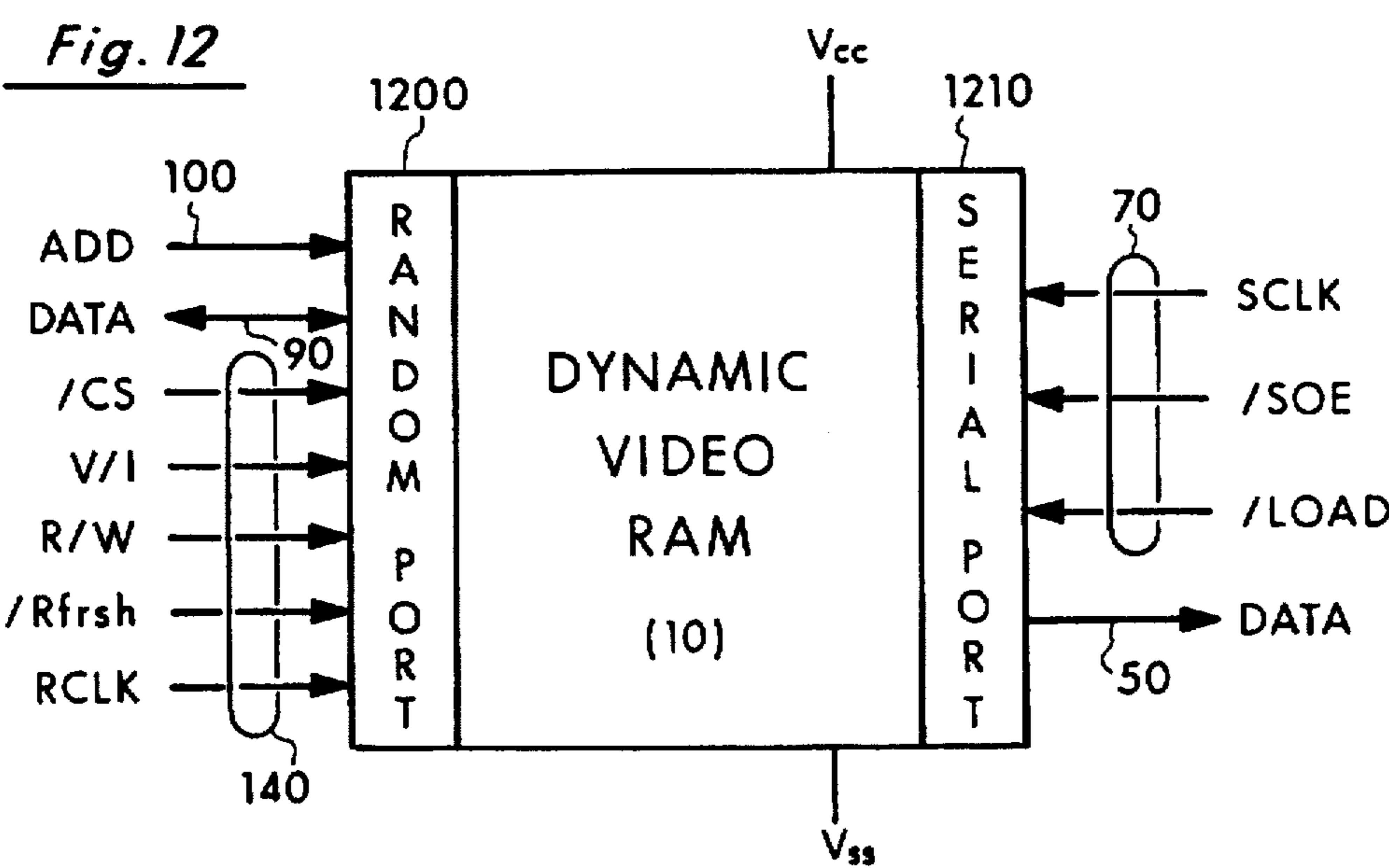
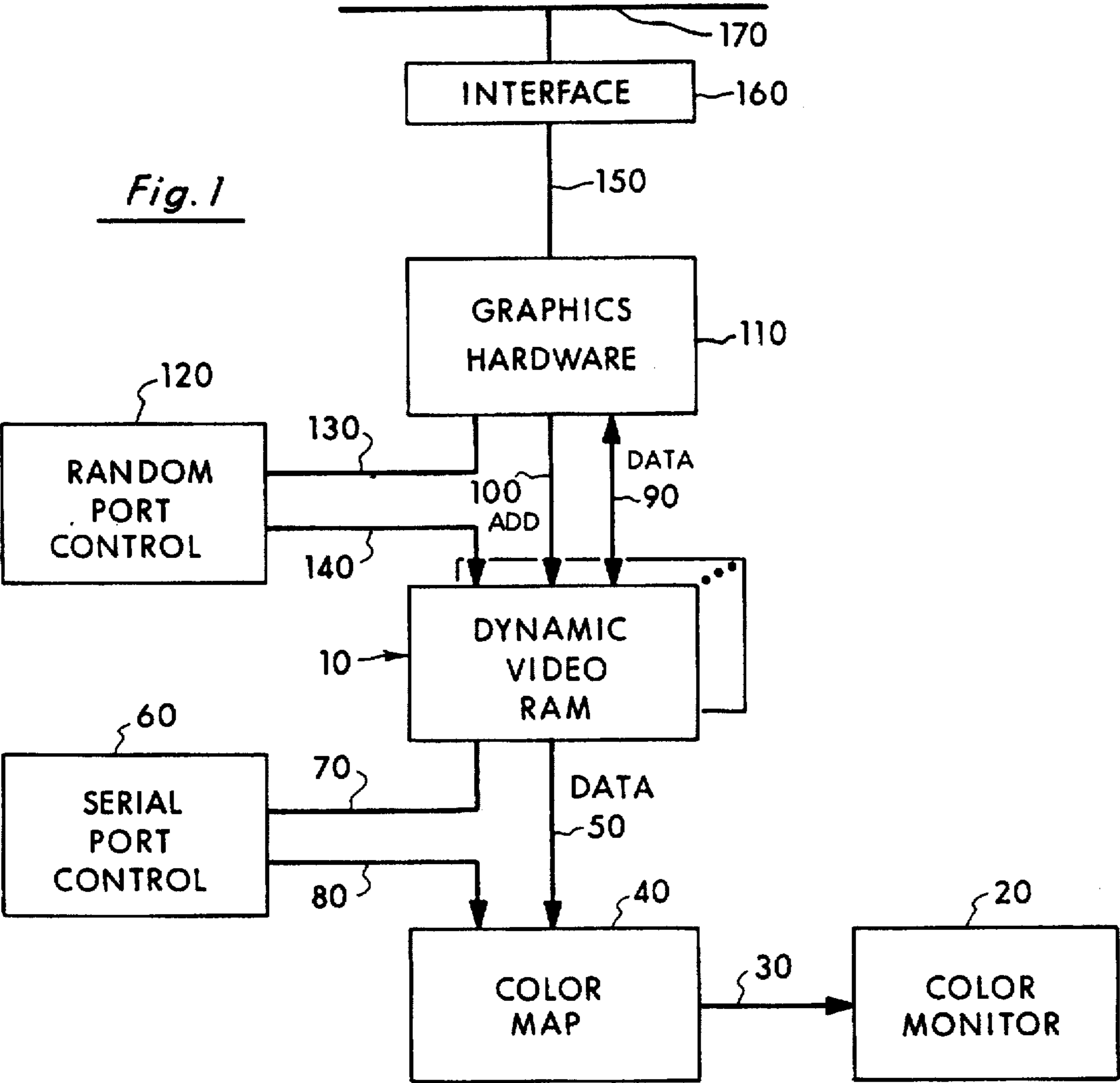
An architecture for a dynamic video random access memory on a single integrated circuit chip having internal circuitry for performing drawing or replacement rule logical operations on an addressed line of stored video information in the RAM and further having the write masking circuitry for modifying selected portions of the line of stored video information between selected START and STOP bit locations within the line.

54 Claims, 13 Drawing Sheets



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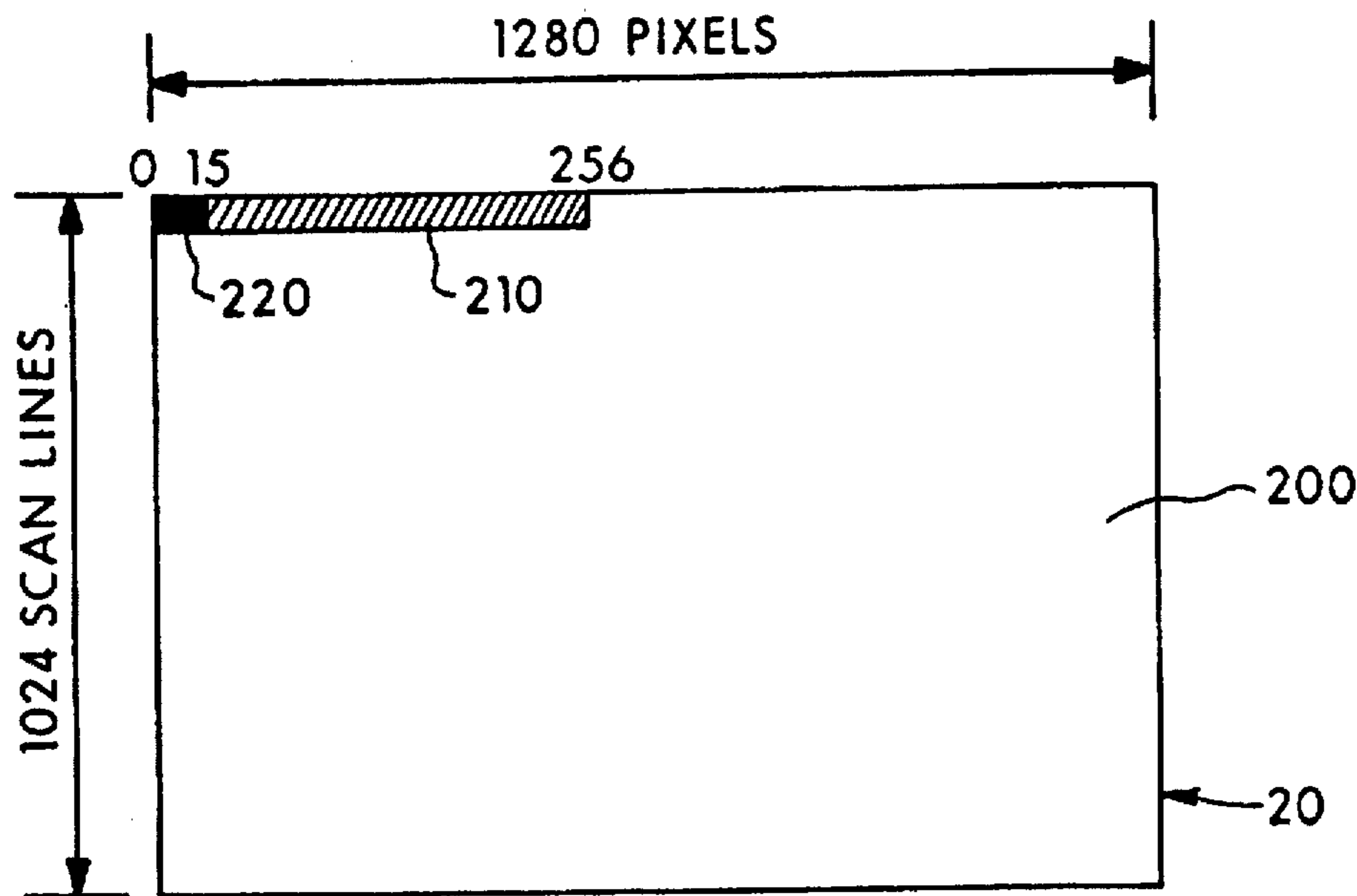


Fig. 2

Fig. 3

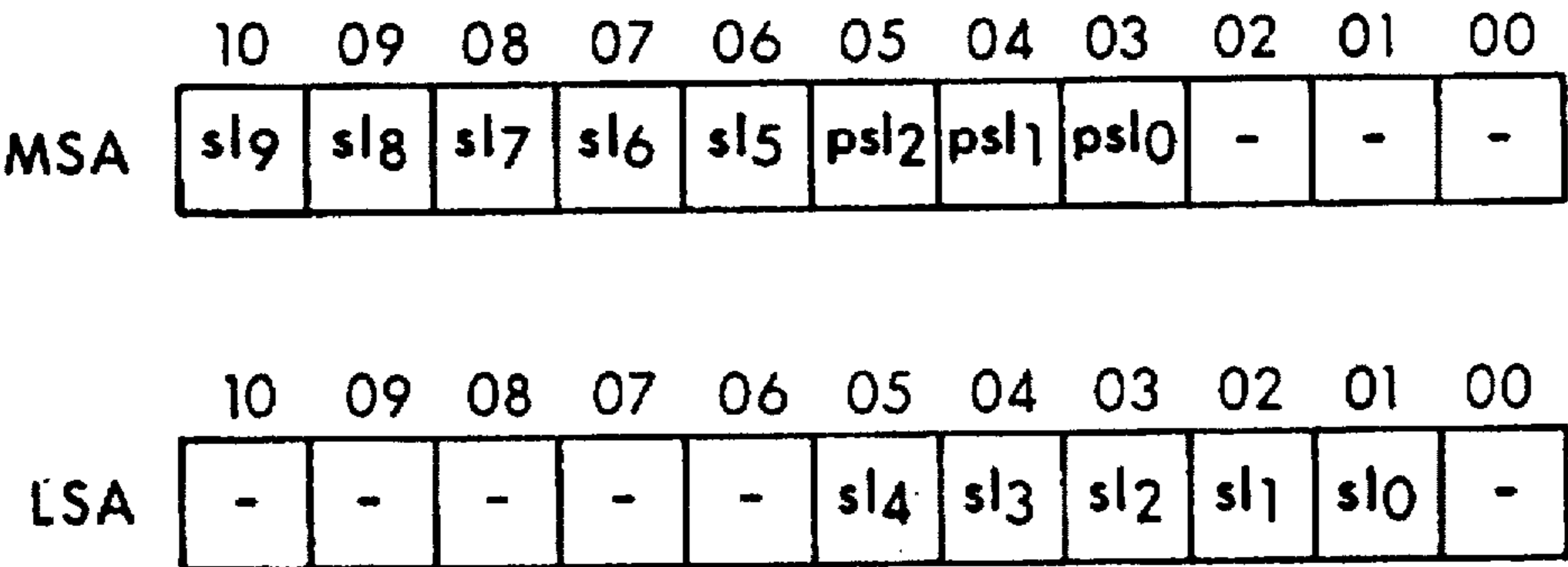
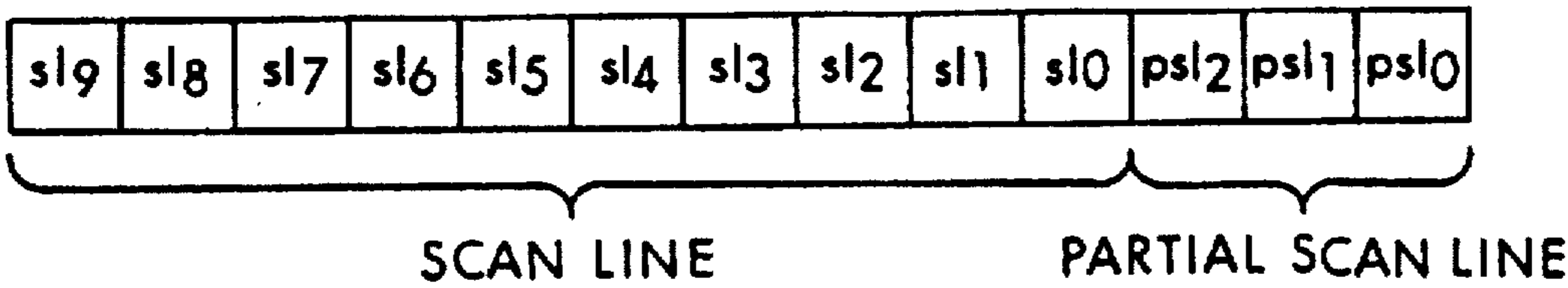


Fig. 4

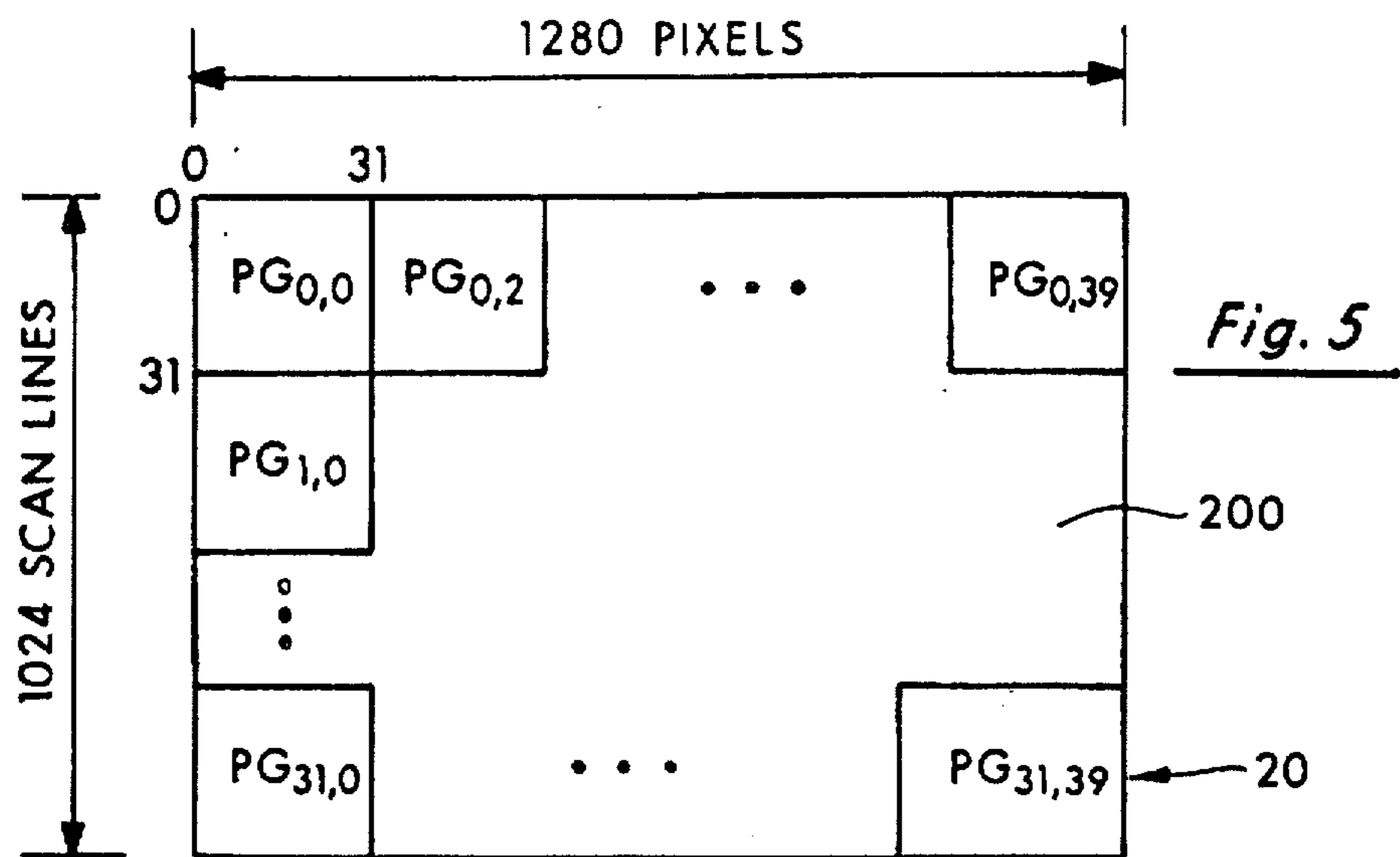


Fig. 5

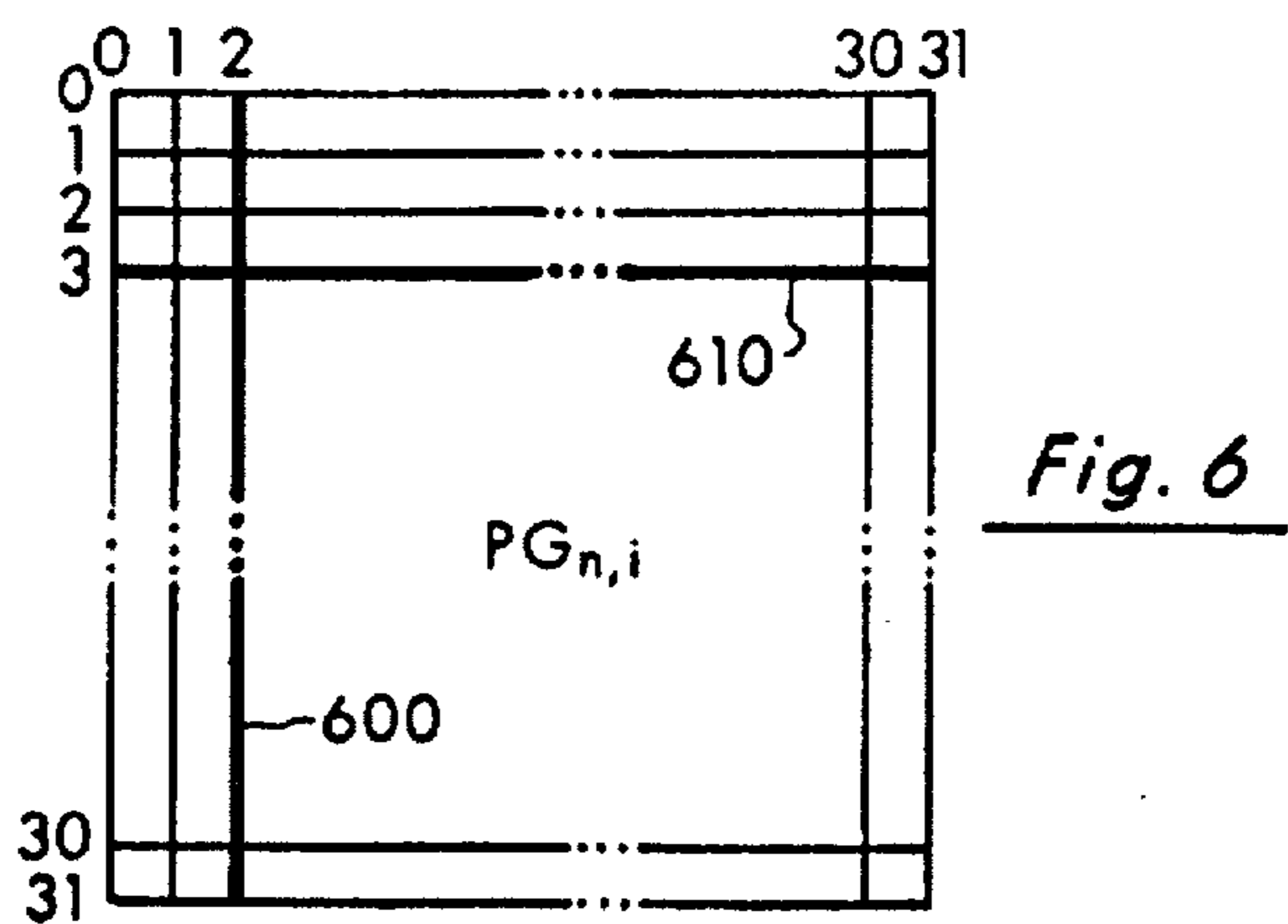


Fig. 6

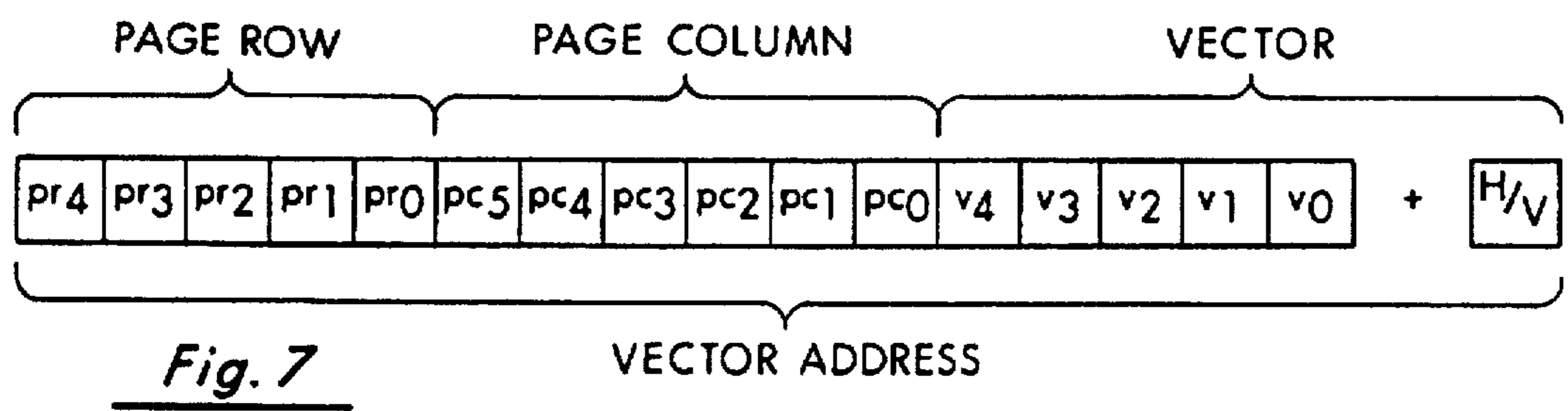


Fig. 7

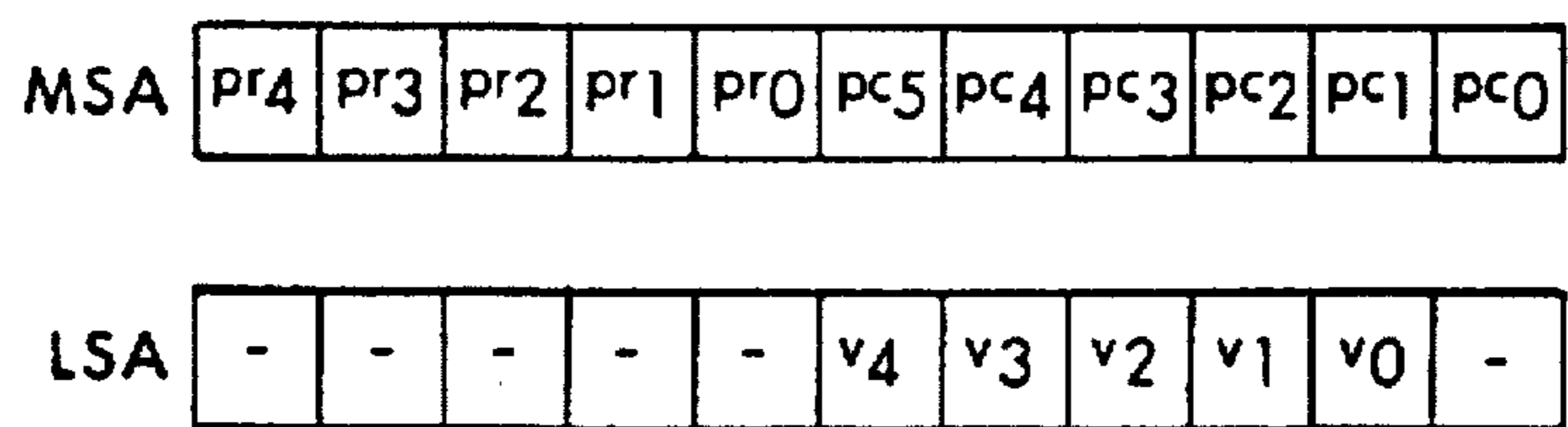


Fig. 8

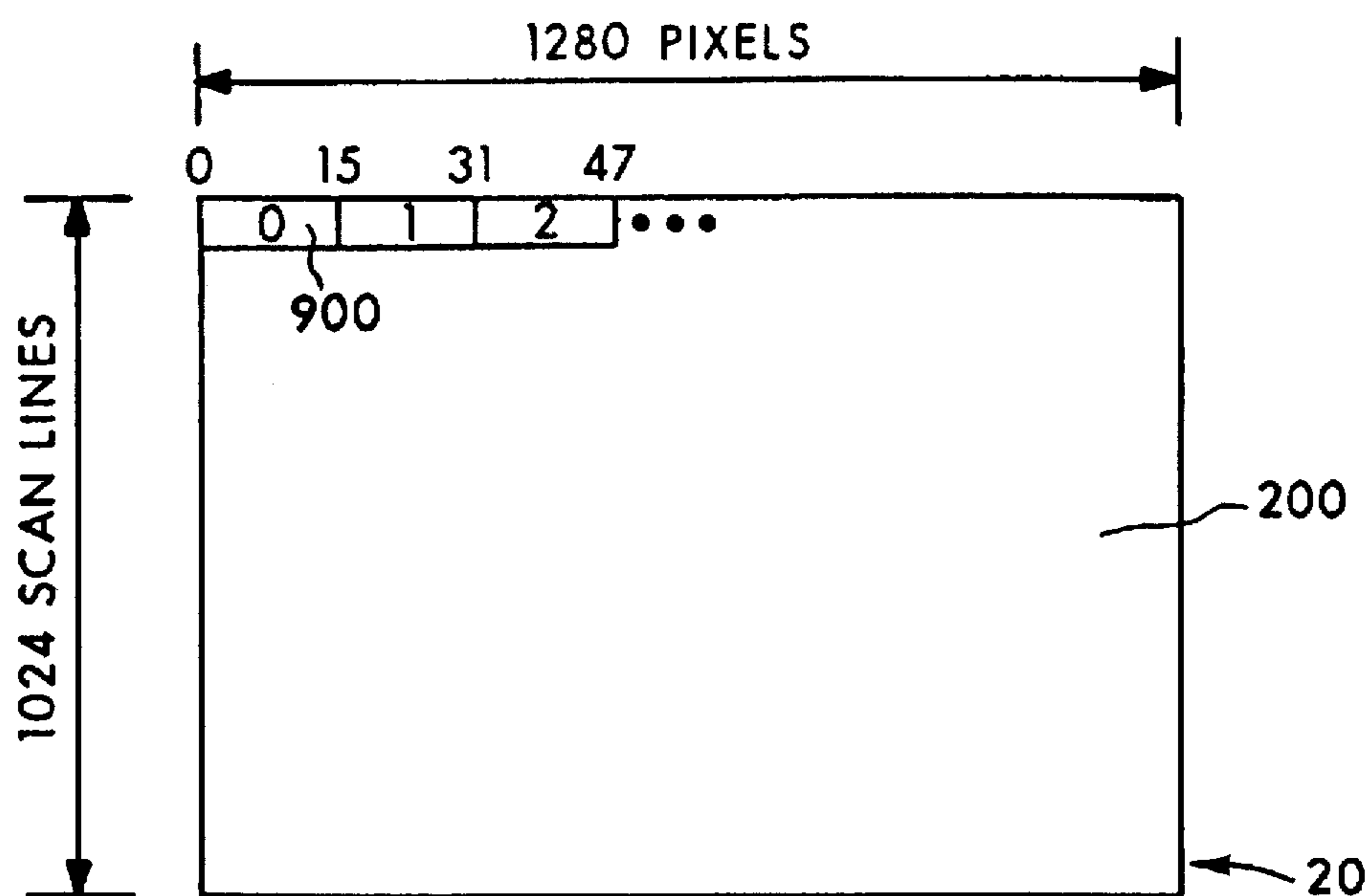


Fig. 9

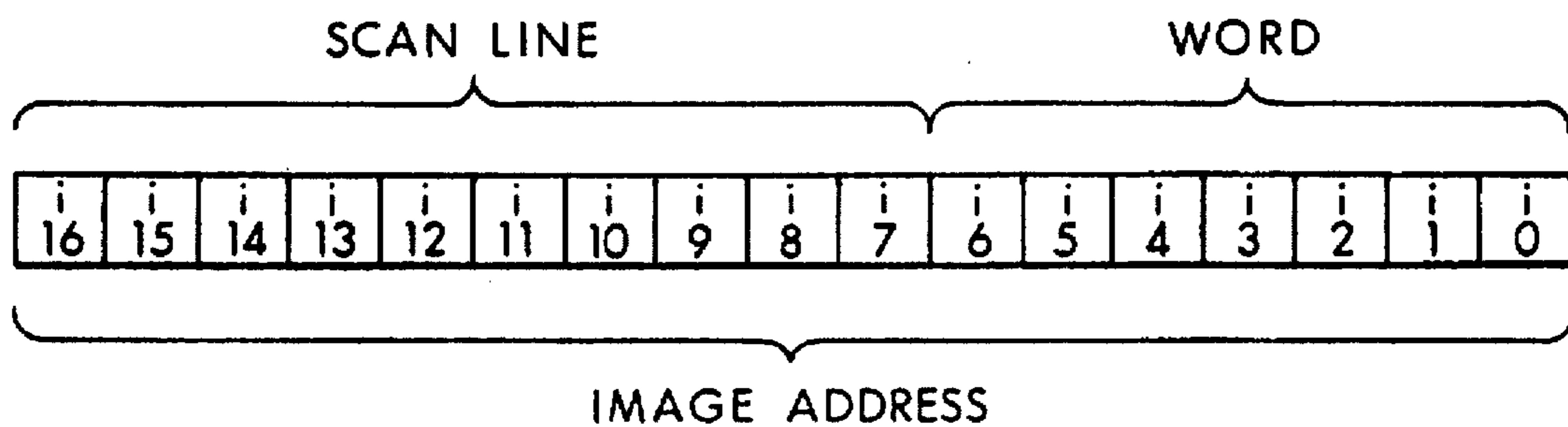


Fig. 10

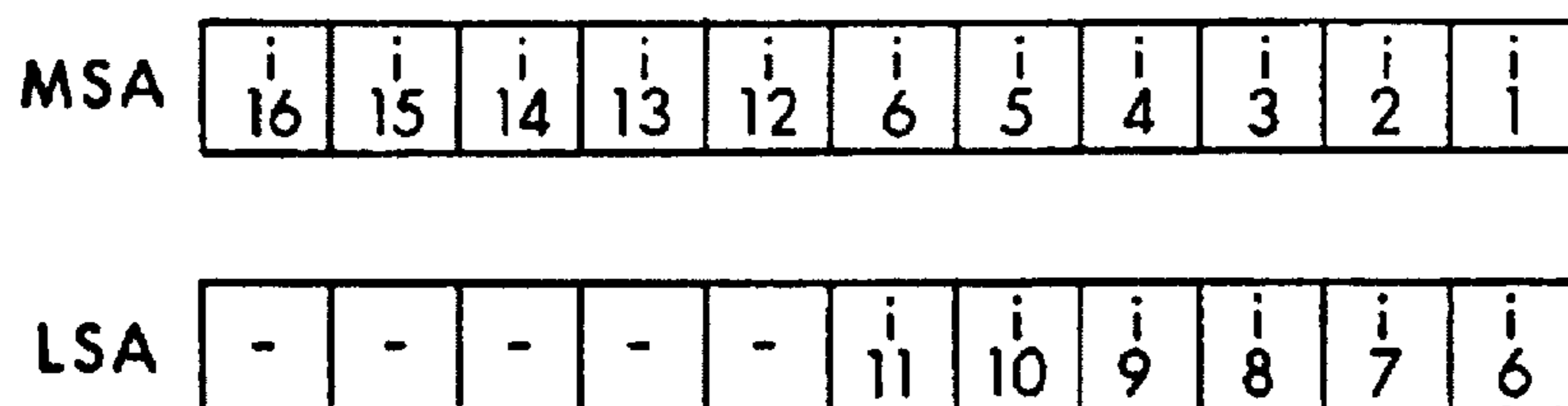
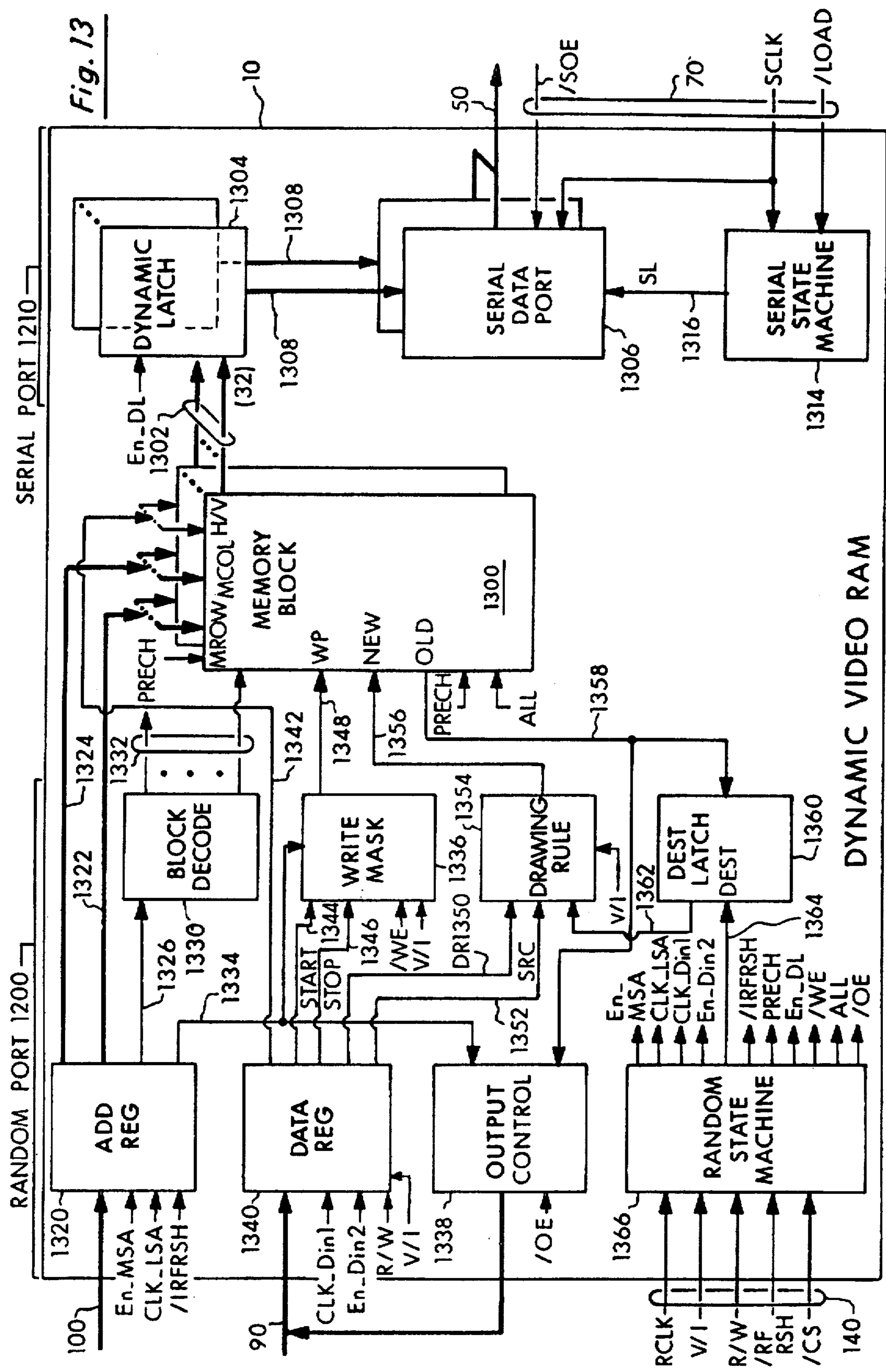
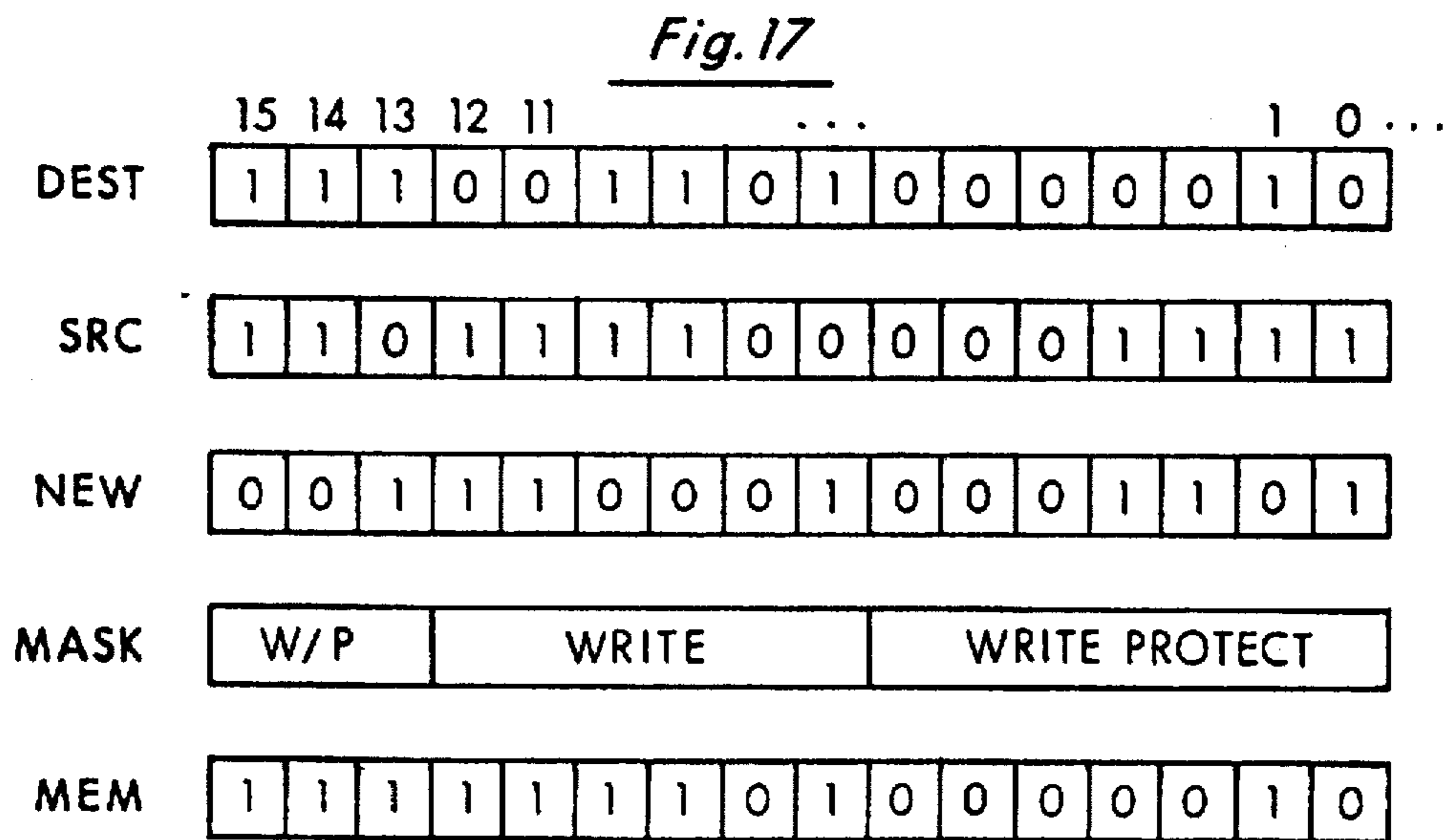
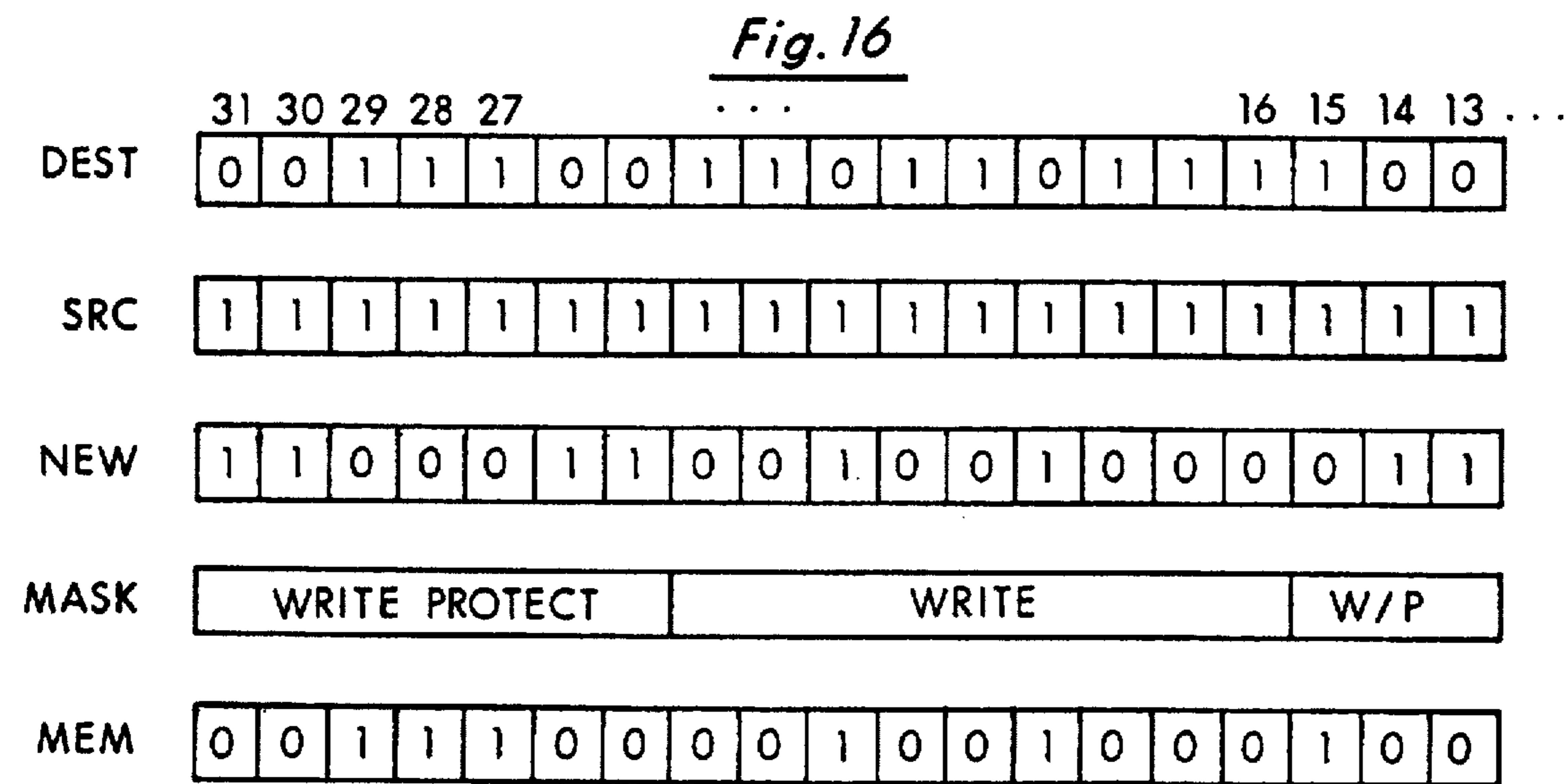
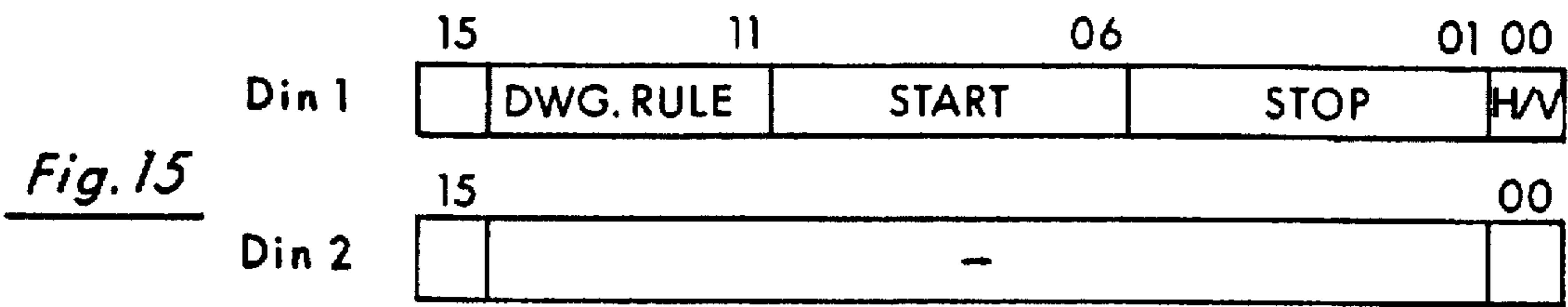
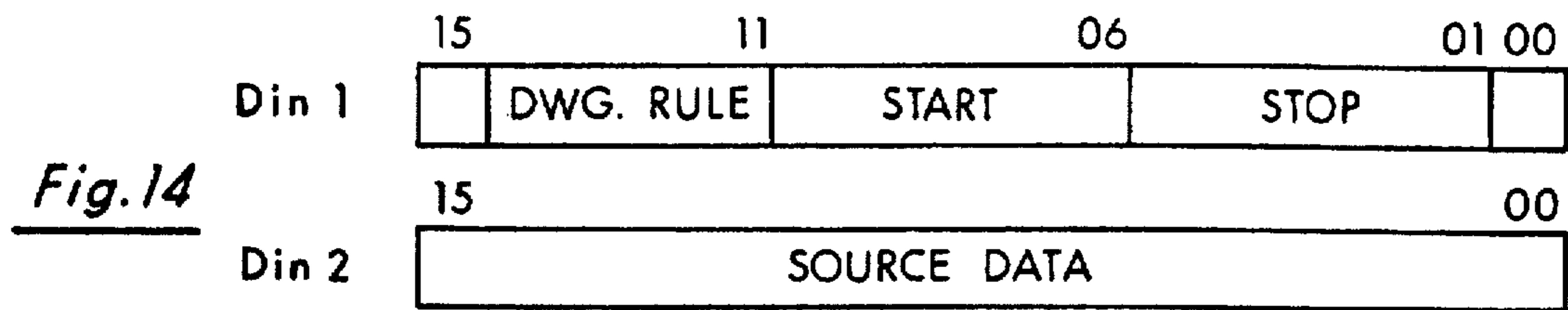


Fig. 11





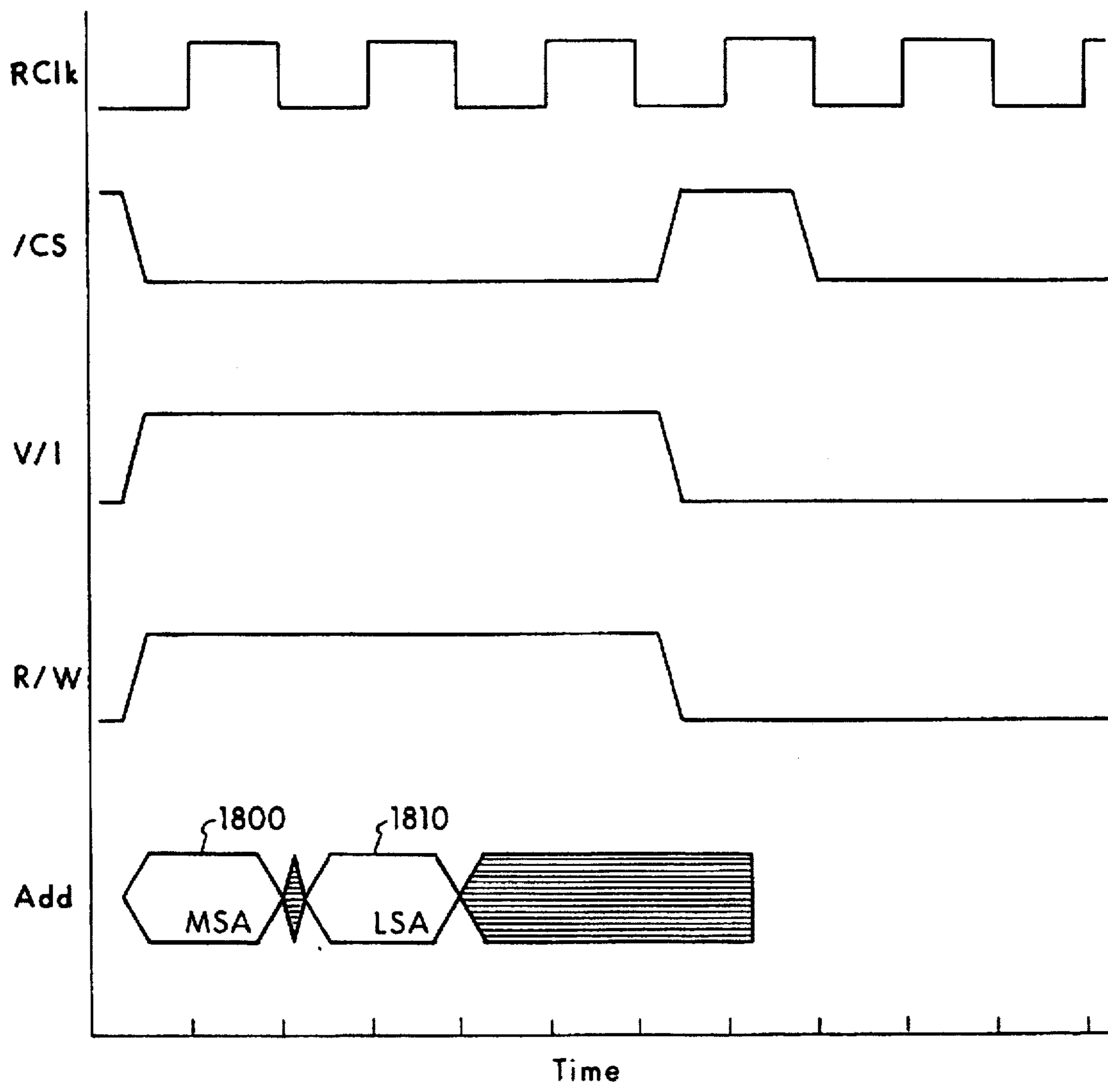


Fig. 18

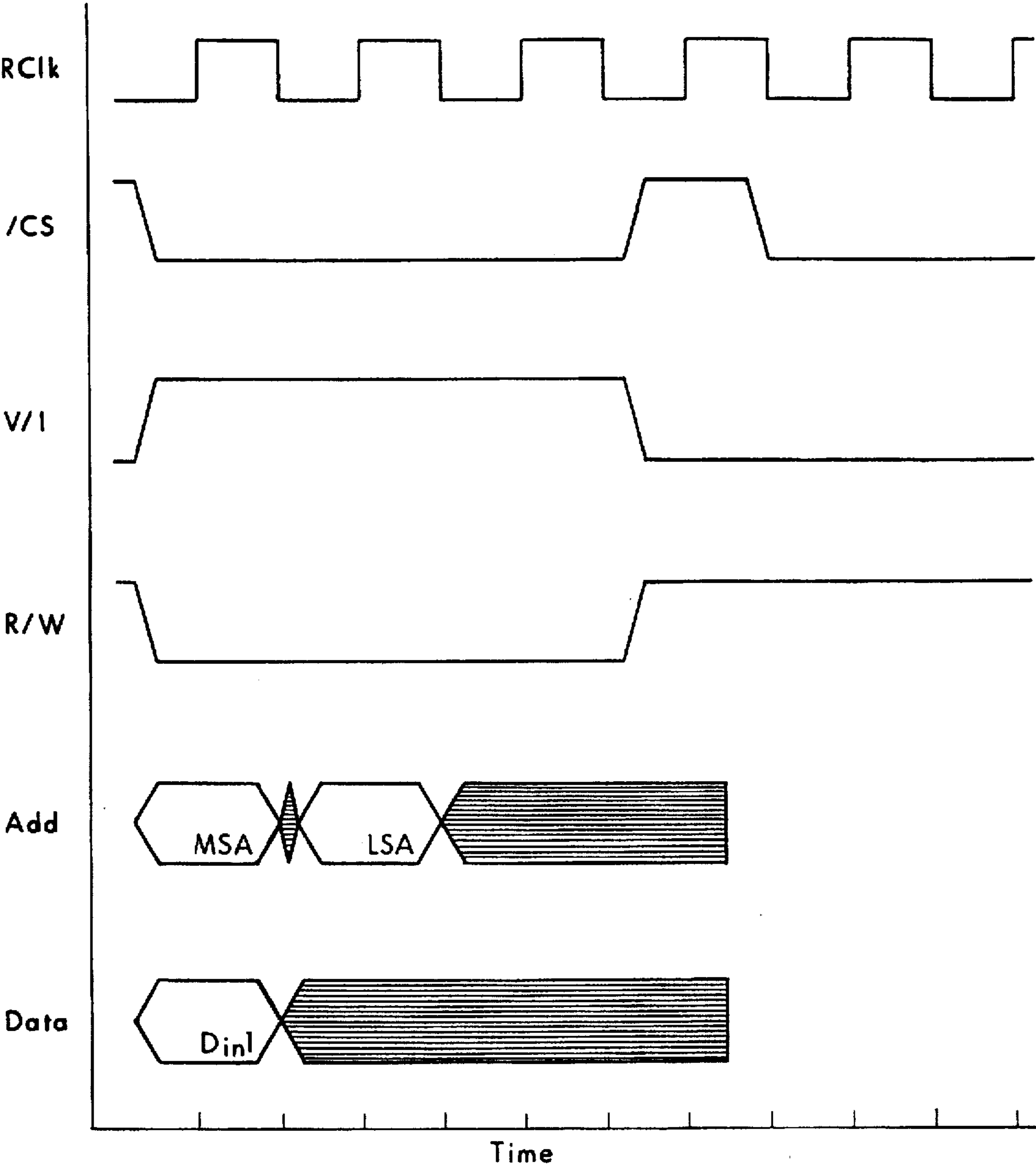


Fig. 19

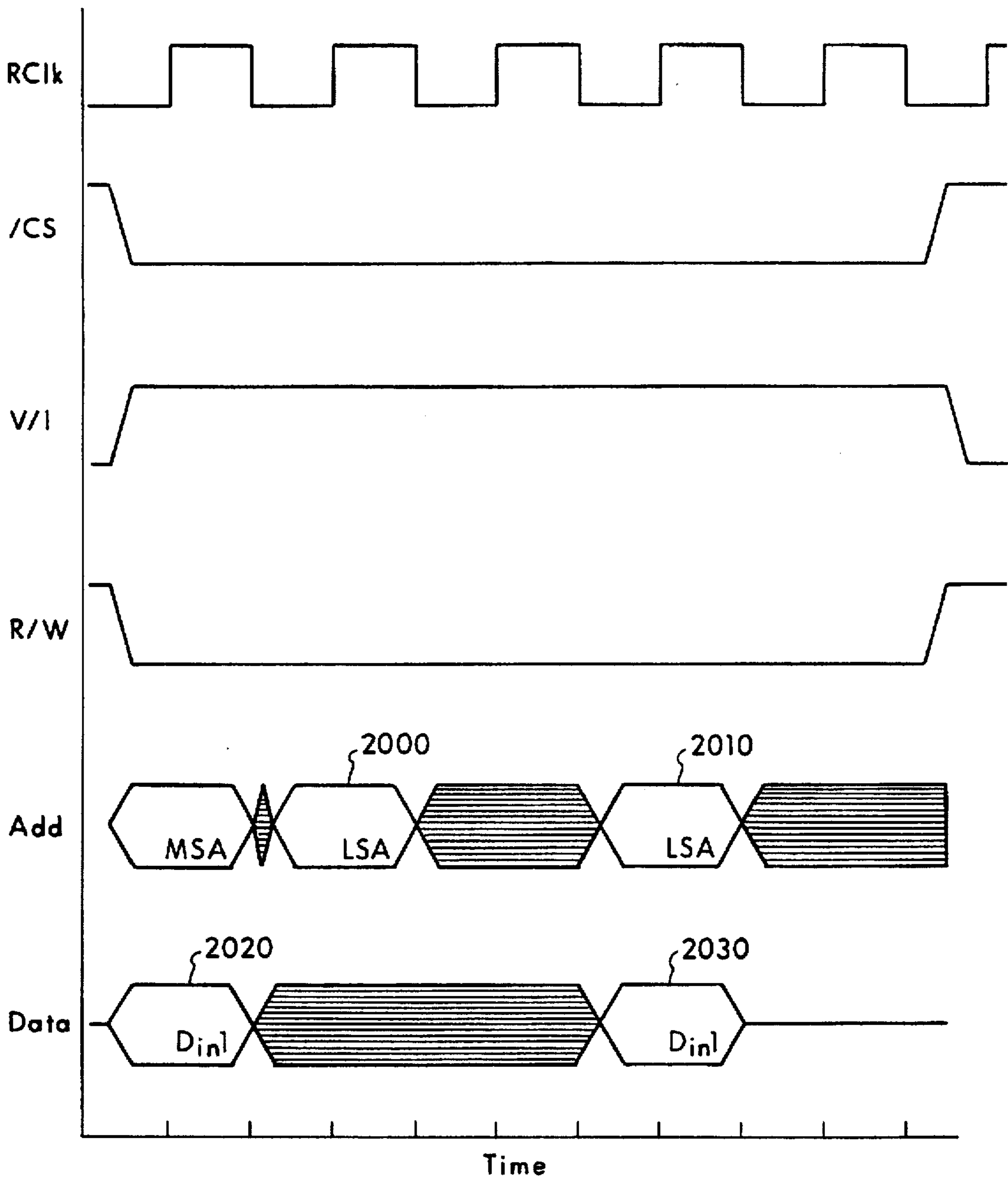


Fig. 20

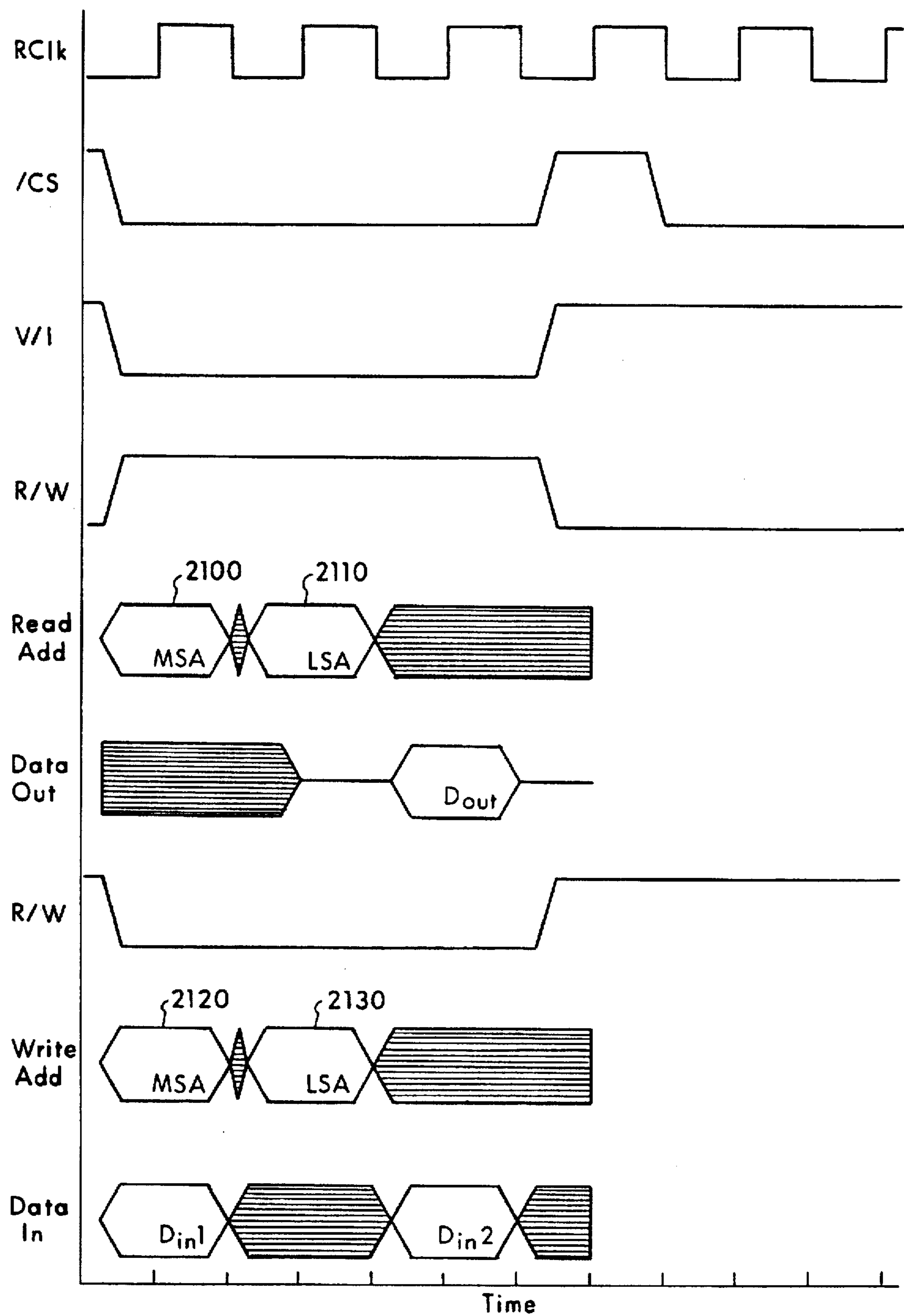
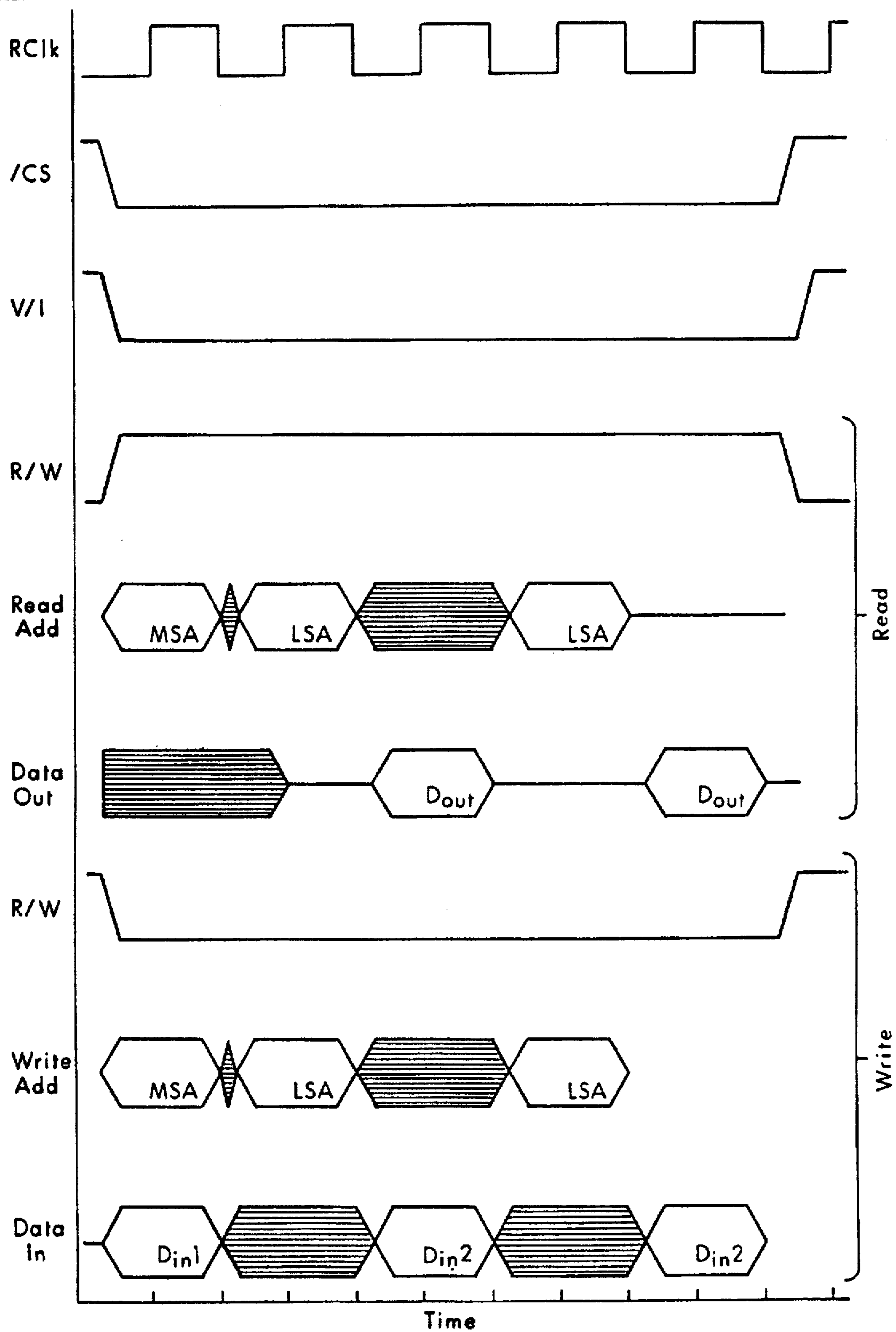


Fig. 21

Fig. 22



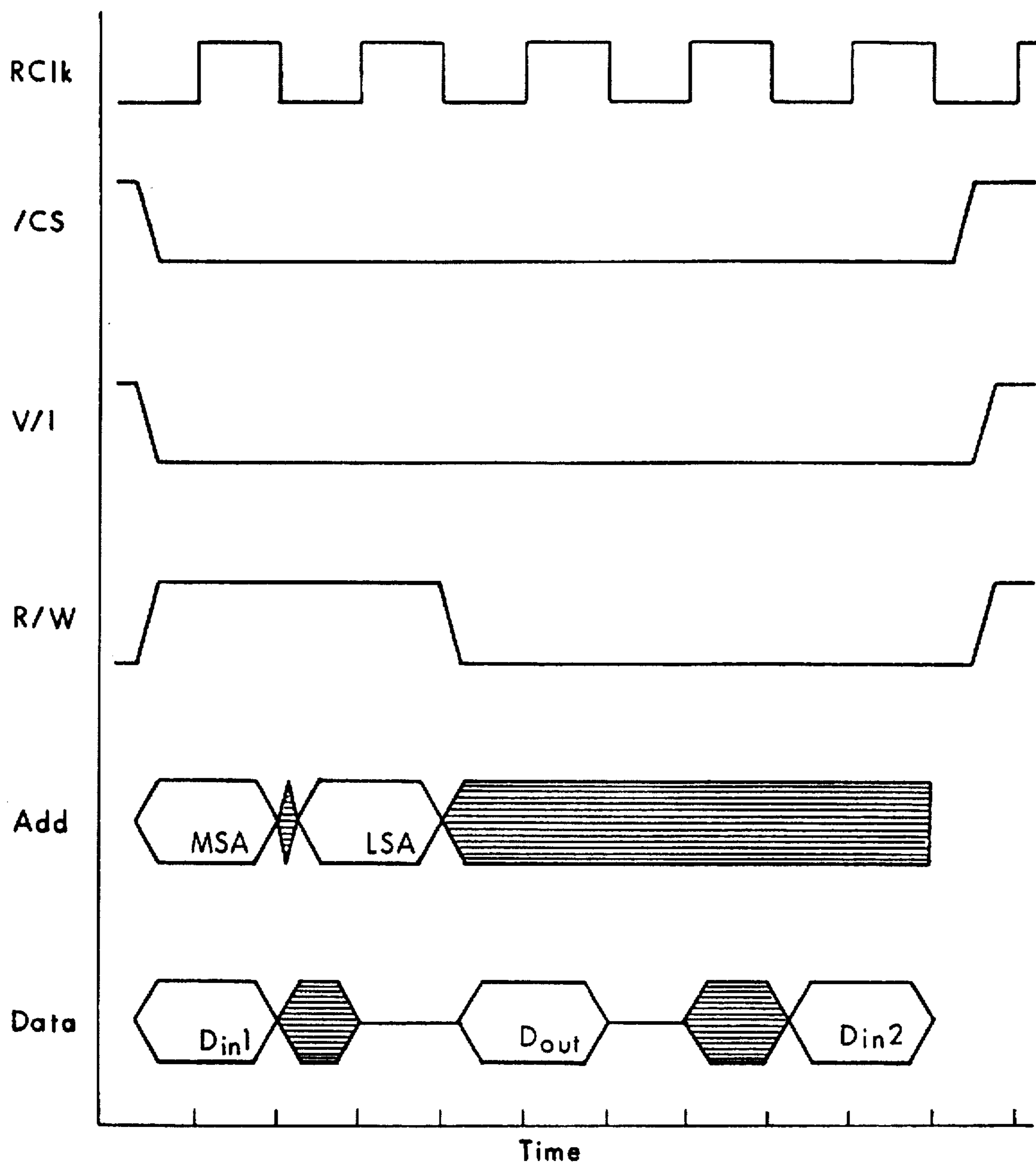


Fig. 23

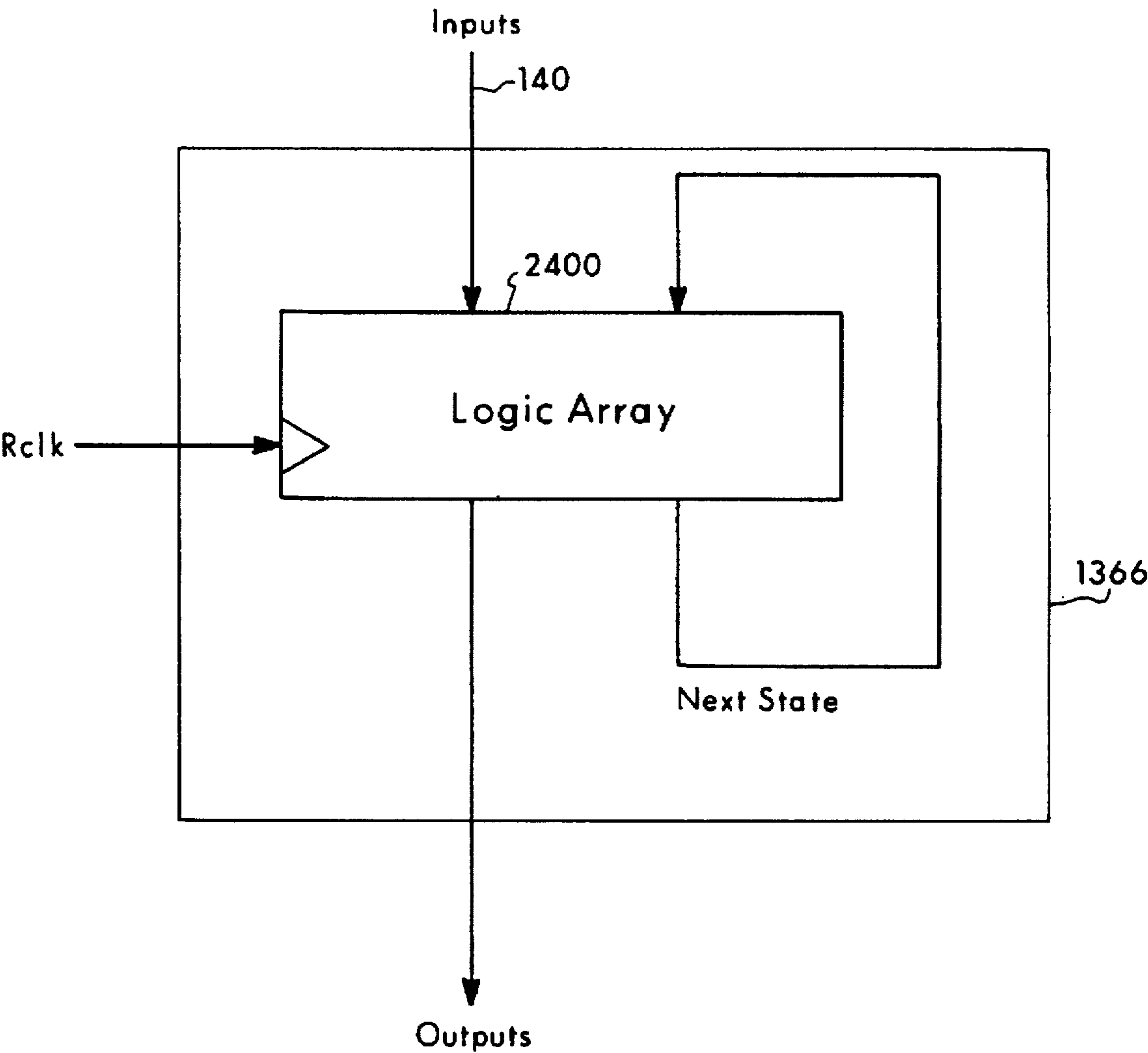


Fig. 24

DYNAMIC VIDEO RAM INCORPORATING ON CHIP VECTOR/IMAGE MODE LINE MODIFICATION

Matter enclosed in heavy brackets [] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

This application is a continuation of Ser. No. 08/306,180 filed Sep. 14, 1994, now abandoned, which is a reissue of Ser. No. 07/277,687 filed Nov. 29, 1988, now U.S. Pat. No. 5,148,524.

BACKGROUND OF THE INVENTION

Related Inventions

This invention is related to: Dynamic Video Ram Incorporating on Chip Vector/Image Mode Line Modification, Ser. No. 07/278,33, filed Nov. 29, 1988 and Dynamic Video Ram Incorporating Single Clock Random Port Control, Ser. No. 07/277,637, filed Nov. 29, 1988.

Field of the Invention

The invention relates to a dual ported, dynamic memory designed for the in raster scan graphic applications and, more particularly, to a high density dynamic video RAM incorporating to a single integrated circuit chip drawing or replacement logical rules as well as masking operations for the modification of a line of video information stored in the memory.

Statement of the Problem

With the cost per bit of semiconductor memory and the price of computer systems dropping, personal work stations and other computer systems using graphics such as CAD/CAM systems are becoming more readily available. A crucial component in such systems is the dynamic video RAM which supports the graphics applications.

Conventional dynamic video RAMS, available on multichips, have a random port and a serial port enabling a computer to access the dynamic video RAM through the random port and enabling the serial port to deliver the necessary graphics information to drive, for example, a color monitor.

In designing dynamic video RAMS, several features are of critical importance.

First, it is important to package the video RAM on a single integrated circuit chip while minimizing the number of external pins from the chip. Secondly, it is important to maximize the memory contained on the chip. Third, it is important to perform as many of the modification operations on chip, rather than having off chip hardware perform these operations at a much slower rate off the chip. Fourth, it is important to maximize the addressing capabilities of the data stored within the chip.

The following patents are representative of issued patents involving dynamic RAMs commercially available. In each of these patents, no provision is made for incorporating the drawing or replacement rules onto the chip carrying the RAM. Rather, in order to modify a given line of information stored in the RAM, the information to be modified must be read out from the dynamic video RAM and modified off chip according to the acquired logical operation. The present invention performs the drawing or replacement rule with circuitry located on the chip and further is able to selectively mask the areas of modified information to be read back into the RAM.

The 1987 patent issued to Novak, et al. (U.S. Pat. No. 4,688,197) sets forth a video computer system having a RAM chip with a shift register connected to its serial output terminal which is actuated by a first clock and a second clock is utilized to load the serial chip register. The 1987 patent to Redwine et al. (U.S. Pat. No. 4,689,741) pertains to the same invention as the '197 patent but provides for coupling of data between column lines and the chip register to prevent two or more different data bits from simultaneously appearing.

The 1987 patent to Thaden (U.S. Pat. No. 4,665,495) sets forth a single chip dynamic RAM controller and CRT controller system arrangement. This invention minimizes the control circuit of prior systems thus eliminating potential bottle necks at the RAM by utilizing a single controller. A related patent also issued to Thaden et al. is U.S. Pat. No. 4,656,596.

The 1985 patent to Bruce (U.S. Pat. No. 4,546,451) sets forth a dynamic RAM which permits "page mode" addressing.

The 1987 patent to Voss (U.S. Pat. No. 4,646,270) sets forth a video graphic dynamic RAM having the capability of serially reading out data at a high rate of speed while performing standard RAM operations.

There is no disclosure in any one of the above patents of circuitry to perform drawing rule modification on chip with the random access memory.

In the target specification of the Hitachi HM53462 Multi Port DRAM, logic operation and masking occur on a single chip. However, in this approach the system must first deliver the logic operation to the chip and then cycle to address the memory, deliver the new source data, read from memory and then modify the read information.

A need exists not only for providing the drawing rule and masking circuitry on the chip with the RAM but also to maximize the performance by delivering the drawing rule with the addresses to the chip at the same time.

Solution to the Problem

The present invention provides a solution to the above problem by placing on an integrated circuit chip the drawing rule and masking circuitry which is responsive to the delivery of the addresses and the drawing rule at the same time so that it can execute with each address cycle.

SUMMARY OF THE INVENTION

The present invention, in a preferred embodiment, is a 1,310,720 bit dual period, dynamic memory having random and serial ports. There is well over one million bits of stored information stored in the memory. The random port supports the two modes of access: a vector access to a 32 by 32 bit page and an image access to a 16 by 1 word. The serial port consists of eight, thirty-two bit dynamic latches providing 256 consecutive bits for a screen refresh. The dynamic video RAM of the present invention incorporates built-in drawing rule cycles, a clocked random port for synchronous operation, optimized vector operation and sixteen bit read and write access.

In the preferred embodiment, the video RAM is packaged on a chip where the random port is accessed by an eleven pin address, a sixteen pin data path, chip select, vector/image select, read/write signal and random port clock. The serial port is supported by the serial clock, serial output enable, load signal and four serial output data lines. The chip is powered by at least two Vcc and two Vss lines. While the preferred invention has at least forty-four pins on this chip, more pins could be added.

In the vector mode of operation, the dynamic video RAM of the present invention writes both horizontal and vertical vectors to a thirty-two by thirty-two bit page. The cells within a page in the preferred embodiment are addressed as a thirty-two bit vertical or horizontal vector column or row. However, the calls could be any desired selection such as "n"×"m." The address selects the page location of the vector and the row-column of the vector within the page. The data lines carry START and STOP locations within the page and the horizontal/vertical orientation of the vector within the cell. The drawing rule of the vector is also carried on the data lines with a source of the vector always defaulting to one. Once selected, a vector page can be accessed as a series of page mode cycles specifying column or row and START and STOP locations. In the preferred embodiment, vectors are write only.

Under the image mode of operation, the dynamic video RAM of the present invention allows the random access memory port array to be written and read directly. On writes, the address input of the address lines selects a thirty-two by thirty-two bit page, the page identical to that selected in vector mode. The row within the page is identical to the vector row selected while in the vector mode. The word is masked according to the START and STOP locations specified in the first data mode of the cycle. This first data word also carries the drawing rule specification. The second data word of the cycle carries the sixteen bit word image word. Reads are also sixteen bits wide and the address is specified in the write cycle, with the addition of the least significant address to control whether the least or the most significant word in the row is placed on the sixteen bit data bus. The START, STOP, and drawing rule have no effect on read cycles. Page mode works for both reads and writes, allowing the full thirty-two by thirty-two page to be accessed in one page cycle. The present invention provides a conventional internal refresh to the memory.

Finally, transferring data to the shift register is accomplished by executing a cycle with the vector/image line asserted to vector and the read/write line asserted to read. This places the contents of 256 cells in a dynamic latch ready to be loaded into the serial port register. While only 256 cells are written to an internal latch, the full 8,192 cells are accessed and refreshed during the serial data transfer. The 256 bits transferred during the transfer are refreshed to as a partial scan line and replacement rules have no effect on serial data transfer.

DESCRIPTION OF THE DRAWING

FIG. 1 is a block diagram of a system incorporating the dynamic video RAM of the present invention;

FIG. 2 illustrates the screen of the color monitor 20 of the system of FIG. 1 and a partial scan line;

FIG. 3 illustrates the serial data transfer address of the present invention;

FIG. 4 illustrates the most significant address and least significant address of the serial data transfer address of FIG. 3;

FIG. 5 sets forth the page layout of the screen of the color monitor 20 of the present invention;

FIG. 6 shows vectors within an individual page;

FIG. 7 is the format for a page address;

FIG. 8 shows the most significant address and least significant address bits of the page address of FIG. 7;

FIG. 9 shows the image mode addressing scheme of the color monitor of the present invention;

FIG. 10 shows the format of the image address;

FIG. 11 shows the most significant and least significant address portions of the image address of FIG. 10;

FIG. 12 illustrates the structure of a single chip of the dynamic video RAM of the present invention;

FIG. 13 sets forth the circuit block diagram of the dynamic video RAM chip of the present invention;

FIG. 14 sets forth the format of the data inputs for the image mode of operation;

FIG. 15 sets forth the format for the data inputs for the vector mode of operation;

FIG. 16 is an illustration of a vector mode operation;

FIG. 17 is an illustration of an image mode operation;

FIG. 18 shows the timing for serial data transfer;

FIG. 19 shows the timing for vector write;

FIG. 20 shows the timing for vector write, page mode;

FIG. 21 shows the timing for image read/write;

FIG. 22 shows the timing for image read/write, page mode;

FIG. 23 shows the timing for image read modify write; and

FIG. 24 sets forth an implementation of a random port state machine.

DETAILED SPECIFICATION

1. General Description

FIG. 1 sets forth the dynamic video RAM 10 of the present invention in a system environment having a color monitor 20 interconnected over lines 30 with a color map circuit 40. The color map circuit 40 is in turn connected over video data bus 50 to the dynamic video RAM 10 of the present invention. Both the dynamic video RAM 10 and the color map 40 are under control of a serial port control 60 over lines 70 and 80. The dynamic video RAM 10 is also interconnected over a data bus 90 and an address bus 100 to a graphics hardware circuit 110. A random port controller 120 controls the graphic hardware circuit 110 over lines 130 and the dynamic video RAM 10 over lines 140. The graphics hardware circuit 110 is interconnected over lines 150 to an interface circuit 160 which communicates with a standard bus 170.

The dynamic video RAM 10 of the present invention stores the image which is actually being displayed on the color monitor 20. The stored information in the video RAM 10 is delivered over the data bus 50, sequentially, to the color map circuit 40 for display on the monitor 20. The serial port control 60 controls the transfer of the stored information in the dynamic video RAM 10 to the color map 40.

When it is desired to change the stored information in the dynamic video RAM 10 in order to change the displayed image on the color monitor 20, appropriate commands come over bus 170 such as from a CPU or the like, not shown, and is received by the interface circuit 160 for delivery into the graphics hardware circuit 110. The random port control 120 controls the changing of the information stored in the dynamic video RAM based upon the information received by the graphics hardware from bus 150. The address for the information to be changed is delivered over address bus 100 and the data for the change is delivered over data bus 90. In this fashion, the dynamic video RAM information can be modified to change the image on the color monitor 20.

It is to be expressly understood that the system environment shown in FIG. 1 is for purposes of illustration only and

that the dynamic video RAM of the present invention could be utilized in other environments. For example, a color map and color monitor may not be present.

In the preferred embodiment of a single chip as shown in FIG. 12, the random port bus comprises an address bus 100 which is eleven bits wide, a data bus 90 which is sixteen bits wide and a control bus 140 which is five bits wide. The serial port bus comprises a data bus 50 which is four bits wide and a control bus 70 which is three bits wide. Hence, the dynamic video RAM 10 has thirty-nine pins plus four pins for power and ground for a total of forty-four. The present invention as set forth next, however, is not limited to a configuration having this number of pins. As shown in FIG. 1, a number of these single chips can be utilized in a system environment. The /CS control enable carried by control bus 140 selects which chip is accessed.

Three modes of addressing and operating the dynamic video RAM 10 over address bus 200 are present. They are (a) the serial data transfer mode, (b) the vector address mode, and (c) the image address mode. Each mode will be discussed in the following.

a. Serial Data Transfer Mode

In FIG. 2, the screen 200 of monitor 20 is shown. Screen 200 is conventional and may have, for example, 1280 pixels across the screen in a horizontal line with 1024 scan or raster lines in the vertical direction. It is to be expressly understood that any configuration of pixels and scan lines could be used under the teachings of the present invention. In FIG. 2, a partial scan line 210 is also shown. A "partial scan line" is defined herein to be 256 contiguous pixels in a scan line. A "word" is defined to be 16 pixels. Hence, a partial scan line contains 16 words. This corresponds to conventional image mode addressing found in other video RAM devices.

The dynamic video RAM 10 of the present invention is capable of being addressed over random port address bus 100 to perform serial port data transfers over data bus 50. In FIG. 3, the serial data transfer address is shown. The 1024 scan lines are selected by the ten bit scan line field and the partial scan lines 210 are selected by the three bit partial scan line field. A total of thirteen bits are required to perform serial data transfer addressing. Since address bus 100 is only eleven bits wide, two addresses are delivered as shown in FIG. 4. The first transfer being the most significant address (MSA) and the second transfer being the least significant address (LSA). Again, it is to be expressly understood that the present invention is not limited to this number of bits or to this configuration of addressing.

FIGS. 2-4, therefore, show the serial data transfer mode of addressing the dynamic video RAM 10 of the present invention.

b. Vector Addressing Mode

The present invention provides a mode of vector addressing wherein a page can be accessed either horizontally or vertically on the screen. This is shown in FIGS. 5-8.

A page is defined to be a 32 by 32 array of pixels. In FIG. 5, the part PG (0,0) has 32 horizontal scan lines by 32 vertical pixels. It is to be expressly understood that a page could be of any similar "m"×"n" configuration. The screen monitor of FIG. 5 has 32 times 40 or 1280 pages. The term "page column" is defined to be the horizontal location of a page and the term "page row" is the vertical location of a page. For example, for page PG (31,39), the page column is 39 and the page row is 31. The page row in the preferred

embodiment of 32 rows can be addressed by a 5 bit word. For example, the page row value for page PG (31,0) is 11111. Likewise, the 40 page columns, in the preferred invention of 1280 pixels can be addressed by a six bit word.

FIG. 6, shows an individual page PG (n,i). The term "vector column" identifies the vertical location of a vector within a page. For example, vector 600 is located in vertical row 2. The term "vertical row" is defined to mean the horizontal location at a vector within a page. For example, vector 610 is located in column 3. In the vector mode addressing scheme of the present invention, one bit, the H/V bit is used to define whether the vector is horizontal 610 or vertical 600. Five bits are then utilized to locate the vector within the page. For example, for the vector 610, the H/V bit equals 1 to designate a horizontal vector and the remaining 5 bits are 00011. The vertical vector 600 has the H/V bit set to 0 and the remaining 5 bits are 00010.

The vector addressing scheme shown in FIGS. 5 and 6 is unique to the present invention and permits not only a select page PG to be addressed but also to address a vertical or horizontal vector within the page.

Therefore, the necessary page address, as shown in FIG. 7 and in the preferred embodiment, is a 16 bit word having 5 bits to identify the page row, 6 bits to identify the page column, and 5 bits to identify the vector. The additional horizontal/vertical (H/V) bit identifies whether the vector is horizontal or vertical within the page. In this fashion, a specific vector such as either vector 600 or 610 in FIG. 6 in a selected page on the screen 200 can be addressed.

Since, the address bus 100 in FIG. 1 is 11 bits wide, the graphics hardware 100 outputs the vector address of FIG. 7 as two separate transfers. The first transfer being the most significant address (MSA) and the second address being the least significant address (LSA) both shown in FIG. 8.

It is to be expressly understood that FIGS. 5 through 8 set forth one approach under the teachings of the present invention and that, other bit layouts and address configurations could be used to accomplish the vector mode of addressing.

c. Image Address Mode

The present invention is also capable of conventional image mode addressing as shown in FIGS. 9-11. To locate a scan line on screen 200, would require 10 bits in the example shown of 1024 scan lines. A scan 1 defined as the set of contiguous pixels making up a complete scan line on a raster scan display. There are eighty 16 bit words in a scan line. Therefore, seven bits are required to locate a word in a given scan line. Hence, the image address as shown in FIG. 10 has 10 bits to identify the scan line and 7 bits to identify a word within the scan line. Because of the structure of the video RAM of the present invention, the address bus 100 as shown in FIG. 1 is limited to 11 bits and, therefore, as shown in FIG. 11, the image address is transferred in an MSA cycle and an LSA cycle. As discussed above, three modes of addressing occur on address bus 100. These three modes are serial data transfer (FIGS. 2-4), vector mode addressing (FIGS. 5-8) and image mode addressing (FIGS. 9-11) cause the video RAM of the present invention to operate in these different modes. The serial data transfer mode effectuates transfer of information from the RAM 10 over data bus 50. The vector and image modes permit changes to be made to the information stored within the RAM 10.

d. Chip Configuration

In FIG. 12, the dynamic video RAM 10 of the present invention is shown as a discrete single integrated circuit

chip. With reference back to FIG. 1, the random port side 1200 of the RAM 10 has the following pin designations:

- 1. Address Bus 100 (11 pins)
- 2. Data Bus 90 (16 pins)
- 3. /CS—chip select
- 4. V/I—Vector/Image Select
- 5. R/W—Read/Write Select
- 6. XRfrsh—Refresh
- 7. Rclk—Random Port Clock

On the serial port side 1210 of the dynamic video RAM 10 the following pins are designated:

- 1. Sclk—Serial Clock
- 2. /SOE—Serial Output Enable
- 3. /LOAD - Load Signal
- 4. Data Bus (4 pins)

In addition, two voltage, Vcc, pins and two ground pins, Vss, are required.

The chip select signal (/CS) selects which chip is being selected. For example, in FIG. 1, any number of chips 10 can be positioned within the system environment. If, for example, sixteen chips are required, then the appropriate /CS pin would be activated by the random port control 120.

As previously discussed, the vector-image signal (V/I) determines whether the chip is being addressed in the vector or image modes. In the preferred embodiment, when V/I is high, the chip is in the vector mode and when the V/I signal is low, the chip executes in the image mode.

The read/write signal (R/W) performs as follows. When R/W is high, the chip 10 is in the read mode and data appears on data bus 90. When R/W is low, the chip is in the write mode and the data is written into the memory found within chip 10. The following modes of operation occur within the chip 10:

TABLE I

V/I	R/W	Cycle
0	0	Image write
0	1	Image read
1	0	vector write
1	1	serial data transfer

The random port clock (Rclk) is a single clock signal delivered to the chip 10. All internal random port operations of the chip 10 are synchronized with and derived from this clock signal. This is the only clock signal to the random port.

The address signals on random port bus 100 carries the bit addresses for the MSA and LSA addresses as shown in FIG. 4 for serial data transfer. In FIG. 8 for vector mode addressing, and in FIG. 11 for image mode addressing.

The data appearing on random port data bus 90 is sixteen parallel bits and is delivered into the chip 10 as two sets of data—Din1 and Din2. This is shown in the following table:

TABLE II

Mode	Din1	Din2
Vector	DR, Start/Stop, H/V	—
Image	DR, Start/Stop	Read or Write
Data	—	—

(Where DR=Drawing Rule, H/V=Horizontal/Vertical)

Also delivered to the RAM 10 of the present invention from the random port control 120 is a /Refresh which is used as an internal refresh signal. The RAM 10 of the present

invention also receives control signals from the serial port control 60 over serial port control bus 70. The Sclk signal is a single serial port clock, the /SOE is a serial output enable signal. When /SOE is low, serial read data appears on the data bus 50. The /LOAD is a data load signal. The present invention only uses a single clock on the serial port 1210 to transfer data over the serial port.

The two Vcc pins shown in FIG. 12 provide power which in the preferred embodiment is plus five volts and the Vss pins are two ground pins. More or less than two pins for power and ground can be used under the teachings of the present invention.

The single integrated chip shown in FIG. 12 contains in the random port 1200 and in the serial port 1210 all of the necessary circuitry to operate the RAM in the three modes of operation (Serial data transfer, Vector addressing and Image Addressing). The random port is controlled through receipt of one of a plurality of sets of control enables over bus 140 which configure the RAM to operate in its various modes of operation. The delivery of the single clock Rclk then is used to produce the necessary internal control enables to execute the selected mode of operation.

The signals appearing on the pins shown in FIG. 12 will now be discussed in the following detailed description of the internal configuration and operation of the dynamic video RAM 10 of the present invention. It is to be expressly understood that the pin number and selection represents only a preferred embodiment and that other embodiments may be designed within the teachings of the present invention.

2. Detailed Description

This section discusses the detailed structural embodiment of the dynamic video RAM chip 10 of the present invention and the preferred operation. The individual register, latch, shift, and other disclosed circuits are individually conventional in operation and design. The combined circuit layout, however, is unique and while one preferred layout is shown, it is to be expressly understood that other layouts based upon the teachings of this invention could be used.

a. Serial Port Side 1210 Configuration

The components of the dynamic video RAM 10 of the present invention are set forth in FIG. 13 to include a plurality of memory blocks 1300. Each memory block 1300 is, in the preferred embodiment, 160 memory cells by 1024 memory cells. There are 8 memory blocks for a total of 1,310,720 cells on a single chip although it is to be expressly understood that any number could be used.

The output from the memory block 1300 is delivered over lines 1302 into a plurality of dynamic latches 1304. Each dynamic latch stores 32 bits of information as read from its respective interconnected memory block 1300. The eight latches, therefore, hold 256 bits or a partial scan line. The output of each dynamic latch 1304 is delivered to a respective serial data port register 1306 over interconnecting line 1308. Each serial data port 1306 contains a 32 bit register which is capable of delivering 4 bits, in a serial fashion, onto data bus 50 for delivery, for example, into the color map 10 as shown in FIG. 1. The control signals 70 from the serial port control 60 are delivered into the serial state machine 1314. Which is interconnected over lines 1316 to the serial data port in order to control the serial reading of information from the memory block 1300.

Hence, the dynamic latch 1304, the serial data port 1306, and the serial state machine 1314 constitute the serial port side 1210 of the dynamic video RAM 10 of the present invention.

b. Random Port Side 1200 Configuration

The random port side 1200 includes an address register 1320 which is interconnected to the random port address bus 100 and is further connected over lines 1322 (eight bits) and 1324 (five bits) to the memory block 1300. The address register 1320 is also interconnected over lines 1326 (three bits) to a block decode circuit 1330 which is interconnected over lines 1332 to the memory block 1300. The address register is also interconnected over line 1334 to the write mask 1336 and to the output control 1338.

The data register 1340 is interconnected to the data bus 90 and is further interconnected over line 1342 (H/V bit) to the memory block 1300, over lines 1344 (START - five bits) and 1346 (STOP - five bits) to the write mask 1336. The write mask 1336 is further interconnected over lines 1348 (32 bits) to the memory block 1300. The data register 1340 is further interconnected over lines 1350 (four bits) and 1352 (sixteen bits) to the drawing rule circuit 1354 which in turn is interconnected over lines 1356 (thirty-two bits) to the memory block 1300.

The output control 1338 is also interconnected to the random port data bus 90 and is also interconnected over lines 1358 to the memory block 1300. Destination latch 1360 is also connected to lines 1358 and is further connected over lines 1362 (thirty-two bits) to the drawing rule circuit 1354 and over line 1364 to the random state machine 1366. The random state machine 1366 receives the random port control input signals over random port control bus 140.

Hence, the address register 1320, the block decode circuit 1330, the data register 1340, the write mask 1336, the output control 1338, the drawing rule circuit 1354, the destination latch 1360, and the random state machine 1366 constitute the random port side 1200 of the dynamic video RAM 10 of the present invention. While a preferred embodiment of the present invention is shown, variations to the design could be made under the teachings of the claimed invention. For example, the latch 1360 could be designed using strobed combinational logic to deliver or hold the stored video information.

Serial Port Side 1210 Operation

The operation of the dynamic video RAM of the present invention will first be discussed with respect to the operation of the serial data transfer mode of operation wherein the information contained within the memory block 1300 is issued to generate the image, for example, on the color monitor 20 of FIG. 1. This scan line transfer mode of operation utilizes the addressing techniques shown in FIGS. 2-4.

In the timing and control diagram of FIG. 18, the Rclk, /CS, V/I, and R/W enables are delivered over random port control bus 140 from the random port control 120. The address, ADD, is delivered over bus 100 from the graphics hardware 110. The /CS signal selects which dynamic video RAM chip 10 is being activated. In this mode of operation, i.e., serial data transfer, the R/W bit is high to read the memory 1300. When a serial data transfer occurs the V/I bit, set high (see Table I) (i.e., vector or image) is also selected and as shown in FIG. 18, the vector mode is selected. Hence, the address (MSA and LSA) of the data to be transferred from the memory 1300 to the dynamic latch 1304 is contained on bus 100—see FIG. 4. The single clock signal Rclk causes the random state machine 1366 to input the address (MSA and LSA) into the address register 1320 during a first time interval (i.e., at times 1800 and 1810) as shown in FIG. 8. When it is desired to read the memory block 1300 so that

the contents can be serially delivered to the color map 40, the transfer of the addressed partial scan line for a screen refresh occurs in the following manner. Thirty two bits of information from each of the eight memory blocks 1300 are read over lines 1302 into the dynamic latches 1304. The dynamic latch 1304 receives a signal over line En-DL from the random state machine 1366 indicating that it is to read the data from the memory block. All eight dynamic latches are so enabled and each will read in 32 bits for a 256 bit partial scan line. After reading, EN-DL is appropriately activated to deliver the read information over lines 1308 into the serial data port 1306. Again, this is a parallel transfer of 32 bits of information for each of the eight serial shift registers. Each of the eight serial data ports 1306 is under control of the serial state machine 1314 and the serial clock Sclk. When the serial data port 1306 is enabled over line SL, each clock signal transfers out four bits from a given serial data port 1306 to data bus 50.

The transfer of the data occurs in the following fashion. Serial state machine 1314 has a counter contained therein which counts the serial clock pulses Sclk. Hence, as the Sclk pulses come in, they are delivered to the serial data port 1306 which after eight such pulses sequentially gates out the 32 bits stored therein, four bits at a time. Then, the next eight Sclk pulses transfer the 32 bits out from that next memory block portion. In this fashion, the serial state machine 1314 is capable of causing the serial data port to transmit the stored data from each of the memory blocks until a partial scan line is transmitted. After a partial scan line is delivered, a /LOAD signal is received over serial port control bus 70 to the serial state machine 1314 and over line 1316 to load all of the serial data port with the data for the next partial scan line. The /SOE input to serial data port 1306 enables the multiplexer to deliver the information four bits at a time to the color map 40.

It is to be expressly understood that other conventional configurations for the serial port could be utilized under the teachings of the present invention. The serial port is asynchronous from the random port and can transfer data over bus 50 while the chip 10 is performing other operations.

d. Random Port Side 1200 Operation

The operation of the random port 1200 of the dynamic video RAM 10 will now be explained.

The term "drawing rule" is defined to be a logical operator combining a "source" and a "destination" upon write to the memory block 1300. Drawing rules, in the preferred embodiment, are specified by the following table:

TABLE III

Drawing Rule	Product
0000	clear (all source)
0001	source and destination
0010	source and (not destination)
0011	source
0100	(not source) and destination
0101	destination
0110	source not destination
0111	source or destination
1000	source not destination
1001	source user destination
1010	not destination
1011	source or (not destination)
1100	not source

TABLE III-continued

Drawing Rule	Product
1101	(not source) or destination
1110	source read destination
1111	not (all once)

The operation of this table will be discussed in the following. In addition, the present invention incorporates two data cycles termed Din1 and Din2. In FIG. 14, Din1 and Din2 are shown for the image mode of operation. FIG. 15 shows Din1 and Din2 for the vector mode of operation.

Under the teachings of the present invention, the drawing rule function is incorporated directly in the dynamic video RAM chip 10. This permits faster modification of data within the memory block 1300. Conventional video RAM designs require that the information in the memory block be read out of the video RAM chip and be modified in another chip or circuit. After modification off the chip, it is rewritten back into the memory block. This is a slow process.

Under the teachings of the present invention up to 32 pixel elements can be changed in one operation. Conventional approaches are the image mode of operation whereas the present invention also incorporates the vector mode of operation wherein a horizontal or vertical vector in a defined page can be modified and changed according to the selected design rule. This feature significantly speeds up the time for modification of the information contained in the memory block. For example, if under a conventional approach, a vertical line from screen 200 is to be modified, a number of horizontal scan lines would have to be read out of the memory in order to modify the one bit corresponding to the vertical line. Under the teachings of the present invention, only one vertical vector would have to be accessed and modified significantly increasing the performance of the system over conventional approaches. It is estimated that current video RAM systems can process these vectors at the rate of 300,000 to 700,000 vectors per second. Under the teachings of the present invention, three to four million horizontal and vertical vectors per second can be processed.

The speed up is due to the provision of the vector write mode of operation as will be discussed in the following. In the vector write mode of operation, the MSA and LSA addresses of FIG. 8 are sequentially loaded into the address register 1320. This is shown in the timing diagram of FIG. 19 where the /CS selects the proper chip, the V/I lead is high to select the vector mode, and R/W is low for write. Hence, the MSA and LSA of the address (FIG. 8) are loaded into the address register 1320 as well as the drawing rule, start, and stop (FIG. 15) over the random port data bus 90 into the data register 1340. The vector address (MSA and LSA) and the data (Din1) is delivered during a first time interval.

In FIG. 20, the timing for vector write, page mode is shown. Here, the MSA remains the same whereas the LSA and the Din are changed at times 2000 and 2010 for the LSA and times 2020 and 2030 for the Din1. The MSA and LSA addresses containing the page row, page column and vector identification of FIG. 8 and are stored into the address register 1320. Eight outputs are delivered over lines 1322 to address the memory row of memory block 1300, five of the bits are delivered over lines 1324 to address the memory column of memory block 1300, and the three remaining bits are delivered over lines 1326 to the block decode circuitry 1330. The block decode circuitry 1330 is simply a one out of eight decode to selectively activate one of the eight memory blocks 1300.

In the vector mode of operation, Din1 as shown in FIG. 15 is read into the data register 1340 over data bus 90. Din2 is not used in this mode. The five START bits are delivered over lines 1344 to the write mask 1336 and the five STOP bits are delivered over lines 1346 to the write mask 1336. The four drawing rule bits are delivered over lines 1350 to the drawing rule circuit 1354. The H/V bit is delivered from the data register 1340 over line 1342 to the memory block 1300.

The address register is of conventional register design that enables data to be read from a bus and to store the information in the register. The address register is enabled to read the most significant address by the MSA enable and the least significant address by the LSA enable. Likewise, the data register 1340 is of conventional design and reads in data from the data bus 90 and stores it internally upon being selectively enabled by the Din1 and Din2 enable lines. At this point and time, the address register 1320 and the data register 1340 have the necessary vector information to identify either a horizontal or vertical vector to perform a drawing rule operation on it. Other circuits could be designed to perform the above described address and data functions.

In reference back to FIGS. 5-8, it is seen that a selected vertical 600 or horizontal 610 vector is composed of 32 pixel elements or when resident in the memory block 1300, 32 memory cells. The START and STOP information conveys the precise portion of the vector to be modified according to the drawing rule. For example, if the desired place to start the modification within a vector is seven bits from the start of the vector, the START command would be 00111 and if the STOP location is the fifteenth bit, the STOP command would be 01111. The START and STOP information is delivered to the write mask which provides 32 possible write protect WP signals over lines 1348. Hence, in our example of starting at location 7 and stopping at location 15 in a 32 bit vector, the first seven bits would be activated in the write protect mode and the last sixteen bits would be activated in the write protect mode so that when NEW data is read back into memory over lines 1356 only the desired portion of memory cells between the START and STOP locations are written into the memory.

In FIG. 16 is shown an example of performing a drawing rule operation in the vector write page mode. The address register 1320 addresses a specific horizontal or vertical vector in the memory block 1300. Whether or not the vector is horizontal or vertical is determined by the H/V signal on lead 1342 which is the first bit in Din1 of FIG. 15. The OLD information is read out of the memory block on line 1358 and in FIG. 16 is designated DEST for "destination." It is to be noted that information could be delivered through the output control 1338 to data bus 90 for delivery back into the system if desired or into the destination latch 1360. The appropriate enable signal DEST on lead 1364 enables the destination latch 1360 to read in the OLD information. All 32 bits of the destination information of FIG. 16 are read into the latch 1360. The output 1362 of the destination latch 1360 is delivered as the destination input to the drawing rule circuit 1354. For vector mode operation, the SOURCE (SRC) signals on leads 1352 from the data register 1340 are set to all ones and are shown in FIG. 16. The drawing rules are set forth in Table III.

In the example of FIG. 16, the "not destination" drawing rule 1010 appears in the data register 1340. Hence, the OLD information or destination data DEST is inverted to result in a new modified vector which is termed NEW as shown in FIG. 16. However, the writing of this information into the

memory block occurs under control of the write mask 1336 and as previously explained, for our example, bits 31–26 and 15–0 are write protected. Only bits 25–16 of the NEW data can be written into memory. In a similar fashion, all of the logical functions of the drawings rules can be implemented for the entire vector or a portion thereof based upon the START and STOP information.

In the vector mode of operation, up to 32 pixel elements stored in memory block 1300 can be changed in one operation on chip. The present invention is capable of changing a vector located either horizontally or vertically as shown in FIG. 6 through use of the H/V bit.

In the image mode of operation, the MSA and LSA addresses of FIG. 11 are utilized. In FIG. 21, the timing for both image read and image write is shown. Again /CS is properly enabled, and V/I is set low for the image mode. When R/W is set high for read, the read address (MSA 2100 and LSA 2110) is delivered over bus 100 and the data DOUT is read out over bus 90. When R/W is set low for write, the write address (MSA 2120 and LSA 2130) is delivered to the chip over bus 90. Here, the address and Din1 (i.e., drawing rule and START/STOP) are delivered during the first time interval and Din2 (i.e., source data) is delivered during the second time interval.

FIG. 22 shows the timing for the image read and write in the page mode. When R/W is set high for read, the read address (MSA 2100 and LSA 2110) is delivered over bus 100 and the data DOUT is read out over bus 90. When R/W is set low for write, the write address (MSA 2120 and LSA 2130) is delivered over bus 100 and the data Din1+Din2 is delivered to the chip over bus 90. Here, the address and Din1 (i.e., drawing rule and START/STOP) are delivered during the first time interval and Din2 (i.e., source data) is delivered during the second time interval.

FIG. 22 shows the timing for the image read and write in the page mode. In the page mode, the LSA portion of the address changes. Hence, when reading, the changing of LSA causes new data DOUT to be read out. When writing R/W is low, new data is delivered right after delivery of the LSA.

Finally, FIG. 23 shows the timing for image read modify write wherein Din1 of FIG. 14 delivers the start, stop and drawing rule, DOUT is the data at the addressed location and Din2 is the SOURCE data to be read into the chips. As before, the MSA and LSA are read into the address register 1320 and the corresponding Din1 and Din2 data configurations in FIG. 14 are read into the data register 1340. In image mode of operation, a 16 bit word from a scan line is read from the memory block 1300 and is delivered into the destination latch 1360.

In FIG. 17 is an example of a word called DEST read as OLD information from the memory block 1300. In the image mode operation, source data is delivered on Din2 as shown in FIG. 14 and designated SRC. FIG. 17 shows an example of source data. This 16 bit source data SCR is delivered over lines 1352 into the drawing rule circuit 1354. If a drawing rule such as “exclusive-or” (DR=0110) is utilized, circuit 1354 outputs on leads 1356 the NEW word as shown in FIG. 17. Again, the image mode of operation can have a START and STOP location within the word and for masking purposes. In the example assume START equals 0011 and STOP equals 1000. Hence, the mask circuit 1336 provides write protect WP for the bits indicated as in MASK in FIG. 17. What is written into memory is shown as NEW in FIG. 17. The present invention is capable of performing drawing rule operations on chip in the image mode of operation.

As discussed above and as shown in FIG. 23, the present invention delivers the drawing rule to integrated circuit chip

with the delivery of the address during the same time interval and concurrently with the address cycle. This provides a significant speed up over the Hitachi approach which requires a separate time interval in which to deliver the drawing rule.

In the serial data transfer mode of operation, the MSA and LSA address of FIG. 4 are utilized and read into the address register 1320. As set forth in TABLE II above, there are no corresponding Din1 or Din2 data words. When these MSA and LSA address words are read in, the appropriate scan line and scan line portion are read from the memory block 1300 into the dynamic latch 1304 as previously discussed.

The random state machine 1366 is of conventional design and based upon the incoming set of control enables (i.e., V/I, R/W, Rfrsh, and /CS) delivers, according to the pulses of the signal clock Rclk, the following internal random port enable pulses: (1) En-MSA and Clk-LSA to enable the reading of the most significant and least significant address on address bus 100 into the address register 1320, (2) Clk-Din1 and En-Din2 to read in the data appearing on bus 90 into the data register 1340, (3) DEST to enable the destination latch 1360, (4) PRECH to pre-charge each of the memory blocks 1300 in a conventional fashion, (5) En-DL to enable the dynamic latch 1304 to read in data from the memory block 1300, (6) /WE to enable the WRITE mask 1336 to write protect the memory block 1300 based upon the START and STOP information, (7) ALL to access all of the memory blocks rather than a particular block as specified by the block select portion of the address (this is asserted during all regular and serial data transfer cycles), and (8) the OE signal which enables the output control 1338 to output data onto the data bus 90. While the preferred embodiment uses these internal enables other cables could be used in variations on this approach.

The random port state machine 1360 can comprise, for example, a programmable logic array shown in FIG. 24 wherein the inputs 140 (i.e., a set of control enables) based upon the use of only a single clock Rclk to generate the outputs set forth above. Internal to the random state machine 1366 is a next state for the logic array 2400. The next state table is set forth as Table IV.

TABLE IV

Input		Next State		Input		Next State		Input		Next State	
3210	3210	3210	3210	3210	3210	3210	3210	3210	3210	3210	3210
00xx	0000	0100	0101	0000	1000	0111	0000	0001	00xx	0000	0100
00xx	0001	xxxx	0101	0001	xxxx	0111	0001	0011	00xx	0001	xxxx
00xx	0010	xxxx	0101	0010	xxxx	0111	0010	0000	00xx	0010	xxxx
00xx	0011	xxxx	0101	0011	xxxx	0111	0011	0010	00xx	0011	xxxx
00xx	0100	0110	0101	0100	xxxx	0111	0100	xxxx	00xx	0100	xxxx
00xx	0101	xxxx	0101	0101	xxxx	0111	0101	xxxx	00xx	0101	xxxx
00xx	0110	0111	0101	0110	xxxx	0111	0110	xxxx	00xx	0110	xxxx
00xx	0111	0000	0101	0111	xxxx	0111	0111	xxxx	00xx	0111	xxxx
00xx	1000	xxxx	0101	1000	1100	0111	1000	xxxx	00xx	1000	xxxx
00xx	1001	xxxx	0101	1001	1011	0111	1001	xxxx	00xx	1001	xxxx
00xx	1010	xxxx	0101	1010	xxxx	0111	1010	xxxx	00xx	1010	xxxx
00xx	1011	xxxx	0101	1011	1100	0111	1011	xxxx	00xx	1011	xxxx
00xx	1100	xxxx	0101	1100	1101	0111	1100	xxxx	00xx	1100	xxxx
00xx	1101	xxxx	0101	1101	1100	0111	1101	xxxx	00xx	1101	xxxx
00xx	1110	xxxx	0101	1110	xxxx	0111	1110	xxxx	00xx	1110	xxxx
00xx	1111	xxxx	0101	1111	1011	0111	1111	xxxx	00xx	1111	xxxx
0100	0000	1000	0110	0000	1000	1xxx	0000	0000	0100	0000	1xxx
0100	0001	xxxx	0110	0001	xxxx	1xxx	0001	0000	0100	0001	xxxx
0100	0010	xxxx	0110	0010	xxxx	1xxx	0010	0000	0100	0010	xxxx
0100	0011	xxxx	0110	0011	xxxx	1xxx	0011	0000	0100	0011	xxxx
0100	0100	xxxx	0110	0100	xxxx	1xxx	0100	0000	0100	0100	xxxx
0100	0101	xxxx	0110	0101	xxxx	1xxx	0101	0000	0100	0101	xxxx
0100	0110	xxxx	0110	0110	xxxx	1xxx	0110	0000	0100	0110	xxxx

TABLE IV-continued

Input	State	Next	Input	State	Next	Input	State	Next
3210	3210	3210	3210	3210	3210	3210	3210	3210
0100	0111	xxxx	0110	0111	xxxx	1xxx	0111	0000
0100	1000	1001	0110	1000	1001	1xxx	1000	0000
0100	1001	1011	0110	1001	1011	1xxx	1001	0000
0100	1010	xxxx	0110	1010	xxxx	1xxx	1010	0000
0100	1011	1001	0110	1011	1111	1xxx	1011	0000
0100	1100	1101	0110	1100	1101	1xxx	1100	0000
0100	1101	1001	0110	1101	1001	1xxx	1101	0000
0100	1110	xxxx	0110	1110	xxxx	1xxx	1110	0000
0100	1111	1011	0110	1111	1011	1xxx	1111	0000
Input ₃	N_CS							
Input ₂	N_RFRSH							
Input ₁	V_I							
Input ₀	R_W							

In Table IV the input set format is: /CS, Rfrsh, V/I, and R/W. As can be seen above for each different set of enables (INPUT) from the control bus 140, the random state machine produces a predetermined sequence as derived from the clock (Rclk) signal of the state table (STATE) to produce the control pulses which are defined next.

The output STATE signals are decoded from the state and are set forth in Table V.

TABLE V

State	Output										
3210	10	9	8	7	6	5	4	3	2	1	0
0000	1	1	x	0	x	x	1	1	0	1	0
0001	0	0	0	x	x	x	1	1	1	1	0
0010	0	0	x	x	x	x	1	1	1	1	0
0011	0	0	1	x	x	x	1	1	1	1	1
0100	0	x	x	x	x	x	1	1	1	0	0
0101	x	x	x	x	x	x	x	1	x	x	x
0110	0	x	x	x	x	x	1	1	1	0	0
0111	0	x	x	x	x	x	1	1	1	0	0
1000	0	0	0	1	x	x	1	1	0	1	0
1001	0	0	1	0	1	1	1	1	0	1	0
1010	x	x	x	x	x	x	x	1	x	x	x
1011	0	0	0	0	0	0	0	1	0	1	0
1100	0	0	1	0	x	x	1	0	0	1	0
1101	0	0	0	0	x	x	1	1	0	1	0
1110	x	x	x	x	x	x	x	1	x	x	x
1111	0	0	1	1	x	1	1	1	0	1	0

The output relationships are set forth in Table VI.

TABLE VI

Output ₁₀	PRECHARG
Output ₉	EN_MSA
Output ₈	CLK_LSA
Output ₇	CLK_DIN1
Output ₆	EN_DIN2
Output ₅	EN_DEST
Output ₄	N_WE
Output ₃	N_OE
Output ₂	ALL
Output ₁	N_RFRSH
Output ₀	EN_DL

The random port control signals set forth in Table VI becomes valid in the random port 1200, as shown in FIGS. 18 through 23 with the edges of the clock Rclk.

It can clearly be seen based upon this disclosure only a single clock pulse Rclk controls the random port 1200 of the present invention. In other words, the random port 1200 of the present invention receives a set of control signals (i.e.,

INPUT of Table IV). Each set corresponding to a different mode of operation for the random port. The random state machine 1366 provides the sequential configuration (i.e., STATE and NEXT STATE of Table IV) for the received set. Each different set has a different sequential configuration resulting in its own predetermined sequence of internal control pulses (i.e., Table V). The simple random port clock provides the timing signal necessary for executing the configured sequence of internal control pulses so that the random port operates in the mode of operation corresponding to the received set of control signals. It is to be expressly understood that while a preferred approach is set forth in Table IV, V, and VI that other configurations of control signals and states can be defined under the teachings of the present invention to work on the provision of a single random port clock which in the present embodiment is 16.7 MHz.

Combining the aforesaid state tables with the timing diagrams of FIGS. 19 through 23, the method of modifying the stored information in the memory is based upon a series of time intervals which are derived from the single random clock Rclk. During a first time interval, the vector or image address as well as the drawing rule and the START and STOP locations are delivered to the chip. Based upon the set of control enables, the Rclk then sequences through the appropriate state table. Hence, during a second time interval, the addressed information is delivered from memory and the source data is delivered to the chip. During a third interval, the delivered information (i.e., DEST in FIGS. 16 and 17 is modified with the source data (i.e., SRC of FIGS. 16 and 17) based upon the drawing rule (i.e., Table III). During a fourth time interval, the modified information (i.e., NEW of FIGS. 16 and 17) is written between the START and STOP bit locations (i.e., MASK of FIGS. 16 and 17) into memory. Variations to this method are possible under the teachings of the present invention.

It is to be expressly understood that the preferred embodiment illustrates certain bit fields and patterns, certain pin configurations and layouts; however, the present invention is not so limited that under the teachings of the present invention other embodiments could be used.

While preferred embodiments of the present invention have been shown, it is to be expressly understood that modifications and changes may be made thereto and that the present invention is set forth in the following claims.

I claim:

1. An architecture for addressing and modifying vectors in a dynamic video random access memory placed on an integrated circuit chip, said dynamic video random access memory being connected to a bus (90, 100), said bus delivering vector addresses, source data, drawing rules and START and STOP locations, said source data being new data to be used to modify an addressed vector, said START and STOP locations defining the portion of said addressed vector to be modified, and said drawing rule being the logical operation combining said source data with said data portion between said START and STOP locations of said addressed vector, said architecture on said integrated circuit chip comprising:

a memory (1300) for storing vectors of video information, said memory having a plurality of "n"×"m" bit pages (PG), each of said pages having defined page column (PC) and page row (PR) locations in said memory, each said page containing a plurality of horizontal (610) and vertical (600) vectors, each said horizontal vector being defined by a vector row location in said page and each said vertical vector being defined by a vector column in said page,

address means (1360) connected to said bus for receiving the address of a horizontal or vertical vector in a page of said memory to be modified, said address comprising:

- (a) a first plurality of bits for defining the page row of said addressed page,
- (b) a second plurality of bits for defining the page column of said addressed page, and
- (c) a third plurality of bits for defining the addressed vector in said addressed page,

data means (1340) connected to said bus for receiving said source data, and

control means (1366, 1360, 1354, 1336) connected to said memory, said address means, and said data means for modifying the stored video information with said source data at the addressed vector in said memory wherein said data means further receives said drawing rule from said bus, said drawing rule being used by said control means to modify said line of stored video information between said START and STOP locations.

2. The architecture of claim 1 wherein said third plurality of bits includes at least one bit for defining whether the addressed vector is horizontal or vertical.

3. The architecture of claim 1 wherein said memory has at least 32 by 32 bit pages.

4. The architecture of claim 1 wherein said memory comprises a plurality of memory blocks of at least 160 memory cells by 1024 memory cells.

5. The architecture of claim 1 wherein said control means utilizes a single clock input to said integrated circuit chip for performance of said modification.

6. The architecture of claim 1 wherein said architecture is capable of modifying at least three million vectors per second.

7. The architecture of claim 1 further comprising means (1360) connected to said memory for delivering said vector of stored video information from said memory based upon said addressed vector from said address means.

8. The architecture of claim 1 further comprising:

drawing rule means (1354) receiving said line of stored video information and connected to said data means for obtaining said drawing rule, said drawing rule means logically combining said line of stored video information and said source data according to said drawing rule logical operation to modify said line of stored video information,

write mask means (1336) connected to said data means for obtaining said START and STOP locations and connected to said memory for allowing said writing of said logical combination only between said START and STOP bit locations of said line, and

said control means activating said drawing rule means to perform said logical combination, and said control means then writing said modified line of video information resulting from said logical combination into said memory only between said START and STOP bit locations.

9. The architecture of claim 1 wherein said bus comprises an address bus (100) and a data bus (90).

10. An architecture for addressing and modifying vectors in a dynamic video random access memory placed on a single integrated circuit chip, said dynamic video random access memory being connected to a bus (90, 100); said bus delivering vector addresses, source data, drawing rules and START and STOP locations, said source data being new data to be used to modify an addressed vector, said START and

STOP locations defining the portion of said addressed vector to be modified, and said drawing rule being the logical operation combining said source data with said data portion between said START and STOP location of said addressed vector, said architecture on said integrated circuit chip comprising:

a memory (1300) for storing vectors of video information, address means (1360) connected to said bus for receiving the address of a vector in said memory to be modified,

data means (1340) connected to said bus for receiving said source data for modifying the stored video information at said addressed vector, and

control means (1366, 1360, 1354, 1336) connected to said memory, said address means, and said data means for modifying the stored video information with said source data at the addressed vector location in said memory wherein said data means further receives a drawing rule from said bus, said drawing rule being used by said control means to modify said addressed vector of stored video information, said data means further receiving the START and STOP locations for said modification of said addressed vector of stored video information between said START and STOP locations.

11. The architecture of claim 10 wherein said control means utilizes a single clock input to said chip for performance of said modification.

12. The architecture of claim 10 wherein said architecture is capable of modifying at least three million vectors per second.

13. The architecture of claim 10 further comprising:

drawing rule means (1354) receiving said addressed vector of stored video information and connected to said data means for obtaining said drawing rule, said drawing rule means logically combining said addressed vector of stored video information and said source data according to said drawing rule logical operation to modify said addressed vector of stored video information,

write mask means (1336) connected to said data means for obtaining said START and STOP locations and connected to said memory for allowing said writing of said logical combination only between said START and STOP bit locations of said addressed vector, and

said control means activating said drawing rule means to perform said logical combination, and said control means then writing said modified line of video information resulting from said logical combination into said memory only between said START and STOP bit locations.

14. The architecture of claim 10 wherein said bus comprises an address bus (100) and a data bus (90).

15. An architecture for addressing a dynamic video random access memory with both image and vector addresses, said dynamic video random access memory being connected to a bus (90, 100), said bus providing said image and vector addresses and source data, said source data for modifying the stored video information at said vector and image addresses, said architecture comprising:

a memory (1300) for storing video information, said memory being addressed with said vector and image addresses, said memory:

- (a) when addressed with said vector addresses, having a plurality of pages (PG), each of said pages having defined page column (PC) and page row (PR) locations in said memory, each said page containing a

plurality of horizontal (610) and vertical (600) vectors, each said horizontal vector being defined by a vector row location in said page and each said vertical vector being defined by a vector column in said page,

(b) when addressed with said image addresses, having a plurality of scan lines, each of said scan lines containing a plurality of words,

address means (1360) connected to said bus for receiving an address mode (V/I), and either the vector address for a horizontal or vertical vector to be modified in said memory or the image address of a word to be modified in said memory,

said vector address comprising:

- (a) a first plurality of bits for defining the page row of said addressed page,
- (b) a second plurality of bits for defining the page column of said addressed page, and
- (c) a third plurality of bits for defining the page addressed vector in said addressed page,

said image address comprising:

- (a) a first plurality of bits for defining the scan line being addressed, and
- (b) a second plurality of bits for defining the addressed word in said addressed scan line,

data means (1340) connected to said bus for receiving said source data, and

control means (1366, 1360, 1354, 1336) connected to said memory, said address means, and said data means for addressing said memory with said address in said address means to modify the stored video information with said source data in said data means.

16. The architecture of claim 15 wherein said memory, said address means, said data means, and said control means reside on a single integrated circuit chip.

17. The architecture of claim 16 wherein said control means utilizes a single clock input to said chip for performance of said modification.

18. The architecture of claim 15 wherein said data means further receives a drawing rule from said bus, said drawing rule being the logical operation for modifying said addressed vector of stored video information, said data means further receiving the START and STOP locations for modifying said addressed vector of stored video information, said START and STOP locations being the beginning and ending bit locations in said addressed vector between which said modification of said line occurs.

19. The architecture of claim 18 further comprising:

drawing rule means (1354) receiving said addressed vector of stored video information and connected to said data means for obtaining said drawing rule, said drawing rule means logically combining said addressed vector of stored video information and said source data according to said drawing rule logical operation to modify said addressed vector of stored video information,

write mask means (1336) connected to said data means for obtaining said START and STOP locations and connected to said memory for allowing said writing of said logical combination only between said START and STOP bit locations of said addressed vector, and

said control means activating said drawing rule means to perform said logical combination, and said control means then writing said modified line of video information resulting from said logical combination into said memory only between said START and STOP bit locations.

20. The architecture of claim 15 wherein said third plurality of bits in said vector address includes at least one bit for defining whether the addressed vector is horizontal or vertical.

21. The architecture of claim 15 wherein said memory in the vector mode has at least 32 by 32 bit pages.

22. The architecture of claim 15 wherein said memory comprises a plurality of memory blocks of at least 160 memory cells by 1024 memory cells.

23. The architecture of claim 15 wherein said architecture is capable of modifying at least three million vectors per second.

24. The architecture of claim 15 wherein said bus comprises an address bus (100) and a data bus (90).

25. An architecture for addressing a dynamic video random access memory with both image and vector addresses, said dynamic video random access memory being connected to a bus (90, 100), said bus providing said image and vector address and source data, said source data for modifying the stored video information at said vector and image addresses, said architecture comprising:

a memory (1300) for storing video information, said memory being addressed with said vector and image addresses, said memory:

- (a) when addressed with said vector addresses, having a plurality of pages (PG), each said page containing a plurality of vectors,
- (b) when addressed with said image addresses, having a plurality of scan lines, each of said scan lines containing a plurality of words,

address means (1360) connected to said bus for receiving an address mode (V/I), and either the vector address for a vector to be modified in said memory or the image address of a word to be modified in said memory,

said vector address comprising:

- (a) a first plurality of bits for defining said addressed page, and
- (b) a second plurality of bits for defining the addressed vector in said addressed page,

said image address comprising:

- (a) a first plurality of bits for defining the scan line being addressed, and
- (b) a second plurality of bits for defining the addressed word in said addressed scan line,

data means (1340) connected to said bus for receiving said source data, and

control means (1366, 1360, 1354, 1336) connected to said memory, said address means, and said data means for addressing said memory with said address in said address means to modify the stored video information with said source data in said data means.

26. An architecture for addressing with both image and vector addresses a dynamic video random access memory, said dynamic video random access memory being connected to a bus (90, 100), said bus providing said image and vector address and source data, said source data for modifying the stored video information at said vector and image addresses, said architecture comprising:

a memory (1300) for storing video information; said memory being addressed with said vector address or with said image address; said memory, in the vector address mode, having a plurality of pages (PG) each of said pages containing a plurality of vectors; said memory, in the image address mode having a plurality of scan lines; each of said scan lines containing a plurality of words,

address means (1360) connected to said address bus for receiving said vector address of a vector to be modified in said memory or said image address of a word to be modified in said memory; said vector address defining (a) said addressed page and (b) the addressed vector in said addressed page; said image address defining (a) the scan line being addressed and (b) the word in said addressed scan line,

data means (1340) connected to said bus for receiving said source data for modifying the stored video information at said vector or image address, and

control means (1366, 1360, 1354, 1336) connected to said memory, said address means, and said data means for addressing said memory with said address in said address means to modify the stored video information with said source data.

27. The architecture of claim 26 wherein said vector mode can be addressed by horizontal or vertical vectors.

28. The architecture of claim 26 wherein said control means utilizes a single clock input to said chip for the performance of said modification.

29. The architecture of claim 26 wherein said architecture is capable of modifying at least three million vectors per second.

30. The architecture of claim 26 wherein said bus comprises an address bus (100) and a data bus (90).

31. The architecture of claim 26 wherein said memory, said address, said data means and said control means reside on a single integrated circuit chip.

32. A dynamic video RAM connected to a random bus and to a serial bus, said RAM comprising:

- a single integrated circuit chip (10) connected to said serial and random buses,
- a memory (1300) on said chip for storing video information, said memory being addressed in serial data transfer, vector, and image modes of operation, said memory:
 - (a) in said vector address mode, having a plurality of pages (PG), each said page containing a plurality of horizontal (610) and vertical (600) vectors,
 - (b) in said image address mode, having a plurality of scan lines, each of said scan lines containing a plurality of scan words,
 - (c) in said serial data transfer mode, having a plurality of partial scan lines, each of said partial scan lines containing a plurality of partial scan words,

address means (1360) on said chip and connected to said random bus for receiving the mode of operation and (1) the vector mode address for a vector in said memory, (2) the image mode address for a scan line in said memory, or (3) the serial data transfer address for the partial scan line in said memory,

random control means (1366, 1360, 1354, 1336, 1340) connected to said memory and said address means for accessing information at the memory locations of said image mode or vector mode addresses, said random control means reading said memory at said serial data transfer addresses, and

serial port control means (1304, 1306, 1314) connected to said memory for delivering said read information at said serial data transfer address to said serial bus.

33. The RAM of claim 32 wherein said random port control means receives over the random bus (1) a vector/image (V/I) signal for determining the vector or image addressing mode of operation, (2) a read/write (R/W) signal for determining whether to read or write said memory, and

(3) a clock signal (RCLK) for performing all random port operations of said dynamic video RAM.

34. The architecture of claim 32 wherein said random port control means is a random state machine.

35. A system comprising a memory, a circuit for accessing said memory, and a bus connecting said circuit to said memory,

said circuit comprising means for providing a first address and a second address on said bus, said first address being valid on said bus on a first edge of a clock signal and said second address being valid on said bus on a second edge of said clock signal, said first edge of said clock signal being different from said second edge of said clock signal; and

said memory being a synchronous dynamic random access memory integrated circuit comprising:

a memory block including a plurality of memory cells for storing information;

an input for receiving said clock signal;

address input means for receiving and holding said first address from said bus in response to said first edge of said clock signal, and for receiving and holding said second address from said bus in response to said second edge of said clock signal; and

access means for accessing a location in said memory block corresponding to said first address and said second address held by said address input means.

36. The system of claim 35, wherein said access means comprises:

output means for outputting, to said bus, information stored at said location of said memory block in response to a third edge of said clock signal.

37. The system of claim 36,

said circuit for accessing further comprising:

means for providing on said bus a control input, said control input being valid on an edge of said clock signal,

said memory further comprising:

control means for supplying a first enable signal and a second enable signal to said address input means in response to said control input on an edge of said clock signal, and for supplying an output enable signal to said output means in response to said control input on an edge of said clock signal, each of said first enable signal, said second enable signal and said output enable signal being synchronous with an edge of said clock signal, and

wherein said address input means holds said first address based on said first enable signal, said address input means holds said second address based on said second enable signal, and said output means outputs said information based on said output enable signal.

38. The system of claim 35,

said circuit for accessing further comprising:

means for providing data on said bus which is valid on a third edge of said clock signal,

wherein said access means comprises:

data input means for receiving said data from said bus, said data input means holding said data in response to said third edge of said clock signal; and

write means for writing said data to said memory block at said location corresponding to said first address and said second address in response to a fourth edge of said clock signal.

39. The system of claim 38,

said circuit for accessing further comprising:

means for providing on said bus a control input, said control input being valid on an edge of said clock signal;

said memory further comprising:

control means for supplying a data enable signal to said data input means in response to said control input on an edge of said clock signal, and for supplying a write enable signal to said write means in response to said control input on an edge of said clock signal, each of said data enable signal and said write enable signal being synchronous with an edge of said clock signal, and

wherein said data input means provides said data to said write means in response to said data enable signal.

40. The system of claim 35,

wherein said bus includes an address bus for conveying said first address and said second address and a data bus for conveying said data.

41. The system of claim 35, wherein said clock signal has a frequency of about 16.7 MHZ.

42. The system of claim 35, wherein:

said bus comprises a first bus on which said first address and said second address are provided and which also conveys data between said circuit and said memory, and a second bus connecting said circuit to said memory for conveying a control input defining an operation mode;

said circuit further comprises means for providing said control input on said second bus, and means for providing access information defining a specification of said operation mode on said first bus, said access information being valid on said first bus on a third edge of said clock signal, and said control input being valid on said second bus on an edge of said clock signal; and

said memory further comprises:

access information input means for receiving said access information through said first bus, said access information input means providing said access information as an output in response to said third edge of said clock signal; and

control means for receiving said control input through said second bus, and for controlling operations of said address input means, said access information input means and said access means in response to said control input on an edge of said clock signal.

43. The system of claim 35, wherein:

said circuit further comprises means for providing a control input on said bus, said control input being valid on said bus on an edge of said clock signal; and

said memory operates by use of edges of said clock signal and further comprises control means for receiving said control input indicating a read/write mode defining one of a read mode and a write mode, and for changing said read/write mode based on a difference of level of said control input at two successive edges of said edges of said clock signal.

44. The system of claim 43, wherein:

said first address held by said address input means is maintained before and after a level change of said control input resulting in said difference of level.

45. The system of claim 35, wherein:

said circuit further comprises means for providing a control input on said bus, said control input being valid on said bus on an edge of said clock signal; and

said memory further comprising control means for outputting an internal control signal defining a timing of

an internal operation of said synchronous dynamic random access memory based on a control input on an edge of said clock signal;

wherein said control means generates new state information in accordance with a control input and state information output in response to a third edge of said clock signal, and outputs a new internal control signal based on said new state information in response to a fourth edge of said clock signal, said third edge of said clock signal being different from said fourth edge of said clock signal.

46. The system of claim 45, wherein:

said internal control signal is a precharge control signal provided to said memory block.

47. The system of claim 35, wherein:

said memory block comprises a plurality of individual memory blocks and said access means further comprises output means for sequentially outputting a plurality of data which belong to separately addressable locations in said individual memory blocks at substantially a same interval, said plurality of data including data stored at a location in said memory block corresponding to said first address and said second address.

48. The system of claim 35, wherein:

said circuit further comprises means for providing a control input on said bus, said control input being valid on said bus on an edge of said clock signal; and

said memory comprises a random state machine.

49. The system of claim 48, wherein:

said random state machine determines a new state based on said control input and a current state, and outputs an internal control signal based on said new state in response to an edge of said clock signal, said internal control signal defining a timing of an internal operation of said memory.

50. The system of claim 49, wherein:

said random state machine comprises decoding means for decoding said new state so as to output said internal control signal.

51. The system of claim 35, said memory further comprising:

control means for receiving a predetermined set of control signals provided from outside of said memory, for transitioning from one state to at least one next state in accordance with said predetermined set of control signals on respective edges of said clock signal, and for outputting internal control signals defining timings of internal operations of said memory based on the at least one next state;

wherein said predetermined set of control signals include a first control signal and a second control signal, said internal operations represent a write operation when said first control signal is active and said second control signal is active, and said internal operations represent a read operation when said first control signal is inactive and said second control signal is active.

52. The system of claim 51, wherein a level of said first control signal is changed during a period when said second control signal is active, and said operation of said memory is changed between said read operation and said write operation in accordance with said level change of said first control signal without the control means reverting back to a state prior to starting either said read operation or said write operation.

53. The system of claim 45, wherein said state information may be any one of a first state information indicating an initial state and a plurality of second state information indicating respective states other than said initial state, and with respect to at least one of the plurality of second state information when said state information output in response to said third edge of said clock signal is said at least one second state information, said new state information may be any one of a predefined plurality of second state information from among said plurality of second state information, each of said predefined plurality of second state information indicating respective states other than said initial state.

54. The system of claim 49, wherein said current state and said new state may be any one of a first state indicating an initial state and a plurality of second states each indicating a state other than said initial state, and with respect to at least one of the plurality of second states when said current state is said at least one second state, said new state may be any one of a predefined plurality of second states from among said plurality of second states, each of said predefined plurality of second states indicating states other than said initial state.

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