

United States Patent [19]

[11] E

US00RE34484E Patent Number:

Re. 34,484

Nagashima et al.

[45] Reissued Date of Patent: Dec. 21, 1993

[54]	GOLD-PLATED	ELECTRONIC
-	COMPONENTS	

Teruyoshi Nagashima; Akio Takami; Inventors:

Akiyo Kasugai, all of Aichi, Japan

NGK Spark Plug Co., Ltd., Aichi, [73] Assignee:

Japan

Appl. No.: 800,462

Filed: Nov. 29, 1991

Related U.S. Patent Documents

Reissue of:

[75]

[64] 4,465,742 Patent No.:

Aug. 14, 1984 Issued: Appl. No.: 344,158

Filed:

Jan. 29, 1982

U.S. Applications:

[63] Continuation of Ser. No. 72,750, Sep. 5, 1979,

abandoned.

[30] Foreign Application Priority Data

Sep. 5, 1978 [JP] Japan 53-108976

[52] 428/336; 428/433; 428/672; 428/901; 439/894 Field of Search 428/621, 336, 433, 672, 428/901; 200/268; 439/894

[56] References Cited

U.S. PATENT DOCUMENTS

3,691,289	9/1972	Rohloff	357/72 X
3,707,358	12/1972	Masselink	29/195
		Kamata	
3,729,820	5/1973	Ihochi et al	29/627
		Anderson et al	
, ,		Nobel et al	

OTHER PUBLICATIONS

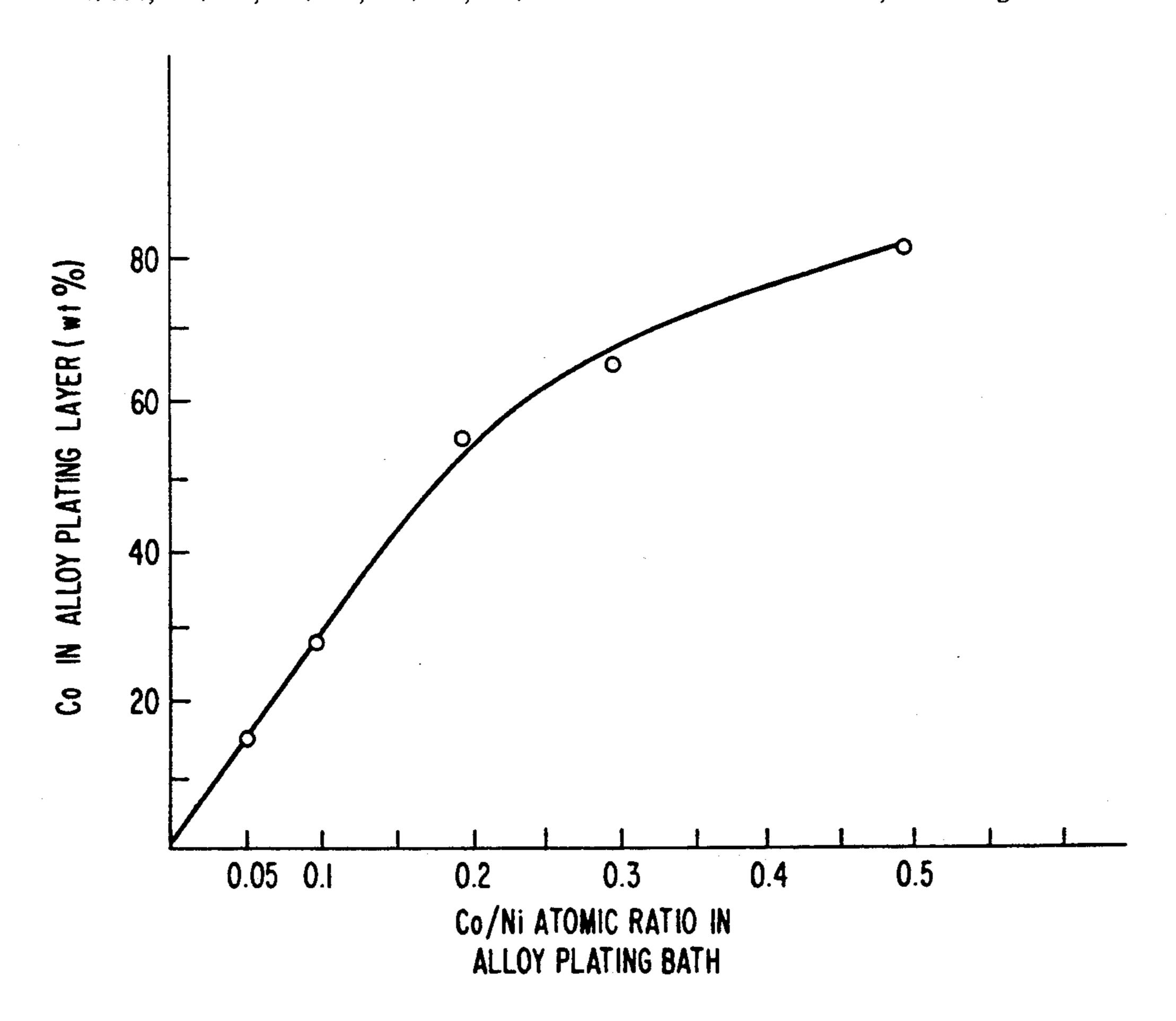
F. A. Lowenheim, Electroplating, McGraw-Hill Book Co., New York, 1978, pp. 416-419.

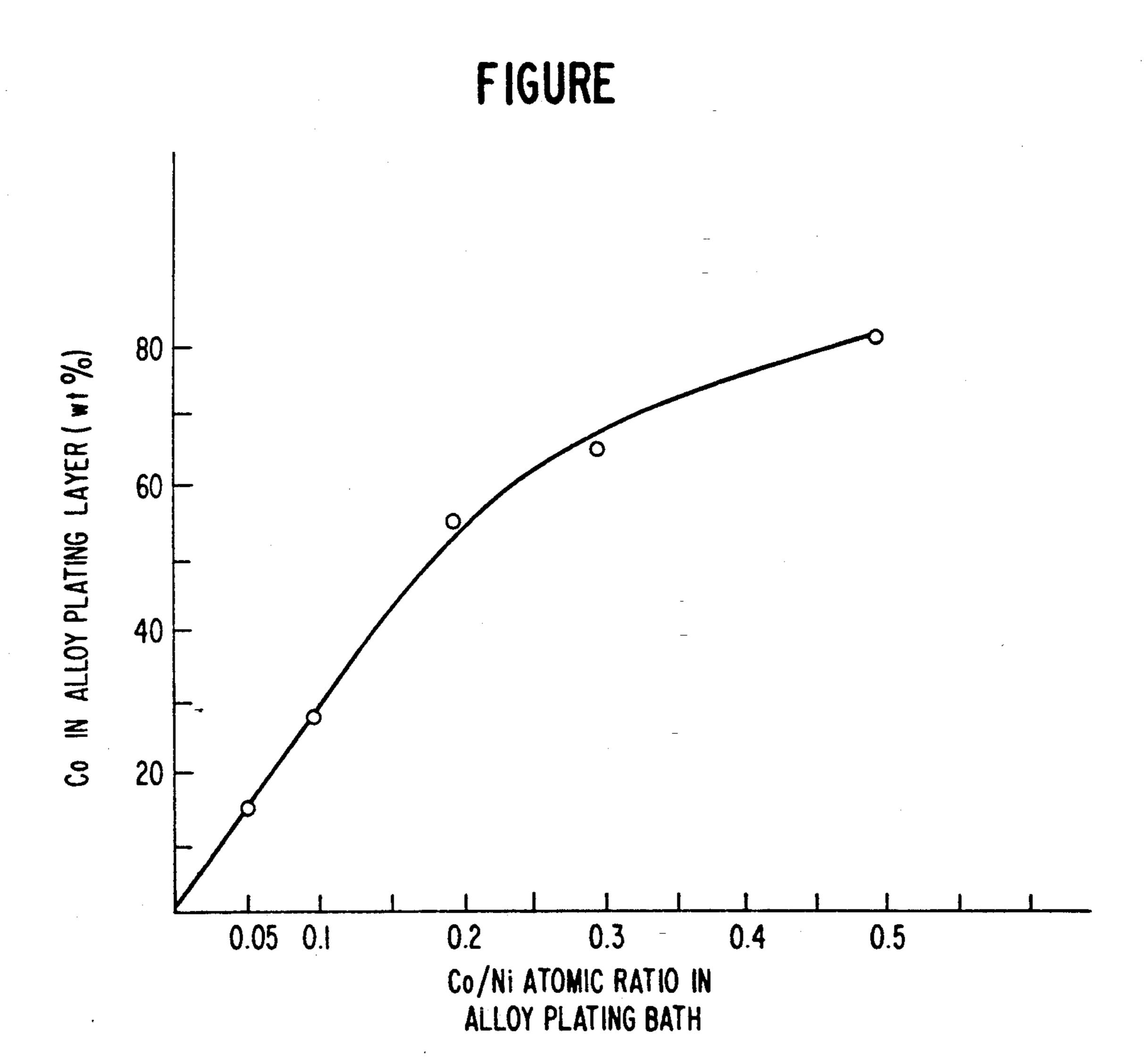
Primary Examiner—John Niebling Assistant Examiner—William T. Leader Attorney, Agent, or Firm—Sughrue, Mion, Zinn, Macpeak & Seas

ABSTRACT [57]

Gold-plated electronic components are disclosed, as well as a process for producing the same, wherein an alloy of nickel and cobalt or an alloy containing these elements as essential ingredients is used as an undercoatfor the gold-plated layer.

2 Claims, 1 Drawing Sheet





2

GOLD-PLATED ELECTRONIC COMPONENTS

Matter enclosed in heavy brackets [] appears in the original patent but forms no part of this reissue specifica-5 tion; matter printed in italics indicates the additions made by reissue.

This is a continuation of application Ser. No. 72,750, filed Sept. 5, 1979, now abandoned.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to gold-plated electronic components and, more specifically, to electronic components of high quality having a thin gold-plated layer and to a method for their production.

2. Description of the Prior Art

Because of its superior physical properties, gold has been widely used as a plated layer on various electronic 20 components. When gold is used in electronic components composed of metallized ceramics, it exhibits good connecting properties in bonding, brazing, soldering, etc. Since gold is very expensive, it is desired to use it in a layer having the smallest possible thickness. In spite of 25 this strong incentive, it has not been realized for one or more reasons. For example, when the gold-plated layer is made thin, an undercoat of plated Ni or Cu, or the metallized layer diffuses into the gold-plated layer because such an undercoat layer or the metallized layer 30 cannot be made compact, i.e., pore free. On the other hand through pinholes in the gold coating, the undercoat layer is degenerated, and discolored under heat. There are further deteriorations in heat resistance and connecting properties, such as the peeling of a silicon 35 tip, deterioration of bonding, and poor cap attachment of an Au/Sn seal. Thus, despite the high cost, a thick gold-plated layer has been required.

SUMMARY OF THE INVENTION

In view of the state of art, extensive investigations of electronic components having a metal surface which do not undergo deterioration in performance even when overcoated with a thin gold-plated layer have been made. These investigations have led to the discovery 45 that such electronic components can be provided by applying a plating of a special alloy as an undercoat layer for gold plating.

The present invention provides an electronic component having a metal surface and a gold-plated layer 50 applied to the metal surface in which a plated layer of an alloy of nickel and cobalt or an alloy containing these metals as essential ingredients is applied to the metal surface as an undercoat for the gold-plated layer; and a process for producing such an electronic component. 55

BRIEF DESCRIPTION OF THE DRAWING

The FIGURE is a graph showing variations in the Co/Ni ratio in an alloy coating when it is applied from an alloy plating bath having various Co/Ni ratios.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is concerned with electronic components having a gold-plated layer on a metal sur- 65 face. There is no particular restriction on the metal surface to which the gold-plated layer can be formed by the present invention. Examples of the metal surface are

metals which constitute ordinary electronic components such as copper, iron, and aluminum, and ceramic substrates whose surfaces are metallized with materials composed mainly of tungsten, molybdenum, or mixtures thereof. Gold-plated electronic equipment includes, for example, circuit boards for hybrid IC, IC package boards, LSI packages, boards for LED, microswitches, small switches, and connector plugs. Gold is used for a variety of purposes including the wire bonding, tip attachment and soldering (including sealing) of electronic component parts, the provision of conductors and contacts, and also for rust-proofing of these parts. The present invention is applicable to all of these applications.

The present invention is characterized by applying a plated layer of an alloy of nickel and cobalt or an alloy containing these metals as essential ingredients as an undercoat for the gold-plated layer in these electronic components. The method of applying the alloy plating is not limited. It is formed in a thickness of about 0.1 to 10 microns, preferably about 0.5 to 5 microns, by electroplating, electroless plating, etc. The preferred contents of cobalt in the alloy is from about 2 to 60% by weight, and especially from about 7 to 40% by weight. In most cases the balance of the alloy is nickel. If the cobalt content is less than 2 by weight, the heat resistance and connecting property of the resulting alloy coating are not improved appreciably. On the other hand, if the cobalt content exceeds 55% by weight, solderability becomes inferior, and moreover, this is economically disadvantageous because cobalt is much higher in price than nickel. In electroless plating, when sodium hypophosphite is used as reducing agent, the alloy will be 2 to 60% cobalt, 88 to 30% nickel and the remainder, about 10% phosphorus. When sodium borohydride is used as reducing agent, the alloy will be 2 to 60% cobalt, 95-37% nickel and the remainder, about 3% boron. Hydrazine can also be employed as reducing agent.

The plating conditions for the alloy layer are not limited. In the case of electrolytic plating ordinary Ni plating conditions may be used such as 40° to 60° C. and a current density of 1 A/dm². In the case of electroless plating, when a hypophosphite group is used as reducing agent, the liquid temperature is 90° to 95° C. When a borohydride is used as reducing agent, liquid temperature is 70° to 80° C.

Preferably, the alloy-plated layer is treated in a non-oxidizing atmosphere, such as nitrogen, ammonia-decomposition gas, or hydrogen gas at a temperature of at least about 700° C. and preferably about 700° to 1000° C. This makes the alloy coating compact i.e., free from pores, and increases adhesion between the plated layer and its substrate.

The present inventors have examined the Co/Ni atomic ratio in the alloy coating prepared from an alloy plating bath having varying Co/Ni atomic ratios, and found that as shown in the FIGURE, cobalt deposits preferentially to nickel. To maintain the Ni/Co atomic ratio in the alloy coating constant, it is necessary to supply Co to the plating bath. A supplemental solution for this purpose should contain Ni and Co in a lower Ni/Co atomic ratio than the Ni/Co atomic ratio of the alloy plating bath. A Co/Ni atomic ratio of 0.01 to 0.3 and preferably 0.03 to 0.15 is suitable for the plating bath, but the ratio may vary outside those ranges. A plated coating of uniform quality can be obtained by performing the plating of the alloy while adding a sup-

plemental solution, Ni and Co can also be supplied from the anode in addition to from the solutions.

After the alloy coating is formed by the above method, gold plating is performed in a known manner. Conventional electronic components have a gold plated 5 layer usually having a thickness of about 2 to 4 microns, although the thickness varies depending upon the uses of the components. In contrast, in the present invention, the same performance can be obtained even when the thickness of the gold coating is decreased by 1 to 2 10 microns because a plated layer of an alloy of nickel and cobalt or an alloy containing these metals as main ingredients is formed as an undercoat for the gold-plated layer. For example, in a ceramic package for LSI, a gold-plated layer usually having a thickness of about 3 15 to 4 microns is formed when a nickel plated layer is applied as an undercoat. In contrast, in the present invention, the provision of a gold-plated layer having a thickness of about 1.5 to 2 microns is sufficient. The same performance as in conventional articles can be 20 obtained even when the thickness of the gold coating is reduced. This is presumably because the inclusion of cobalt in the undercoat layer greatly inhibits the diffusion of the elements of the undercoat layer into the gold, for example, the diffusion of nickel to gold, and thus 25 makes it possible to retain the purity of the gold-plated layer.

In spite of the thin gold-plated layer in the electronic equipment in accordance with this invention, good performance is obtained. Accordingly, the cost of production can be maintained low, and the present invention has much practical utility.

The following Examples illustrate the present invention in greater detail. It should be understood that the invention is not limited by these Examples.

EXAMPLE 1

A metallized layer composed mainly of W was printed on green sheets formed from alumina and a resin. The green sheets were laminated and sintered to 40 produce a standard side-braze type LSI ceramic package. A coating 2 microns in thickness having an Ni/Co ratio varying as shown in the table was formed from a plating bath consisting of a Watt bath as a base and cobalt sulfate as to use it as an undercoat for a gold coating. Then, a gold-plated layer, 1.5 microns thick, was formed from a commercially available gold plating bath ("Tempelex 401", a trademark for a product of

Tanaka Noble Metals Co., Ltd.). Various properties of the resulting product were evaluated.

Testing Methods

(1) Die Bonding Test

A silicon tip was bonded while it was scribed in N₂ gas at 450° C. Those products in which at least 90% of the area around the tip was wetted with an Au/Si eutectic alloy were regarded as acceptable.

(2) Aging Test

A die-bonded sample was allowed to stand in N₂ gas at 300° C., and the tip was pushed with a force of 500 g at 0, 15, 30, 50, 75, 150 and 200 hours to determine at which time peeling of the tip occurred. Those products in which the tip did not peel for at least 30 hours were regarded as acceptable.

(3) Lid Seal Test

A 1.0 t Kovar cap (with a gold plated-layer of 2.0 microns in thickness) was sealed in a hydrogen furnace at 300° C. for 6 minutes using a 50 μ thick 80Au/20Sn preform. Then, a He leak test was conducted in accordance with MIL-STD 883, 1014, and those products which did not show leakage were regarded as acceptable.

(4) Lead Bending Test

A load as exerted on the lead to perform a bending test in accordance with MIL-STD 883,4004. Those products in which the plated coating was not peeled or cracked were regarded as acceptable.

(5) Solderability Test

A lead was dip-soldered in accordance with MIL-STD 883, 2003 and those products in which at least 95% of the lead was wetted with the solder were regarded as acceptable.

(6) High Temperature Standing Test

Samples were allowed to stand in atmosphere air at 175° C. for 250 hours, and those products which did not develop rust were regarded as acceptable.

For each sample tested 10 runs were made. The number of unacceptable runs out of the 10 in each of the above test (1) to (6) is shown in the following table. As is clearly seen from the table, when cobalt is included in a nickel plated undercoating, the results in each test are improved.

TABLE

	5 ' 5	••		Aging test			Lead Bending		Solderability		High Temperature		
Co (%)		Die Bonding	Before	After	Lid Seal Test		<u>Test</u>		Test		Standing Test		
•	in N ₁ Plating	n N ₁ Before lating Aging ⁽²⁾ A	After Aging ⁽²⁾	Aging (hours)	Aging (hours)			Before Aging	After Aging	Before Aging	After Aging	Before Aging	After Aging
1	0	. 2	4	15	0	1	1	0	0	1	3	2	3
2 ⁽¹⁾	0	0	0	30	15	0	0	0	0	0	1	0	1
3	1.2	1	0	30 .	15	0	1	0	0	1	1	1	1
4	2.3	0	0	50	30	0	0	0	0	0	0	0	1
5	5.2	0	0	75	50	0	0	0	0	0	0	0	1
6	7.5	0	0	150	50	0	0	0	0	0	0	0	0
7	10.2	0	0	200	75	0	0	0	0	0	0	0	0
8	21.3	0	0	>200	150	0	0	0	0	0	0	0	0
9	30.6	0	0	>200	150	0	0	0	0	0	0	0	0
10	39.5	0	0	>200	150	0	0	0	1	0	0	0	0
11	52.4	0	0	>200	150	0	0	3	2	0	0	0	0
12	58.0	. 0	0	150	75	0	0	5	5	0	2	0	0
13	69.3	0	0	150	75	0	0	10	7	0	5	1	2
14	76.5	1	0	75	50	0	1	10	7	3	5	3	5
15	83.7	0	0	50	30	1	1	10	10	5	7	4	7

(1)Sintered in H₂ atmosphere at 800° C.

⁽²⁾ Aging was conducted by heating gold-plated test pieces in the air at 450° C. for 10 minutes to impart an aging effect (i.e., to impart a corroding effect in the process).

EXAMPLE 2

Example 1 was repeated except that 5% of Fe was included in an Ni/Co alloy. Substantially the same results as in Example 1 were obtained.

While the invention has been described in detail and with reference to specific embodiment thereof, it will be apparent to one skilled in the art that various changes 10 and modifications can be made therein without departing from the spirit and scope thereof.

What is claimed is:

1. An electronic component, comprising a member consisting of:

- a ceramic board substrate having a metallized surface formed thereon;
- a metal alloy layer coated on the substrate, the metal alloy layer consisting essentially of nickel and cobalt, wherein the cobalt is contained in an amount of 7 to 40% by weight, wherein the metal alloy layer is formed in a thickness of 0.5 to 5 microns; and
- a gold-plated outer surface layer coated on said metal alloy, said gold-plated outer surface layer forming the outer-most surface of the electronic component, wherein the gold-plated outer surface layer is formed in a thickness of [0.5] 1.5 to 2 microns.

2. The electronic component of claim 1, wherein the balance of said alloy is nickel.

20

25

30

35

40

45

50

55

60