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(12) **United States Design Patent**
Arakawa et al.

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(54) **APPARATUS FOR EVALUATING SEMICONDUCTOR SUBSTRATE**

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(**) Term: **15 Years**

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(30) **Foreign Application Priority Data**

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(51) **LOC (14) Cl.** **15-09**

(52) **U.S. Cl.**
USPC **D15/122**

(58) **Field of Classification Search**
USPC D13/118, 158, 162, 184; D15/122, 138,
D15/141, 199
CPC H01L 21/70; H01L 21/67207; H01L
21/68742; H01L 21/67023
See application file for complete search history.

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(57) **CLAIM**

The ornamental design for an apparatus for evaluating semiconductor substrate, as shown and described.

DESCRIPTION

FIG. 1 is a front, top, and right side perspective view of an apparatus for evaluating semiconductor substrate according to the design;

FIG. 2 is a front elevational view thereof;

FIG. 3 is a rear elevational view thereof;

FIG. 4 is a left side elevational view thereof;

FIG. 5 is a right side elevational view thereof;

FIG. 6 is a top plan view thereof;

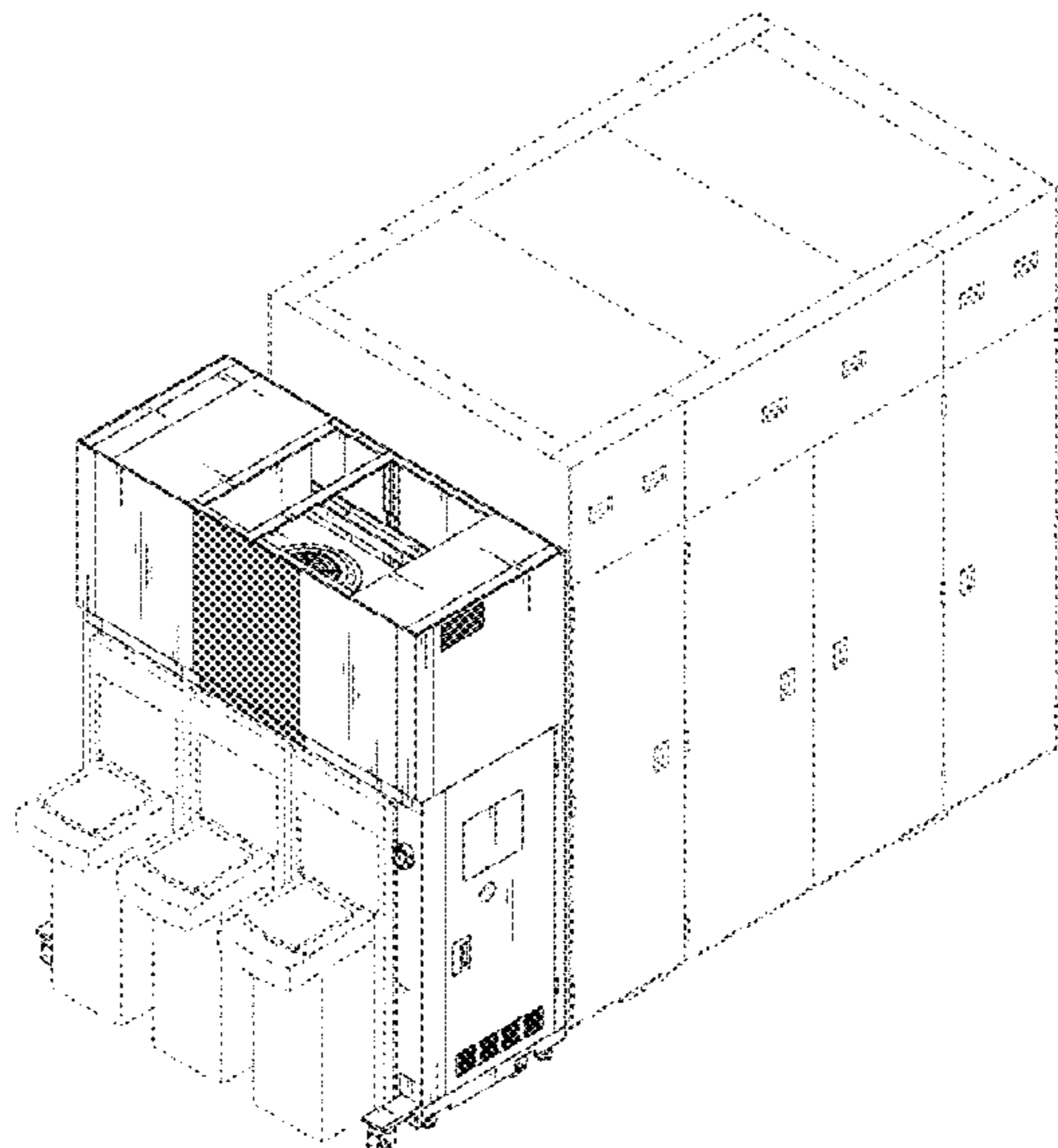
FIG. 7 is a bottom plan view thereof;

FIG. 8 is a cross-sectional view taken along line 8-8 of FIG. 2; and,

FIG. 9 is a cross-sectional view taken along line 9-9 of FIG. 2.

The broken lines illustrate portions of the apparatus for evaluating semiconductor substrate that form no part of the claimed design. The hatching shown in FIG. 8 and FIG. 9 represents unclaimed subject matter and forms no part of the claimed design.

1 Claim, 9 Drawing Sheets



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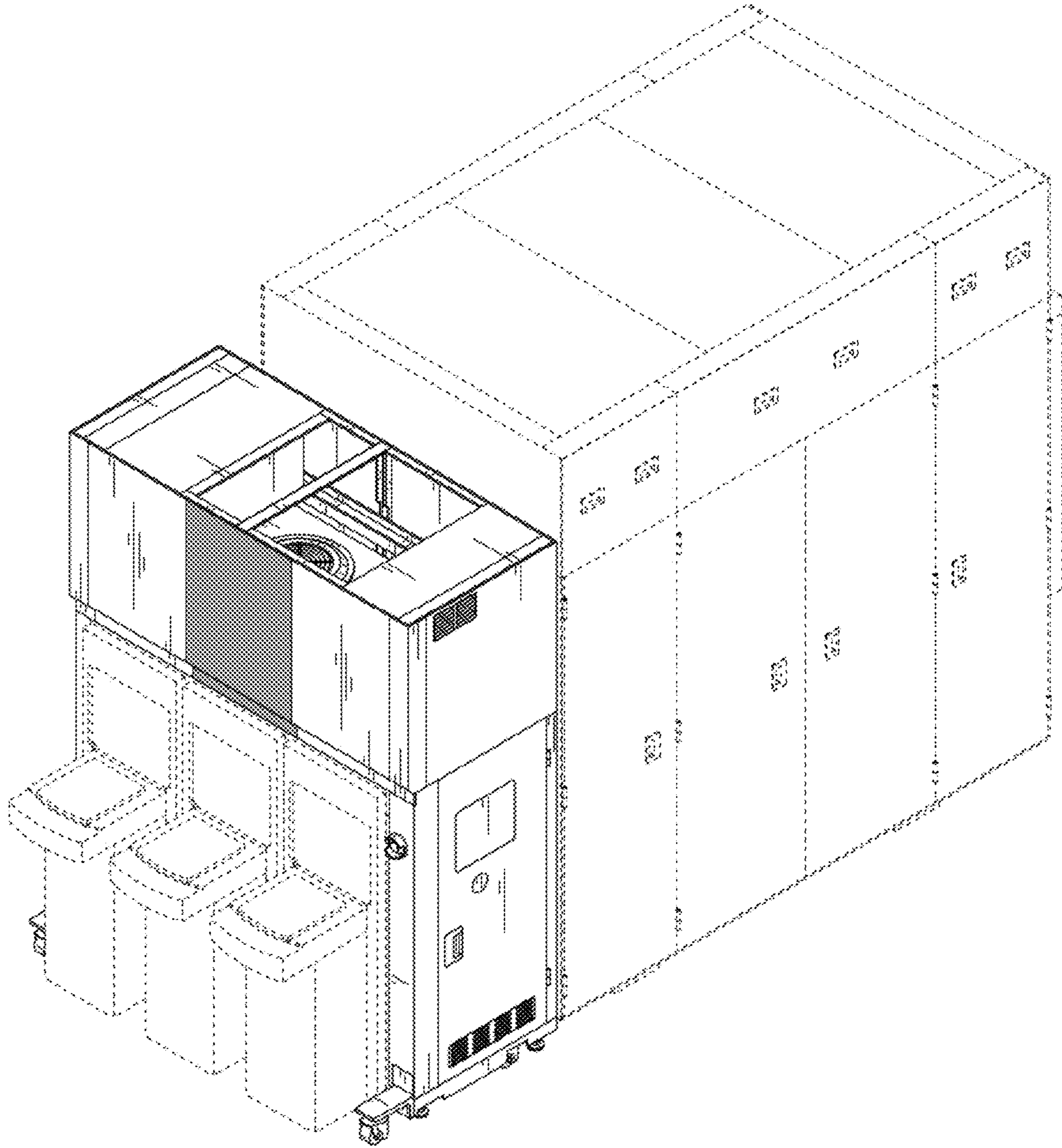


FIG. 1

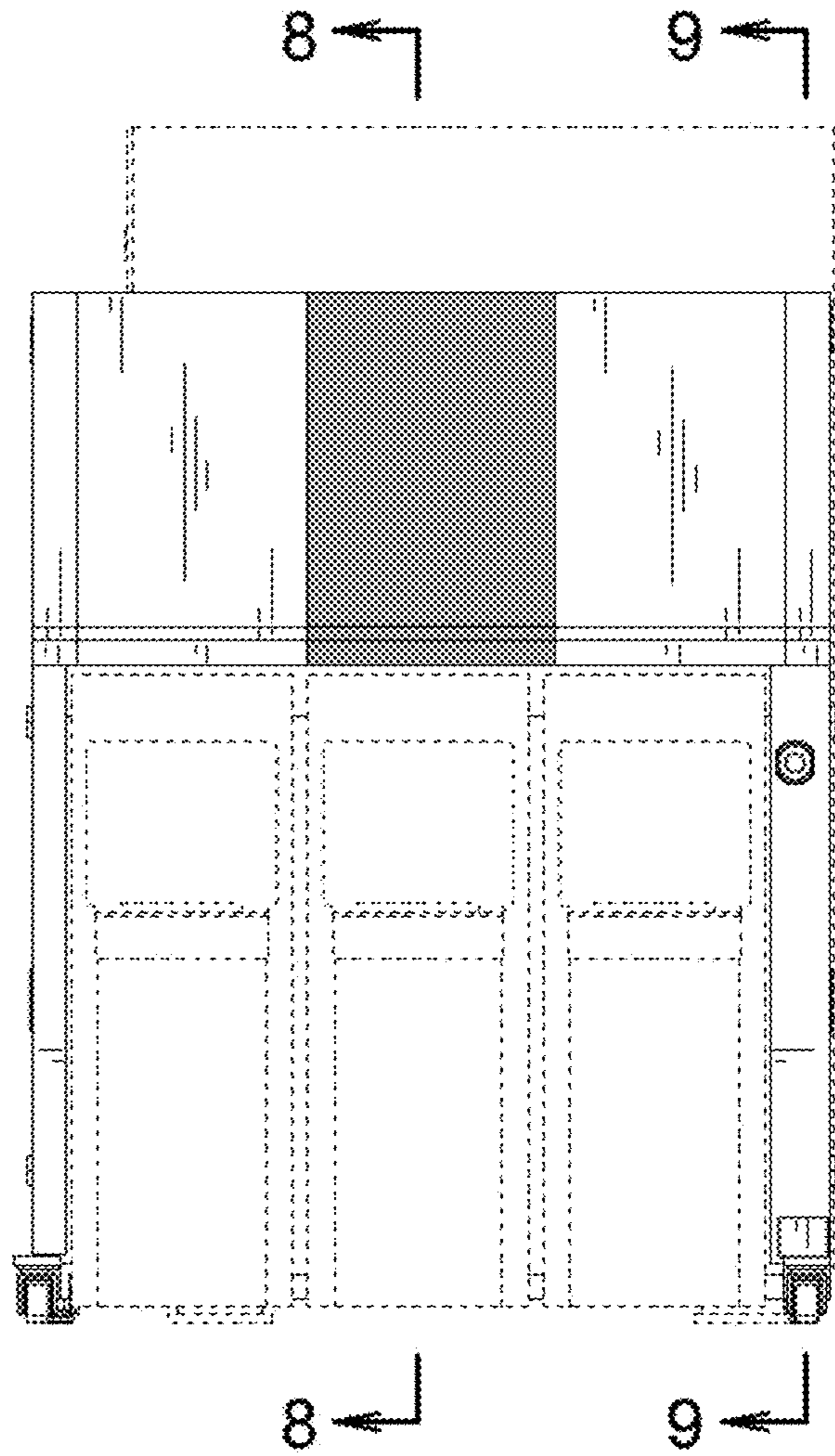


FIG. 2

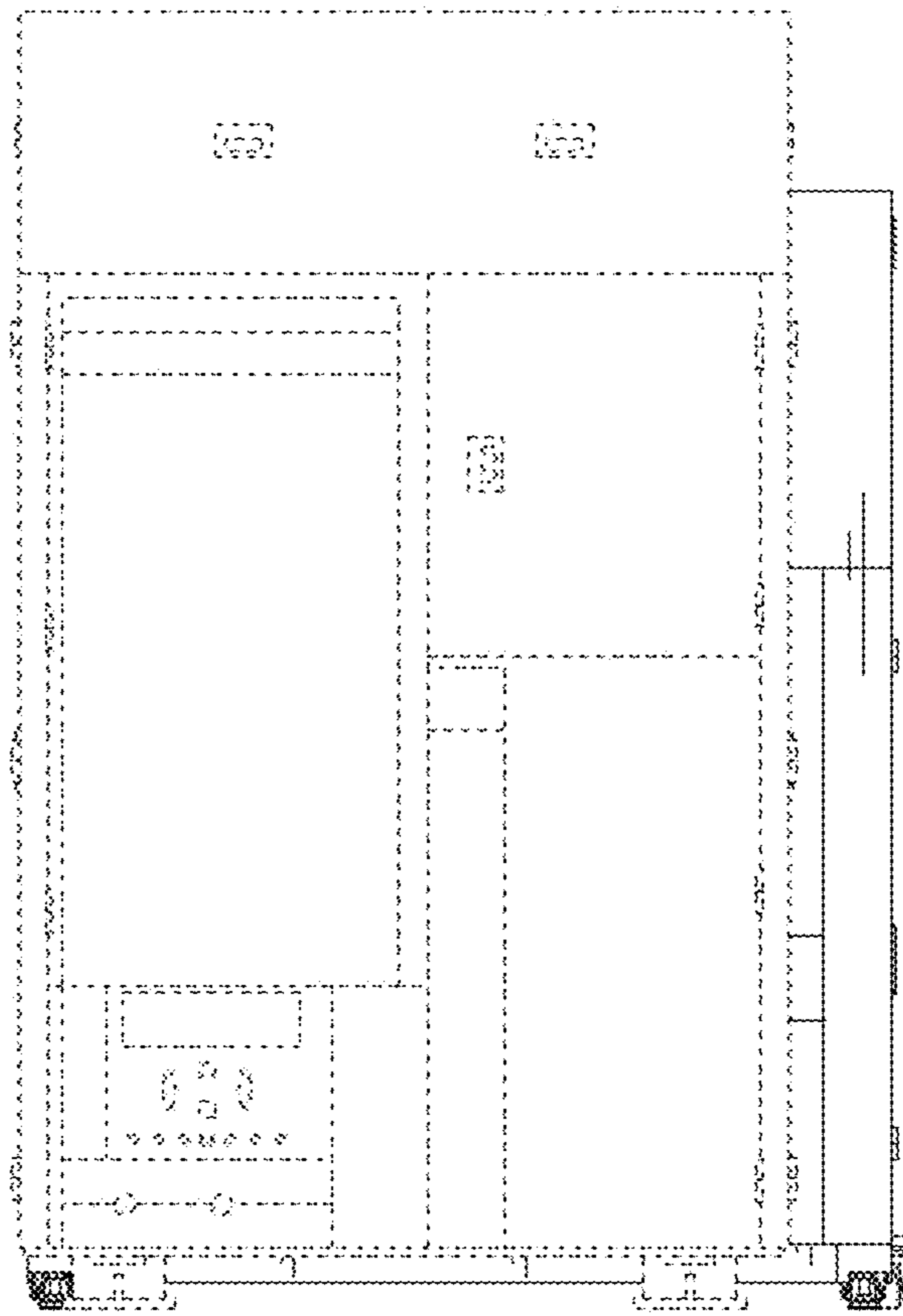


FIG. 3

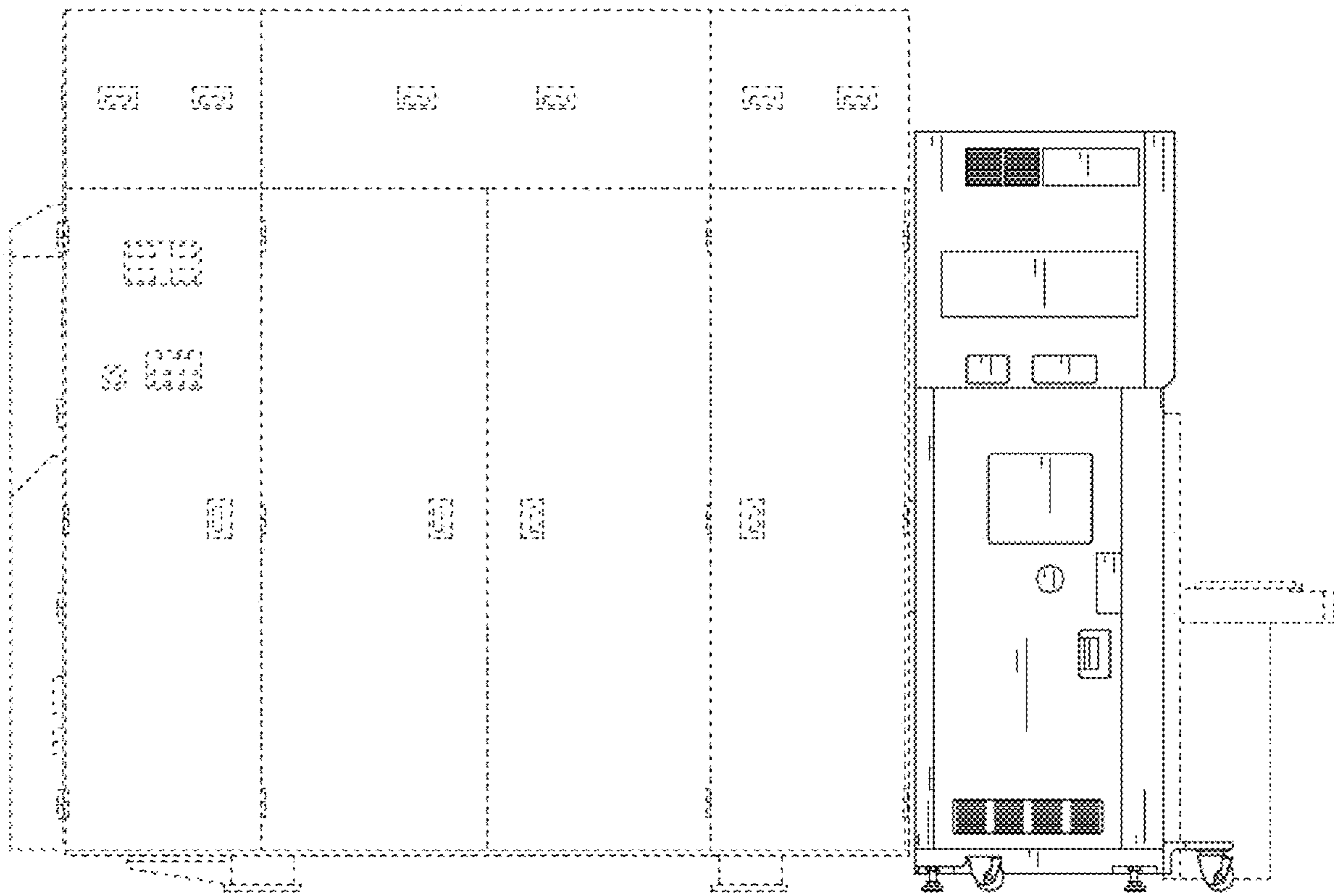


FIG. 4

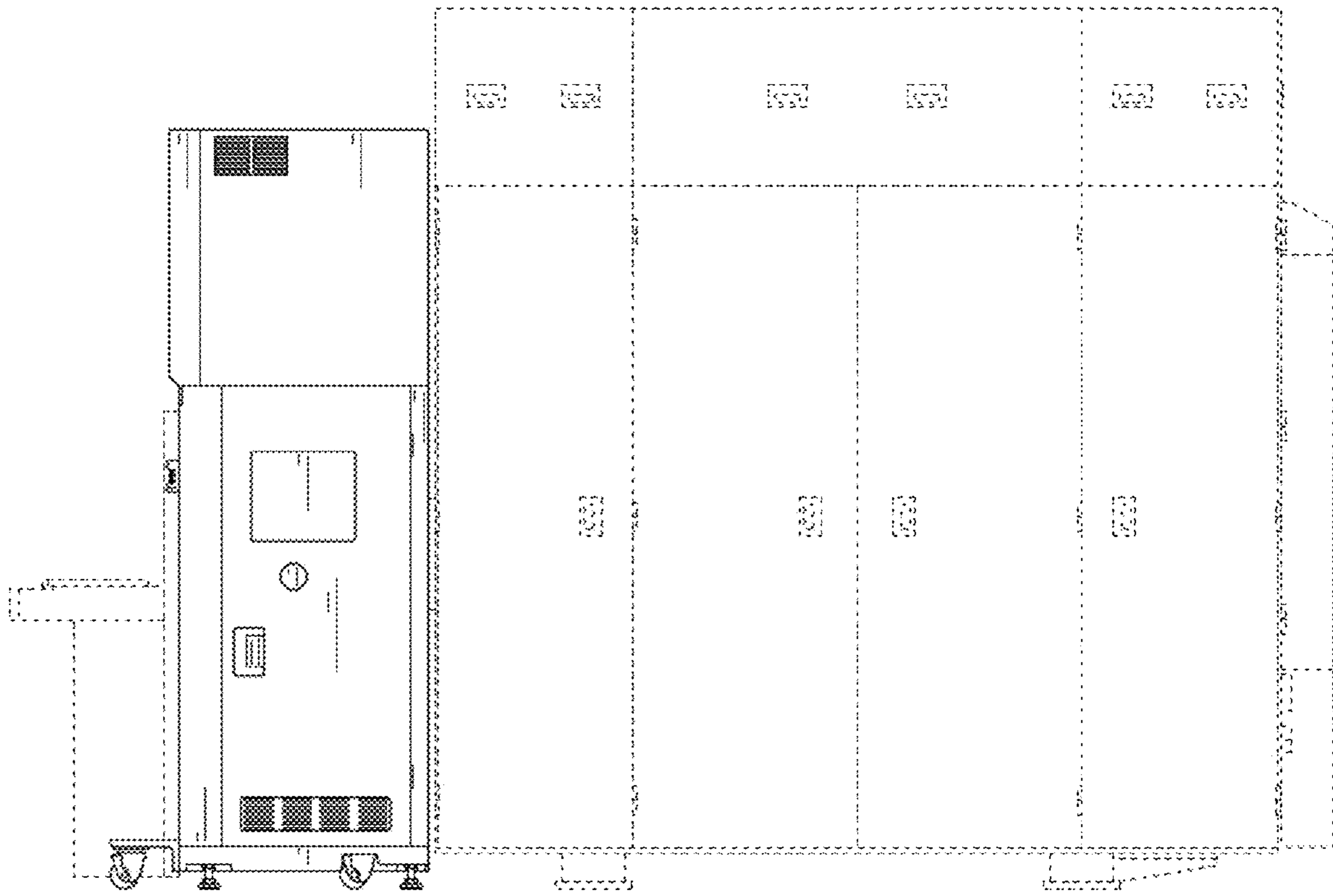


FIG. 5

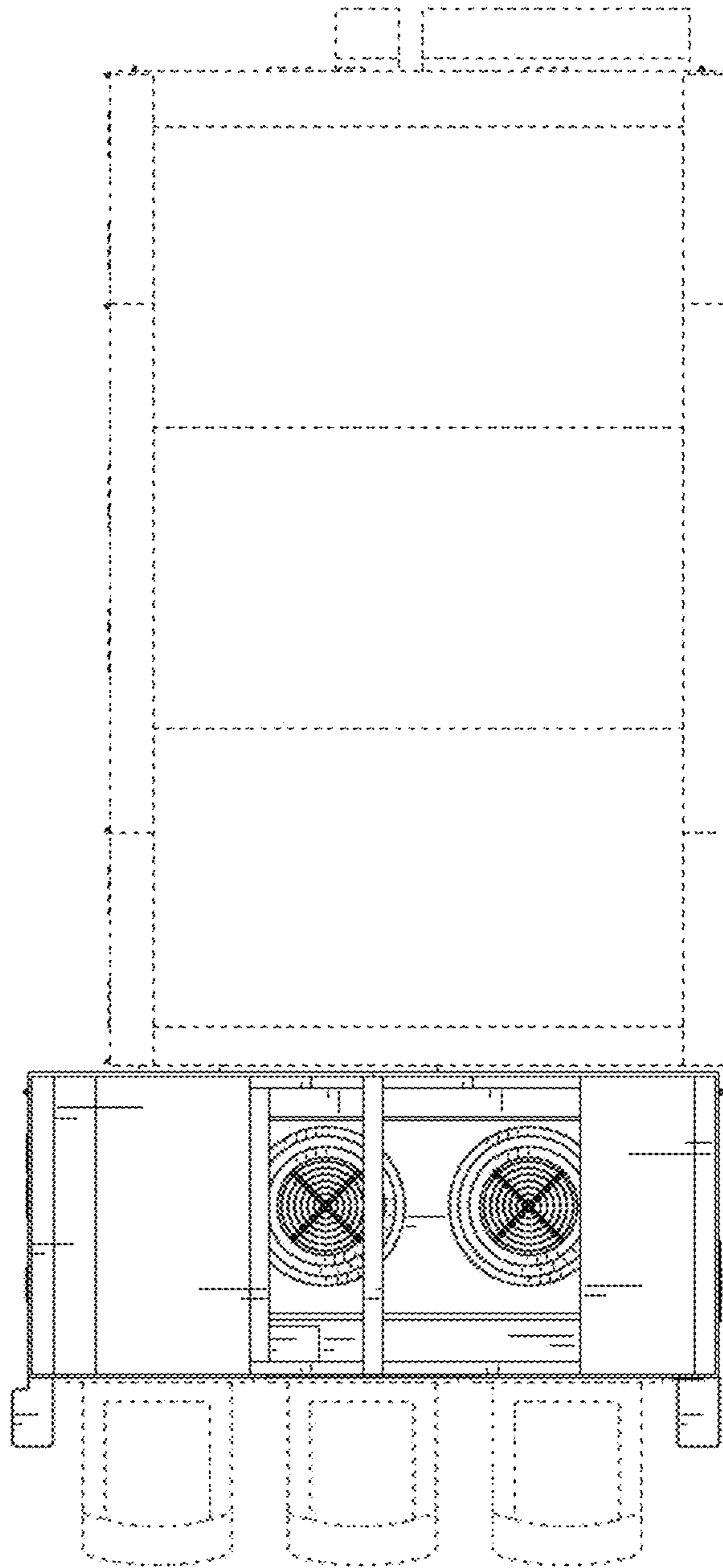


FIG. 6

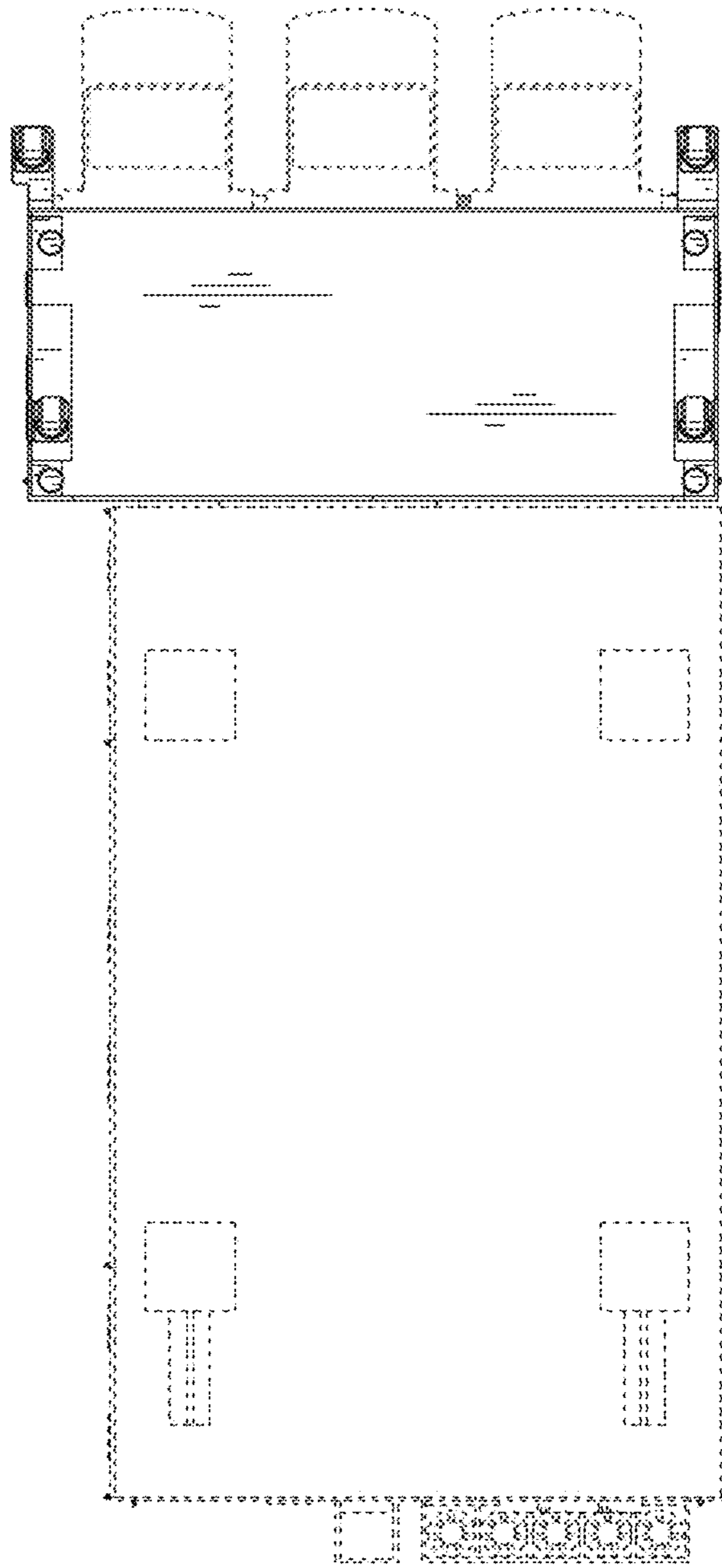


FIG. 7

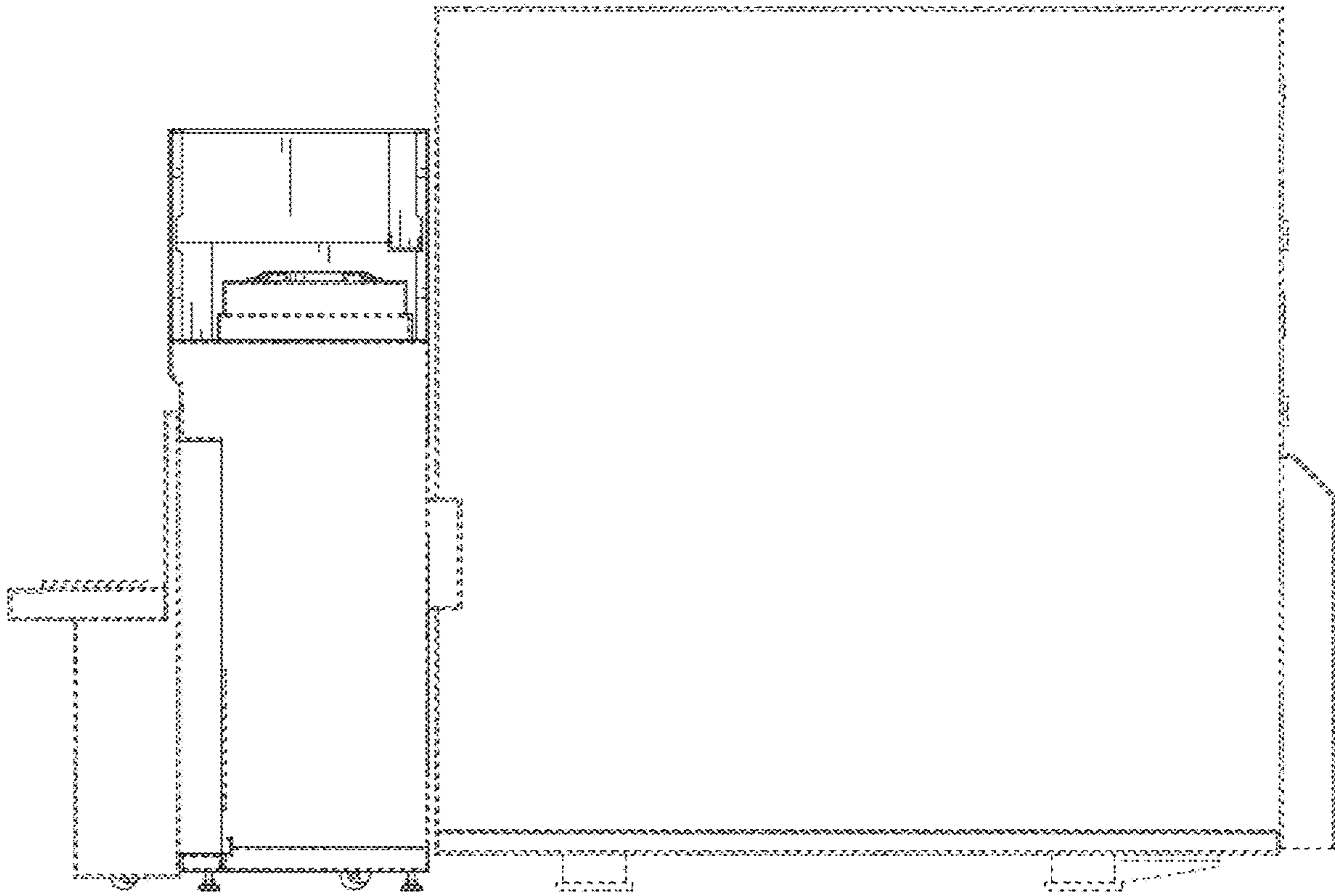


FIG. 8

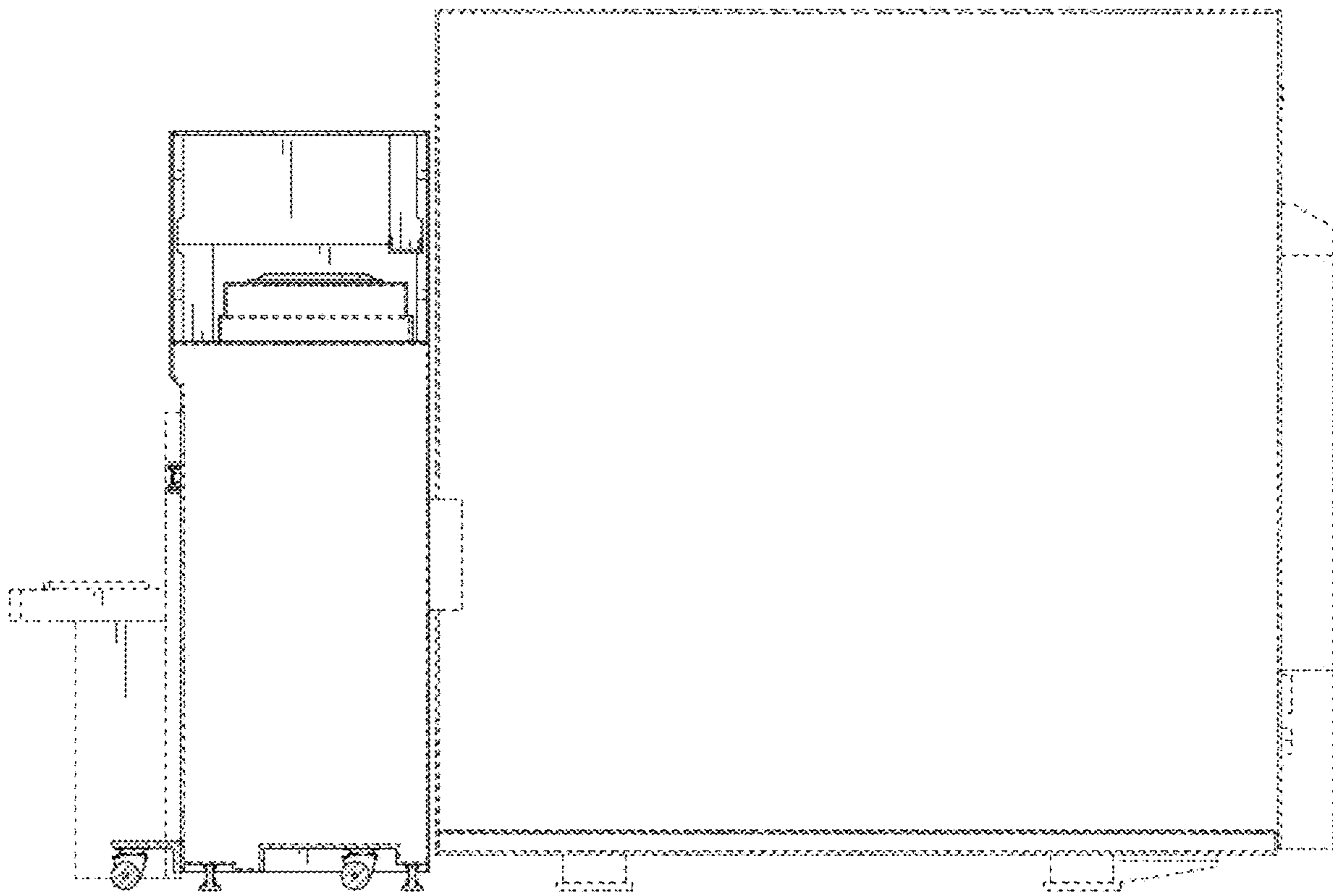


FIG. 9