US00D989144S

(12) **United States Design Patent**
Arakawa et al.

(10) **Patent No.: US D989,144 S**
(45) **Date of Patent: ** Jun. 13, 2023**

(54) **APPARATUS FOR EVALUATING SEMICONDUCTOR SUBSTRATE**

(71) Applicant: **Hitachi High-Tech Corporation**, Tokyo (JP)

(72) Inventors: **Masayuki Arakawa**, Tokyo (JP); **Junpei Hokari**, Tokyo (JP); **Akira Kojima**, Tokyo (JP); **Masaki Mizuochi**, Tokyo (JP); **Tomokazu Kobayashi**, Tokyo (JP); **Takaaki Kikuchi**, Tokyo (JP)

(73) Assignee: **Hitachi High-Tech Corporation**, Tokyo (JP)

(**) Term: **15 Years**

(21) Appl. No.: **29/789,674**

(22) Filed: **Oct. 13, 2021**

(30) **Foreign Application Priority Data**

May 14, 2021 (KR) 30-2021-0023150

(51) **LOC (14) Cl.** **15-09**

(52) **U.S. Cl.**
USPC **D15/122**

(58) **Field of Classification Search**
USPC D13/118, 158, 162, 184; D15/122, 138, D15/141, 199
CPC H01L 21/70; H01L 21/67207; H01L 21/68742; H01L 21/67023
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,281,320	A	*	1/1994	Turner	H01L 21/67751 269/254 R
D350,490	S	*	9/1994	Takao	D10/75
D352,911	S	*	11/1994	Yamamoto	D10/75
D365,584	S	*	12/1995	Nakagome	D15/199
D415,184	S	*	10/1999	Anai	D15/199
D415,776	S	*	10/1999	Anai	D15/199
D426,785	S	*	6/2000	Asai	D10/75
D427,088	S	*	6/2000	Asai	D10/75
D447,967	S	*	9/2001	Terada	D10/75

(Continued)

OTHER PUBLICATIONS

U.S. Appl. No. 29/789,675, filed Oct. 13, 2021.

(Continued)

Primary Examiner — Patricia A Palasik
(74) *Attorney, Agent, or Firm* — Crowell & Moring LLP

(57) **CLAIM**

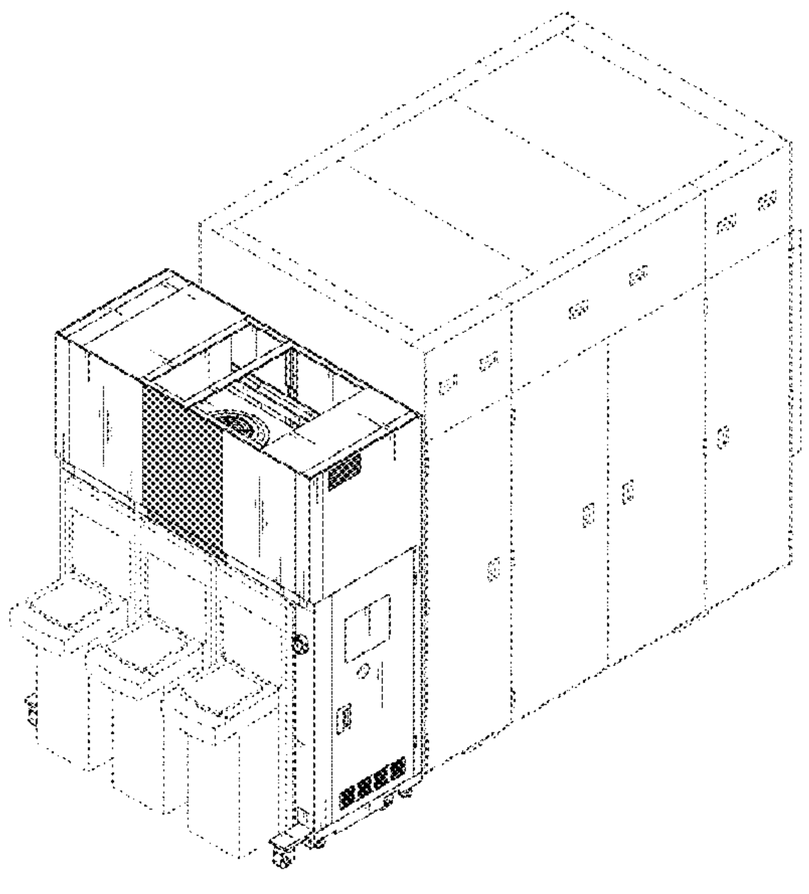
The ornamental design for an apparatus for evaluating semiconductor substrate, as shown and described.

DESCRIPTION

FIG. **1** is a front, top, and right side perspective view of an apparatus for evaluating semiconductor substrate according to the design;
FIG. **2** is a front elevational view thereof;
FIG. **3** is a rear elevational view thereof;
FIG. **4** is a left side elevational view thereof;
FIG. **5** is a right side elevational view thereof;
FIG. **6** is a top plan view thereof;
FIG. **7** is a bottom plan view thereof;
FIG. **8** is a cross-sectional view taken along line **8-8** of FIG. **2**; and,
FIG. **9** is a cross-sectional view taken along line **9-9** of FIG. **2**.

The broken lines illustrate portions of the apparatus for evaluating semiconductor substrate that form no part of the claimed design. The hatching shown in FIG. **8** and FIG. **9** represents unclaimed subject matter and forms no part of the claimed design.

1 Claim, 9 Drawing Sheets



(56) **References Cited**

U.S. PATENT DOCUMENTS

6,454,472	B1 *	9/2002	Kim	G03D 5/00 414/940
6,942,738	B1 *	9/2005	Nelson	H01L 21/68707 414/416.03
D546,354	S *	7/2007	Kihara	D15/199
D637,098	S *	5/2011	Oonuma	D10/75
D657,068	S *	4/2012	Shibata	D24/216
D730,894	S *	6/2015	Hokari	D14/364
D733,134	S *	6/2015	Utsuki	D14/364
D733,135	S *	6/2015	Utsuki	D14/364
D858,590	S *	9/2019	Kazaoka	D15/127
D905,139	S *	12/2020	Ferraro	D15/127
2002/0150449	A1 *	10/2002	Nelson	H01L 21/67754 414/940
2003/0136513	A1 *	7/2003	Lee	H01L 21/67748 156/345.31
2006/0057799	A1 *	3/2006	Horiguchi	H01L 21/67115 438/200
2010/0189880	A1 *	7/2010	Gibson	H01L 21/67288 427/10
2022/0254665	A1 *	8/2022	Wu	H01L 21/68742

OTHER PUBLICATIONS

U.S. Appl. No. 29/789,677, filed Oct. 13, 2021.
United States Notice of Allowance issued in U.S. Appl. No. 29/789,675 dated Mar. 8, 2023 (nine (9) pages).
United States Notice of Allowance issued in U.S. Appl. No. 29/789,677 dated Mar. 8, 2023 (nine (9) pages).

* cited by examiner

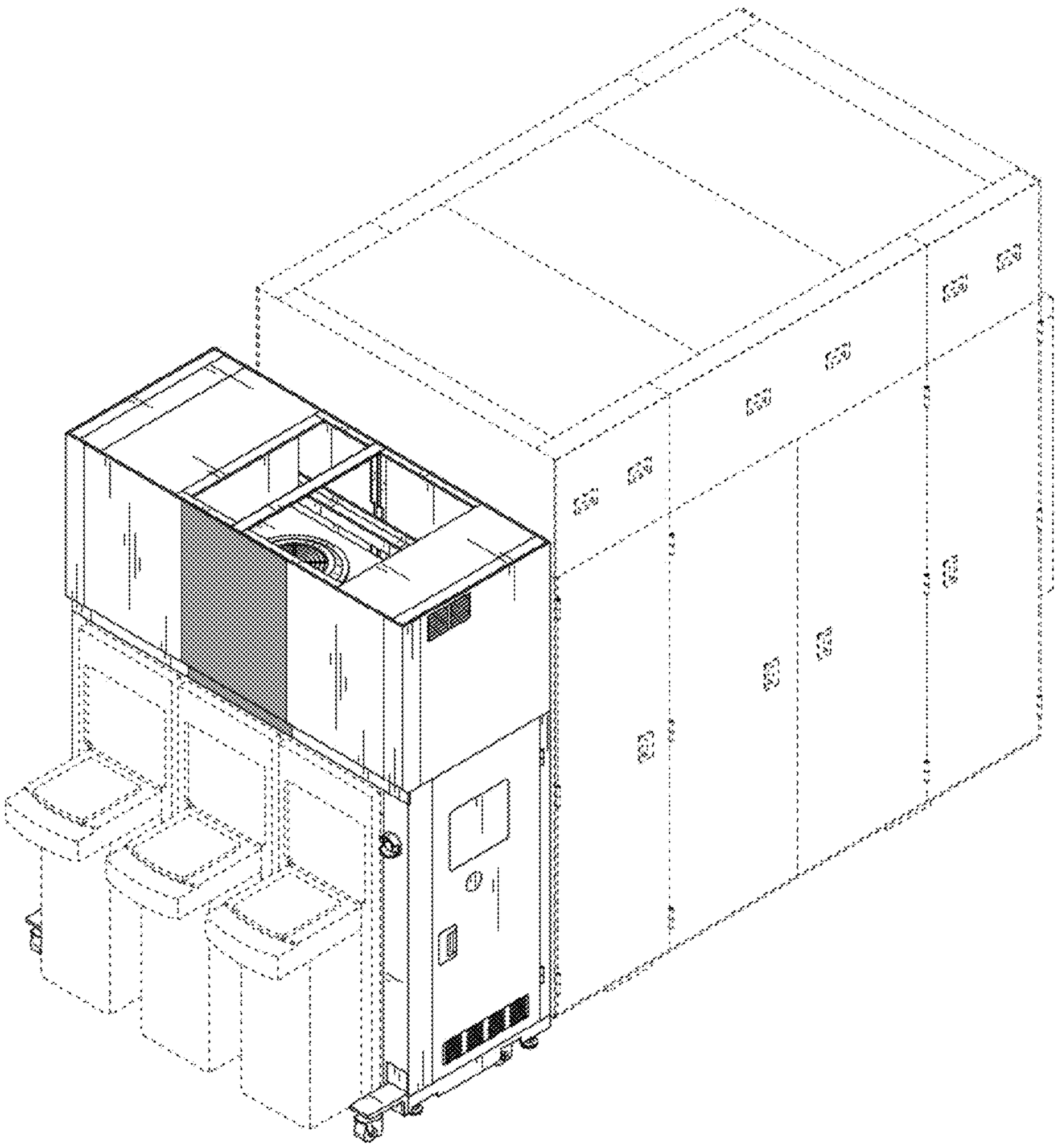


FIG. 1

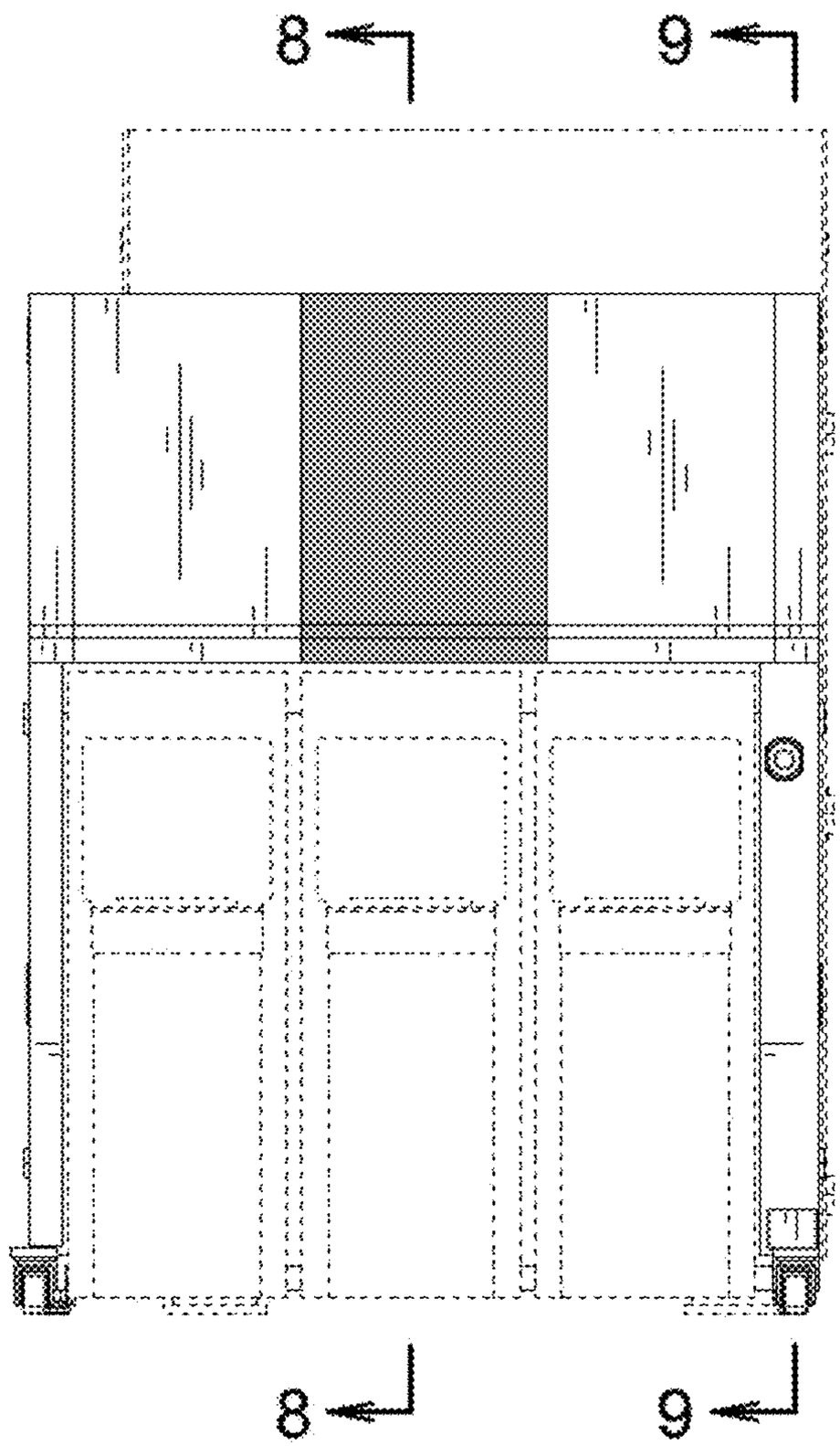


FIG. 2

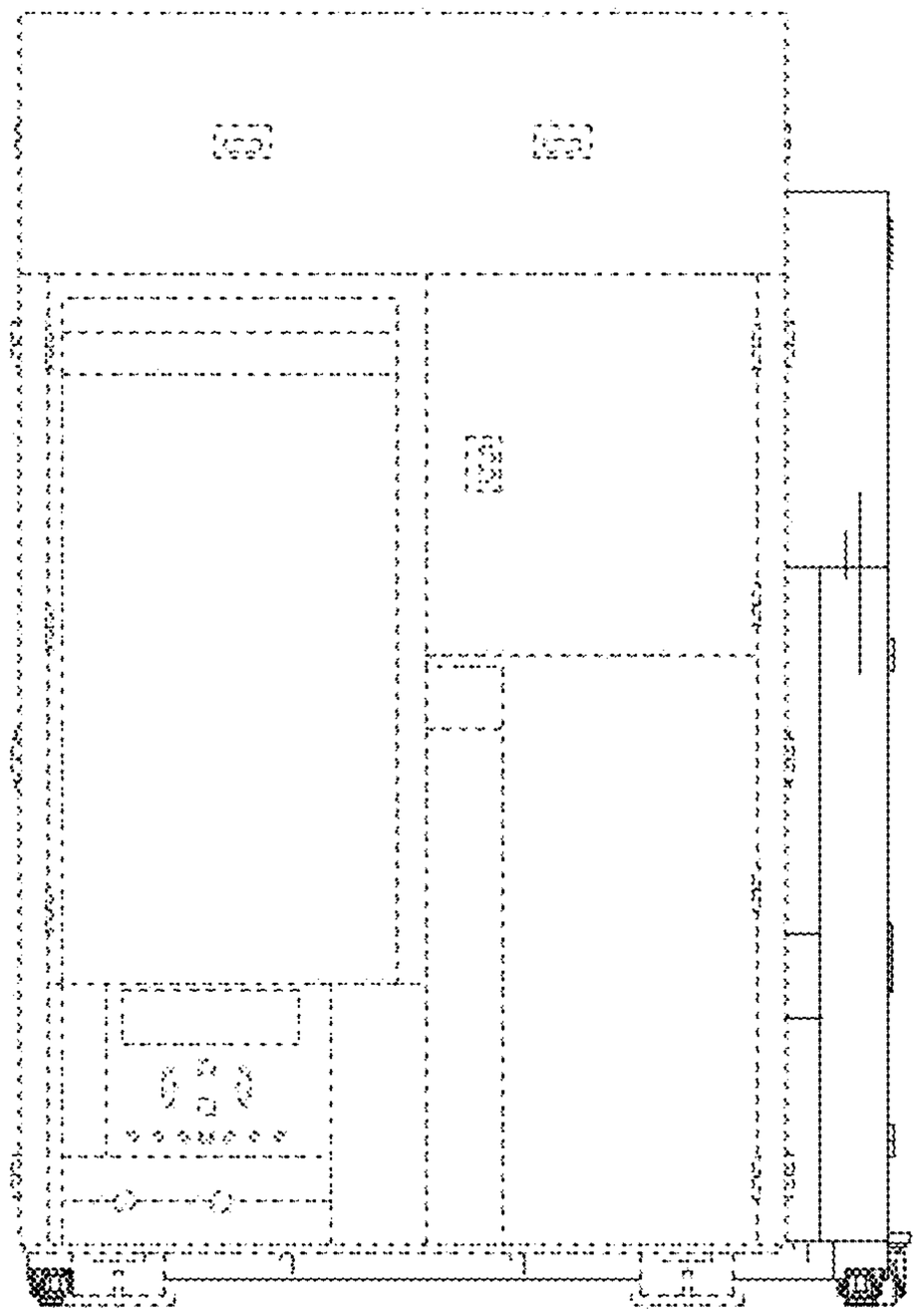


FIG. 3

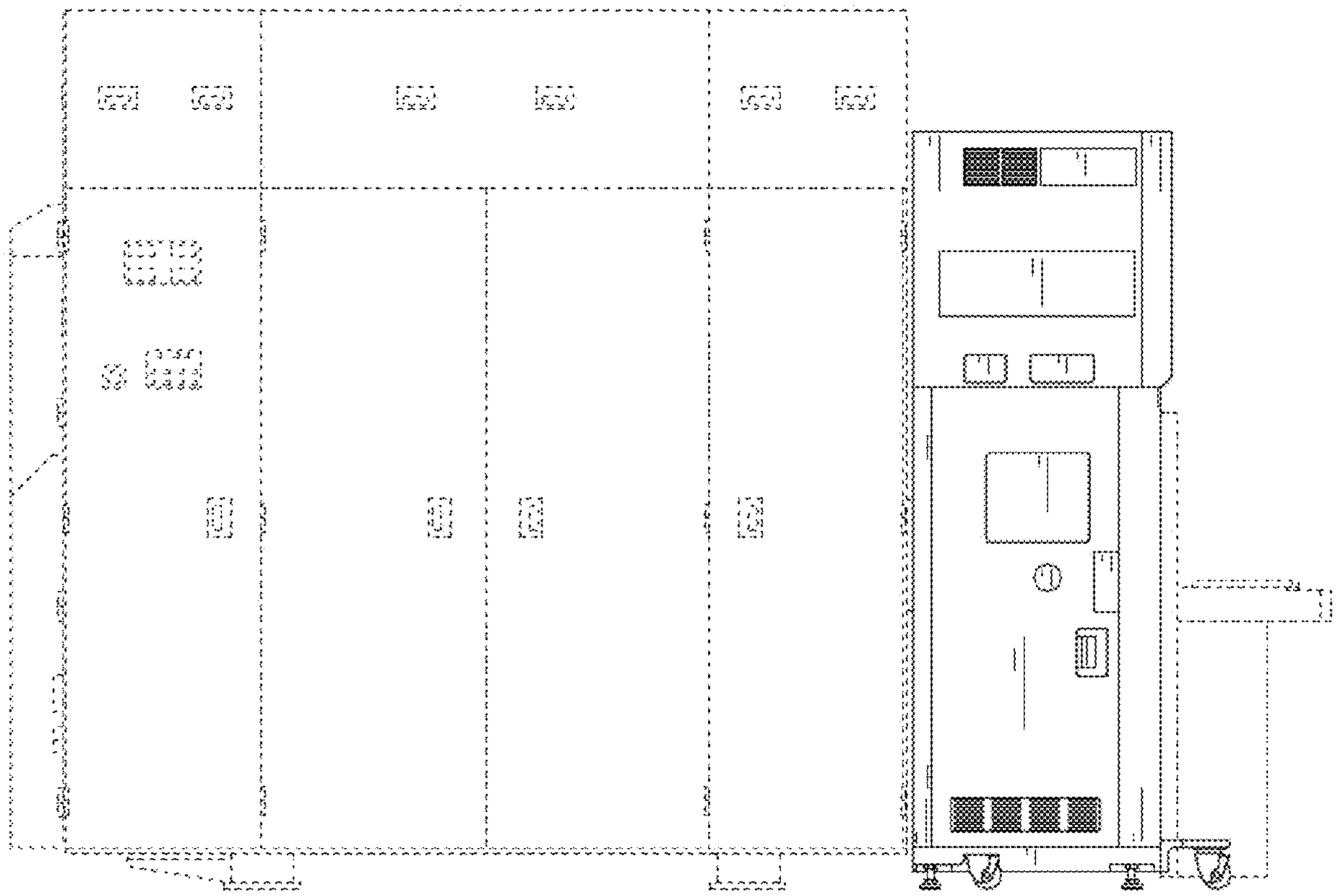


FIG. 4

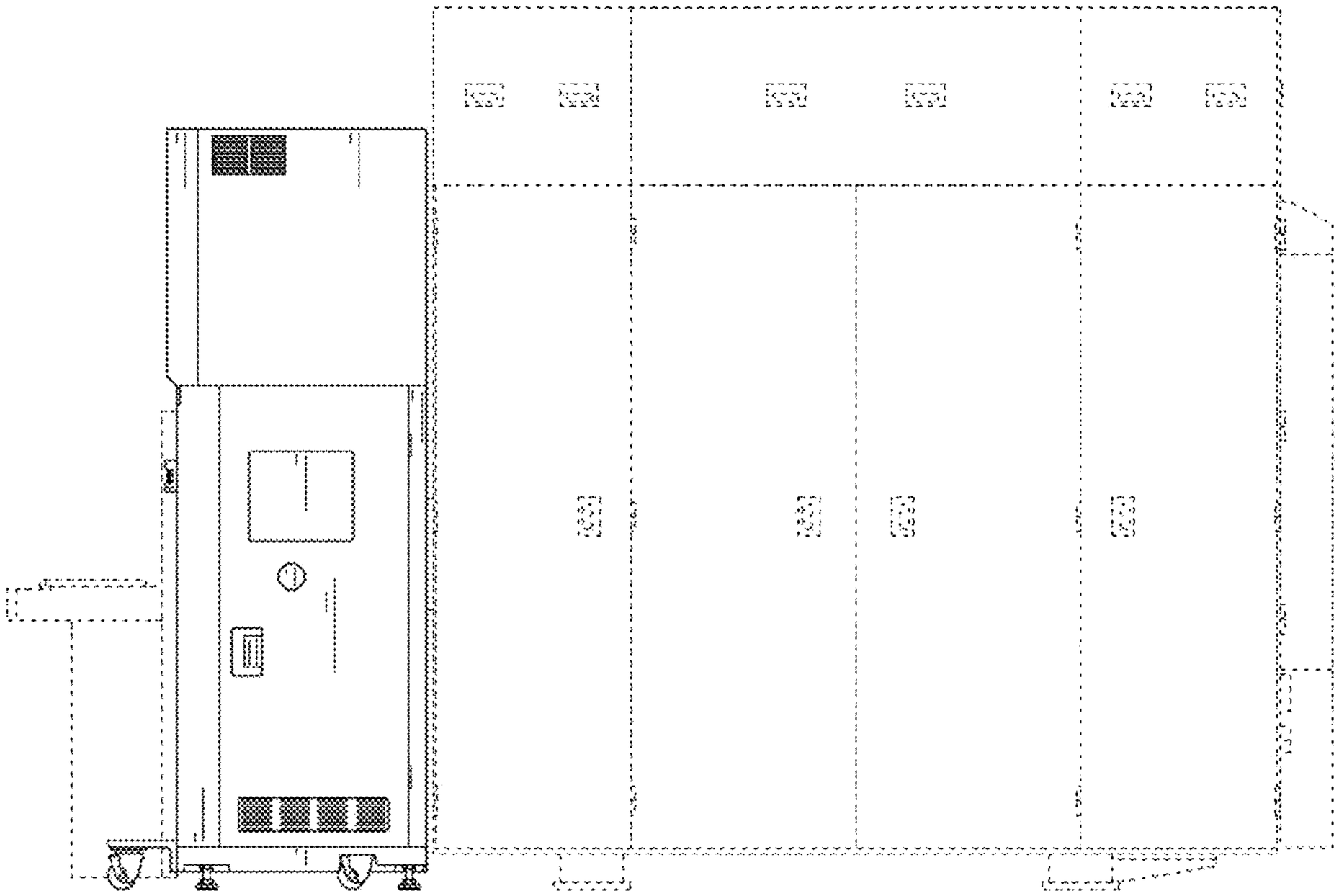


FIG. 5

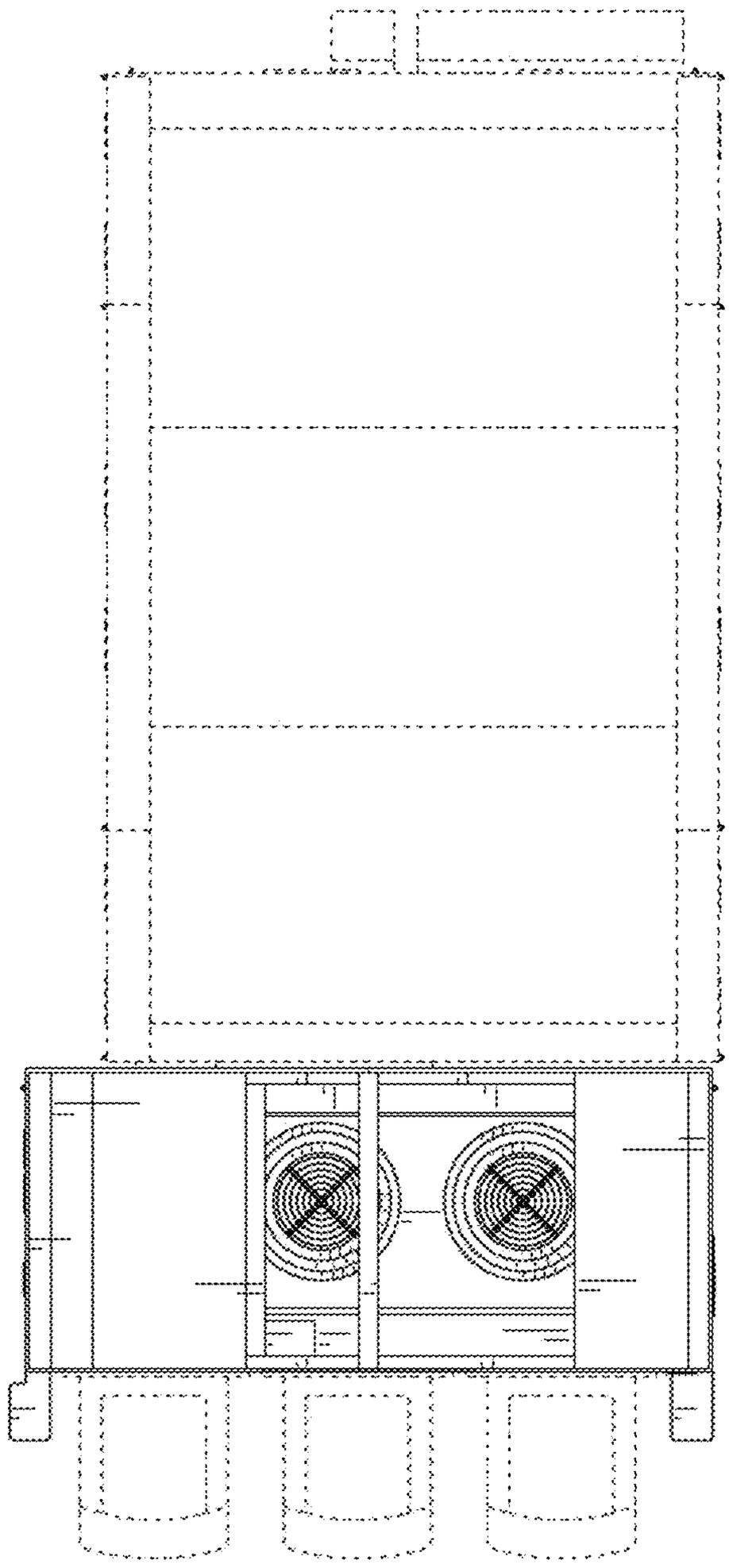


FIG. 6

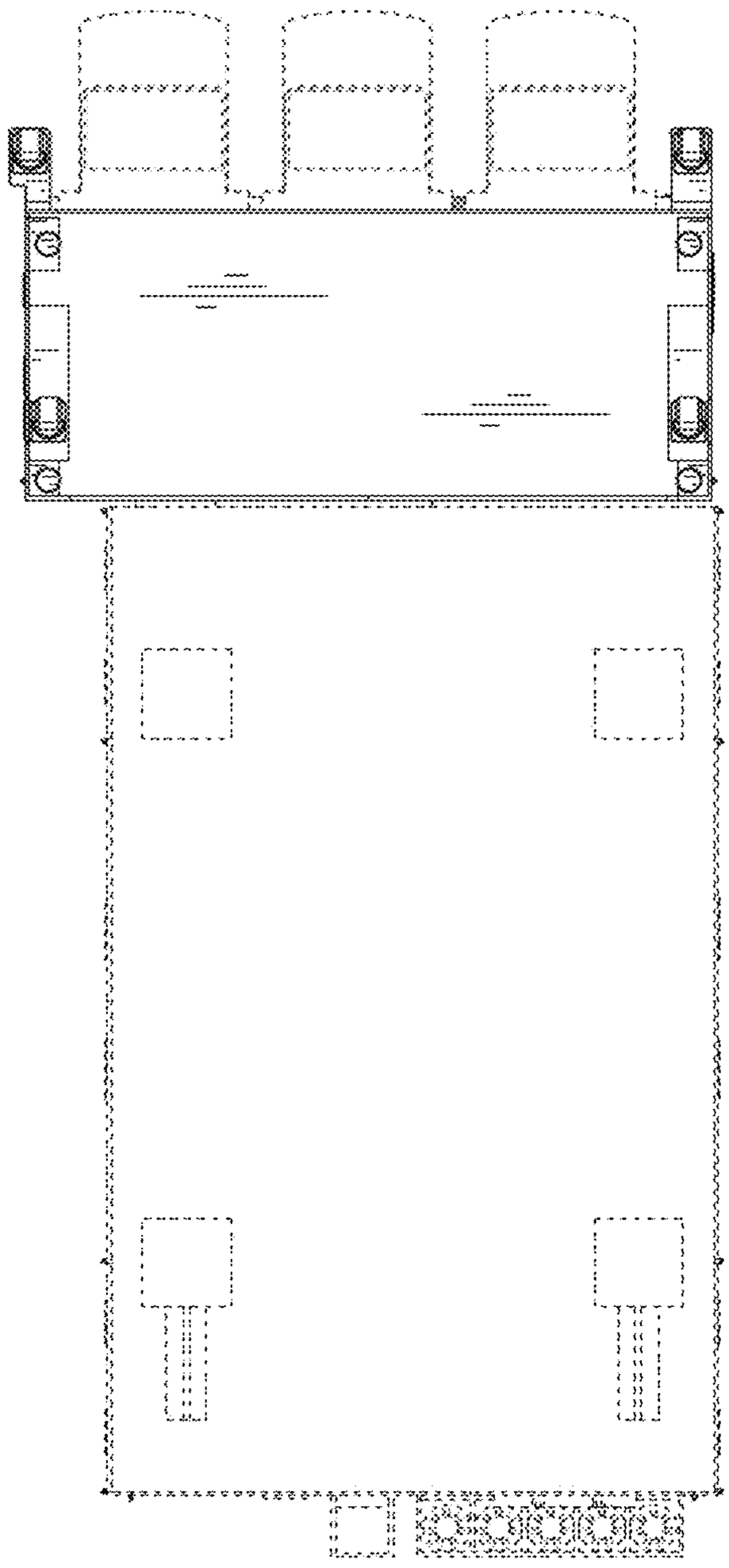


FIG. 7

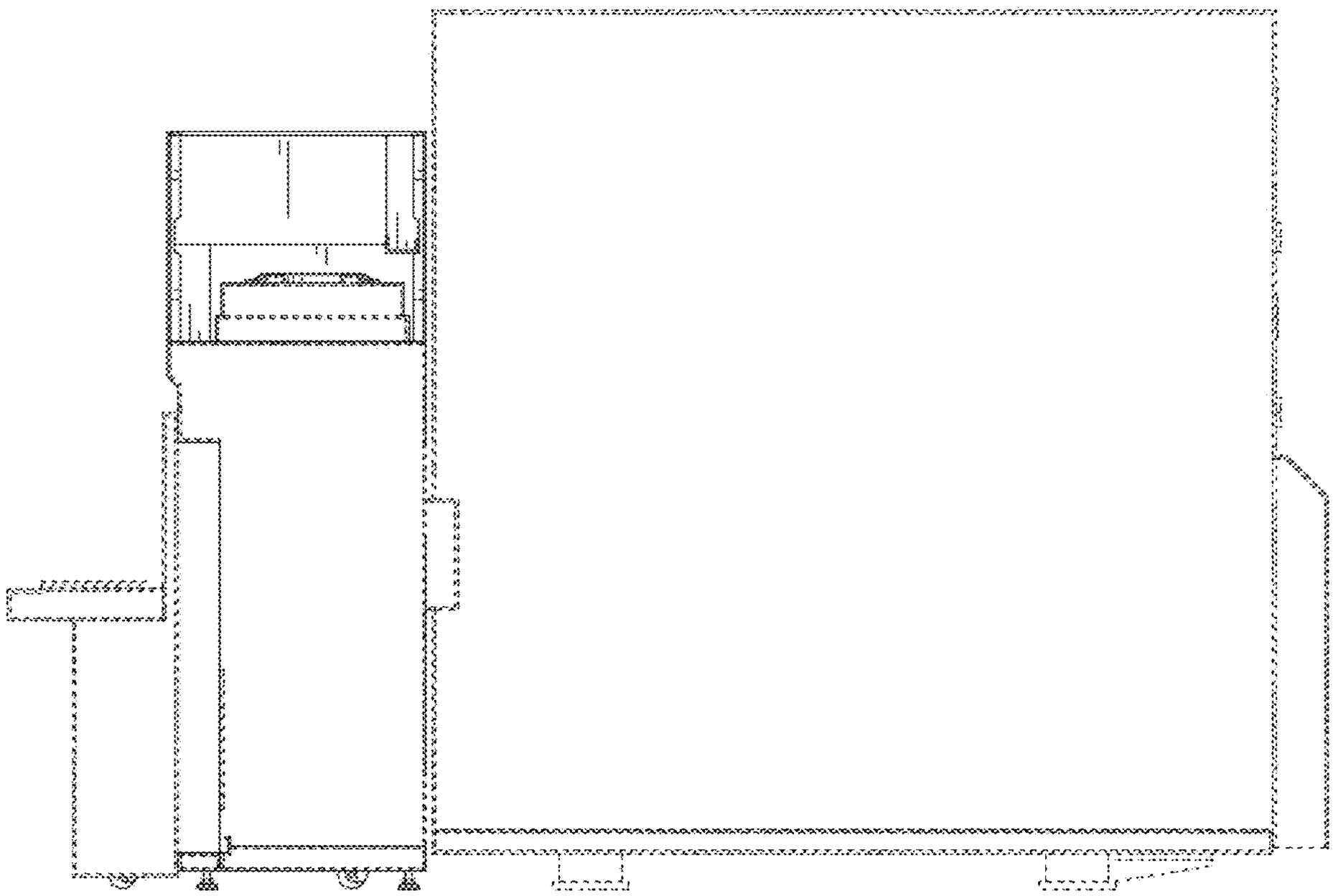


FIG. 8

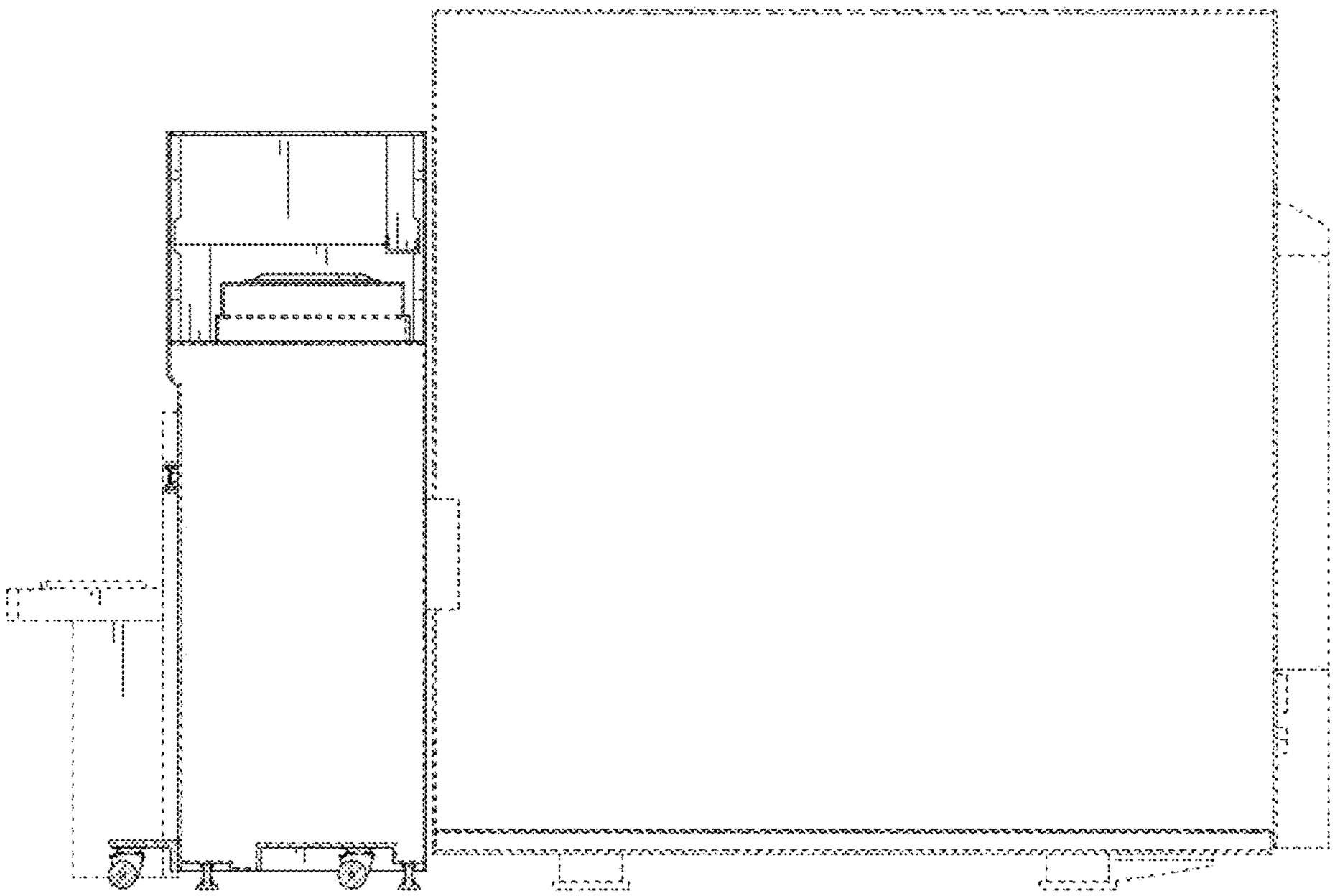


FIG. 9