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(12) **United States Design Patent** (10) **Patent No.:** **US D984,972 S**
Shi (45) **Date of Patent:** **** May 2, 2023**

(54) **ELECTROSTATIC CHUCK FOR SEMICONDUCTOR MANUFACTURE**

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(51) **LOC (14) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182; D15/140**

(58) **Field of Classification Search**

USPC **D13/182; D15/140**

CPC **H01L 21/67098; H01L 21/67109; H01L 21/683; H01L 21/6831; H01L 21/6833; H01L 21/6835; H01L 21/68; H01L 21/67; B23Q 3/15; B23Q 3/154; B23Q 3/1543; B23Q 3/1546; B23B 2270/38; B23B 31/28; G03F 7/70708; G03F 7/707; H02N 13/00; H02N 15/00**

See application file for complete search history.

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Primary Examiner — Elizabeth J Oswecki

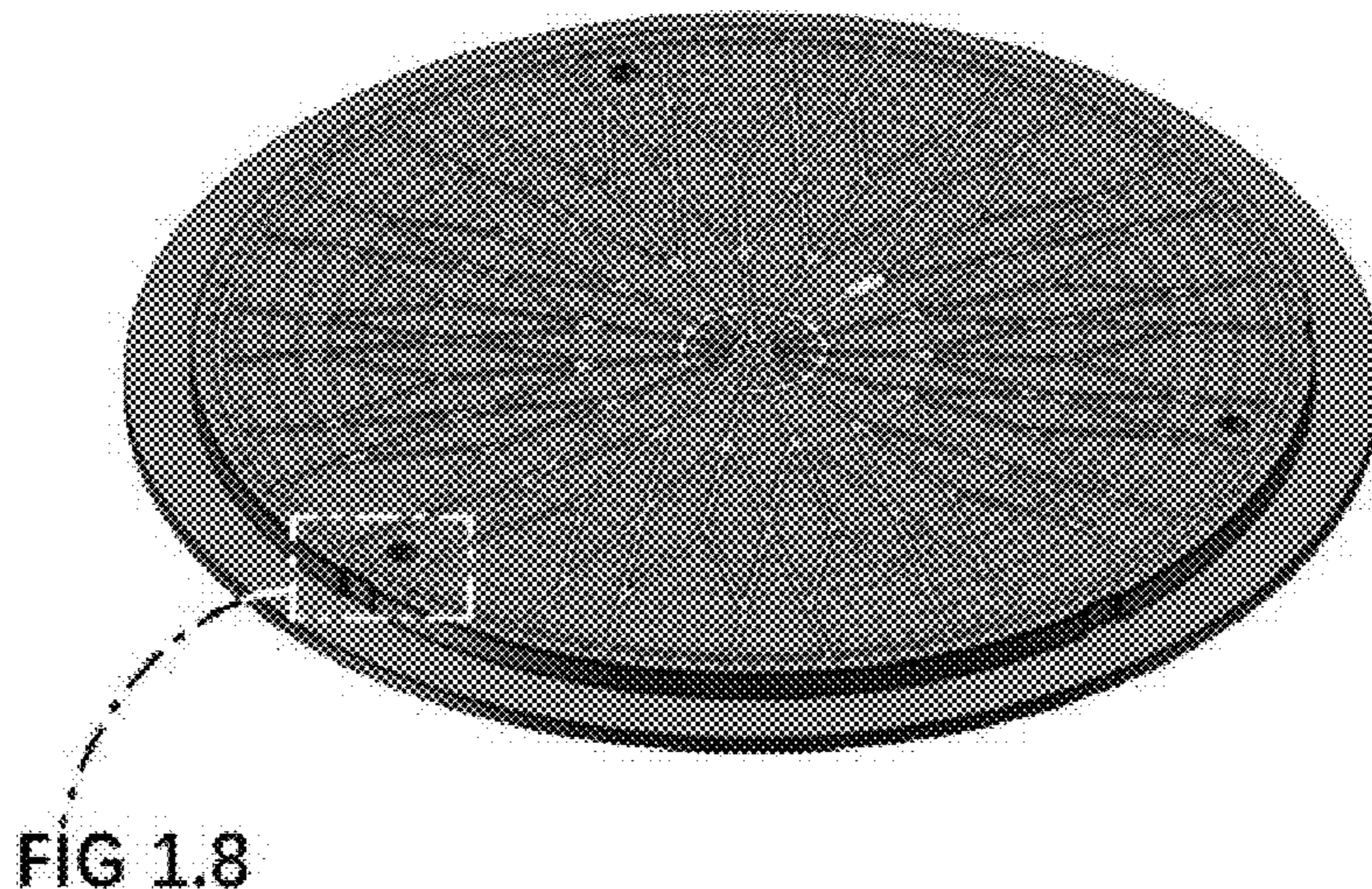
(57) **CLAIM**

The ornamental design for an electrostatic chuck semiconductor manufacture, as shown and described.

DESCRIPTION

1. Electrostatic chuck for semiconductor manufacture
FIG. 1.1 is a front perspective view of an electrostatic chuck for semiconductor manufacture showing my new design;
FIG. 1.2 is another front perspective view thereof;
FIG. 1.3 is a front elevation view thereof;
FIG. 1.4 is a top plan view thereof;
FIG. 1.5 is a bottom plan view thereof;
FIG. 1.6 is a left side elevation view thereof;
FIG. 1.7 is a right side elevation view thereof;
FIG. 1.8 is an enlarged portion view labeled, "Fig. 1.8" in Fig. 1.1; and
FIG. 1.9 is an enlarged portion view labeled, "Fig. 1.9" in Fig. 1.2.
The dashed-dot lines in Figs. 1.1, 1.2, 1.8 and 1.9 denote the boundaries of the enlarged portion views shown in Figs. 1.8 and 1.9 and form no part of the claimed design.

1 Claim, 9 Drawing Sheets



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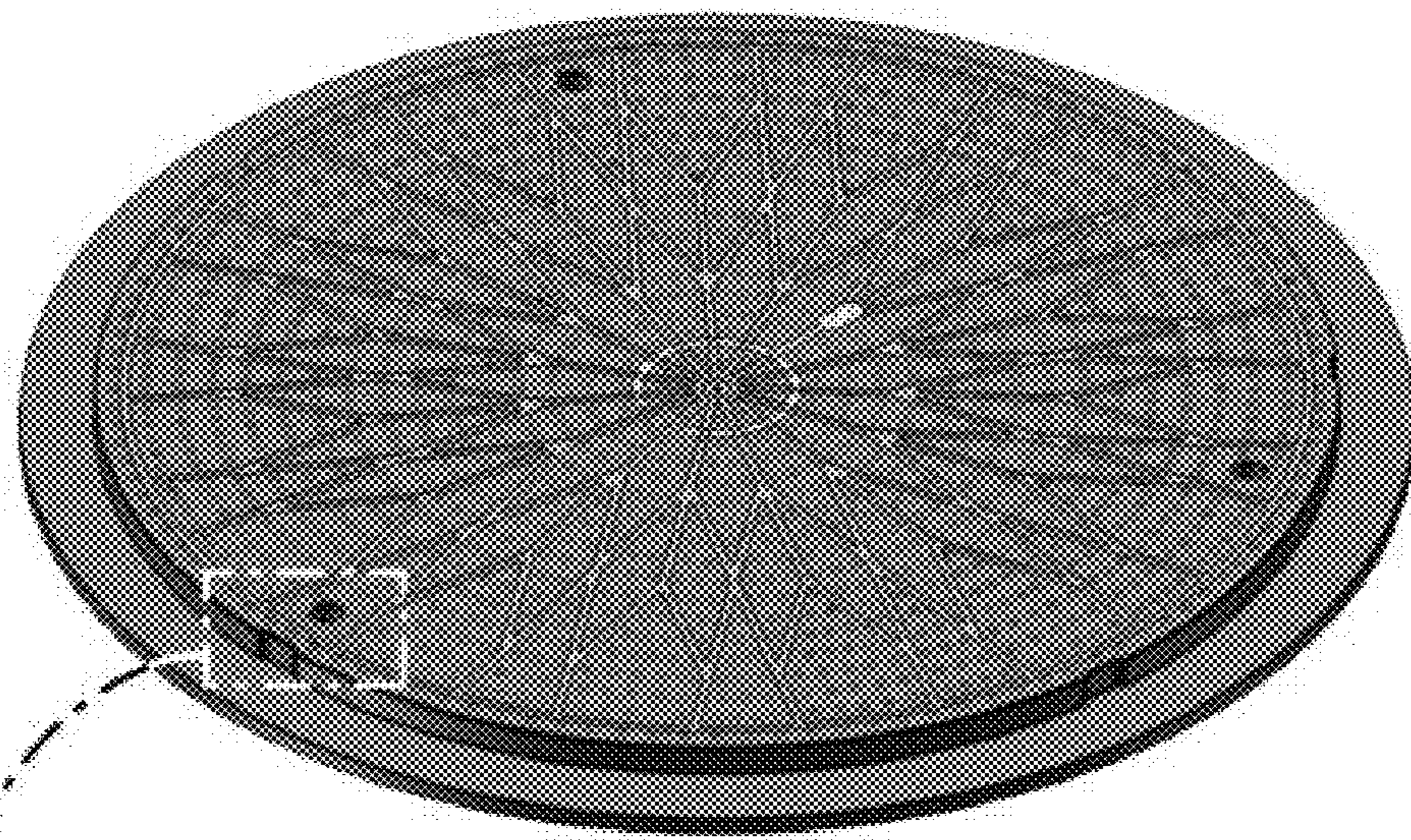


FIG 1.8

FIG 1.1

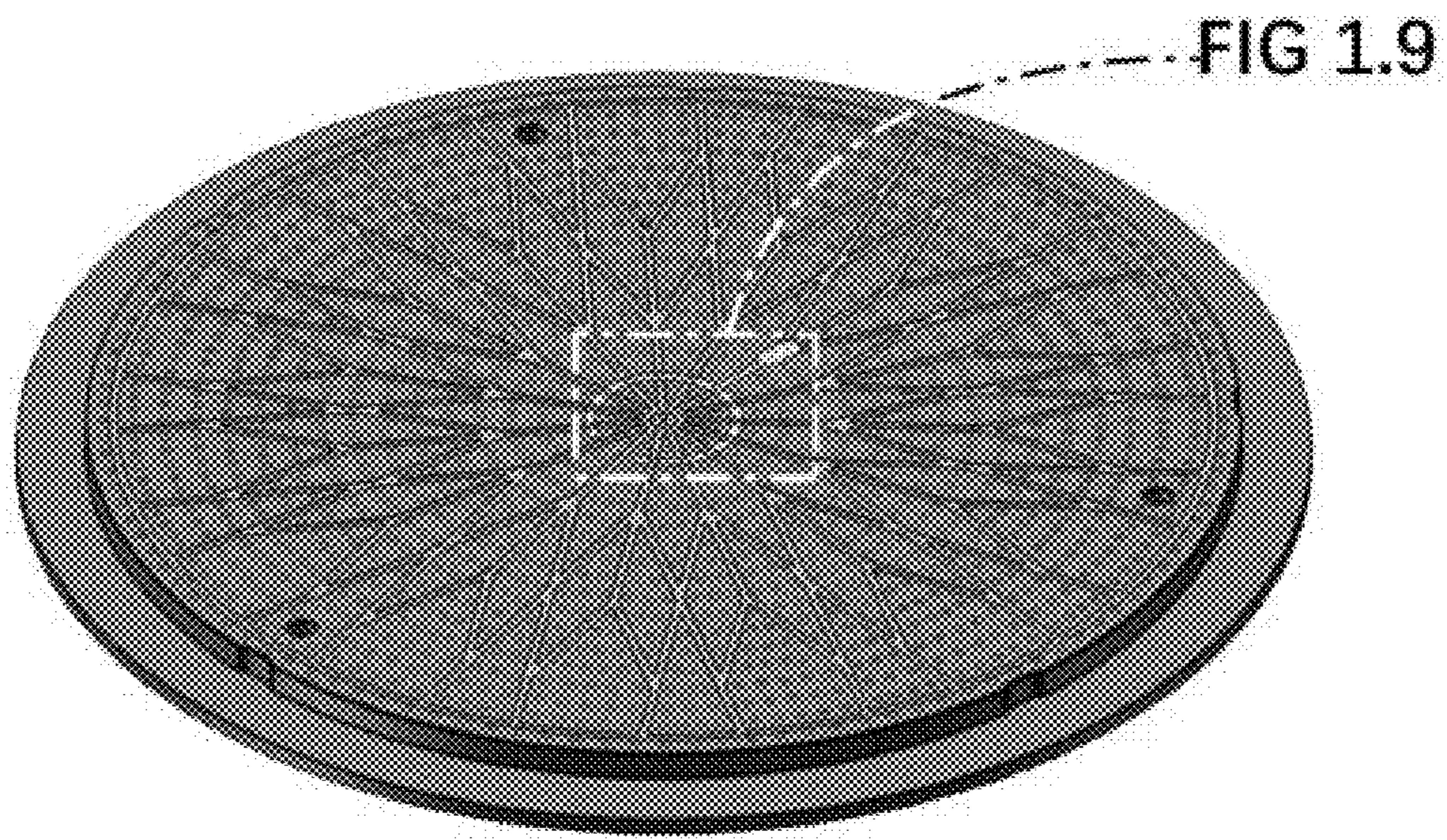


FIG 1.2

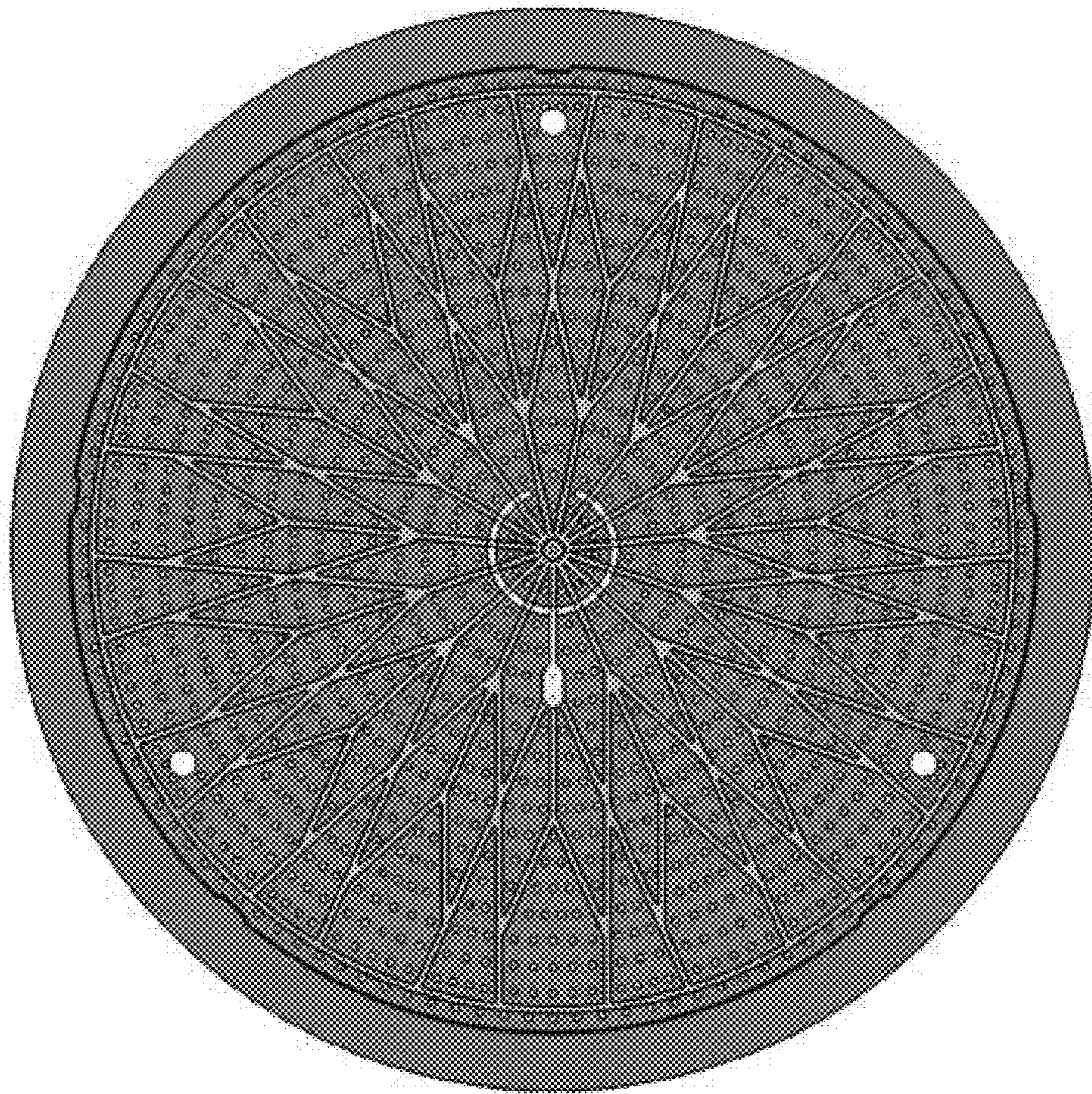


FIG. 1.3



FIG. 1.4

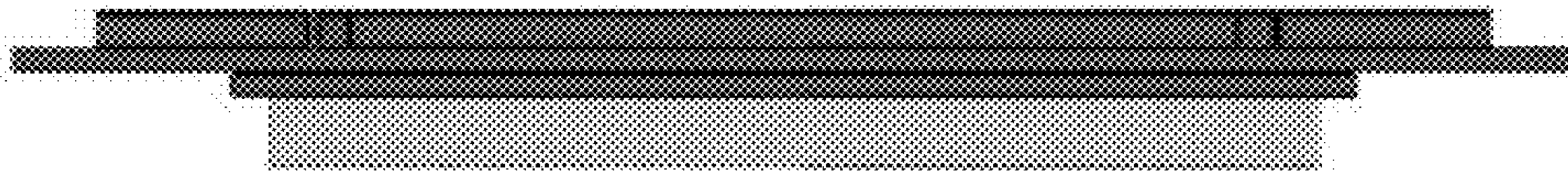


FIG. 1.5

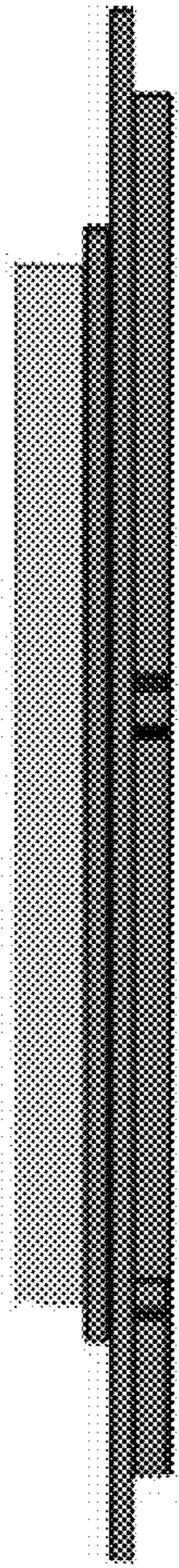


FIG. 1.6

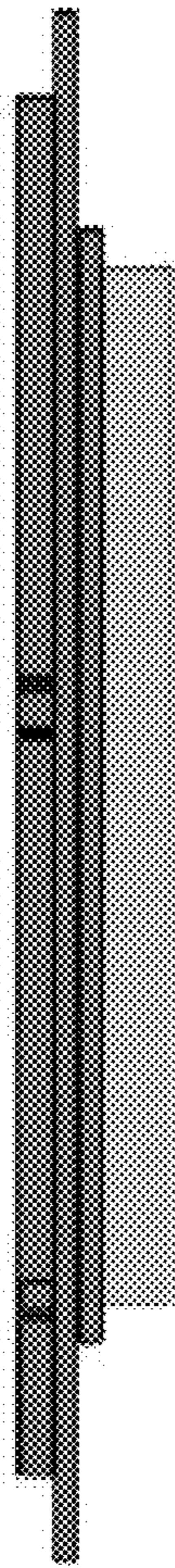


FIG 1.7

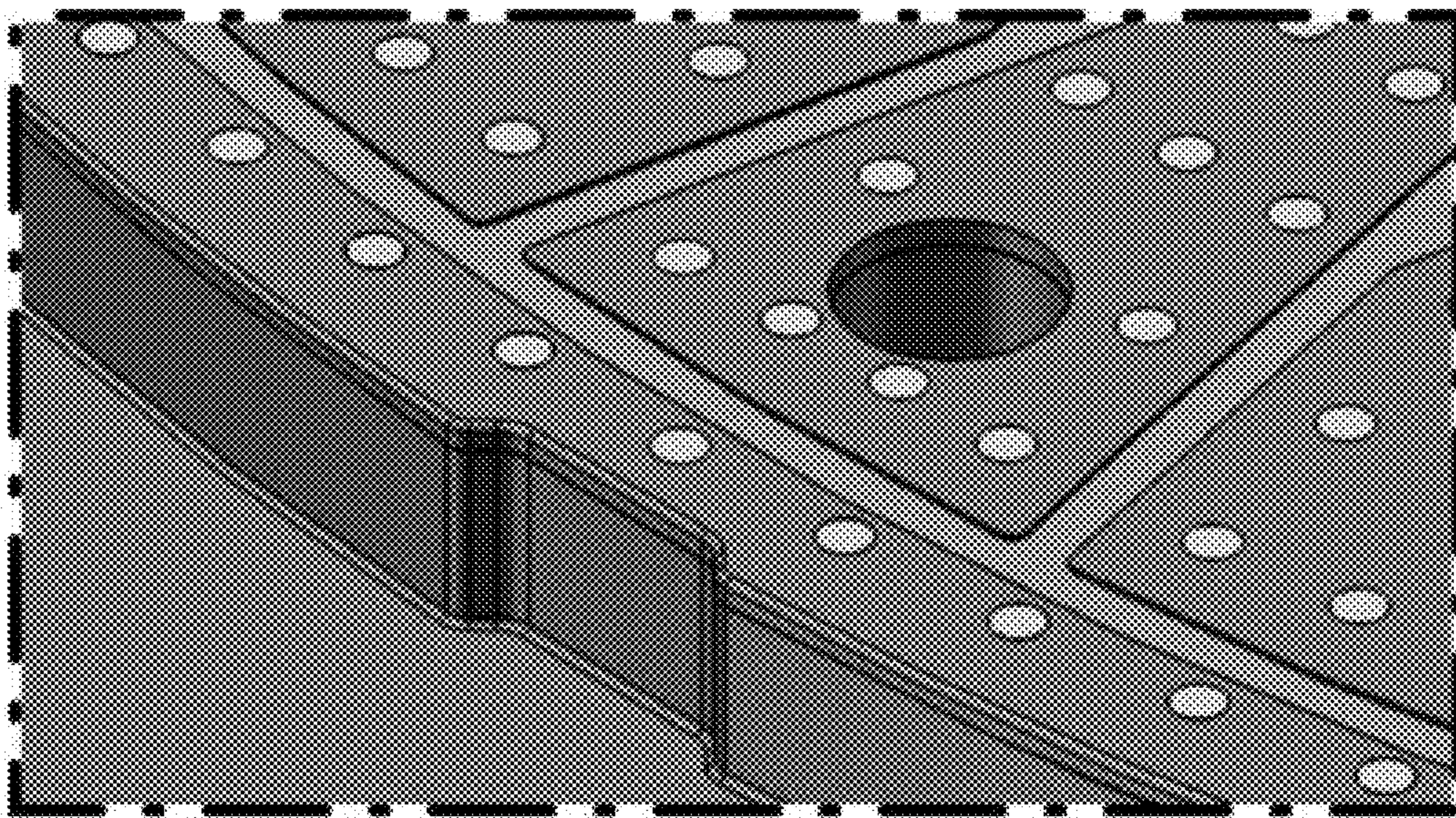


FIG 1.8

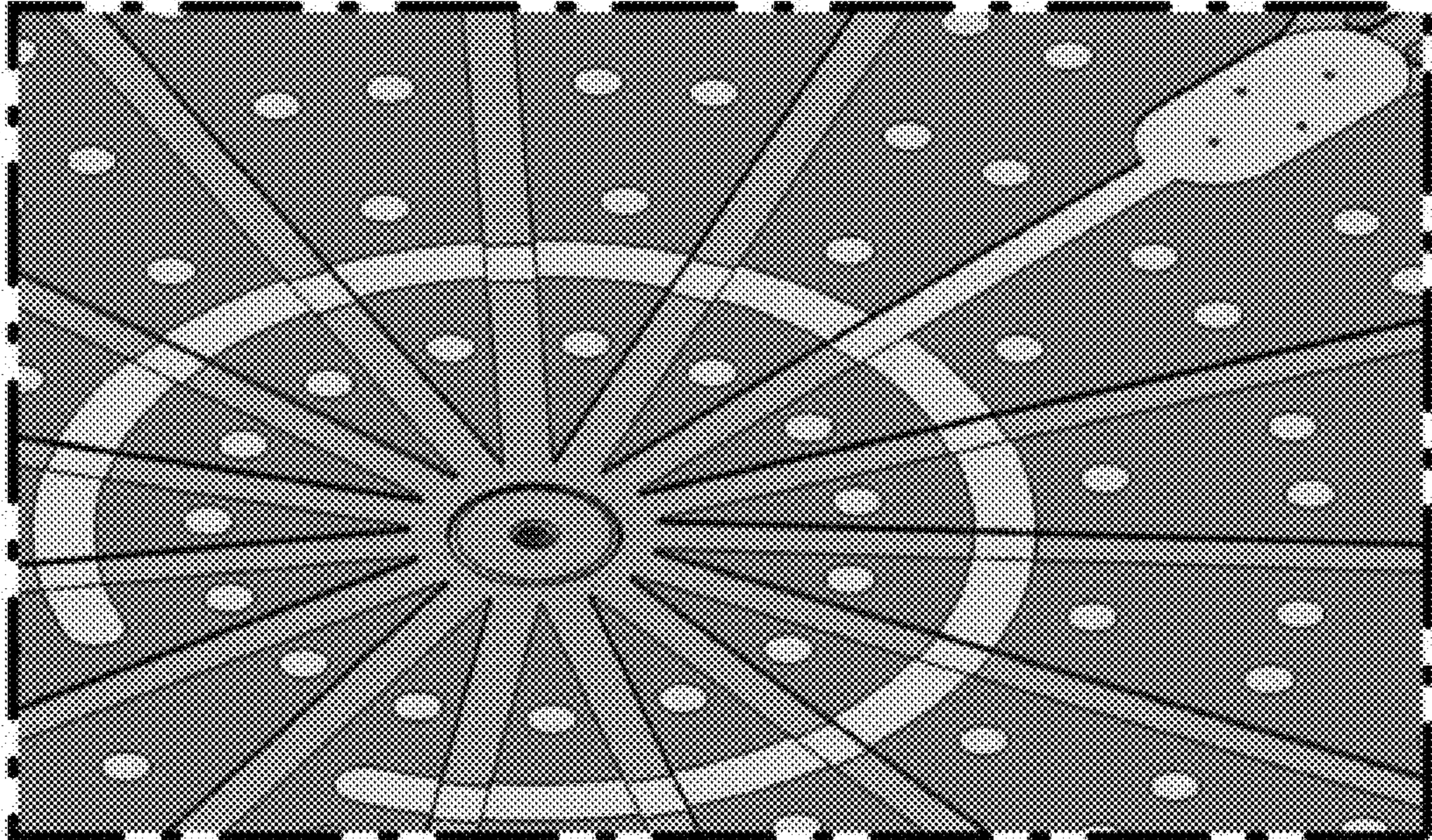


FIG. 1.9