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Kondo et al.

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(54) **SEMICONDUCTOR MODULE**

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(73) Assignee: **ROHM CO., LTD.**, Kyoto (JP)

(**) Term: **15 Years**

(21) Appl. No.: **29/765,196**

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(30) **Foreign Application Priority Data**

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(51) **LOC (14) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/101, 110, 112, 118, 120, 123, 133, D13/146, 147, 159, 154, 156, 174, 182, D13/184, 199; D14/356, 433, 435, 438
CPC H01R 24/00; H01R 12/00; H01R 12/70; H01R 13/62
See application file for complete search history.

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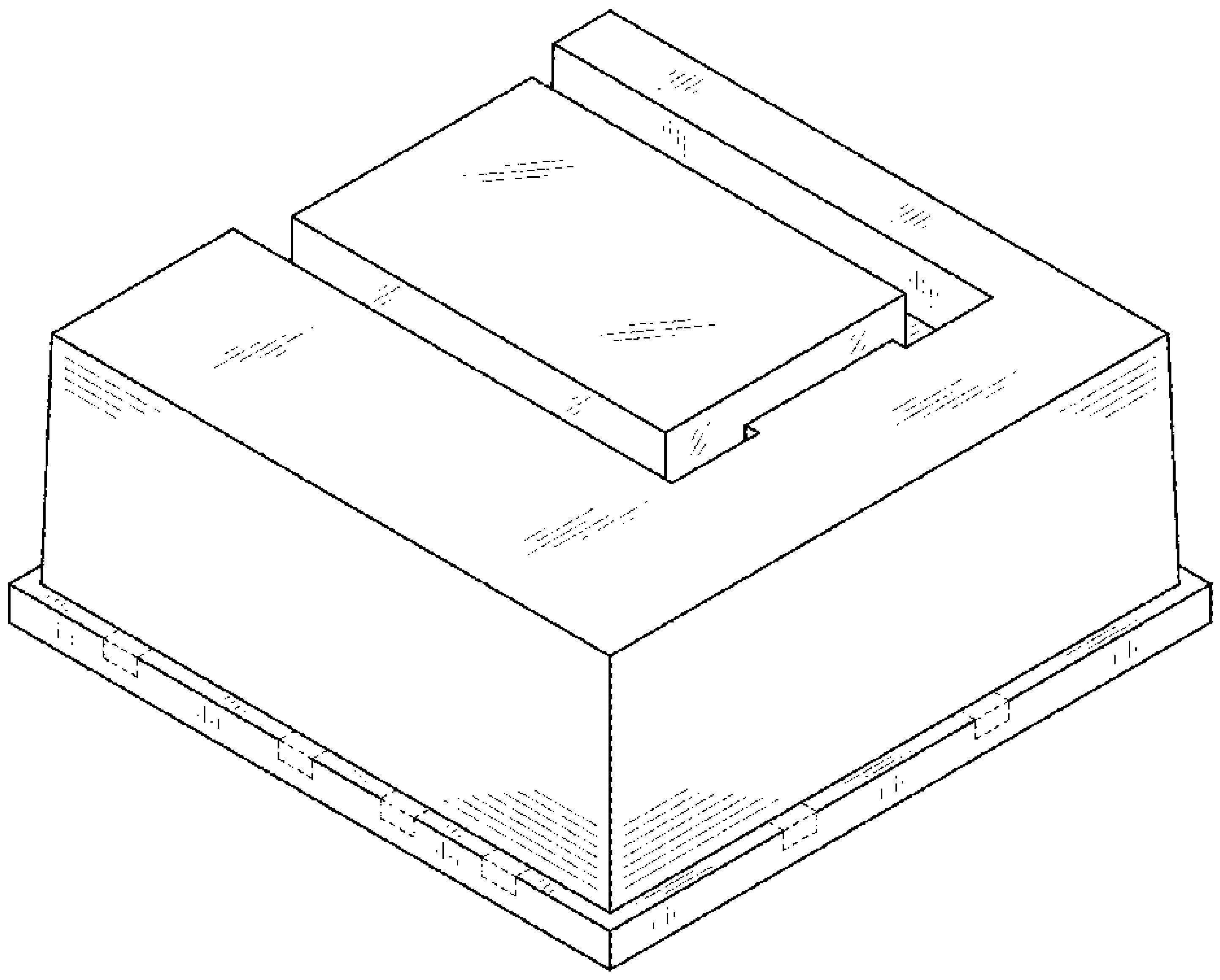
(57) **CLAIM**

The ornamental design for a semiconductor module, as shown and described.

DESCRIPTION

FIG. **1** is a front, top and right side perspective view of a semiconductor module showing our new design;
FIG. **2** is a rear, bottom and left side perspective view thereof;
FIG. **3** is a front view thereof, the rear view being a mirror image of FIG. **3**;
FIG. **4** is a top plan view thereof;
FIG. **5** is a bottom plan view thereof;
FIG. **6** is a right side view thereof; and,
FIG. **7** is a left side view thereof.
The broken lines illustrate portions of the semiconductor module that form no part of the claimed design. The dash-dotted lines denote the boundary of the claim and form no part of the claimed design. The member illustrated with fine, diagonal, parallel lines is translucent.

1 Claim, 7 Drawing Sheets



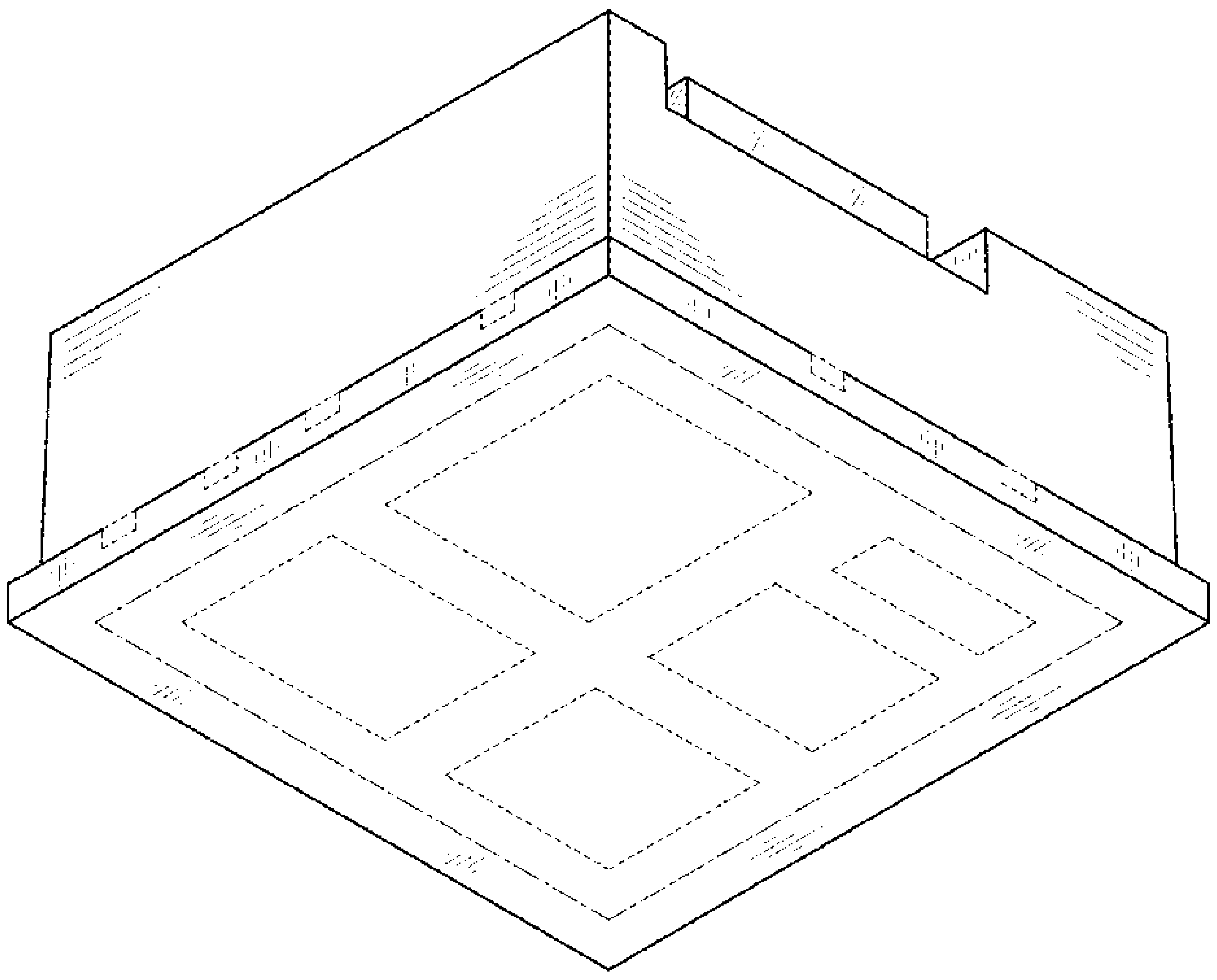


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FIG.1

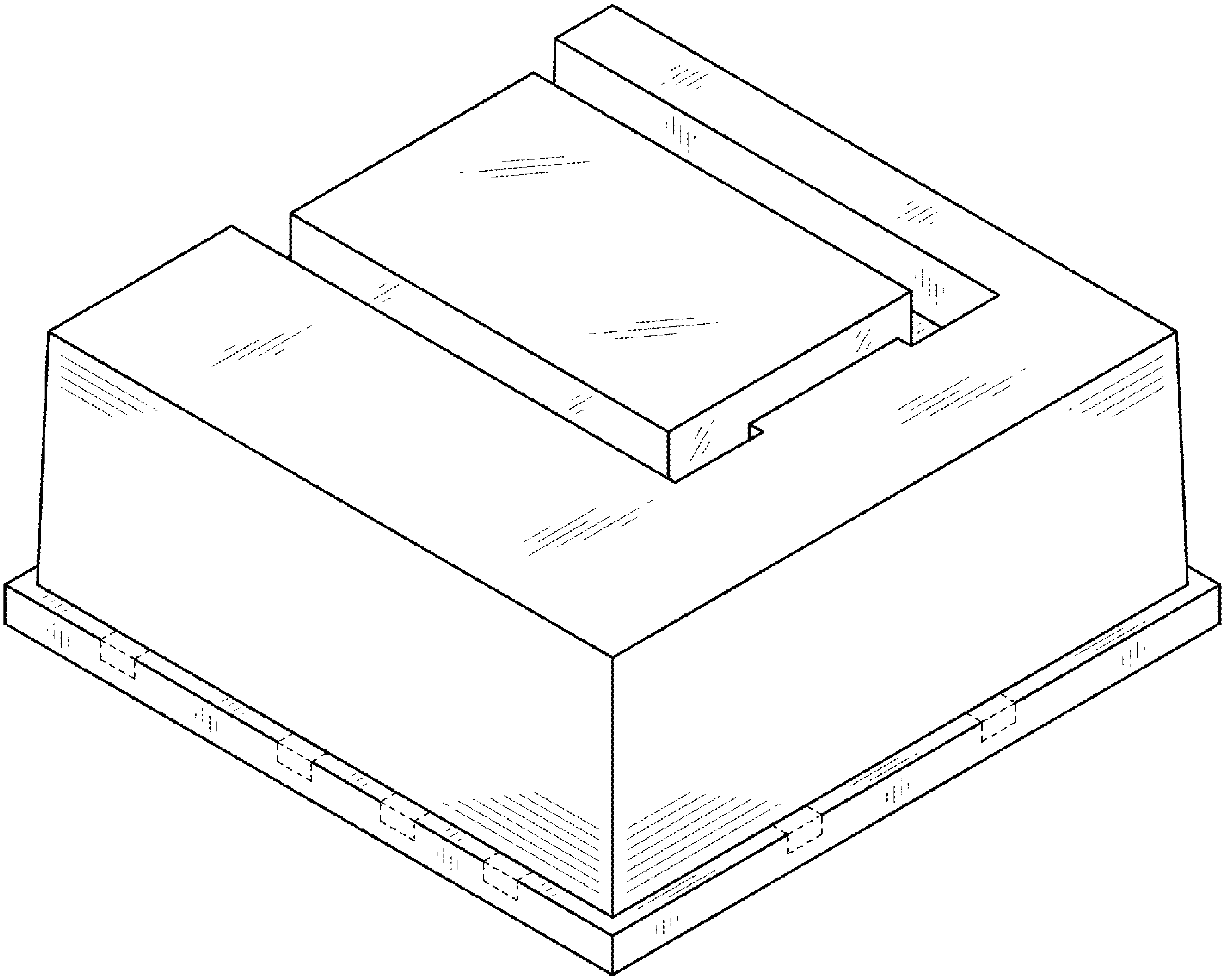

FIG.2

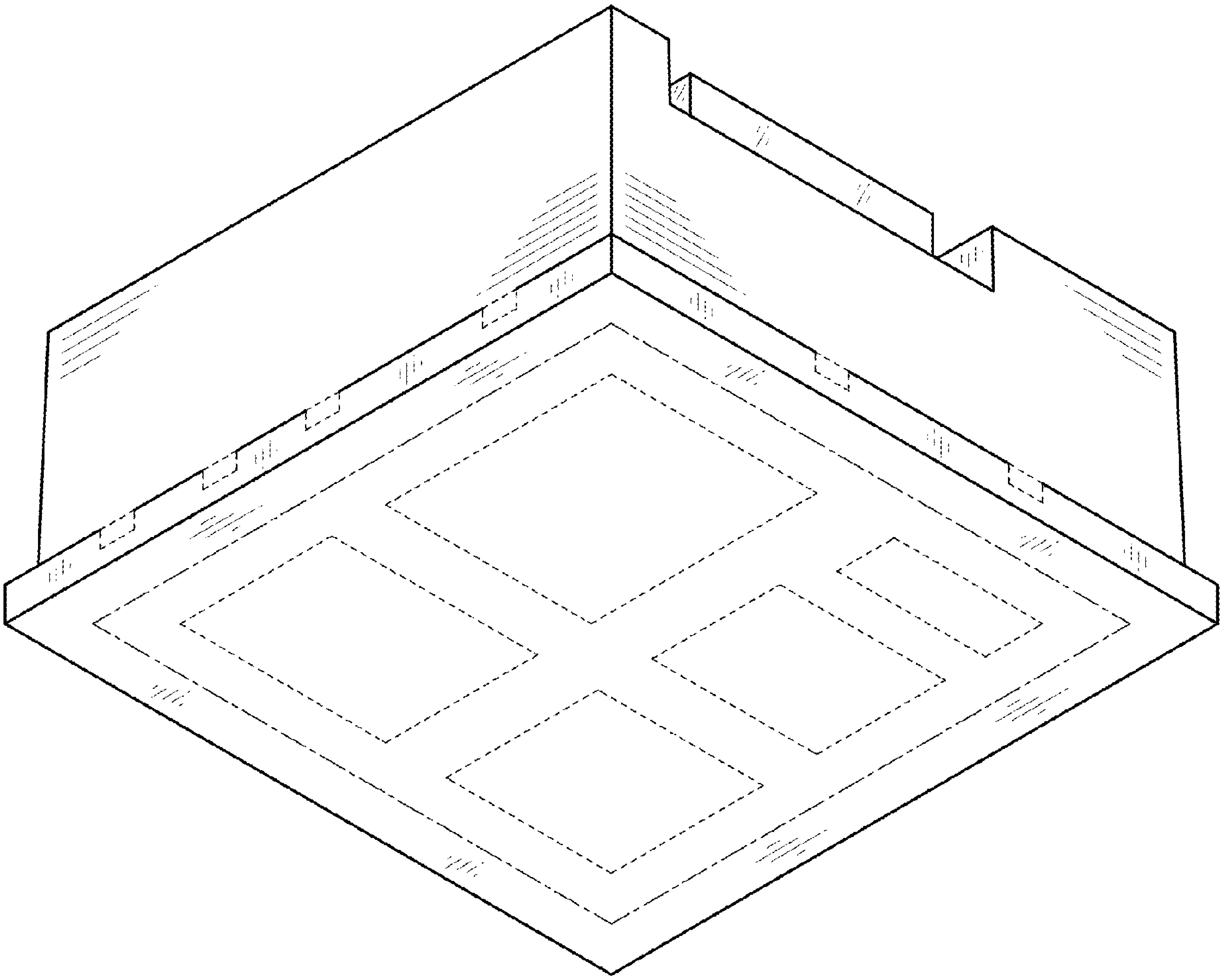

FIG.3

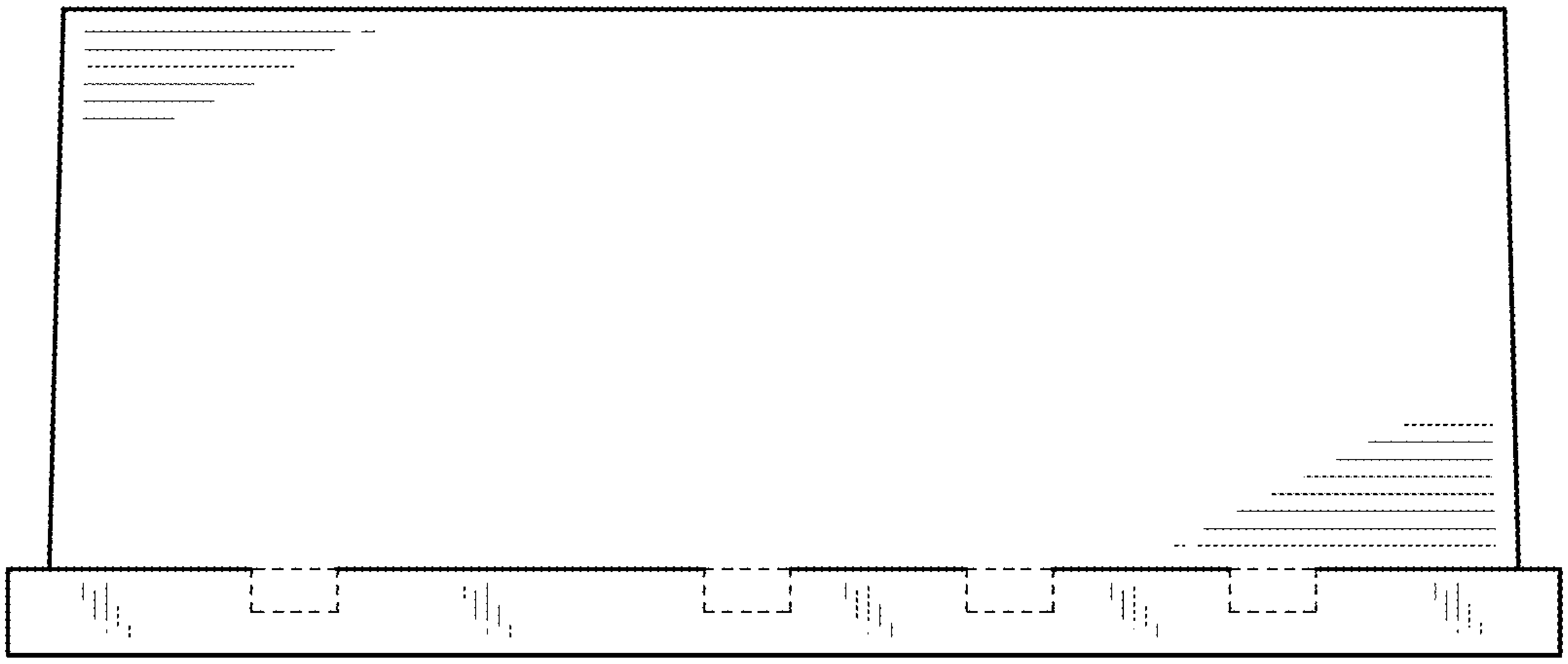

FIG.4

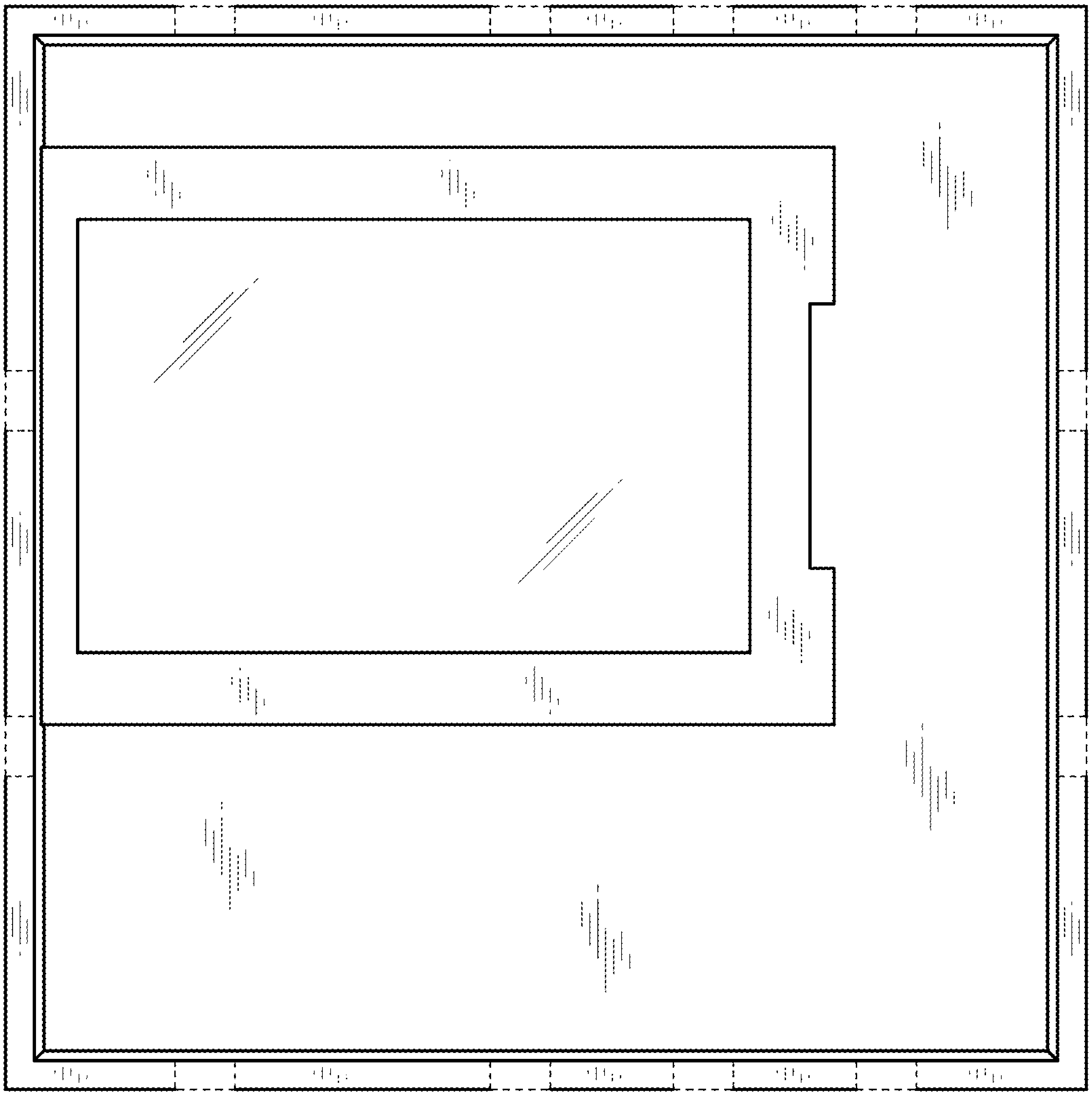

FIG.5

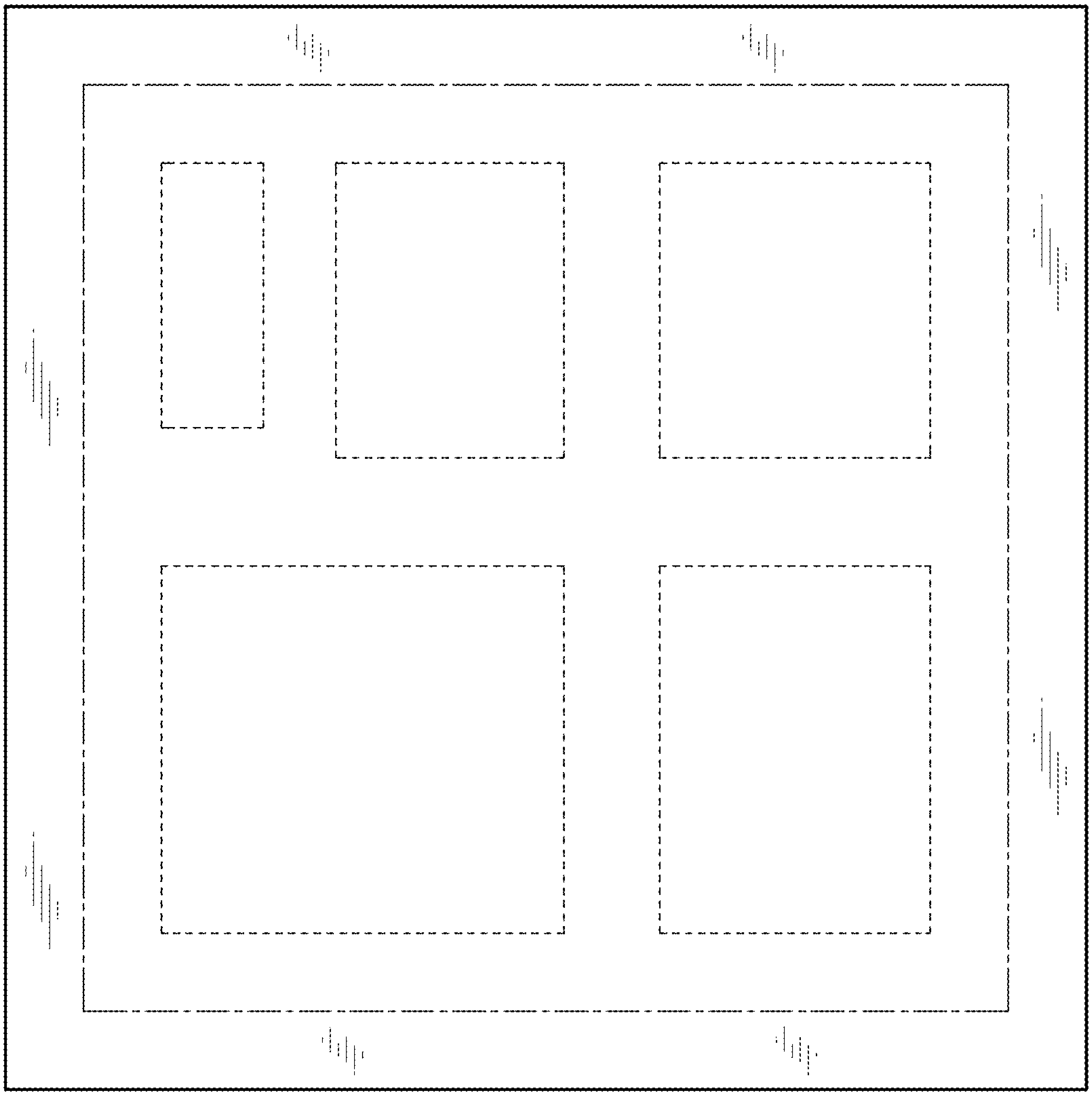

FIG.6

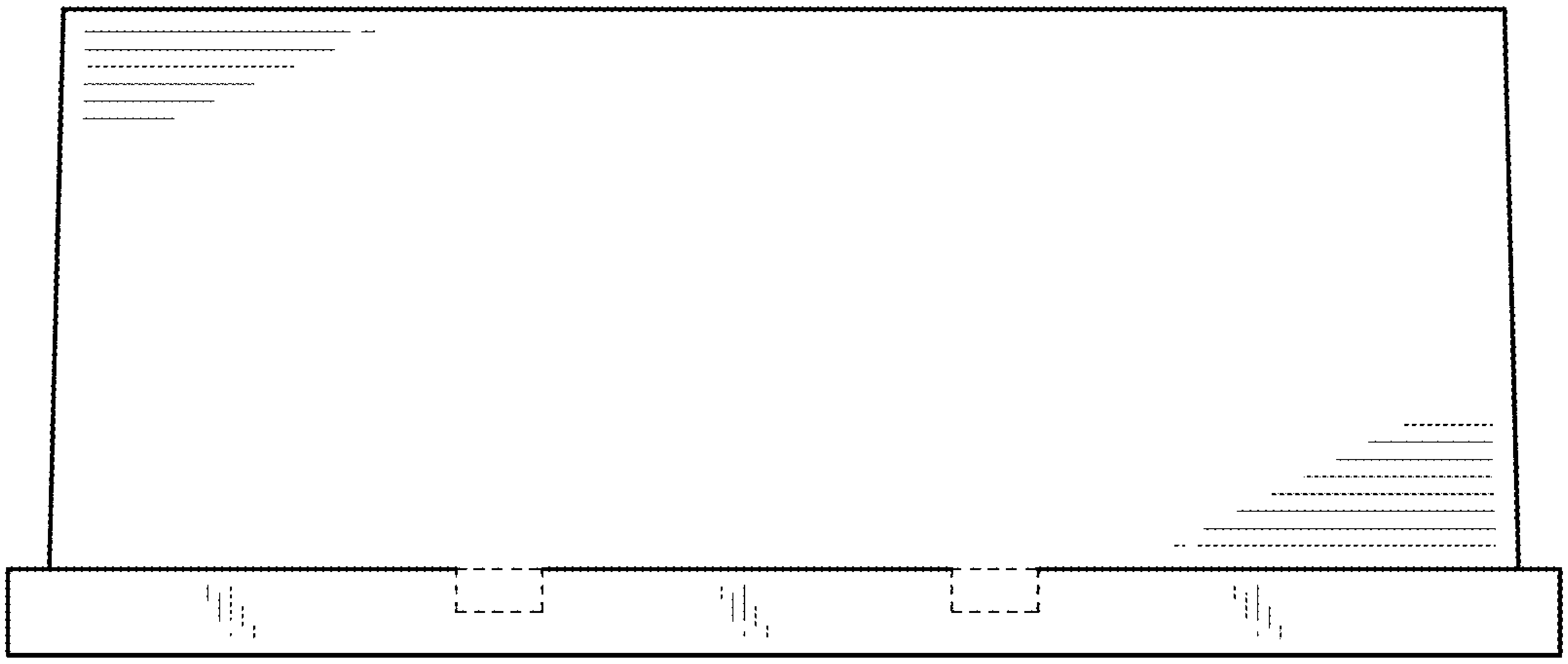

FIG.7