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(12) **United States Design Patent** (10) **Patent No.:** **US D971,168 S**
Rochford et al. (45) **Date of Patent:** **** Nov. 29, 2022**

(54) **CLIP FOR A SEMICONDUCTOR CHIP TRAY**

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(71) Applicant: **BAE Systems Information and Electronic Systems Integration Inc.**, Nashua, NH (US)

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(Continued)

(**) Term: **15 Years**

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(21) Appl. No.: **29/759,675**

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(51) **LOC (13) Cl.** **13-03**

(57) **CLAIM**

(52) **U.S. Cl.**
USPC **D13/184**

The ornamental design for a clip for a semiconductor chip tray, as shown and described.

(58) **Field of Classification Search**
USPC D14/240, 242, 356, 358, 363, 365, 367, D14/370, 432-437, 439, 125, 366, 168, D14/496; D13/103, 107, 108, 118, 119, D13/123, 133, 134, 154, 158, 162, 173, D13/184, 110

DESCRIPTION

CPC H04N 7/00; H04D 10/70
See application file for complete search history.

FIG. 1 is a front perspective view of the clip for a semiconductor chip tray;
FIG. 2 is a front elevated view of the clip for a semiconductor chip tray shown in FIG. 1;
FIG. 3 is a rear elevated view of the clip for a semiconductor chip tray shown in FIG. 1;
FIG. 4 is a right side view of the clip for a semiconductor chip tray shown in FIG. 1;
FIG. 5 is a left side view of the clip for a semiconductor chip tray shown in FIG. 1;
FIG. 6 is a top view of the clip for a semiconductor chip tray shown in FIG. 1; and,
FIG. 7 is a bottom view of the clip for a semiconductor chip tray shown in FIG. 1.

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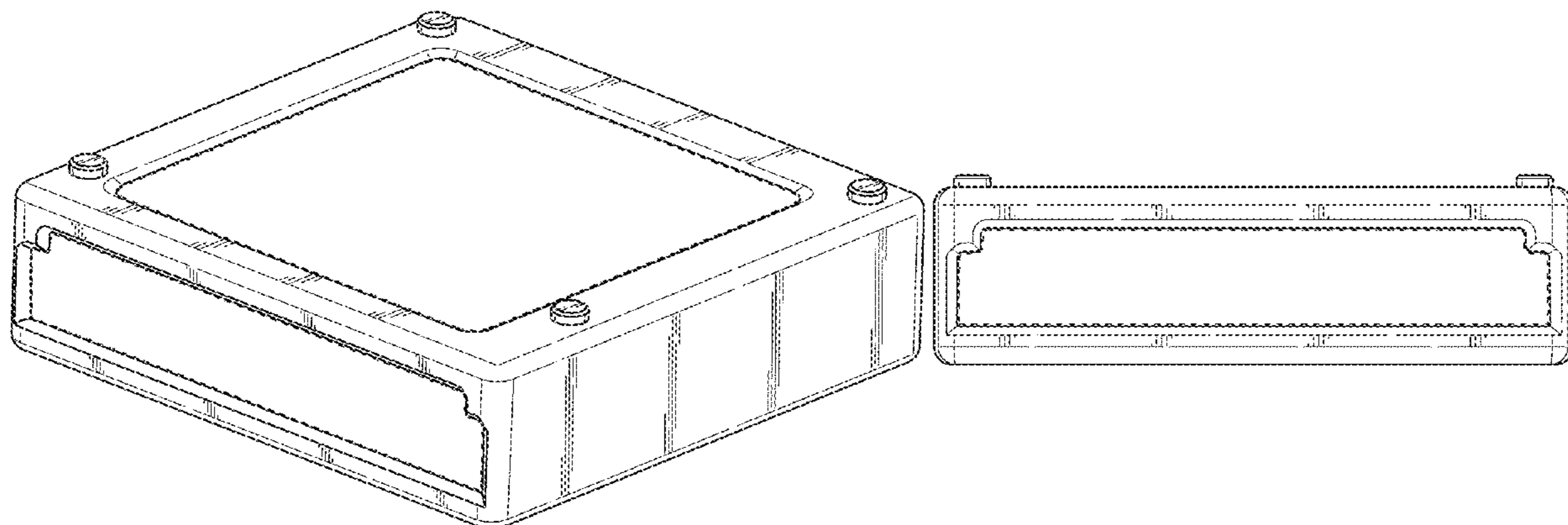
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The broken lines showing of a clip for a semiconductor chip tray which form no part of the claimed design.

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1 Claim, 7 Drawing Sheets



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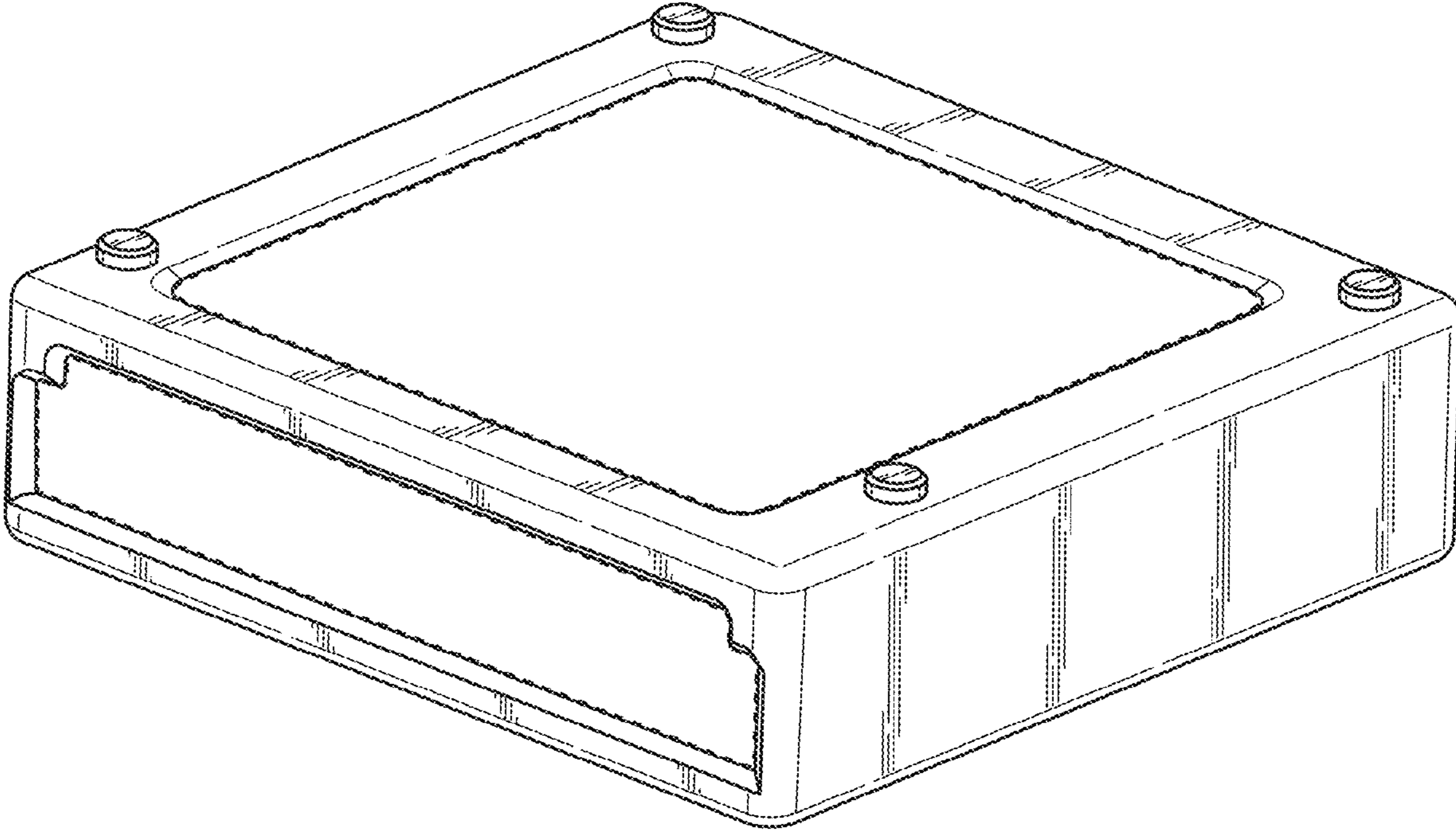


FIG. 1

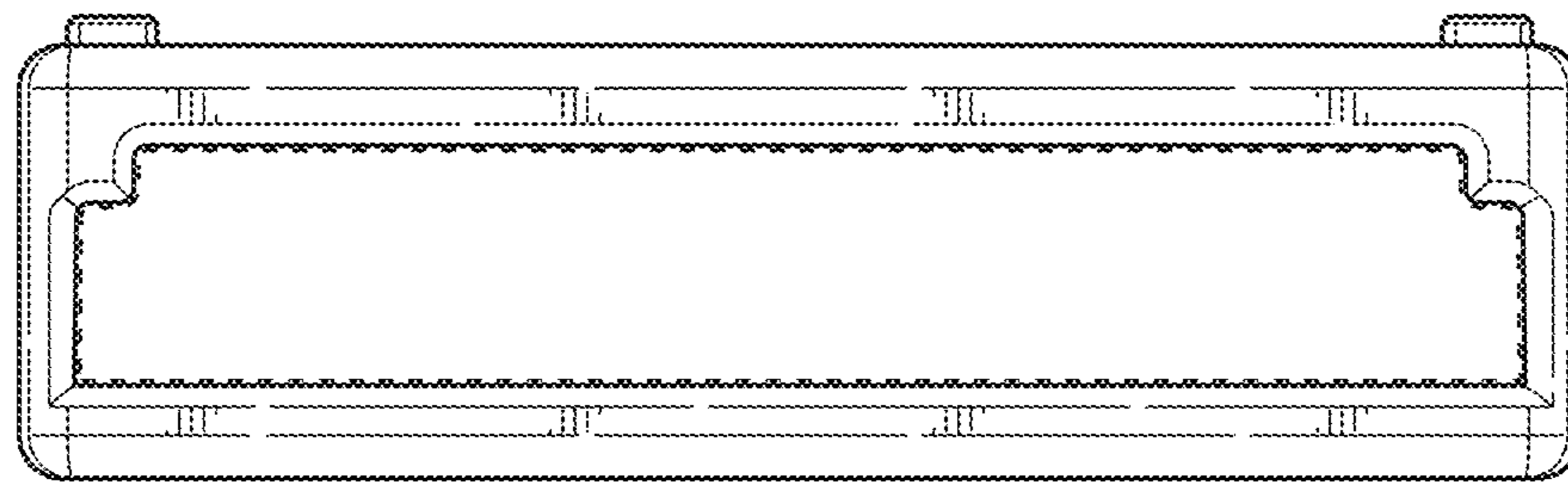


FIG. 2

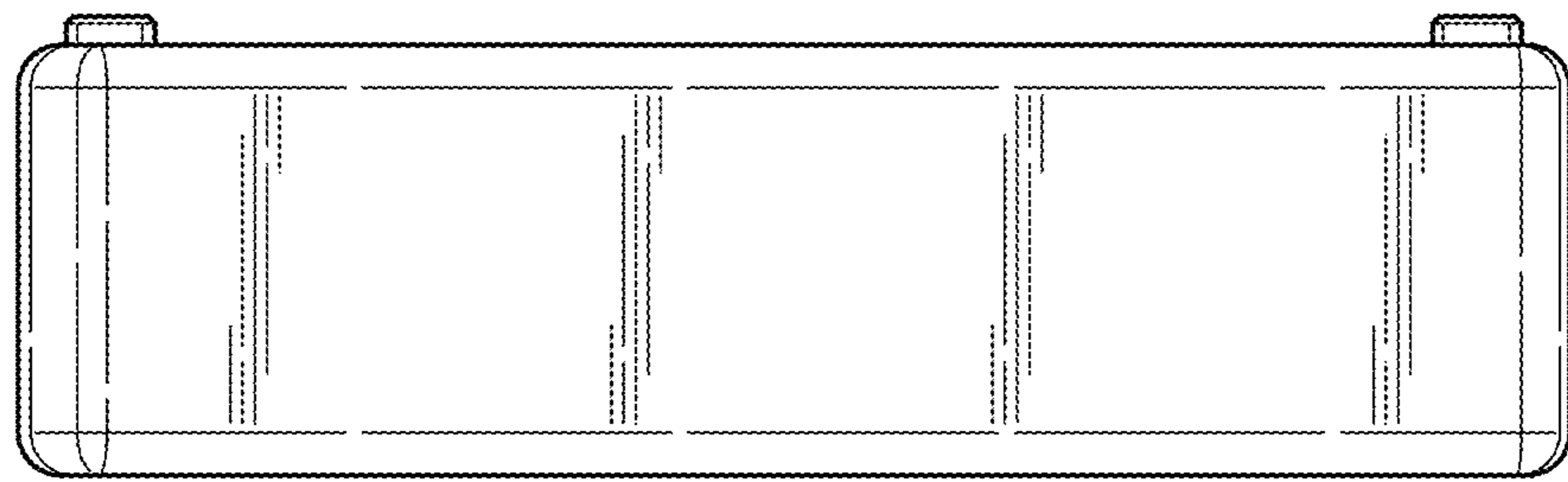


FIG. 3

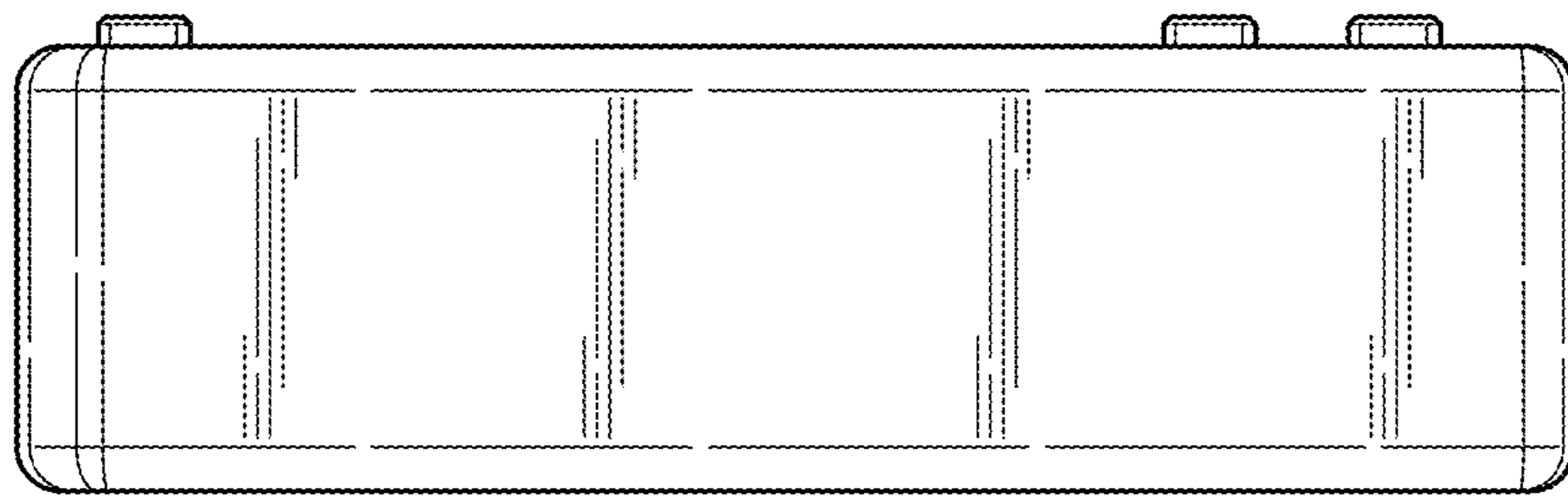


FIG. 4

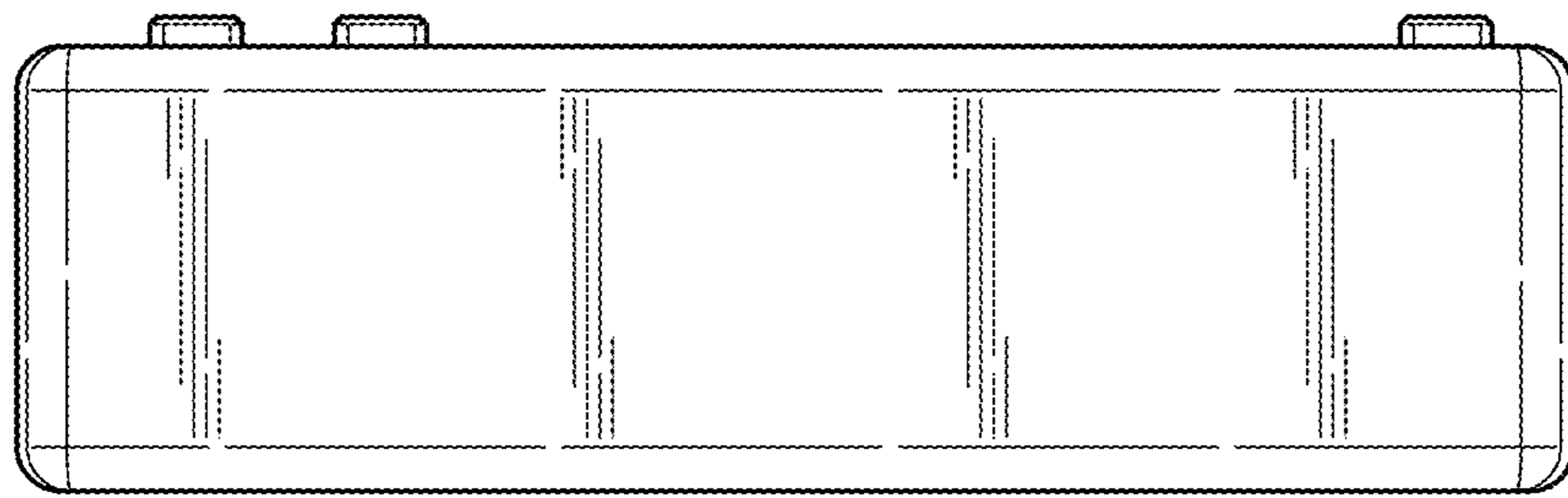


FIG. 5

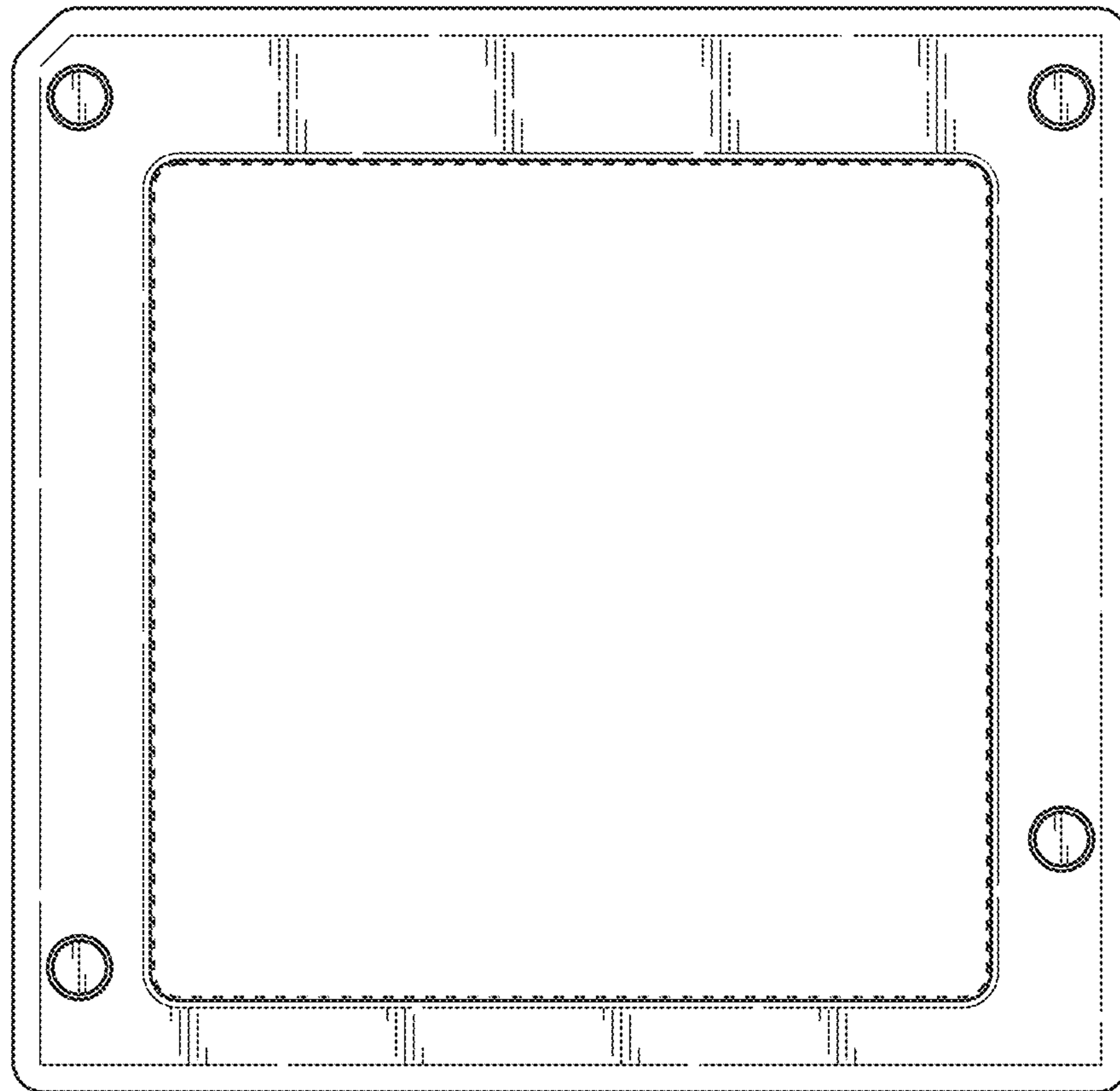


FIG. 6

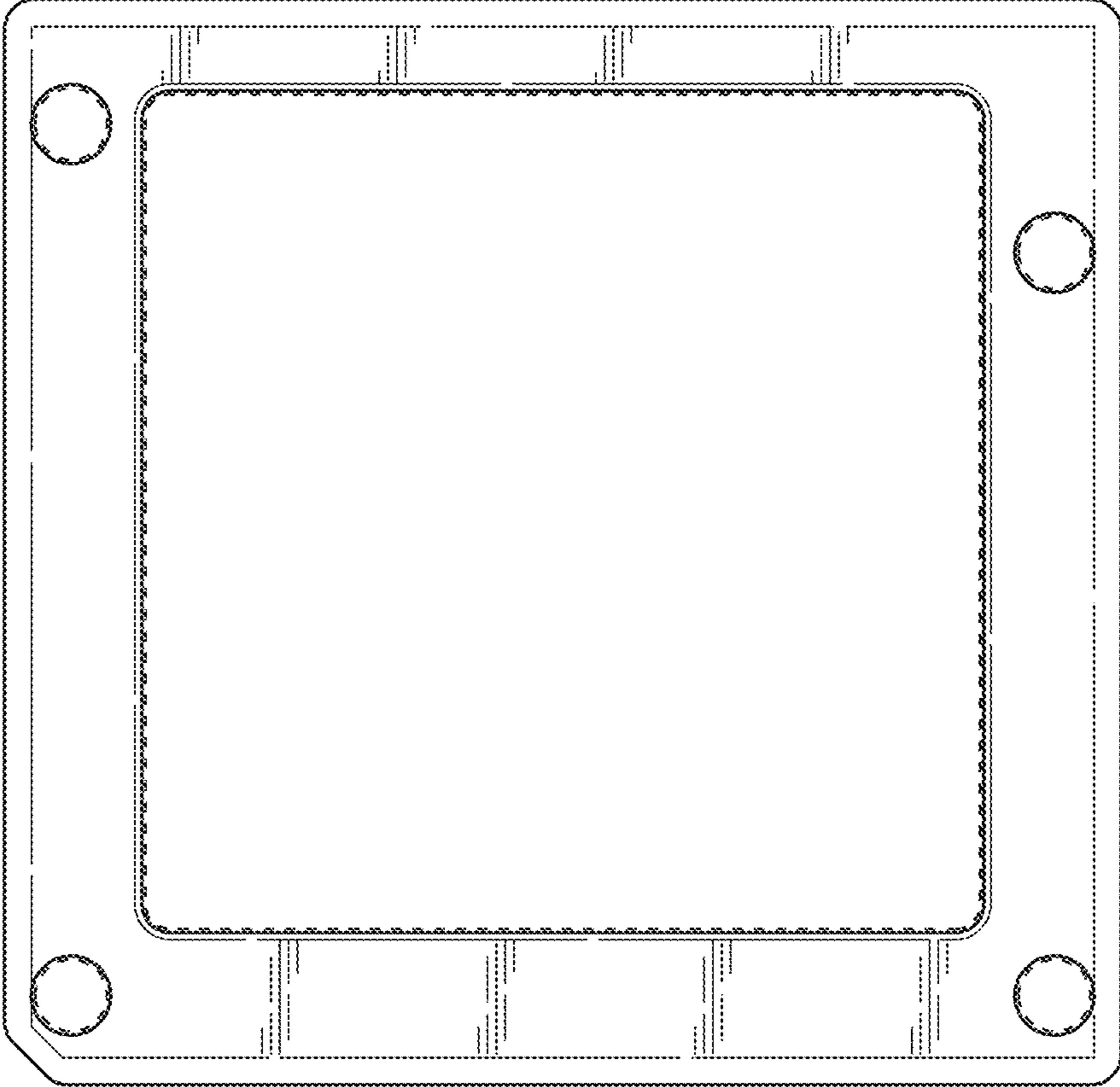


FIG. 7