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Kim et al.

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(54) **TEST CHIP**

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(**) Term: **15 Years**

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(51) **LOC (13) Cl.** **24-01**

(52) **U.S. Cl.**
USPC **D24/216**; D24/225

(58) **Field of Classification Search**
USPC D24/107, 186, 216, 232, 233, 234, 121, D24/122, 223, 224, 225, 227, 231, 119, D24/133; D10/81
CPC B01L 3/5023; B01L 3/523; B01L 3/565; B01L 2300/0809; B01L 3/50229; B01L 2300/0816; B01L 2300/0819; B01L 2300/0822; B01L 2300/0825; A61B 10/0038; A61B 10/0216; G01N 2001/028
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,965,047	A	*	10/1990	Hammond	G01N 33/528 422/430
D392,391	S	*	3/1998	Douglas	D24/225
D420,141	S	*	2/2000	Casterlin	D24/223
D477,670	S	*	7/2003	Jurik	D24/225
D483,496	S	*	12/2003	Kjendlie	D24/223
D694,425	S	*	11/2013	Markovsky	D24/225
D800,001	S	*	10/2017	Winter	D24/225
D889,684	S	*	7/2020	Johnson	D24/225
D895,140	S	*	9/2020	Heron	D24/225
2011/0030458	A1	*	2/2011	Park	B01L 3/502723 73/64.56
2019/0374945	A1	*	12/2019	Hallock	B01L 3/502761
2020/0376485	A1	*	12/2020	Azpiroz	B01L 3/50273

* cited by examiner

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(57) **CLAIM**

The ornamental design for a test chip, as shown and described.

DESCRIPTION

FIG. **1** is a front view of a test chip;
FIG. **2** is a top view thereof;
FIG. **3** is a bottom view thereof;
FIG. **4** is a right side view thereof;
FIG. **5** is a left side view thereof; and,
FIG. **6** is a cross-sectional view taken along line **6**-**6** shown in FIG. **5**.

The rear view is omitted since it is symmetrical to the front view. The broken lines represent portions of the test chip and form no part of the claimed design.

1 Claim, 6 Drawing Sheets

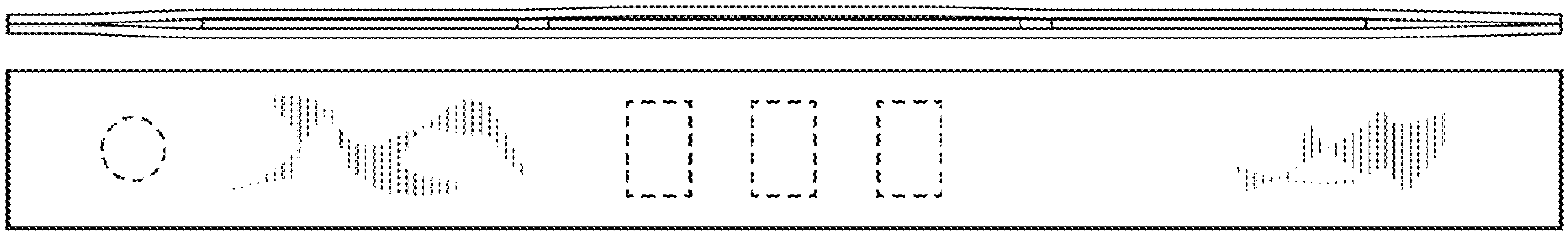

Fig.1

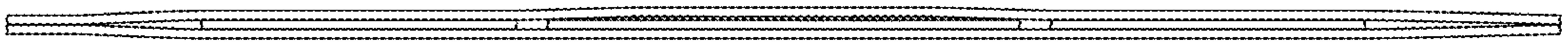

Fig. 2

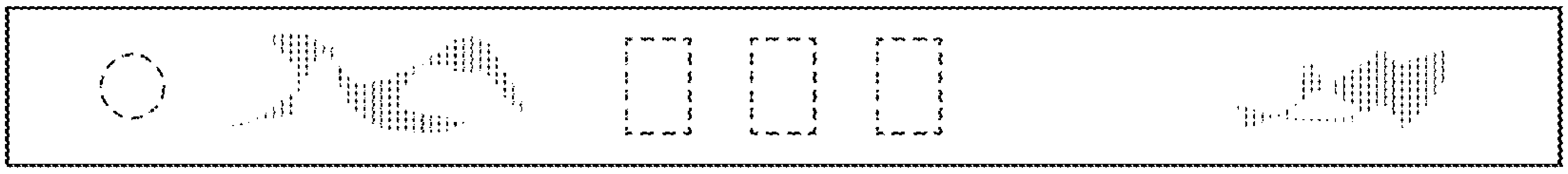

Fig. 3

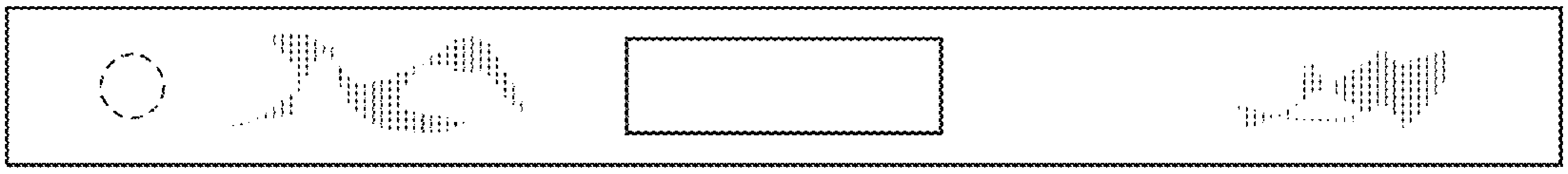

Fig.4

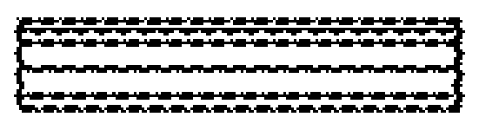

Fig. 5

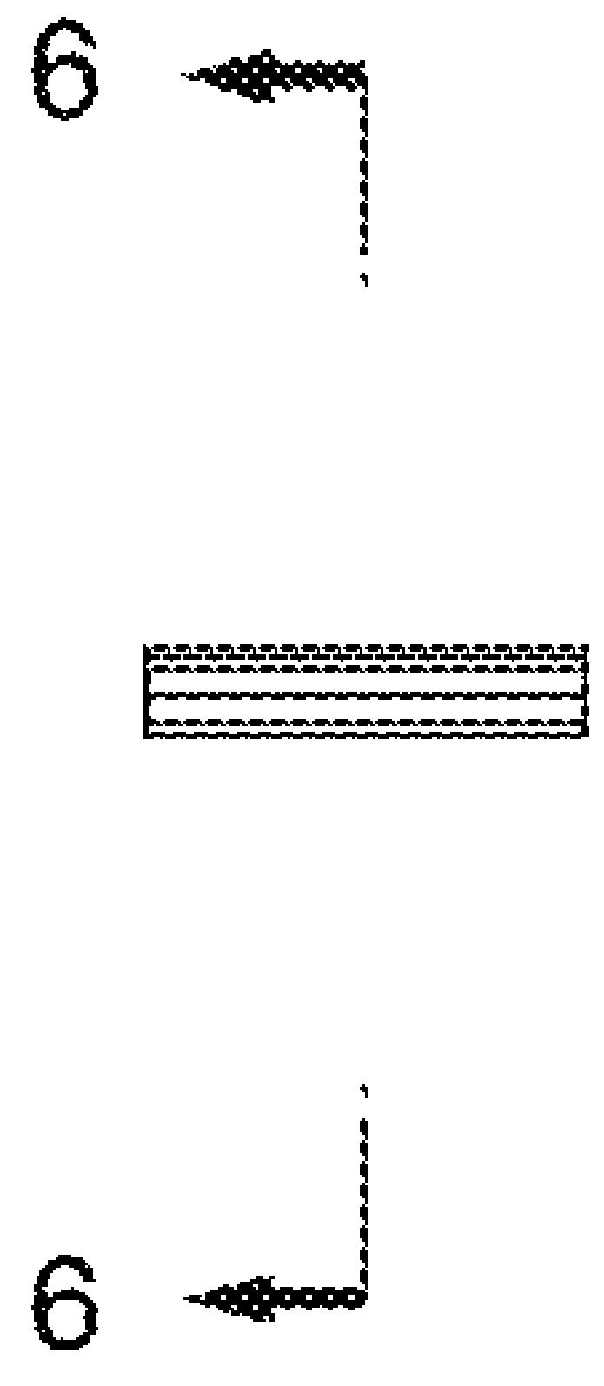

Fig.6