

US00D968387S

(12) **United States Design Patent** (10) **Patent No.:** **US D968,387 S**
Bobyn et al. (45) **Date of Patent:** **** *Nov. 1, 2022**

(54) **SHUFFLE FOR CONNECTING NODES IN A DIRECT INTERCONNECT NETWORK**

H04L 2012/5619; H04L 2012/6443;
H04L 29/12952; H04L 61/6077; H04L
49/90

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See application file for complete search history.

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(*) Notice: This patent is subject to a terminal disclaimer.

(**) Term: **15 Years**

Primary Examiner — Marie D. Fast Horse

(21) Appl. No.: **29/741,764**

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(22) Filed: **Jul. 15, 2020**

(30) **Foreign Application Priority Data**

Jun. 19, 2020 (CA) CA 196392

(51) **LOC (13) Cl.** **14-02**

(52) **U.S. Cl.**
USPC **D14/313; D14/140.4**

(58) **Field of Classification Search**
USPC D14/188, 195, 197, 198, 203.1, 203.6, D14/204, 240, 242, 299, 125, 140, 140.1, D14/140.4, 142, 155, 168, 496, 300, 302, D14/308, 313, 348, 351, 388, 356, 357, D14/358, 361, 362, 363, 365, 367, 370, D14/432, 439, 440, 441, 443; D13/103, D13/107, 108, 123, 124, 152, 158, 162, D13/162.1, 163, 184, 199, 147; D10/46, D10/49, 104.1, 106.6, 116.1, 61, 64, 75, D10/106.9
CPC ... H03F 3/00; H03F 3/45; H03F 3/181; H03F 3/189; H03F 3/20; H03F 1/00; H03F 1/08; H03F 1/18; H04L 49/1592; H04L 9/0855; H04L 12/40006; H04L 12/40195;

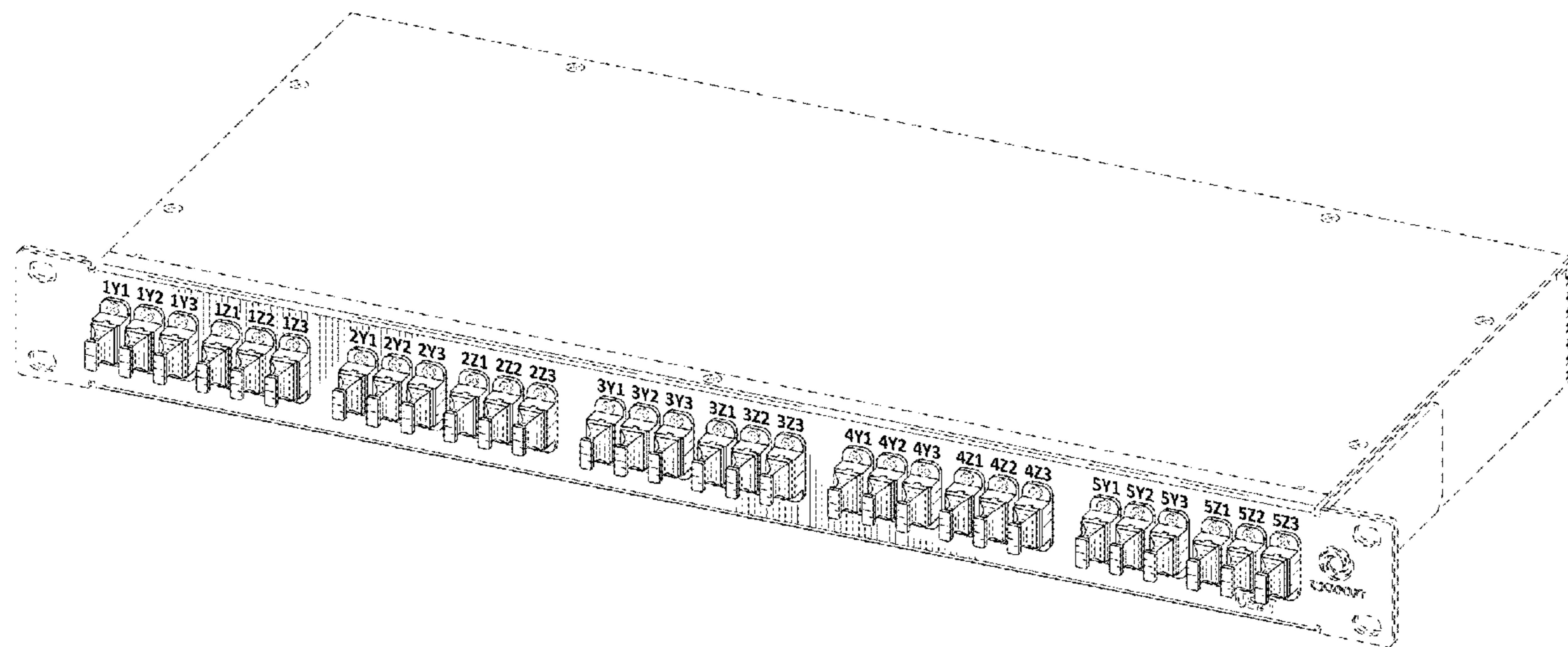
(57) **CLAIM**

The ornamental design for a shuffle for connecting nodes in a direct interconnect network, as shown and described.

DESCRIPTION

FIG. 1 is an upper, right side perspective view of a shuffle for connecting nodes in a direct interconnect network; FIG. 2 is a lower, left side perspective view thereof; FIG. 3 is a front side view thereof; FIG. 4 is a back side view thereof; FIG. 5 is a left side view thereof; FIG. 6 is a right side view thereof; FIG. 7 is a top plan view thereof; and, FIG. 8 is a bottom plan view thereof. The broken lines shown in the drawings depict portions of the shuffle for connecting nodes in a direct interconnect network that form no part of the claimed design. The shade lines indicate the character and contour of the surfaces represented, not to be confused with surface ornamentation.

1 Claim, 6 Drawing Sheets



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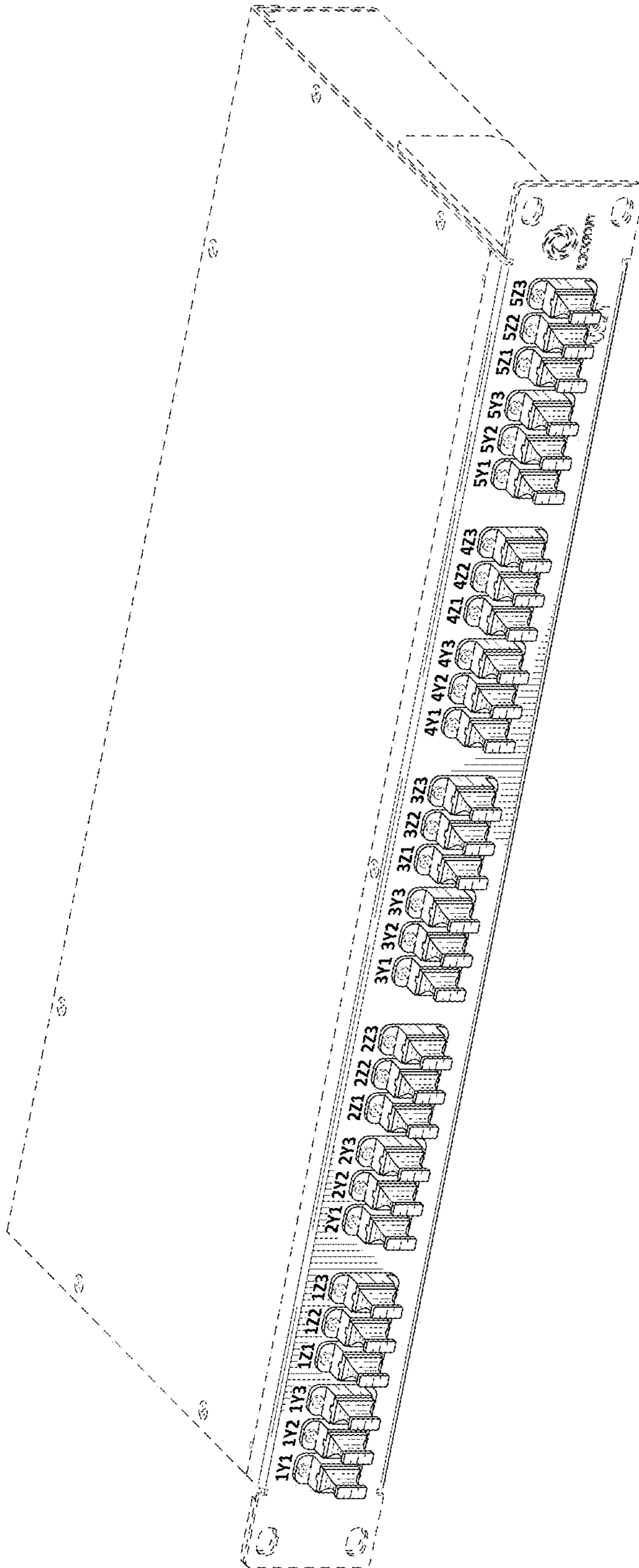


FIG. 1

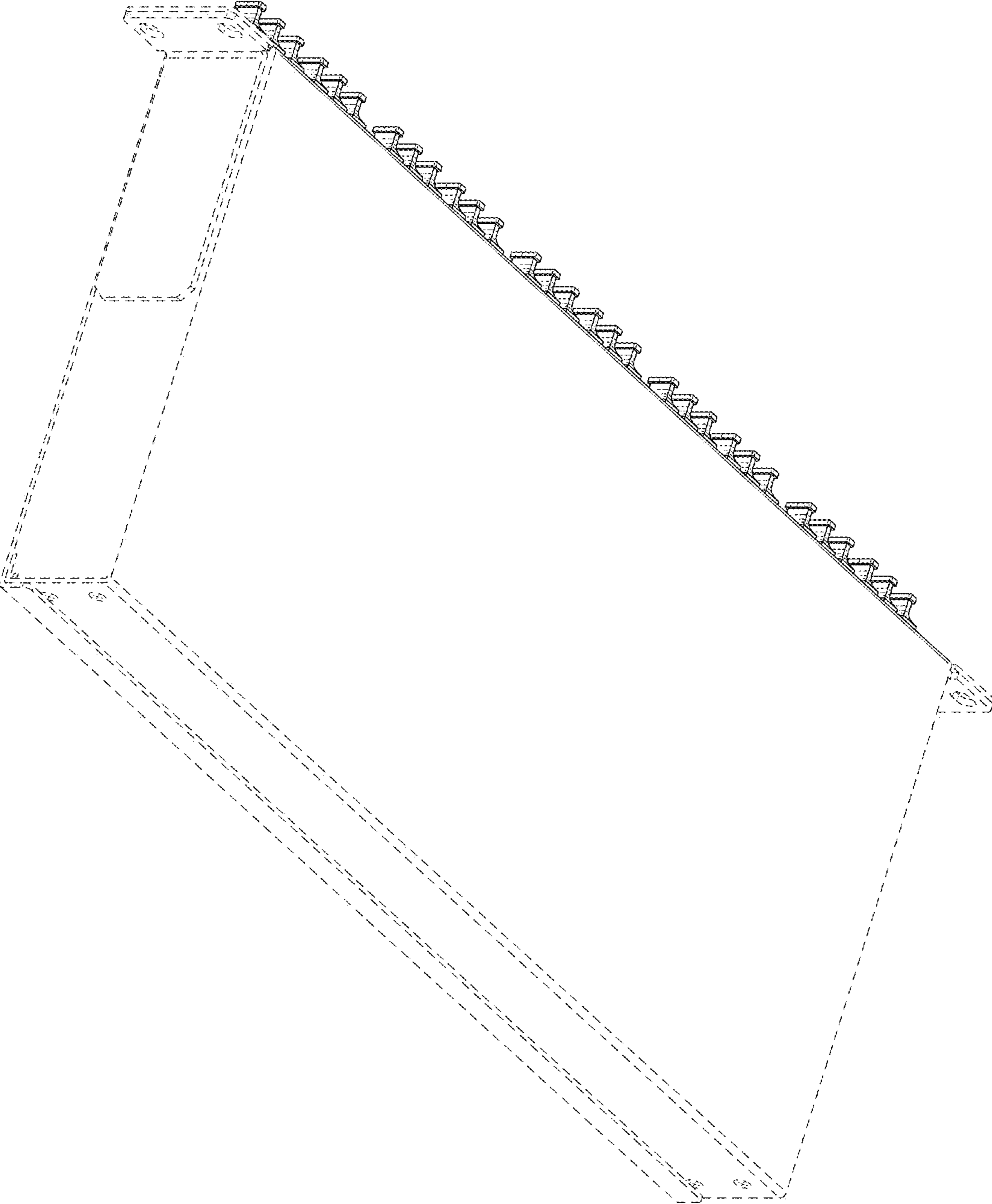


FIG. 2

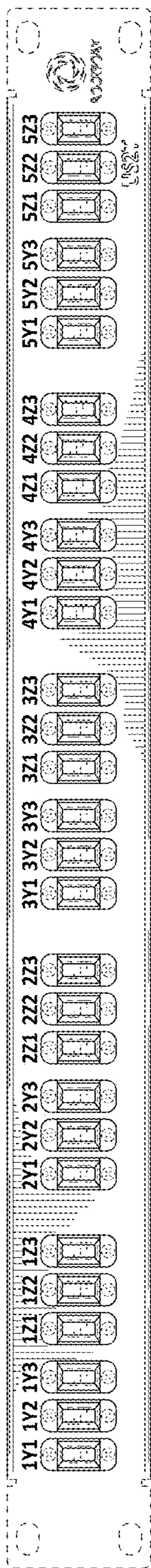


FIG. 3



FIG. 4

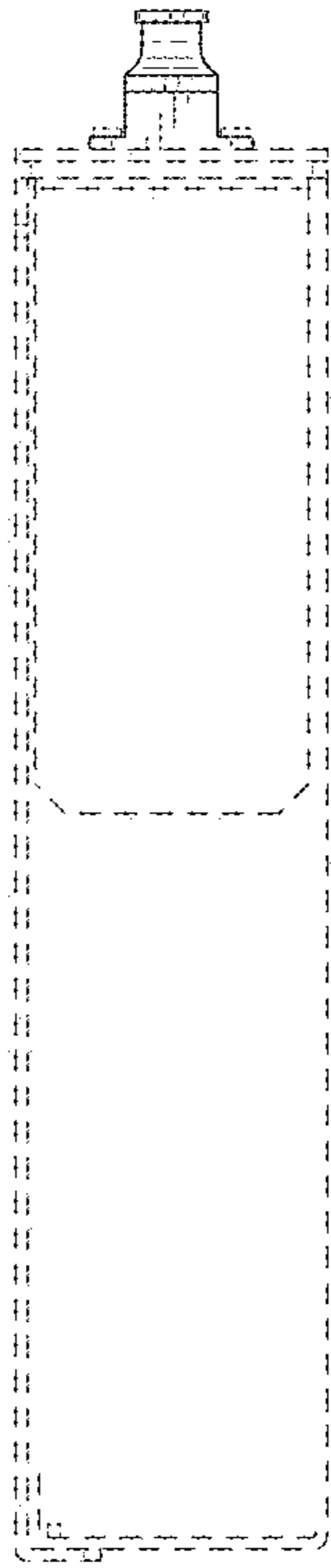


FIG. 5

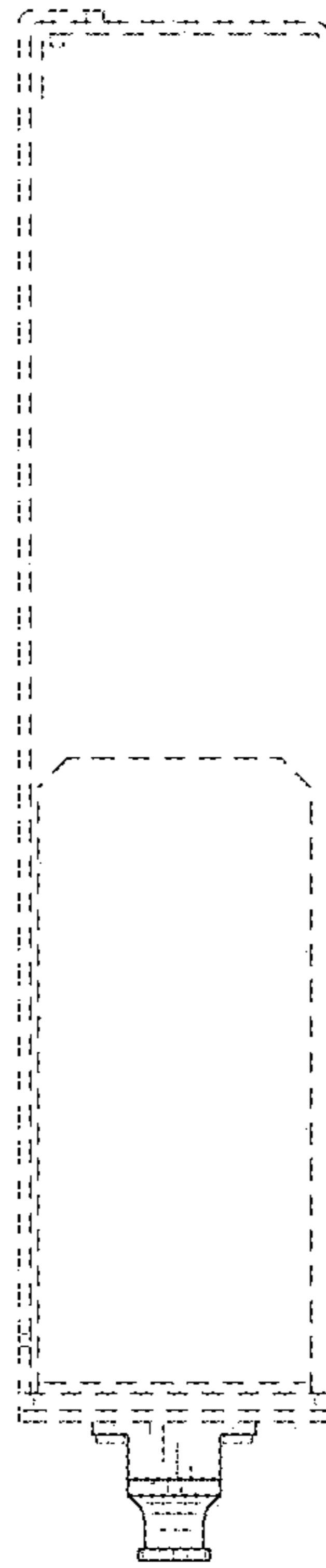


FIG. 6

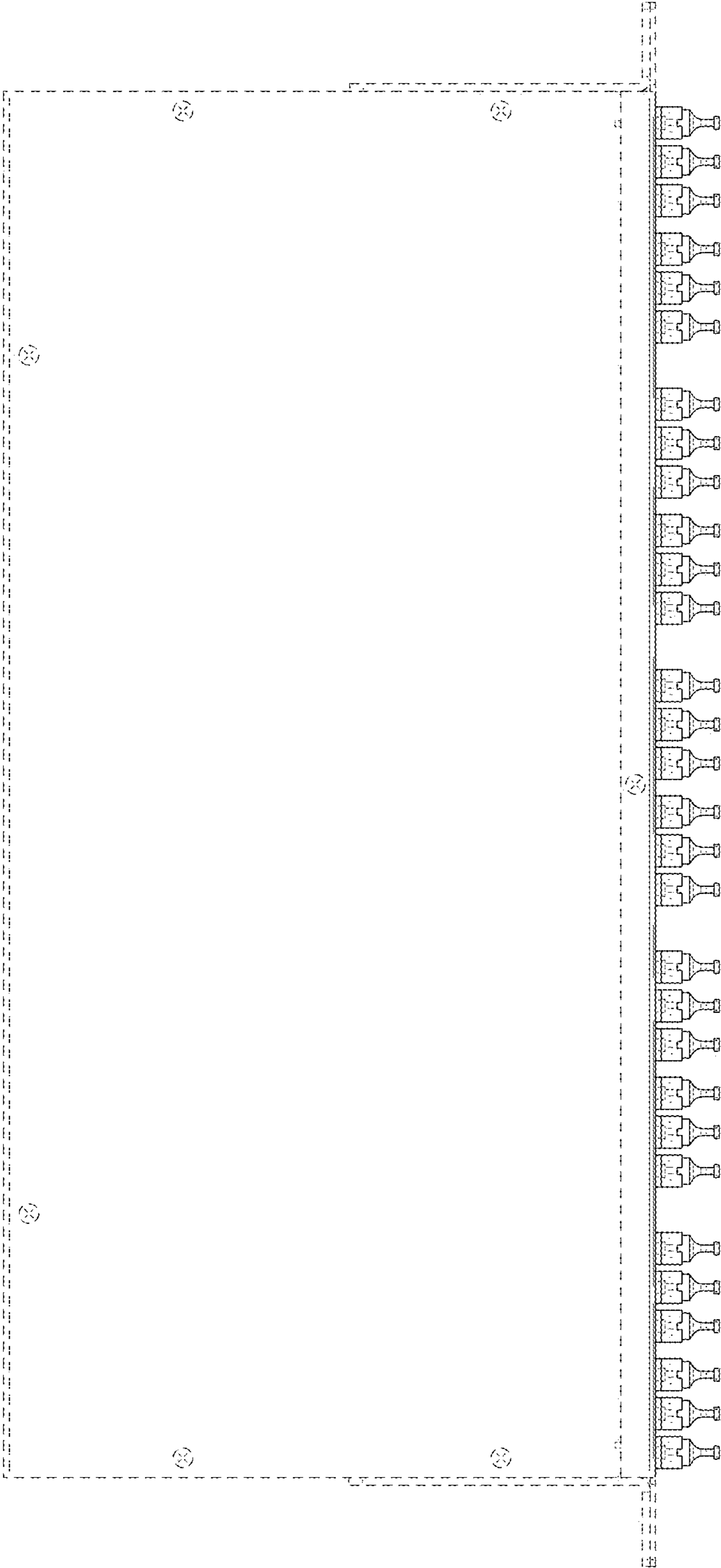


FIG. 7

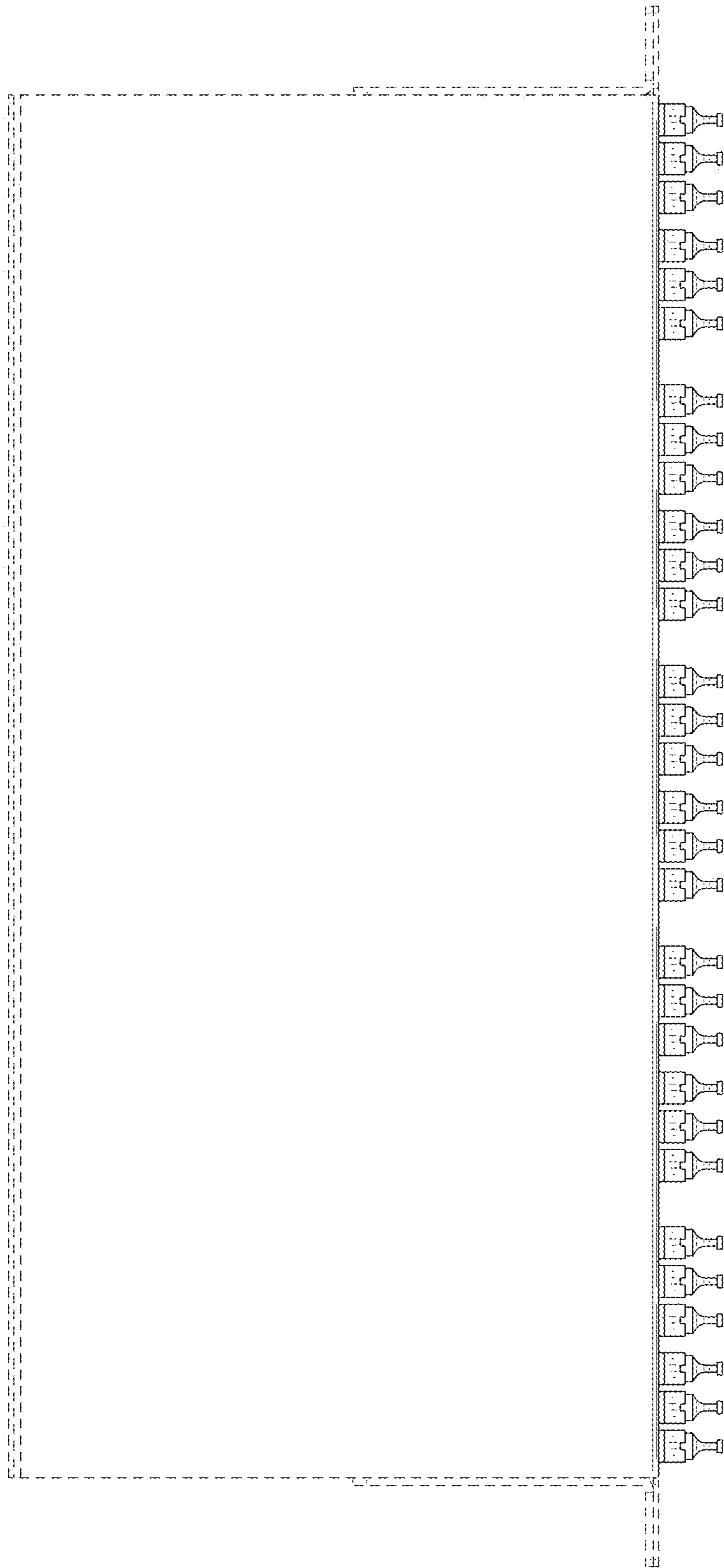


FIG. 8