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(12) United States Design Patent

Juco

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(54) **SEMICONDUCTOR WAFER PROCESSING APPARATUS**

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(73) Assignee: **Lam Research Corporation**, Fremont, CA (US)

(**) Term: **15 Years**

(21) Appl. No.: **29/690,192**

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(51) **LOC (13) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D15/122; D24/108, 164, 169, 170, 233; D16/230–234; D26/27; D10/81; D13/182
CPC B23K 26/00; B23K 26/0006; B23K 26/0096; B23K 26/08; B23K 26/36; B23K 26/32; B23K 26/40; B65C 2009/0043; B65C 2009/1846; H01L 21/00; H01L 21/67; H01S 5/00; H01S 5/02; H01S 5/04; H01S 5/10
See application file for complete search history.

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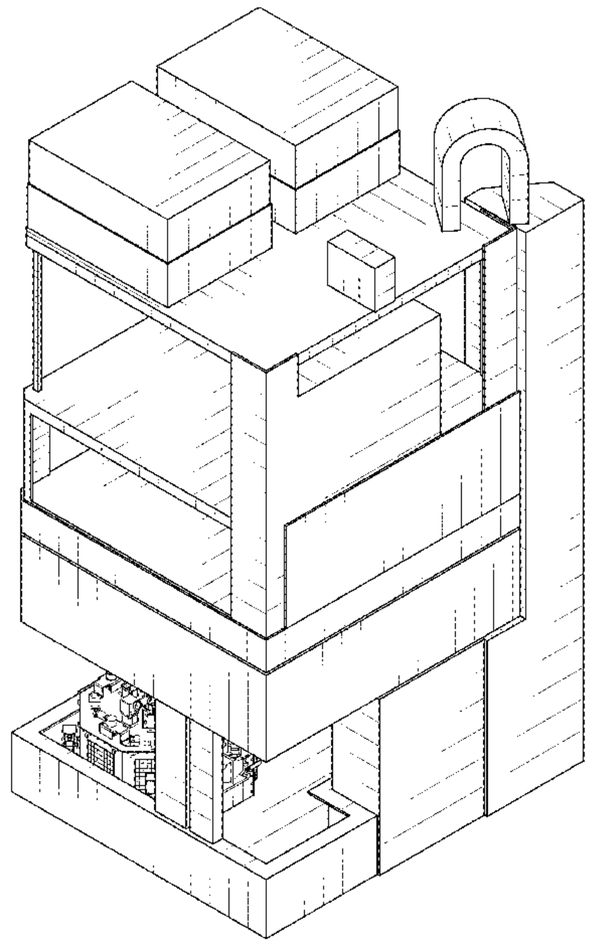
(57) **CLAIM**

The ornamental design for a semiconductor wafer processing apparatus, as shown and described.

DESCRIPTION

FIG. **1** is a perspective view depicting the overall shape of the semiconductor wafer processing apparatus, showing my new design;
FIG. **2** is a front view thereof;
FIG. **3** is a rear view thereof;
FIG. **4** is a left side view thereof;
FIG. **5** is a right side view thereof;
FIG. **6** is a top plan view thereof; and,
FIG. **7** is a bottom plan view thereof.
The broken line showings of portions of the semiconductor wafer processing apparatus and portions of the semiconductor wafer processing tool illustrate environmental structure, and the broken lines form no part of the claimed design.
The shape of the semiconductor wafer processing apparatus is the feature of the design creation content.

1 Claim, 7 Drawing Sheets



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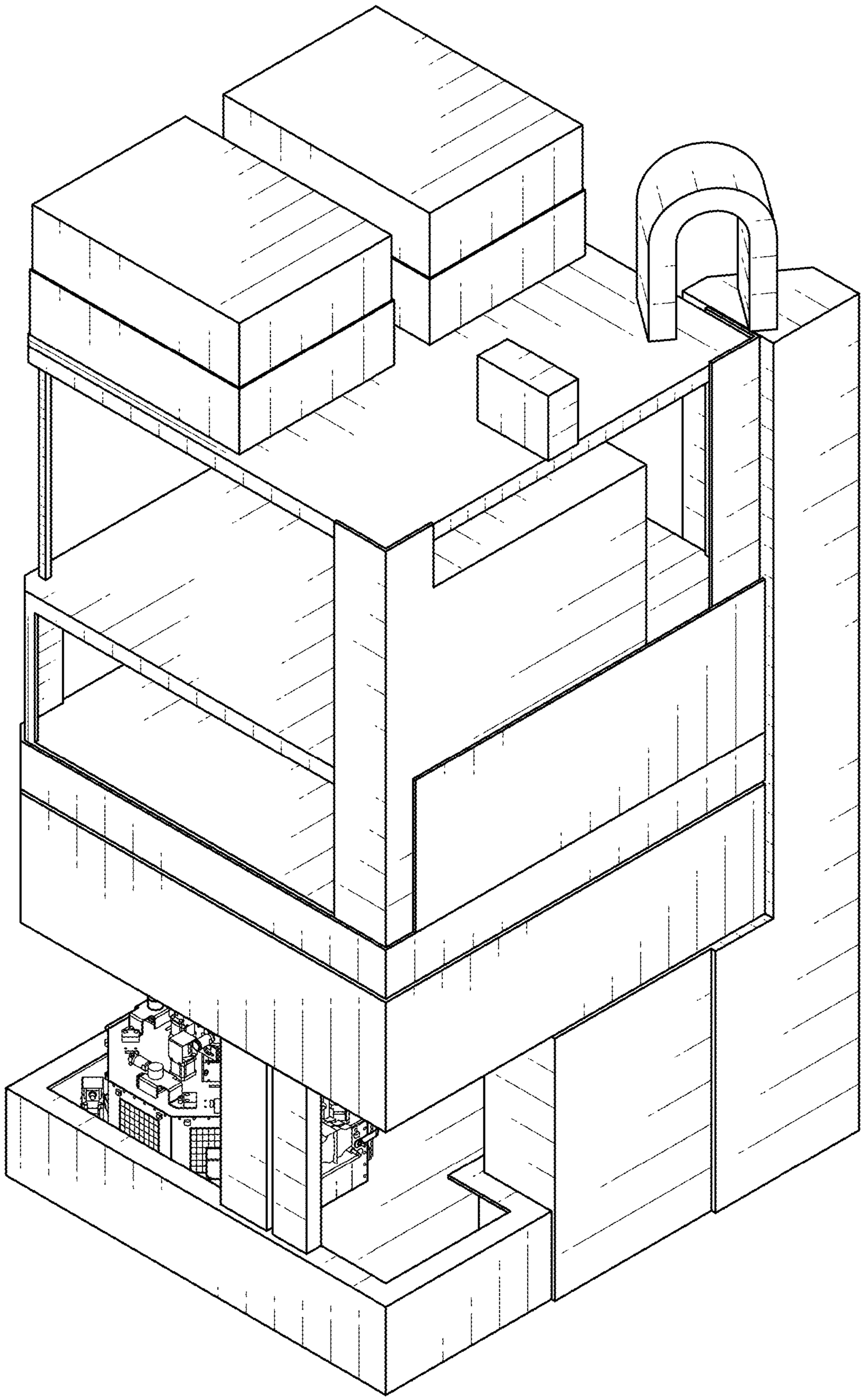

FIG. 1

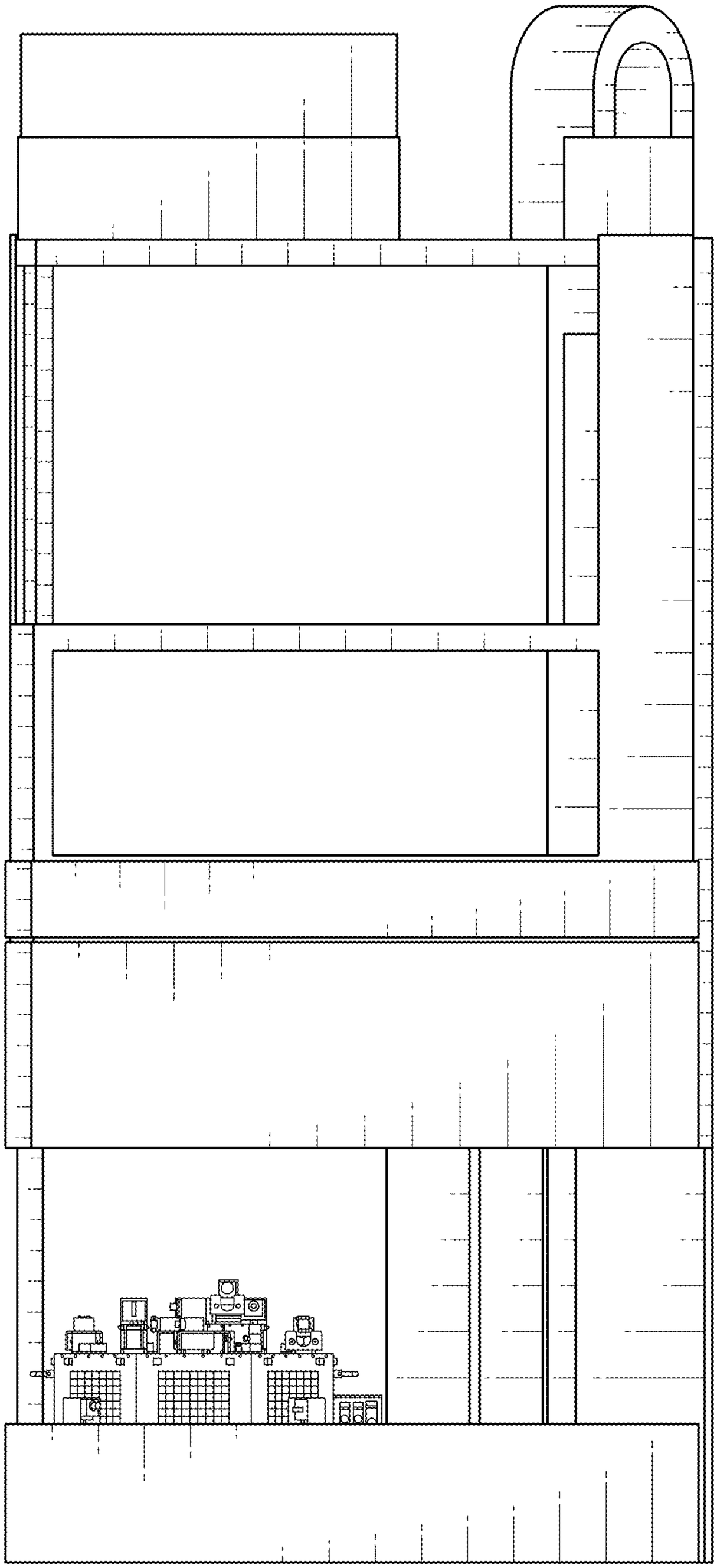

FIG. 2

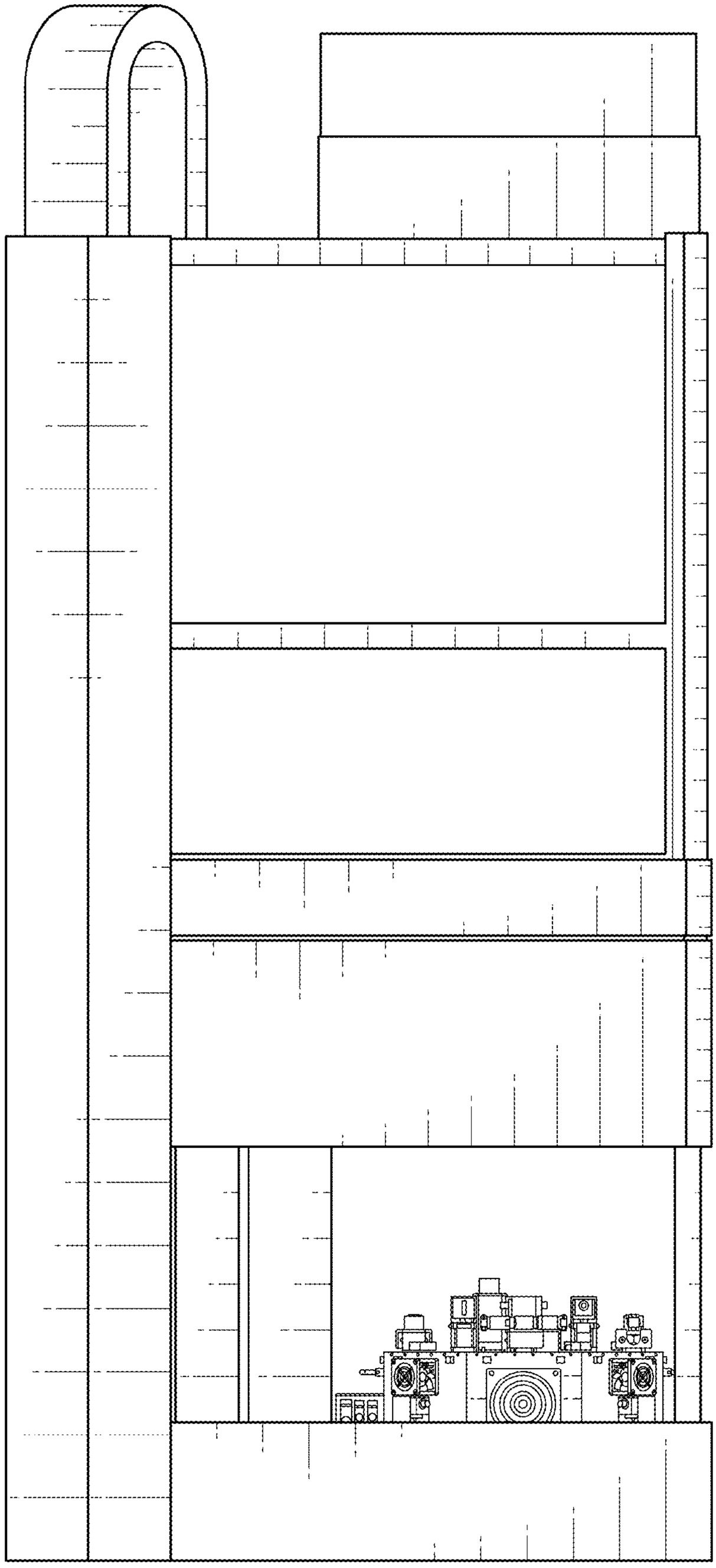

FIG. 3

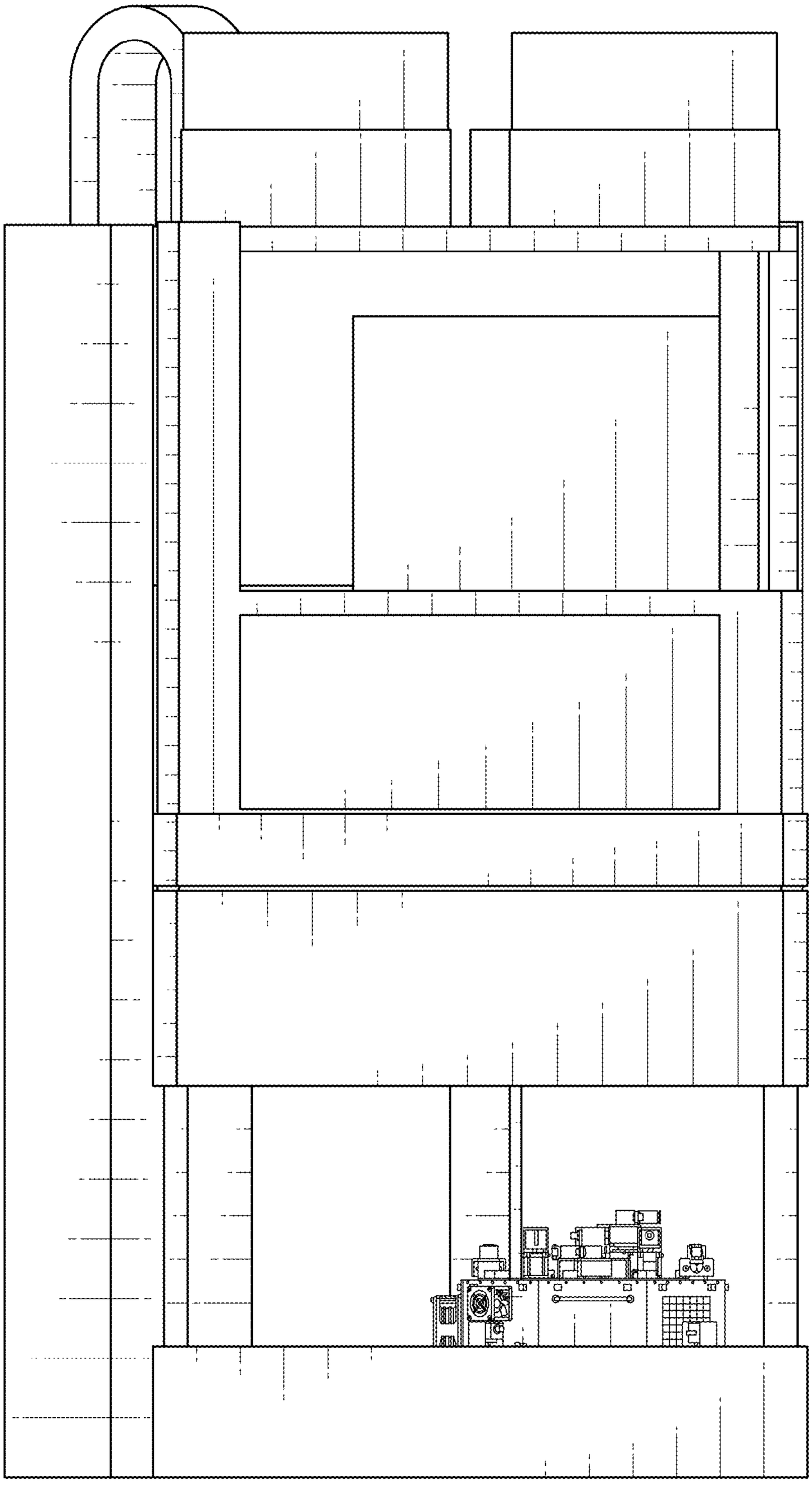

FIG. 4

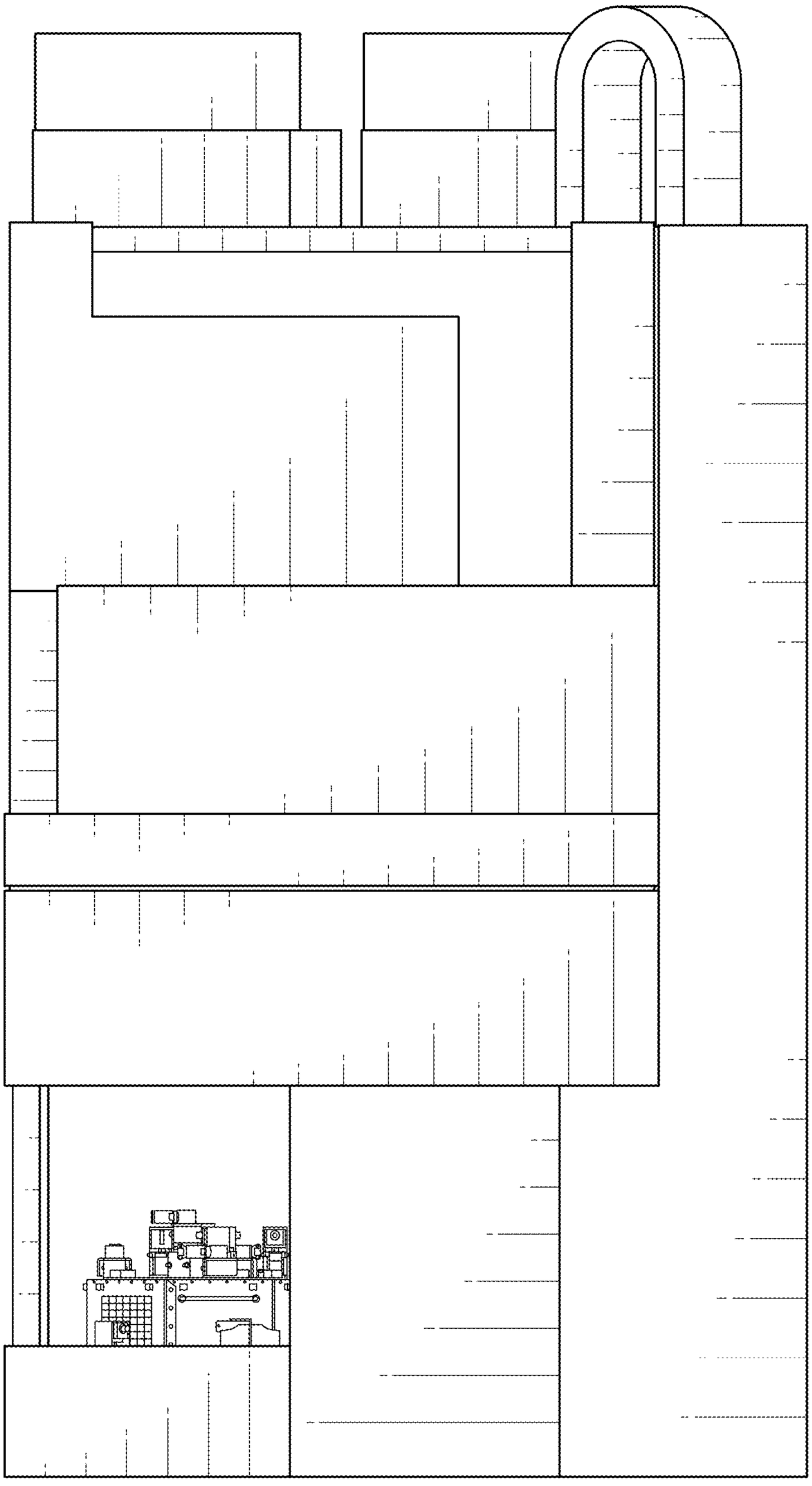

FIG. 5

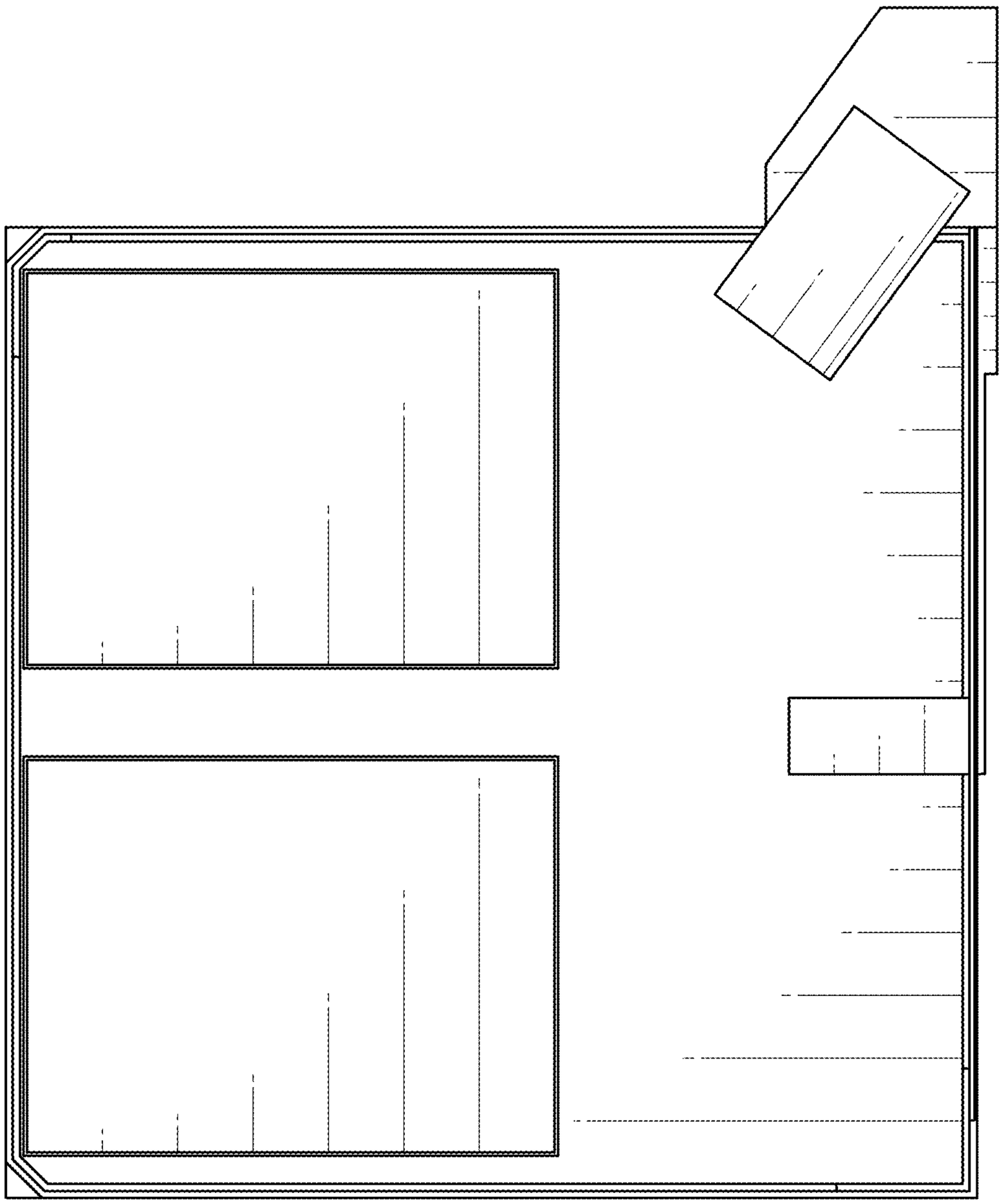

FIG. 6

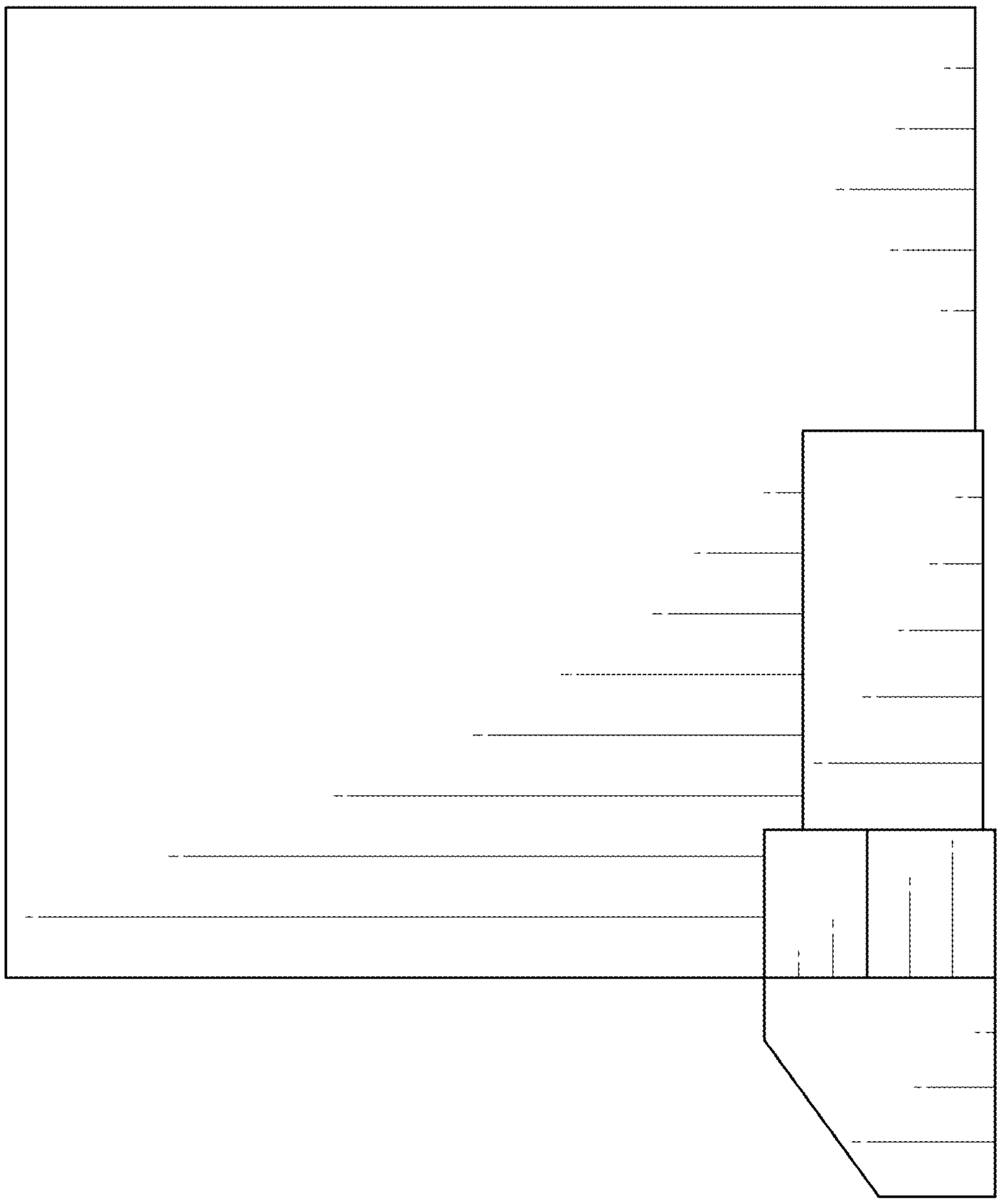

FIG. 7